MICRON

ADVANCE

MT41LC256K32D4(S)
256K x 32 SGRAM

SYNCHRONOUS GRAPHICS RAM

256K x 32 SGRAM

PULSED $\overline{\text{RAS}}$, DUAL BANK, PIPELINED, 3.3V OPERATION

FEATURES

- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Dual internal banks for hiding row access/precharge; dual 128K x 32 architecture
- Programmable burst lengths: 1, 2, 4, 8 or full page
- BLOCK WRITE and WRITE-PER-BIT modes
- Independent byte operation via DQM0-3
- AUTO PRECHARGE and AUTO REFRESH modes
- 17ms, 1,024-cycle refresh (16.6µs/row)
- LVTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply

OPTIONS

OPTIONS		MARKING
• Timing		
10ns access	(≤100 MHz clock rate)	-10
12ns access	(≤83 MHz clock rate)	-12
15ns access	(≤66 MHz clock rate)	-15
• Self Refresh		S
• Plastic Packages		
100-pin TQFP (0.65mm lead pitch)		LG

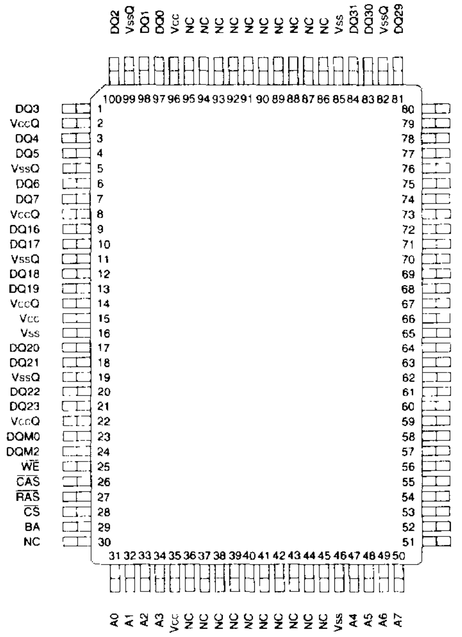
- Part Number Example: MT41LC256K32D4LG -15

KEY TIMING PARAMETERS

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME	SET-UP TIMES	HOLD TIMES
-10	100 MHz	9ns	3ns	1ns
-12	83 MHz	11ns	3.5ns	1.5ns
-15	66 MHz	13ns	4ns	2ns

PIN ASSIGNMENT (TOP VIEW)

100-Pin TQFP
(DC-1)



GENERAL DESCRIPTION

The MT41LC256K32D4(S) SGRAM is a high-speed CMOS dynamic random access memory containing 8,388,608 bits. It is internally configured as a dual 128K x 32 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 128K x 32 bit banks is organized as 512 rows by 256 columns by 32 bits. Read and write accesses to the SGRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA selects the bank, A0-A8 select the row). Then the address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SGRAM provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

GENERAL DESCRIPTION (continued)

The MT41LC256K32D4(S) uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed fully random access. Precharging one bank while accessing the alternate bank will hide the precharge cycles, and provide seamless high-speed random access operation.

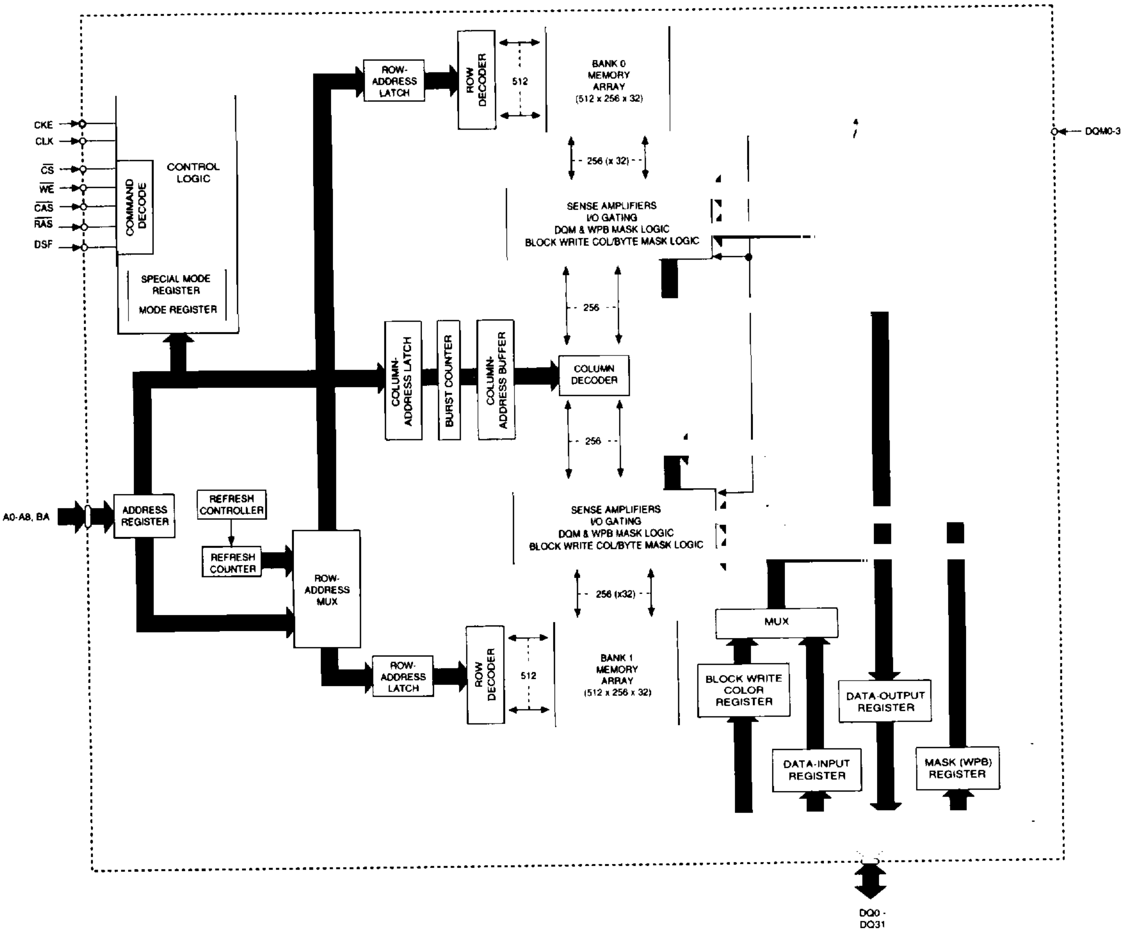
Synchronous graphics RAMs (SGRAMs) differ from synchronous DRAMs (SDRAMs) by providing an eight-column BLOCK WRITE function and a MASKED WRITE (or WRITE-PER-BIT) function to accommodate high-performance graphics applications. The BLOCK WRITE and MASKED WRITE functions may be combined with individual byte enables (DQ mask, or DQM, pins).

The CMOS dynamic memory structure of the MT41LC256K32D4(S) is designed to operate in 3.3V, low-power memory systems. An AUTO REFRESH mode is provided along with a power saving POWER-DOWN mode. All inputs and outputs are LVTTL-compatible.

The two-bank synchronous DRAM and x32 configuration provided by the SGRAM are well suited for applications requiring high memory bandwidth, and when combined with special graphics functions result in a device particularly well suited to high performance graphics applications.

SGRAMs offer substantial advances in dynamic memory operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, the capability to randomly change column addresses on each clock cycle during a burst access, and special functions such as MASKED WRITEs and BLOCK WRITEs.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

TQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
55	CLK	Input	Clock: CLK is driven by the system clock. All SGRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
54	CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides POWER-DOWN mode (all banks idle) and SELF REFRESH mode (all banks idle). CKE is synchronous except after the device enters POWER-DOWN and SELF REFRESH modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during POWER-DOWN and SELF REFRESH modes providing low standby power. CKE may be tied HIGH.
28	$\overline{\text{CS}}$	Input	Chip Select: $\overline{\text{CS}}$ enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when $\overline{\text{CS}}$ is registered HIGH. $\overline{\text{CS}}$ provides for external bank selection on systems with multiple banks. It is considered part of the command code.
27, 26, 53, 25	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ DSF, $\overline{\text{WE}}$	Input	Command Inputs: $\overline{\text{RAS}}$, $\overline{\text{WE}}$, $\overline{\text{CAS}}$, and DSF define the command being entered.
23, 56, 24, 57	DQM0 - DQM3	Input	Input/Output Mask: DQM0-DQM3 are byte specific, nonpersistent I/O buffer controls. The I/O buffers are placed in a High-Z state when DQM is sampled HIGH. Input data is masked when DQM is sampled high during a WRITE cycle. Output data is masked (two-clock latency) when DQM is sampled HIGH during a READ cycle. DQM0 masks DQ0-DQ7, DQM1 masks DQ8-DQ15, DQM2 masks DQ16-DQ23, and DQM3 masks DQ24-DQ31.
29	BA	Input	Bank Address: BA defines to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA is also used to program the 10th bit of the MODE and SPECIAL MODE registers.
31-34, 47-50, 51	A0-A8	Input	Address Inputs: A0-A8 are sampled during the ACTIVE command (row-address A0-A8) and READ/WRITE command (column-address A0-A7 with A8 defining AUTO PRECHARGE) to select one location out of the 128K available in the respective bank.A8 is sampled during a precharge command determining if both banks are to be precharged (A8 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER or LOAD SPECIAL MODE REGISTER command.
97, 98, 100, 1, 3, 4, 6, 7, 60, 61, 63, 64, 68, 69, 71, 72, 9, 10, 12, 13, 17, 18, 20, 21, 74, 75, 77, 78, 80, 81, 83, 84	DQ0-DQ31	Input/ Output	Data I/O: Data bus. The I/Os are byte-maskable during READs and WRITEs.The DQs also serve as column/byte mask inputs during BLOCK WRITEs.
30, 36-45, 52, 58, 86-95	NC	—	No Connect: These pins should be left unconnected.
2, 8, 14, 22, 59, 67, 73, 79	VccQ	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
5, 11, 19, 62, 70, 76, 82, 99	VssQ	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
15, 35, 65, 96	Vcc	Supply	Power Supply: +3.3V ±0.3V.
16, 46, 66, 85	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

In general, the SGRAM is a dual 128K x 32 DRAM with graphics features (BLOCK WRITE and MASKED WRITE) which operates at 3.3V and includes a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 128K x 32 bit banks is organized as 512 rows by 256 columns by 32 bits.

Read and write accesses to the SGRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA selects the bank, A0-A8 select the row). Then the address bits (A0-A7) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

BLOCK WRITE accesses are performed in a manner similar to WRITEs, except that BLOCK WRITEs are not burst oriented, and always apply to the eight column locations selected by A3-A7.

MASKED WRITEs or MASKED BLOCK WRITEs are similar to the unmasked versions except that the write-per-bit mask enabled with the ACTIVE command is applied to the data being written.

Prior to normal operation, the SGRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Initialization

SGRAMs must be powered-up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Once power is applied to Vcc and VccQ (simultaneously) the SGRAM requires a 100µs delay prior to activating CKE. All other inputs should be held HIGH during this phase of power-up.

Once the 100µs delay has been satisfied, the CKE pin must be driven HIGH ^{t}CKS before a positive clock edge, after meeting ^{t}CKH from the previous clock edge. The first command will be registered on the clock edge following ^{t}CKS.

Both banks must then be precharged, thereby placing the device in the "all bank idle" state. Once in the idle state, two AUTO REFRESH cycles must be performed. Once the AUTO REFRESH cycles are complete, the SGRAM is ready for mode register programming. Because the mode register will power-up in an unknown state, it should be loaded prior to performing any operational command.

Register Definition

MODE REGISTER

The mode register is used to define the specific mode of operation of the SGRAM. This definition includes the selection of a burst length, a burst type, a read latency and an operating mode, as shown in Figure 1. The mode register is programmed via the LOAD MODE REGISTER command, and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0 through M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4 through M6 specify the READ latency, and M7 through M9 specify the operating mode.

The mode register must be loaded when both banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements may result in unknown operation.

Burst Length

Read and write accesses to the SGRAM are burst oriented, with the burst length being programmable, as shown in Figure 1. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4, or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

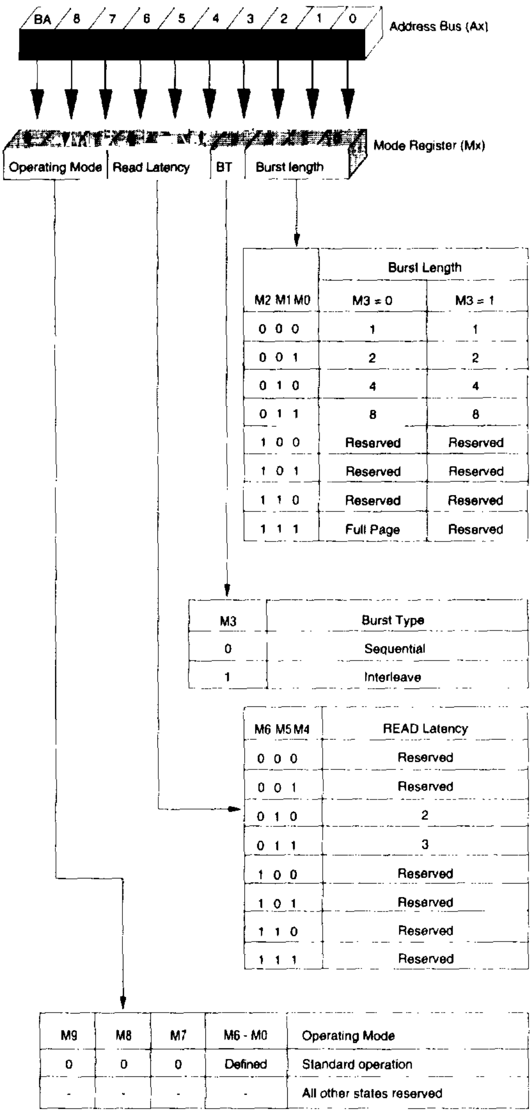
Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is defined by A1-A7 when the burst length is set to two, by A2-A7 when the burst length is set to four and by A3-A7 when the burst length is set to eight. The lower order address bit(s) are used to select the starting location within the block. Full page bursts wrap within the page if the boundary is reached.

Burst Type

Accesses within a given burst may be programmed to be either sequential or "interleaved"; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 1.



M2 M1 M0	Burst Length M3 = 0	Burst Length M3 = 1
0 0 0	1	1
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Full Page	Reserved

M3	Burst Type
0	Sequential
1	Interleave

M6 M5 M4	READ Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

M9	M8	M7	M6 - M0	Operating Mode
0	0	0	Defined	Standard operation
-	-	-	-	All other states reserved

Figure 1
MODE REGISTER DEFINITION

Table 1
BURST DEFINITION

Burst Length	Starting Column Address:			Order of Accesses within a Burst	
				Type = Sequential	Type = Interleaved
			A0		
2			0	0-1	0-1
			1	1-0	1-0
		A1	**A0**		
4		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
	A2	**A1**	**A0**		
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (256)	n = A0 - A7 (location 0 - 255)			Cn, Cn+1, Cn+2 Cn+3, Cn+4... ...Cn-1 (Cn+256), Cn (Cn+257)...	Not supported

NOTE:

1. For a burst length of two, A1-A7 select the block of two burst; A0 selects the starting column within the block.
2. For a burst length of four, A2-A7 select the block of four burst; A0-A1 select the starting column within the block.
3. For a burst length of eight, A3-A7 select the block of eight burst; A0-A2 select the starting column within the block.
4. For a full-page burst, the full row is selected and A0-A7 select the starting column.
5. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
6. For a burst length of one, A0-A7 select the unique column to be accessed, and Mode Register bit M3 is ignored.

Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to 2 or 3 clocks.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available by clock edge *n* + *m*. The DQs will start driving as a result of the clock edge one cycle earlier (*n* + *m* - 1) and, provided that the relevant access times are met, the data will be valid by clock edge *n* + *m*. For example, assuming that the clock cycle time is such that all relevant access times are met, if a read command is registered at T0, and the latency is programmed to 2 clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in Figure 2. Table 2 below indicates the operating frequencies at which each READ latency setting can be used.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

Operating Mode

In normal operation (M7 - M9 = 0), the programmed burst length applies to both read and write bursts.

M7 = 1 is used for vendor specific testing. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

SPECIAL MODE REGISTER

The special mode register is used to load the color and mask registers, which are used in BLOCK WRITE and MASKED WRITE cycles. The control information being written to the special mode register is applied to the address inputs and the data to be written to either the color register or the mask register is applied to the DQs. As shown in Figure 3, when input A6 is "1", and all other address inputs are "0" during a LOAD SPECIAL MODE REGISTER cycle, the color register will be loaded with the data on the DQs. Similarly, when input A5 is "1", and all other address inputs are "0" during a LOAD SPECIAL MODE REGISTER cycle, the mask register will be loaded with the data on the DQs. Applying a "1" to both A5 and A6 (when all other address inputs are "0") or applying a "1" to any address input other than A5 or A6, during a LOAD SPECIAL MODE REGISTER cycle is illegal and unknown operation may result. The special mode register can be loaded when one or both banks are either active or idle.

COLOR REGISTER

The color register is a 32-bit register which supplies the data during BLOCK WRITE cycles. The color register is loaded via a LOAD SPECIAL MODE REGISTER cycle (described in the previous section) and will retain data until loaded again or until power is removed from the SGRAM.

MASK REGISTER

The mask register (or write-per-bit mask register) is a 32-bit register which acts as a per-DQ mask during MASKED WRITE and MASKED BLOCK WRITE cycles. This operation is described under the respective headings later in this data sheet. The mask register is loaded via a LOAD SPECIAL MODE REGISTER cycle (described previously, under the Special Mode Register heading) and will retain data until loaded again or until power is removed from the SGRAM.

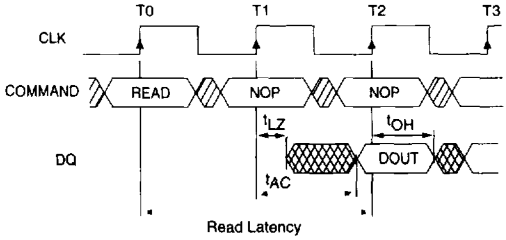
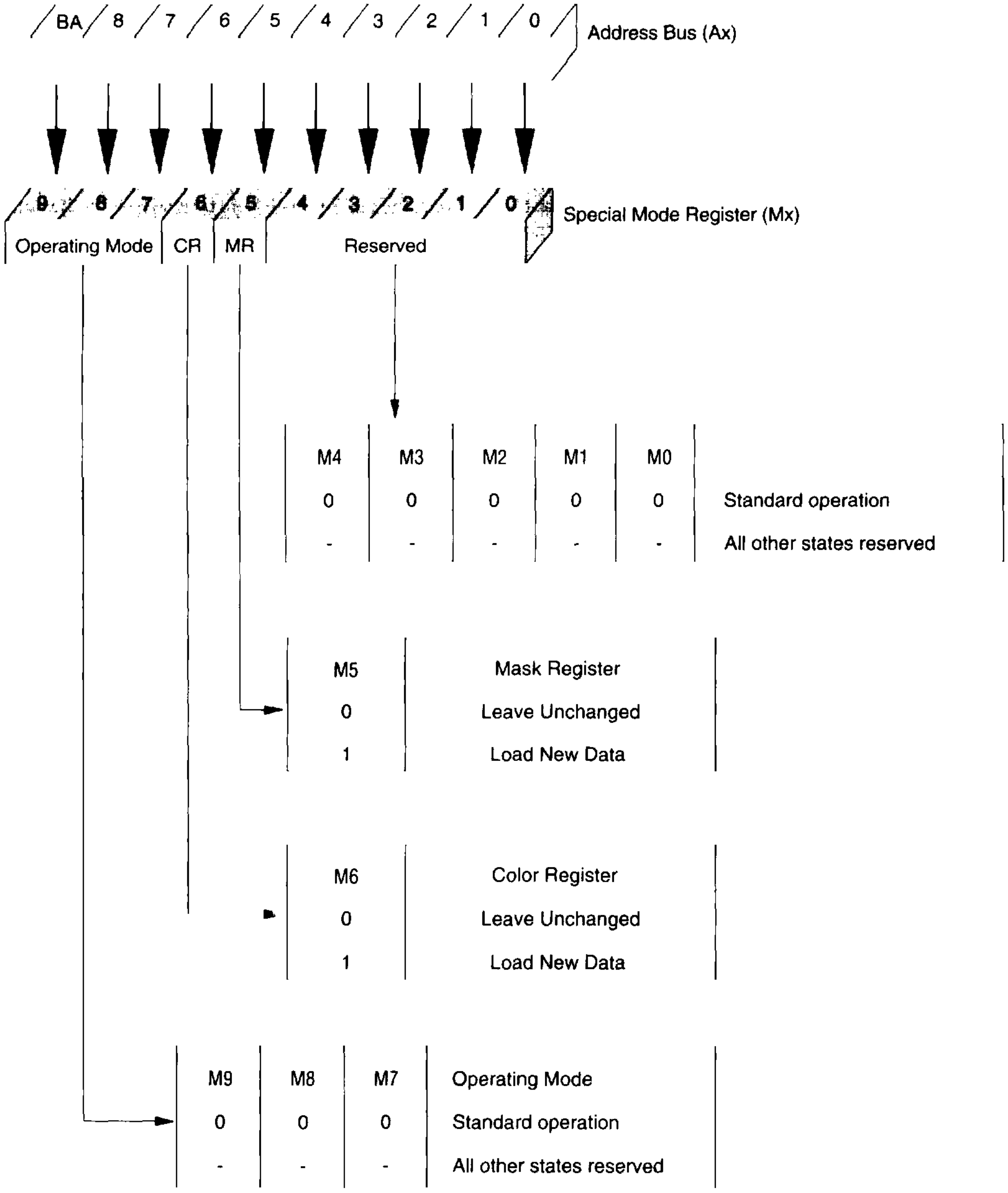


Figure 2
TWO CLOCK READ LATENCY EXAMPLE

Table 2
READ LATENCY

	ALLOWABLE OPERATING FREQUENCY (MHz)	
SPEED	READ LATENCY = 2	READ LATENCY = 3
-10	≤ 66	≤ 100
-12	≤ 55	≤ 83
-15	≤ 44	≤ 66



M4	M3	M2	M1	M0	
0	0	0	0	0	Standard operation
-	-	-	-	-	All other states reserved

M5	Mask Register
0	Leave Unchanged
1	Load New Data

M6	Color Register
0	Leave Unchanged
1	Load New Data

M9	M8	M7	Operating Mode
0	0	0	Standard operation
-	-	-	All other states reserved

Figure 3
SPECIAL MODE REGISTER DEFINITION

Commands

Truth Table 1 provides a quick reference of available commands. This is followed by a verbal description of each command. Two additional Truth Tables appear following the Operation section; these tables provide current state/ next state information.

TRUTH TABLE 1 – Commands and DQM Operation

(Notes: 1)

NAME (FUNCTION)	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	DSF	DQM	ADDR	DQs	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	L	X	X	X	13
ACTIVE (Select bank and activate row)	L	L	H	H	L	X	bank/row	X	3
ACTIVE with WPB (Select bank, activate row and WPB)	L	L	H	H	H	X	bank/row	X	3, 11
READ (Select bank & column and start READ burst)	L	H	L	H	L	X	bank/col	X	4, 13
WRITE (Select bank & column and start WRITE burst)	L	H	L	L	L	X	bank/col	VALID	4
BLOCK WRITE (Select bank & column and start BLOCK WRITE access)	L	H	L	L	H	X	bank/col	MASK	4, 12
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	L	X	Code	X	5, 13
BURST TERMINATE	L	H	H	L	L	X	X	Active	13
AUTO REFRESH or SELF REFRESH (enter SELF REFRESH mode)	L	L	L	H	L	X	X	X	6, 7, 9 13
LOAD MODE REGISTER	L	L	L	L	L	X	OpCode	X	2
LOAD SPECIAL MODE REGISTER	L	L	L	L	H	X	OpCode	VALID	10
Write enable/output enable	-	-	-	-	-	L	-	Active	8
Write inhibit/output High-Z	-	-	-	-	-	H	-	High-Z	8

NOTE:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. A0 through A8 and BA define the op-code written to the mode register.
3. A0 through A8 provide row-address and BA determines which bank is made active (BA LOW = Bank 0 and BA HIGH = Bank 1).
4. A0 through A7 provide column-address; A8 HIGH enables the AUTO PRECHARGE feature (nonpersistent) while A8 LOW disables the AUTO PRECHARGE feature; BA determines which bank is being read from or written to (BA LOW = Bank 0 and BA HIGH = Bank 1).
5. A8 LOW: BA determines bank being precharged (BA LOW = Bank 0 and BA HIGH = Bank 1). A8 HIGH: both banks precharged and BA is a "don't care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "don't care" except for CKE.
8. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay).
9. Enter SELF REFRESH is illegal on non-S version.
10. DQs contain either color data or WPB mask data.
11. Any WRITE or BLOCK WRITE cycles to the selected bank/row while active will be masked according to the contents of the mask register, in addition to the DQM signals and the column/byte mask information (the latter for BLOCK WRITEs only).
12. DQs contain the column/byte mask data for the BLOCK WRITE.
13. DSF is actually "don't care", but it is recommended to be LOW for compatibility with future devices.

COMMAND INHIBIT

The COMMAND INHIBIT function prevents commands from being executed by the SGRAM, regardless of whether the CLK signal is enabled. The SGRAM is effectively deactivated, or deselected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to an SGRAM which is selected ($\overline{CS}$ is LOW). This prevents unwanted commands from being registered during idle or wait states.

LOAD MODE REGISTER

The mode register is loaded via inputs A0-A8 and BA. See Mode Register heading in Register Definition section. The LOAD MODE REGISTER command can only be issued when both banks are idle, and a subsequent executable command cannot be issued until ^{t}MTC is met.

LOAD SPECIAL MODE REGISTER

This command is used to load either the color register or mask register by activating the appropriate bit in the special mode register. The control information is provided on inputs A0-A8 and BA, while the data for the color or mask register is provided on the DQs. See Special Mode Register heading in Register Definition section. The LOAD SPECIAL MODE REGISTER command can be issued when both banks are idle, or one or both are active, but with no READ, WRITE or BLOCK WRITE accesses in progress. A subsequent executable command cannot be issued until ^{t}SML is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA input selects the bank, and the address provided on inputs A0-A8 selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

ACTIVE WITH WPB

This command is similar to the ACTIVE command, except that the write-per-bit mask is activated. Any WRITE or BLOCK WRITE cycles to the selected bank/row while active will be masked according to the contents of the mask register, in addition to the DQM signals, and the column/byte mask information (the latter for BLOCK WRITEs only).

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA input selects the bank, and the address provided on inputs A0-A7 selects the starting column location. The value on input A8 determines whether or not AUTO PRECHARGE is used. If AUTO PRECHARGE is selected, the row being accessed will be precharged at the end of the read burst; if it is not selected, the row will remain open for subsequent accesses. READ data appears on the DQs subject to the values on the DQM inputs two clocks earlier. If a particular DQM signal was registered HIGH, the corresponding DQs will be High-Z two clocks later; if the DQM signal was registered LOW, the DQs will provide valid data.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA input selects the bank, and the address provided on inputs A0-A7 selects the starting column location. The value on input A8 determines whether or not AUTO PRECHARGE is used. If AUTO PRECHARGE is selected, the row being accessed will be precharged at the end of the write burst; if it is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DQM signals registered coincident with the data. If a particular DQM signal is registered LOW, the corresponding data will be written to memory (subject also to the write-per-bit mask, if activated); if the DQM signal is registered HIGH, the corresponding data inputs will be ignored, and the write will not be executed to that byte location.

BLOCK WRITE

The BLOCK WRITE command is used to write a single data value to the block of eight consecutive column locations addressed by inputs A3-A7. The source of the data is the color register, which must be loaded prior to the BLOCK WRITE. The information on the DQs which is registered coincident with the BLOCK WRITE command is used to mask specific column/byte combinations within the block, as described in the Operation section of this data sheet. The DQM signals operate as for WRITE cycles, but are applied to all eight columns.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank, or the open row in both banks. The bank(s) will be available for a subsequent row access some specified time (^tRP) after the precharge command is issued. Input A8 determines whether one or both banks are to be precharged, and in the case where only one bank is to be precharged, input BA selects the bank. Otherwise BA is treated as a "don't care". Once a bank has been precharged, it is in the idle state and must be activated prior to any READ, WRITE or BLOCK WRITE commands being issued to that bank.

AUTO PRECHARGE

AUTO PRECHARGE is a nonpersistent feature which performs all of the same individual-bank precharge functions as previously described. The AUTO PRECHARGE feature allows the user to issue a READ, WRITE or BLOCK WRITE command that automatically performs a precharge upon the completion of the BLOCK WRITE access or READ or WRITE burst, except in the full-page burst mode, where it has no effect.

The use of this feature eliminates the need to "manually" issue a PRECHARGE command during the functional operation of the SGRAM. AUTO PRECHARGE ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command until the precharge time (^tRP) is completed. This is determined as if a manual PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Operation section of this data sheet.

BURST TERMINATE

The BURST TERMINATE command is used to truncate either fixed-length or full-page bursts.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the SGRAM and is analagous to $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) REFRESH in conventional DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required.

The addressing is generated by the internal refresh controller. This makes the address bits a "don't care" during an AUTO REFRESH command. The MT41LC256K32D4(S) requires all of its 1,024 rows to be refreshed every 17ms (^tREF). Providing a distributed AUTO REFRESH command every 16.6µs will meet the refresh requirement and ensure that each row is refreshed. Alternatively, all 1,024 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (^tRC) once every 17ms.

SELF REFRESH

The SELF REFRESH command (on the "S" version) can be used to retain data in the SGRAM, even if the rest of the system is powered down. When in the SELF REFRESH mode, the SGRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). Once the SELF REFRESH command is registered, all the inputs to the SGRAM become "don't cares" with the exception of CKE, which must remain LOW.

Once SELF REFRESH mode is engaged, the SGRAM provides its own internal clocking, causing it to perform its own auto refresh cycles. The SGRAM may remain in SELF REFRESH mode for an indefinite period.

The procedure for exiting SELF REFRESH requires a sequence of commands. First, the system clock must be stable prior to CKE going back HIGH. Once CKE is HIGH, the SGRAM must have NOP commands issued for ^tXSR, because time is required for the completion of any bank currently being internally refreshed.

Operation

BANK/ROW ACTIVATION

Before any READ or WRITE commands can be issued to a bank within the SGRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated.

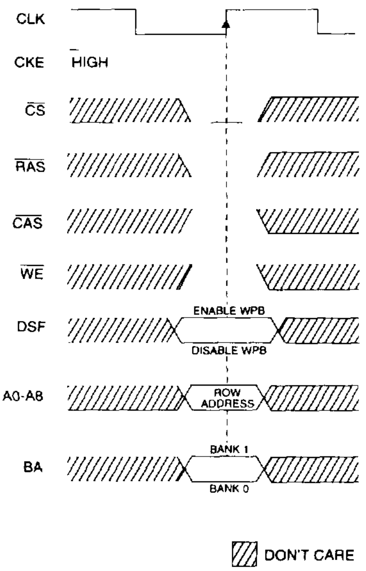


Figure 4
ACTIVATING A SPECIFIC ROW IN A SPECIFIC BANK

The ACTIVE command is also used to determine whether or not the write-per-bit mask is to be applied during WRITE and BLOCK WRITE cycles within that row (see Figure 4). If DSF is HIGH at the time the ACTIVE command is registered (ACTIVE with WPB) then the mask will be applied to all WRITE and BLOCK WRITE cycles to that row until the row is "closed"(precharged).

After opening a row (issuing an ACTIVE command) a READ or WRITE command may be issued to that row, subject to the ^{t}RCD specification. ^{t}RCD MIN should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a ^{t}RCD specification of 30ns with a 90 MHz clock (11.11ns period) results in 2.7 clocks rounded to 3. This is reflected in Figure 5, which covers any case where $3 > {}^{t}\text{RCD MIN}/{}^{t}\text{CK} > 2$. (The same procedure is used to convert other specification limits from time units to clock cycles).

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC.

A subsequent ACTIVE command to the other bank can be issued while the first bank is being accessed, which results in a reduction of total row access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD.

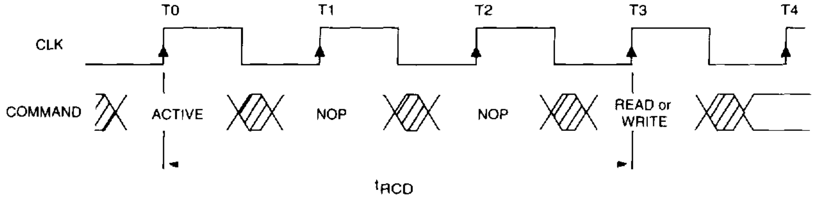


Figure 5
EXAMPLE: MEETING ^{t}RCD MIN WHEN $2 < {}^{t}\text{RCD MIN}/{}^{t}\text{CK} < 3$

READs

READ bursts are initiated with a READ command, as shown in Figure 6.

The starting column and bank addresses are provided with the READ command and AUTO PRECHARGE is either enabled or disabled for that burst access. If AUTO PRECHARGE is enabled, the row being accessed is precharged at the completion of the burst. For the generic READ commands used in the following illustrations, AUTO PRECHARGE is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the READ latency after the READ command. Each subsequent data-out element will be valid by the next positive clock edge. Figure 7 shows the case where the READ latency is set to two, and Figure 8 shows a READ latency of three.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A full-page burst will continue until terminated (at the end of the page it will wrap to column 0 and continue).

A fixed-length READ burst may be followed by, or truncated with, a subsequent READ burst (provided that AUTO PRECHARGE is not activated) and a full-page READ burst can be truncated with a subsequent READ burst. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst, or the last desired data element of a longer burst which is being truncated. The new READ command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where

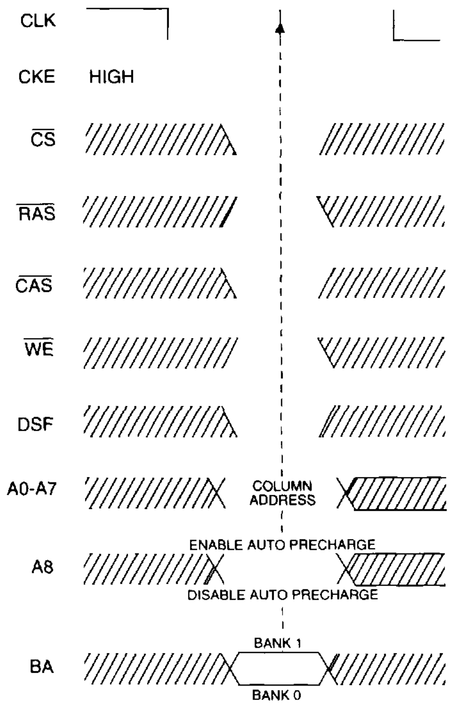


Figure 6
READ COMMAND

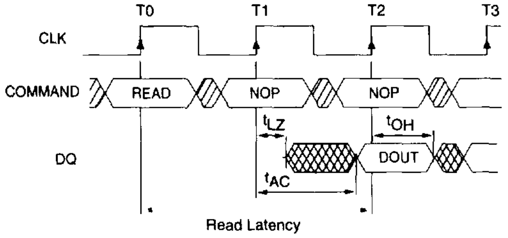


Figure 7
READ BURST WITH READ LATENCY OF TWO

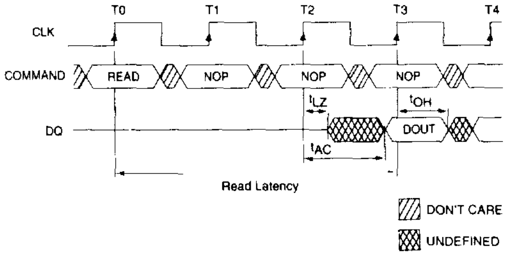
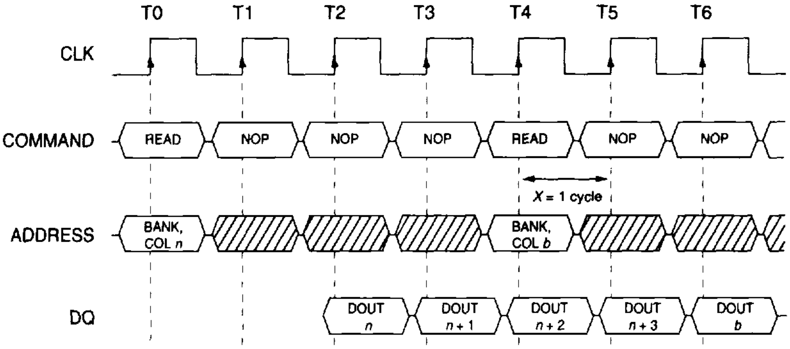


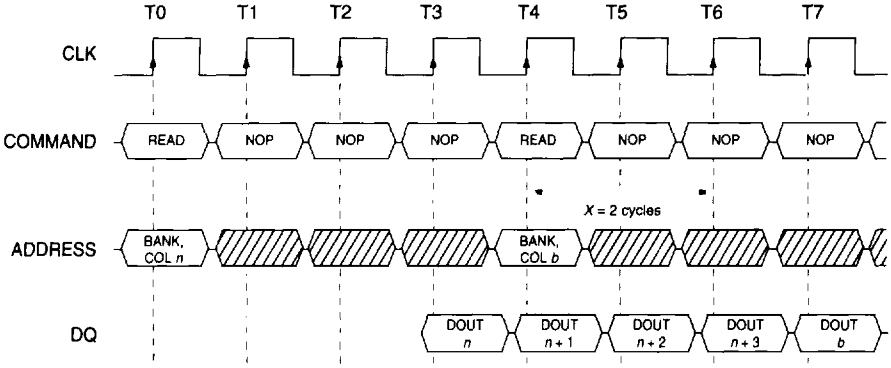
Figure 8
READ BURST WITH READ LATENCY OF THREE

x equals the read latency minus one. This is shown in Figure 9 for a read latency of two and Figure 10 for a read latency of three; data element *n* + 3 is either the last of a burst of four, or the last desired of a longer burst. The SGRAM does not require the 2*n* rule of prefetch architectures, so a READ command can be initiated on any clock cycle following a previous READ command. Full speed random read accesses within a page can be performed as shown in Figures 11 and 12.



NOTE: Covers either successive READs to the active row in a given bank, or to the active rows in different banks. DQMs are all active (LOW).

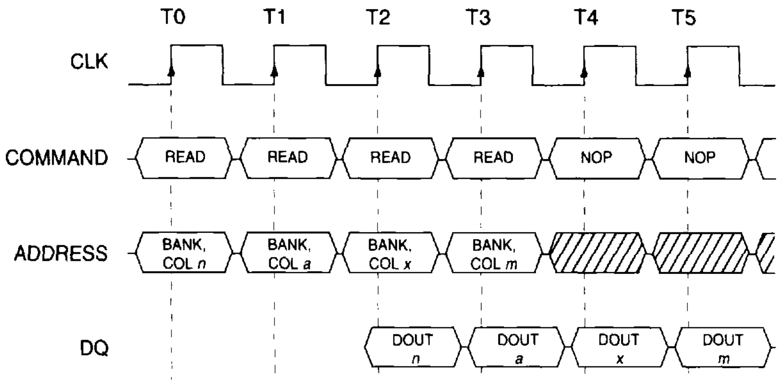
Figure 9
CONSECUTIVE READ BURSTS, READ LATENCY OF TWO



NOTE: Covers either successive READs to the active row in a given bank, or to the active rows in different banks. DQMs are all active (LOW).

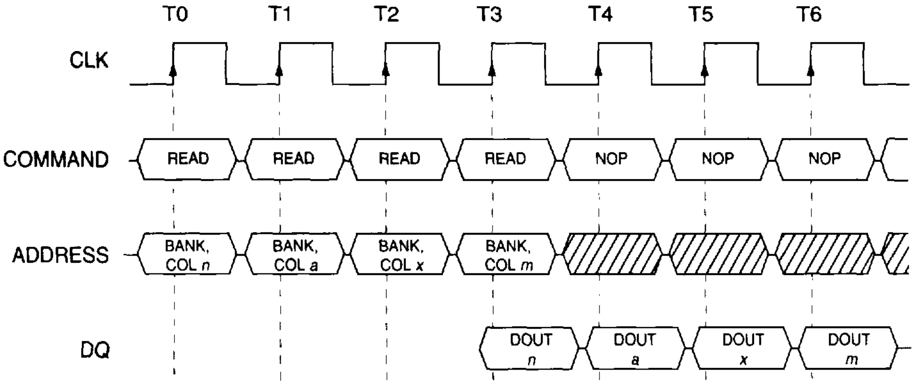
▨ DON'T CARE

Figure 10
CONSECUTIVE READ BURSTS, READ LATENCY OF THREE



NOTE: Covers either successive READs to the active row in a given bank, or to the active rows in different banks. DQMs are all active (LOW).

Figure 11
RANDOM READ ACCESSES WITHIN A PAGE, READ LATENCY OF TWO



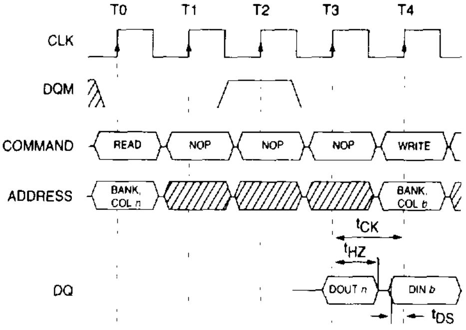
NOTE: Covers either successive READs to the active row in a given bank, or to the active rows in different banks. DQMs are all active (LOW).

▨ DON'T CARE

Figure 12
RANDOM READ ACCESSES WITHIN A PAGE, READ LATENCY OF THREE

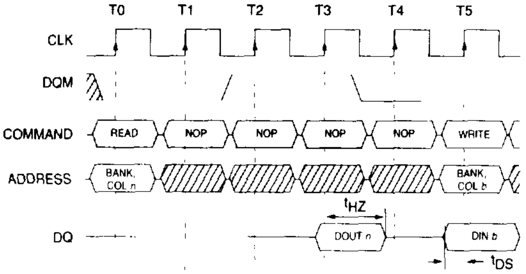
A fixed-length READ burst may be followed by, or truncated with, a WRITE burst or BLOCK WRITE command (provided that AUTO PRECHARGE was not activated) and a full page READ burst may be truncated by a WRITE burst or BLOCK WRITE command. The WRITE burst may be initiated on the clock edge immediately following the last (or last desired) data element from the READ burst, provided that I/O contention can be avoided. If the specifications for a given speed grade do not allow for contention to be avoided at a particular operating frequency, a single cycle delay must occur between the last READ data and the WRITE command.

The DQM inputs are used to avoid I/O contention as shown in Figures 13 and 14. The DQMs must be asserted (HIGH) at least two clocks (DQM latency is two clocks for output buffers) prior to the WRITE command to suppress data-out from the READ. Once the WRITE command is registered, the DQs will go High-Z (or remain High-Z) regardless of the state of the DQM signals. The DQM signals must be de-asserted (DQM latency is zero clocks for input buffers) prior to the WRITE command to ensure that the written data is not masked. Figure 13 shows the case where the clock frequency allows for bus contention to be avoided without adding a NOP cycle, and Figure 14 shows the case where the additional NOP is needed.



NOTE: A READ LATENCY of 3 is used for illustration. A BLOCK WRITE can be substituted for the WRITE, in which case column/byte mask data would be applied to the data inputs.

Figure 13
READ TO WRITE (OR BLOCK WRITE)



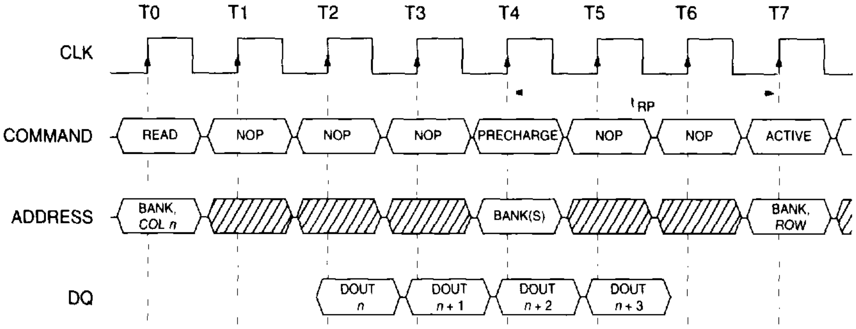
NOTE: A READ LATENCY of 3 is used for illustration. A BLOCK WRITE can be substituted for the WRITE, in which case column/byte mask data would be applied to the data inputs.

▨ DON'T CARE

Figure 14
READ TO WRITE (OR BLOCK WRITE) WITH EXTRA CLOCK CYCLE

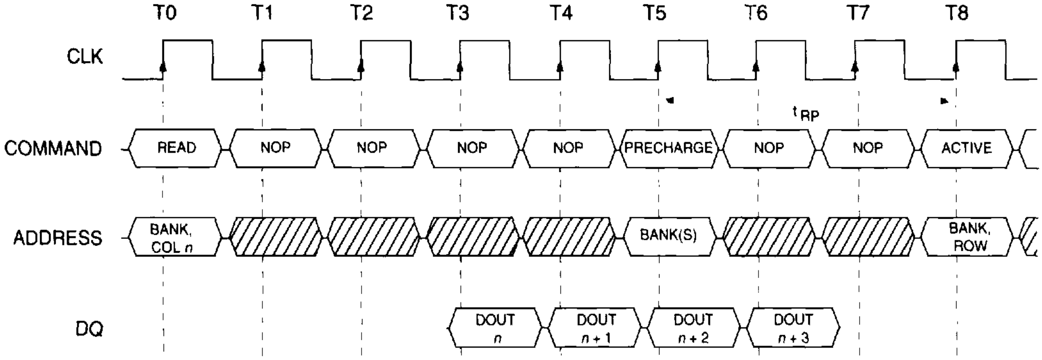
A fixed-length READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that AUTO PRECHARGE was not activated) and a full-page burst may be truncated with a PRECHARGE command to the same bank. The PRECHARGE command should be issued one cycle before the clock edge at which the last desired data element is valid. This is shown in Figure 15 for a read latency of two and Figure 16 for a read latency of three; data element *n* + 3 is either the last of a burst of four, or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ᵗRP is met. Note that part of the row precharge time is hidden during the access of the last data element.

In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst



NOTE: DQMs are all active (LOW).

Figure 15
READ TO PRECHARGE, READ LATENCY OF TWO



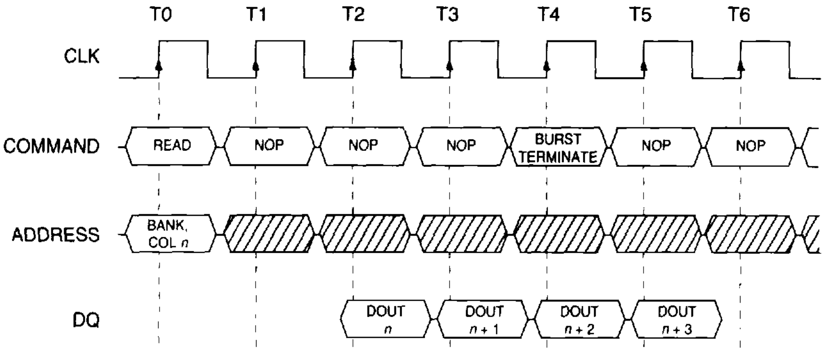
NOTE: DQMs are all active (LOW).

▨ DON'T CARE

Figure 16
READ TO PRECHARGE, READ LATENCY OF THREE

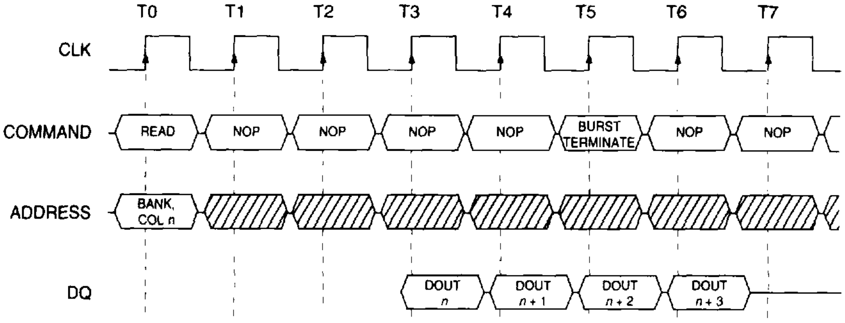
with AUTO PRECHARGE. The disadvantage of the PRECHARGE command is it requires that the command and address busses be available at the appropriate time to issue the command, but the advantage of the PRECHARGE command is that it can be used to truncate fixed-length or full-page bursts. The AUTO PRECHARGE command does not truncate fixed-length bursts and does not apply to full page bursts.

Full-page READ bursts can be truncated with the BURST TERMINATE command, and fixed-length READ bursts may be truncated with a BURST TERMINATE command, provided that auto-precharge was not activated. When truncating a READ burst, the BURST TERMINATE command should be issued 1 cycle before the clock edge at which the last desired data element is valid. This is shown in Figure 17 for a read latency of two and Figure 18 for a read latency of three; data element *n* + 3 is either the last of a burst of four, or the last desired of a longer burst.



NOTE: DQMs are all active (LOW).

Figure 17
TERMINATING A READ BURST, READ LATENCY OF TWO



NOTE: DQMs are all active (LOW).

▨ DON'T CARE

Figure 18
TERMINATING A READ BURST, READ LATENCY OF THREE

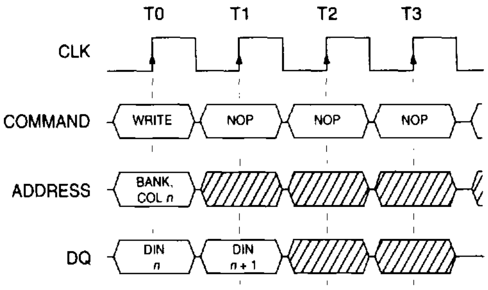
WRITEs

WRITE bursts are initiated with a WRITE command, as shown in Figure 19.

The starting column and bank addresses are provided with the WRITE command, normal or BLOCK WRITE is selected, and AUTO PRECHARGE is either enabled or disabled for that access. If AUTO PRECHARGE is enabled, the row being accessed is precharged at the completion of the burst. BLOCK WRITEs are covered later in this section. For the generic WRITE commands used in the following illustrations, AUTO PRECHARGE is disabled, and all WRITEs are normal WRITEs unless noted.

During WRITE bursts, the first valid data-in element will be registered coincident with the WRITE command. Subsequent data elements will be registered on each successive positive clock edge. Upon completion of a fixed-length burst, assuming no other commands have been initiated, the DQs will remain High-Z, and any additional input data will be ignored (see Figure 20). A full-page burst will continue until terminated (at the end of the page it will wrap to column 0 and continue).

A fixed-length WRITE burst may be followed by, or truncated with, a subsequent WRITE burst or BLOCK WRITE command (provided that AUTO PRECHARGE was not activated) and a full page WRITE burst can be truncated with a subsequent WRITE burst or BLOCK WRITE command. The new WRITE or BLOCK WRITE command can be issued on any clock following the previous WRITE command, and the data provided coincident with the new command applies to the new command. An example is shown in Figure 21. Data *n* + 1 is either the last of a burst of two, or the last desired of a longer burst. The SGRAM does



NOTE: Burst Length = 2.
DQMs are all active (LOW).

Figure 20
WRITE BURST

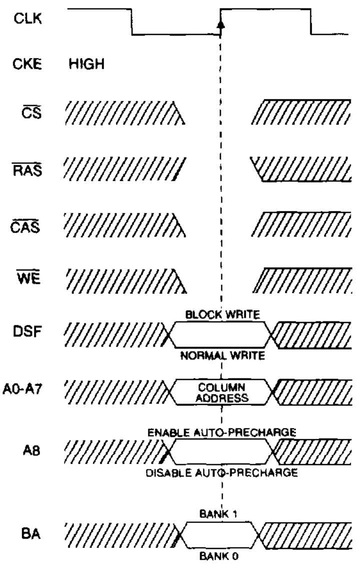
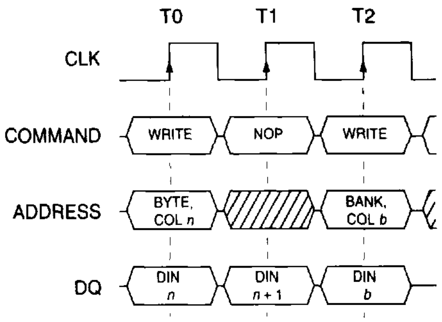


Figure 19
WRITE COMMAND



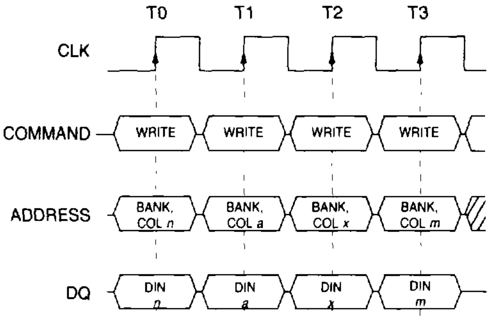
NOTE: DQMs are all active (LOW). The second WRITE can be a BLOCK WRITE, in which case column/byte mask data would be applied to the data inputs.

▨ DON'T CARE

Figure 21
WRITE TO WRITE (OR BLOCK WRITE)

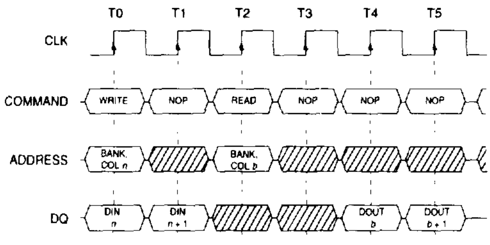
not require the 2*n* rule of prefetch architectures, so a WRITE command can be initiated on any clock cycle following a previous WRITE command. Full speed random write accesses within a page can be performed as shown in Figure 22.

A fixed-length WRITE burst may be followed by, or truncated with, a subsequent READ burst (provided that AUTO PRECHARGE was not activated) and a full-page WRITE burst can be truncated with a subsequent READ burst. Once the READ command is registered, the data inputs will be ignored, and writes will not be executed. An example is shown in Figure 23. Data *n* + 1 is either the last of a burst of two, or the last desired of a longer burst.



NOTE: Covers either successive WRITEs to the active row in a given bank, or to the active rows in different banks. DQMs are all active (LOW).

Figure 22
RANDOM WRITE CYCLES WITHIN A PAGE

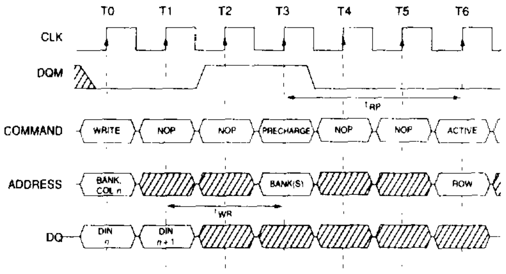


NOTE: Covers either a WRITE and READ to the active row in a given bank, or to the active rows in different banks. DQMs are all active (LOW). READ LATENCY = 2 for illustration.

Figure 23
WRITE TO READ

A fixed-length WRITE burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that AUTO PRECHARGE was not activated) and a full-page WRITE burst may be truncated with a PRECHARGE command to the same bank. The PRECHARGE command should be issued ᵗWR cycles after the clock edge at which the last desired input data element is registered. In addition, the DQM signals must be used to mask input data, starting with the clock edge following the last desired data element and ending with the clock edge on which the PRECHARGE command is entered. An example is shown in Figure 24. Data *n* + 1 is either the last of a burst of two, or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ᵗRP is met.

In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with AUTO PRECHARGE. The disadvantage of the PRECHARGE command is it requires that the command and address busses be available at the appropriate time to issue the command, but the advantage of the PRECHARGE command is that it can be used to truncate fixed-length or full-page bursts. The AUTO PRECHARGE command does not truncate fixed-length bursts and does not apply to full page bursts.



NOTE: The DQMs could remain low in this example if the WRITE burst is a fixed length of 2.

▨ DON'T CARE

Figure 24
WRITE TO PRECHARGE

Fixed-length or full-page WRITE bursts can be truncated with the BURST TERMINATE command. When truncating a WRITE burst, the input data applied one clock edge prior to the BURST TERMINATE command will be the last data written. This is shown in Figure 25, where data *n* + 1 is either the last of a burst of two, or the last desired of a longer burst.

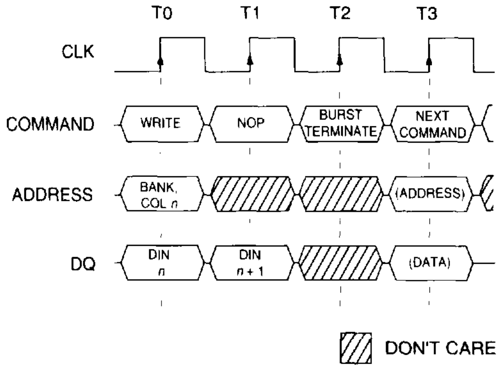


Figure 25
TERMINATING A WRITE BURST

MASKED WRITES

Any WRITE performed to a row that was opened via an ACTIVE with WPB command is a MASKED WRITE (Write-Per-Bit). Data is written to the 32 cells (bits) at the selected column location subject to the mask stored in the WPB mask register. If a particular bit in the WPB mask register is a "0", the data appearing on the corresponding DQ input will be ignored, and the existing data in the corresponding DRAM cell will remain unchanged. If a mask bit is a "1", the data appearing on the corresponding DQ input will be written to the corresponding DRAM cell.

The overall WRITE mask consists of a combination of the DQM inputs, which mask on a per-byte basis, and the WPB mask register, which masks on a per-bit basis. This is shown in Figure 26. If a particular DQM signal was registered HIGH, the corresponding byte will be masked. A given bit is written only if the corresponding DQM signal registered is "0" and the corresponding WPB mask register bit is "1".

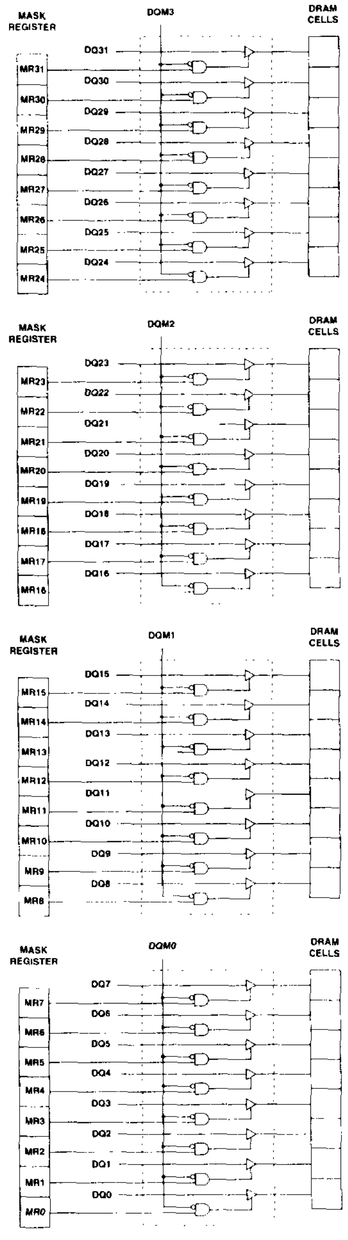


Figure 26
WRITE MASKING – FUNCTIONAL REPRESENTATION

BLOCK WRITES

BLOCK WRITEs are non-burst accesses that write to eight column locations simultaneously. A single data value, which was previously loaded in the color register, is written to the block of eight consecutive column locations addressed by inputs A3-A7. The information on the DQs which is registered coincident with the BLOCK WRITE command is used to mask specific column/byte combinations within the block. The mapping of the DQ inputs to the column/byte combinations is shown in Table 3.

When a "0" is registered on a particular DQ signal coincident with a BLOCK WRITE command, the write to the corresponding column/byte combination is masked (the existing data in the corresponding DRAM cells will remain unchanged). When a "1" is registered, the color register data will be written to the corresponding DRAM cells, subject to the DQM and WPB masking.

The overall BLOCK WRITE mask consists of a combination of the DQM signals, the WPB mask register and the column/byte mask information, as shown in Figure 27. The masking operation provided by the DQM inputs and WPB mask register is similar to that provided in normal WRITEs, with the exception that the mask information is applied simultaneously to all eight columns. Therefore, in a BLOCK WRITE, a given bit is written only if a "0" was registered for the corresponding DQM signal, a "1" was registered for the corresponding DQ signal, and the corresponding bit in the WPB mask register is "1".

A BLOCK WRITE access requires a time period of ^{t}BWC to execute, so in general, the cycle after the BLOCK WRITE command should be a NOP. However, ACTIVE or PRECHARGE commands to the other bank are allowed. When following a BLOCK WRITE with a PRECHARGE command to the same bank, ^{t}BPL (instead of ^{t}BWC) must be met.

Table 3
MAPPING OF DQs TO COLUMN/BYTE LOCATIONS WITHIN A BLOCK

DQ INPUTS	COLUMN-ADDRESS CONTROLLED			DQ PLANES CONTROLLED
	A2	A1	A0	
DQ0	0	0	0	0-7
DQ1	0	0	1	0-7
DQ2	0	1	0	0-7
DQ3	0	1	1	0-7
DQ4	1	0	0	0-7
DQ5	1	0	1	0-7
DQ6	1	1	0	0-7
DQ7	1	1	1	0-7
DQ8	0	0	0	8-15
DQ9	0	0	1	8-15
DQ10	0	1	0	8-15
DQ11	0	1	1	8-15
DQ12	1	0	0	8-15
DQ13	1	0	1	8-15
DQ14	1	1	0	8-15
DQ15	1	1	1	8-15
DQ16	0	0	0	16-23
DQ17	0	0	1	16-23
DQ18	0	1	0	16-23
DQ19	0	1	1	16-23
DQ20	1	0	0	16-23
DQ21	1	0	1	16-23
DQ22	1	1	0	16-23
DQ23	1	1	1	16-23
DQ24	0	0	0	24-31
DQ25	0	0	1	24-31
DQ26	0	1	0	24-31
DQ27	0	1	1	24-31
DQ28	1	0	0	24-31
DQ29	1	0	1	24-31
DQ30	1	1	0	24-31
DQ31	1	1	1	24-31

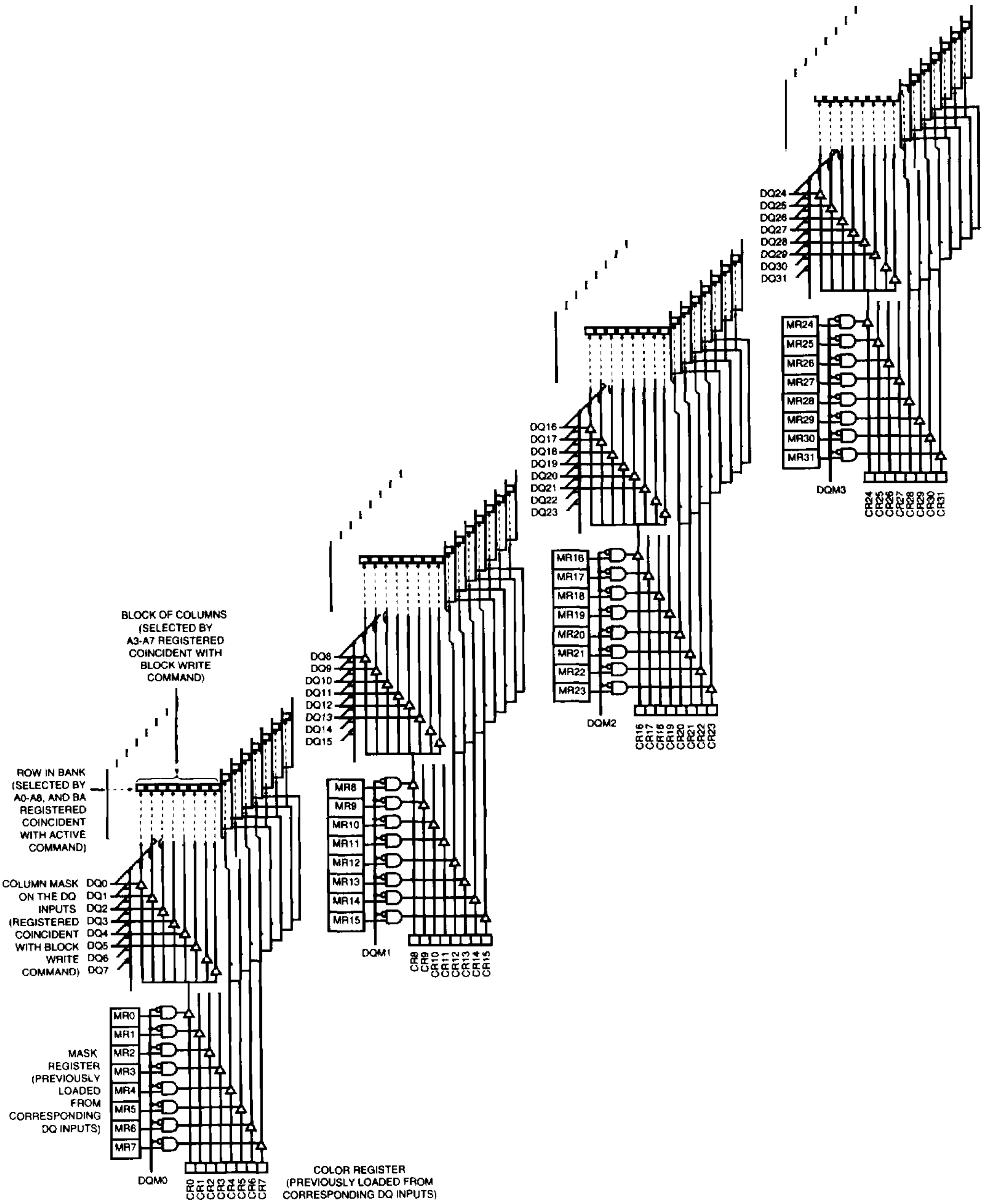


Figure 27
BLOCK WRITE MASKING – FUNCTIONAL REPRESENTATION

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank, or the open row in both banks. The bank(s) will be available for a subsequent row access some specified time (^{t}RP) after the precharge command is issued. Input A8 determines whether one or both banks are to be precharged, and in the case where only one bank is to be precharged, input BA selects the bank. Otherwise BA is treated as a "don't care". Once a bank has been precharged, it is in the idle state and must be activated prior to any READ, WRITE or BLOCK WRITE commands being issued to that bank.

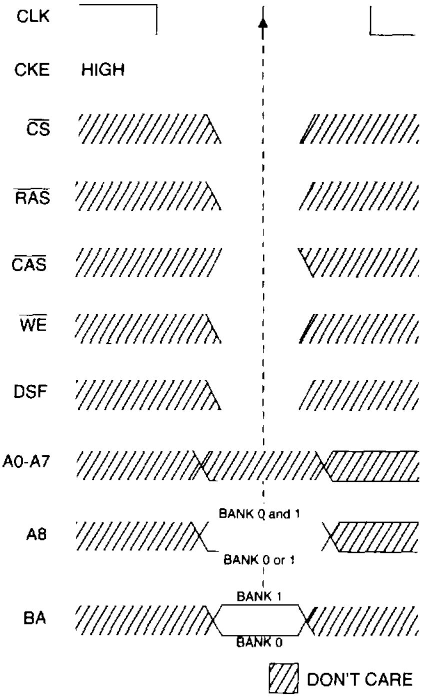


Figure 28
PRECHARGE COMMAND

POWER-DOWN

POWER-DOWN occurs when both banks are in the idle state (precharged) and CKE is registered LOW (see Figure 29). Entering POWER-DOWN deactivates the input and output buffers, excluding CKE, for maximum power savings while in standby. The device may not remain in the POWER-DOWN state longer than the refresh period (17ms) since the command does not perform any refresh operations.

The POWER-DOWN state is exited by taking CKE back HIGH. CKE must go HIGH ^{t}CKS before a positive clock edge, after meeting ^{t}CKH from the previous clock edge. The first command after exiting POWER-DOWN will be registered on the clock edge following ^{t}CKS.

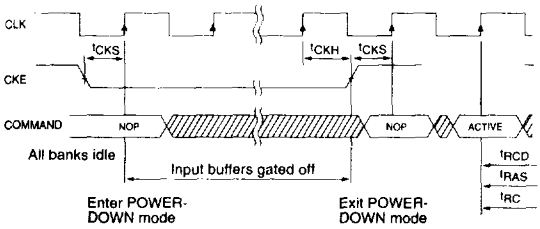


Figure 29
POWER-DOWN

TRUTH TABLE 2 – CKE

(Notes 1-4)

CKE_{n-1}	CKE_n	CURRENT STATE	$COMMAND_n$	$ACTION_n$	NOTES
L	L	POWER-DOWN	X	Maintain POWER-DOWN	
		SELF REFRESH	X	Maintain SELF REFRESH	6
L	H	POWER-DOWN	COMMAND INHIBIT or NOP	Exit POWER-DOWN	7
		SELF REFRESH	COMMAND INHIBIT or NOP	Exit SELF REFRESH	6, 8
H	L	Both Banks Idle	COMMAND INHIBIT or NOP	POWER-DOWN Entry	
		Both Banks Idle	AUTO REFRESH	SELF REFRESH Entry	5
H	H		See Truth Table 3		

NOTE:
1. CKE_n is the logic state of CKE at clock edge n; CKE_{n-1} was the state of CKE at the previous clock edge.
2. CURRENT STATE is the state of the SGRAM immediately prior to clock edge n.
3. $COMMAND_n$ is the command registered at clock edge n and $ACTION_n$ is a result of $COMMAND_n$.
4. All states and sequences not shown are illegal or reserved.
5. Illegal on non "S" devices.
6. Not available on non "S" devices.
7. Exiting POWER-DOWN at clock edge n will put the device in the "all banks idle" state in time for clock edge n+1.
8. Exiting SELF REFRESH at clock edge n will put the device in the "all banks idle" state once ^{t}XSR is met. COMMAND INHIBIT or NOP commands should be issued on any clock edges occuring during the ^{t}XSR period.

TRUTH TABLE 3 – Current State

(Notes 1-4; notes appear on next page)

CURRENT STATE	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	DSF	COMMAND/ACTION	NOTES
Any	H	X	X	X	X	COMMAND INHIBIT (NOP/ continue previous operation)	
	L	H	H	H	L	NO OPERATION (NOP/ continue previous operation)	
Idle	L	L	H	H	L	ACTIVE (Select bank and activate row)	
	L	L	H	H	H	ACTIVE w/WPB (Select bank, activate row and WPB)	
	L	L	L	H	L	AUTO REFRESH	5
	L	L	L	L	L	LOAD MODE REGISTER	5
	L	L	L	L	H	LOAD SPECIAL MODE REGISTER	6
Row Active	L	H	L	H	L	READ (Select bank and column and start READ burst)	7
	L	H	L	L	L	WRITE (Select bank and column and start WRITE burst)	7
	L	H	L	L	H	BLOCK WRITE (Select bank & column and start BLOCK WRITE access	7
	L	L	H	L	L	PRECHARGE (Deactivate row in bank or banks)	8
	L	L	L	L	H	LOAD SPECIAL MODE REGISTER	6
READ (AUTO-PRECHARGE DISABLED)	L	H	L	H	L	READ (Select bank and column and start new READ burst)	7
	L	H	L	L	L	WRITE (Select bank and column and start WRITE burst)	7
	L	H	L	L	H	BLOCK WRITE (Select bank & column and start BLOCK WRITE access)	7
	L	L	H	L	L	PRECHARGE (Truncate READ burst, start precharge)	8
	L	H	H	L	L	BURST TERMINATE	9
WRITE (AUTO-PRECHARGE DISABLED)	L	H	L	H	L	READ (Select bank and column and start READ burst)	7
	L	H	L	L	L	WRITE (Select bank and column and start new WRITE burst)	7
	L	H	L	L	H	BLOCK WRITE (Select bank & column and start BLOCK WRITE access)	7
	L	L	H	L	L	PRECHARGE (Truncate WRITE burst, start precharge)	8
	L	H	H	L	L	BURST TERMINATE	9

NOTE:

1. This table applies when CKE$_{n-1}$ was HIGH and CKE$_n$ is HIGH (see Truth Table 2) and after ^{t}XSR has been met (if the previous state was SELF REFRESH).
2. This table is bank specific, except where noted; i.e., the CURRENT STATE is for a specific bank and the commands shown are those allowed to be issued to that bank, when in that state. Exceptions are covered in the notes below.
3. CURRENT STATE definitions:
   - Idle: the bank has been precharged and ^{t}RP has been met.
   - Row Active: a row in the bank has been activated and ^{t}RCD has been met. No data bursts/ accesses and no register accesses are in progress.
   - Read: a READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
   - Write: a WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occuring during these states. Allowable commands to the other bank are determined by it's CURRENT STATE; refer to Truth Table 3 and these notes.
   - Precharging: Starts with registration of a PRECHARGE command and ends when ^{t}RP is met. Once ^{t}RP is met, the bank will be in the Idle state.
   - Row Activating: Starts with registration of an ACTIVE command and ends when ^{t}RCD is met. Once ^{t}RCD is met, the bank will be in the Row Active state.
   - Read/Precharge: Starts with registration of a READ command with AUTO PRECHARGE enabled, and ends when ^{t}RP has been met. Once ^{t}RP is met, the bank will be in the Idle state.
   - Write/Precharge: Starts with registration of a WRITE command with AUTO PRECHARGE enabled, and ends when ^{t}RP has been met. Once ^{t}RP is met, the bank will be in the Idle state.
   - Block Write/ Precharge: Starts with registration of a BLOCK WRITE command with AUTO PRECHARGE enabled, and ends when ^{t}RP has been met. Once ^{t}RP is met, the bank will be in the Idle state.
   - Block Write: Starts with registration of a BLOCK WRITE command and ends when either ^{t}BPL or ^{t}BWC has been met. ^{t}BPL applies when the BLOCK WRITE is to be followed by a PRECHARGE and ^{t}BWC applies when it is to be followed by any other allowable command. Once ^{t}BWC is met, the bank will be in the Row Active state.
   - Refreshing: Starts with registration of an AUTO REFRESH command and ends when ^{t}RC is met. Once ^{t}RC is met, the SGRAM will be in the "all banks idle" state.
   - Accessing Mode Register: Starts with registration of a LOAD MODE REGISTER command, and ends when ^{t}MTC has been met. Once ^{t}MTC is met, the SGRAM will be in the "all banks idle" state.
   - Accessing Special Mode Register: Starts with registration of a LOAD SPECIAL MODE REGISTER command, and ends when ^{t}SML has been met.
5. Requires that both banks are idle.
6. Requires that the other bank is either idle or in the Row Active state.
7. READ, WRITE and BLOCK WRITE accesses will interact between banks as they do within a bank.
8. If both banks are to be precharged, both must be in a valid state for precharging.
9. BURST TERMINATE is not bank specific; it affects the most recent READ or WRITE burst, regardless of bank.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC}/V_{CCQ} supply relative to V_{SS}	-1V to +4.6V
Voltage on Inputs, NC or I/O pins relative to V_{SS}	-1V to +4.6V
Operating Temperature, T_A (ambient)	0°C to +70°C
Storage Temperature (plastic)	-55°C to +150°C
Power Dissipation	1W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Note: 1) (0°C ≤ T_A ≤ 70°C; V_{CC}/V_{CCQ} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}/V_{CCQ}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.0	V_{CC}+0.3	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-0.3	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{CC} (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ V_{OUT} ≤ V_{CCQ})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)	V_{OL}		0.4	V	

Icc SPECIFICATIONS AND CONDITIONS

(Note: 1, 14) (0°C ≤ T_A ≤ 70°C; V_{CC}/V_{CCQ} = +3.3V ±0.3V)

		MAX				
PARAMETER/CONDITION	SYMBOL	-10	-12	-15	UNITS	NOTES
SELF REFRESH CURRENT: CKE ≤ 0.2V (S version only)	I_{CC1} (S only)	TBD	TBD	TBD	µA	5
STANDBY CURRENT: POWER-DOWN mode, CKE ≤ V_{IL} (MAX), both banks idle	I_{CC2} I_{CC2} (S only)	TBD TBD	TBD TBD	TBD TBD	mA µA	
STANDBY CURRENT: $\overline{CS}$ ≥ V_{IH} (MIN), ^tCK ≥ ^tCK (MIN), CKE ≥ V_{IH} (MIN), both banks idle	I_{CC3}	TBD	TBD	TBD	mA	3, 4, 13
STANDBY CURRENT: $\overline{CS}$ ≥ V_{IH} (MIN), ^tCK ≥ ^tCK (MIN), CKE ≥ V_{IH} (MIN), both banks active after ^tRCD met	I_{CC4}	TBD	TBD	TBD	mA	3, 4, 13
AUTO REFRESH CURRENT (^tRC = 16.6µs)	I_{CC5}	TBD	TBD	TBD	mA	4
OPERATING CURRENT: ACTIVE mode, burst = 2, READ or WRITE, ^tRC ≥ ^tRC (MIN), one bank active	I_{CC6}	TBD	TBD	TBD	mA	3, 4
OPERATING CURRENT: ACTIVE mode, burst = 2, READ or WRITE, ^tRC ≥ ^tRC (MIN), two banks active	I_{CC7}	TBD	TBD	TBD	mA	3, 4
OPERATING CURRENT: BURST mode, full-page burst after ^tRCD met READ or WRITE, ^tCK ≥ ^tCK (MIN), other bank idle	I_{CC8}	TBD	TBD	TBD	mA	3, 4

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A8, BA	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM, CLK, CKE, $\overline{CS}$, DSF	C_{I2}	5	pF	2
Input/Output Capacitance: DQs	C_{IO}	7	pF	2

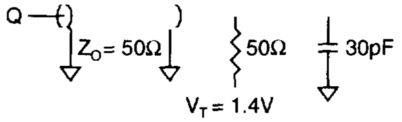
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 8, 9, 10, 12) ($0°C \leq T_A \leq +70°C$) Listed alphabetically by symbol subscript.

AC CHARACTERISTICS		-10		-12		-15			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from CLK (pos. edge)	^{t}AC		9		11		13	ns	
Address hold time	^{t}AH	1		1.5		2		ns	
Address setup time	^{t}AS	3		3.5		4		ns	
BLOCK WRITE to PRECHARGE delay	^{t}BPL	3		3		3		^{t}CK	
BLOCK WRITE cycle time	^{t}BWC	2		2		2		^{t}CK	
$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DSF, DQM hold time	^{t}CH	1		1.5		2		ns	
CLK high level width	^{t}CHI	3.5		4		5		ns	
System clock cycle time	^{t}CK	10		12		15		ns	
CKE hold time	^{t}CKH	1		1.5		2		ns	
CKE setup time	^{t}CKS	3		3.5		4		ns	
CLK low level width	^{t}CL	3.5		4		5		ns	
$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DSF, DQM setup time	^{t}CS	3		3.5		4		ns	
Data-in hold time	^{t}DH	1		1.5		2		ns	
Data-in setup time	^{t}DS	3		3.5		4		ns	
Data-out high-impedance time	^{t}HZ	4	10	4	10	4	10	ns	11
Data-out low-impedance time	^{t}LZ	3		3		3		ns	
LOAD MODE REGISTER command to command	^{t}MTC	2		2		2		^{t}CK	
Data-out hold time	^{t}OH	4		4		4		ns	
ACTIVE to PRECHARGE command period	^{t}RAS	60	120K	72	120K	90	120K	ns	
AUTO REFRESH and ACTIVE to ACTIVE command period	^{t}RC	90		108		135		ns	
ACTIVE to READ, WRITE or BLOCK WRITE delay	^{t}RCD	30		36		45		ns	
Refresh period (1,024 cycles)	^{t}REF		17		17		17	ms	7
PRECHARGE command period	^{t}RP	30		36		45		ns	
ACTIVE bank A to ACTIVE bank B command period	^{t}RRD	30		36		45		ns	
LOAD SPECIAL MODE REGISTER command to command	^{t}SML	2		2		2		^{t}CK	
Transition time	^{t}T	1	30	1	30	1	30	ns	
Write recovery time	^{t}WR	2		2		2		^{t}CK	
Exit SELF REFRESH to ACTIVE command	^{t}XSR	90		108		135		ns	

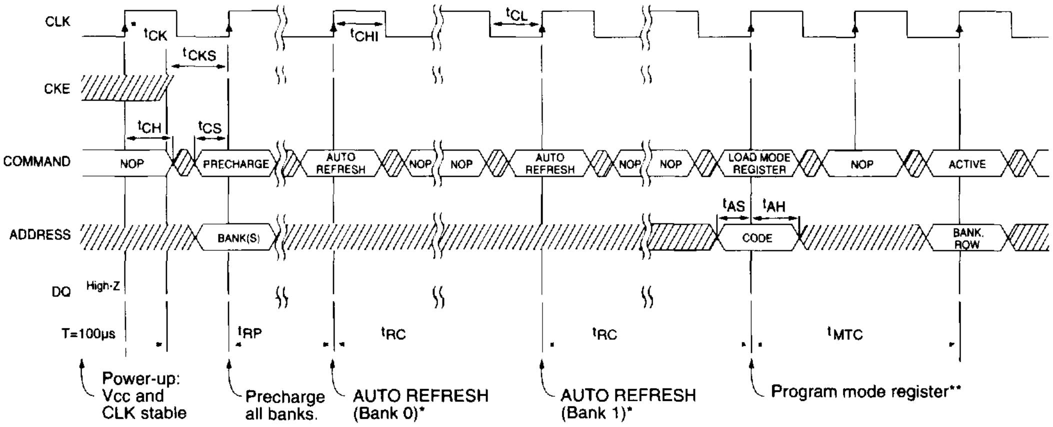
NOTES

1. All voltages referenced to VSS.
2. This parameter is sampled. VCC/VCCQ = +3.3V ±0.3V; f = 1 MHz.
3. ICC is dependent on cycle rates.
4. ICC is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands before proper device operation is assured. The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 1ns.
9. In addition to meeting the transition rate specification, the clock and CKE must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
10. Outputs measured at 1.4V with equivalent load:



11. ^{t}HZ defines the time at which the output achieves the open circuit condition; it is not a reference to VOH or VOL.
12. AC timing tests have VIL = 0V and VIH = 3.0V with timing referenced to 1.4V crossover point.
13. All other inputs at CMOS levels.
14. ICC specifications are tested after the device is properly initialized.

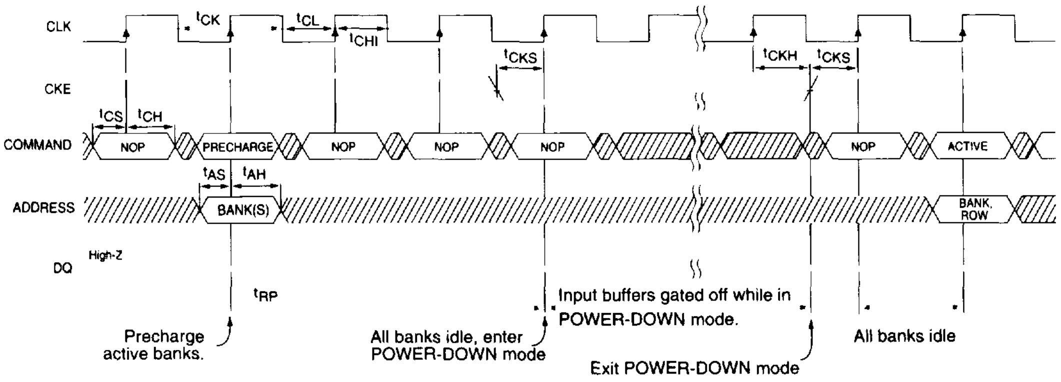
INITIALIZE AND LOAD MODE REGISTER



*Starts at Bank 0 and alternates banks.

**The mode register may be loaded prior to the AUTO REFRESH cycles if desired.

POWER-DOWN MODE



▨ DON'T CARE

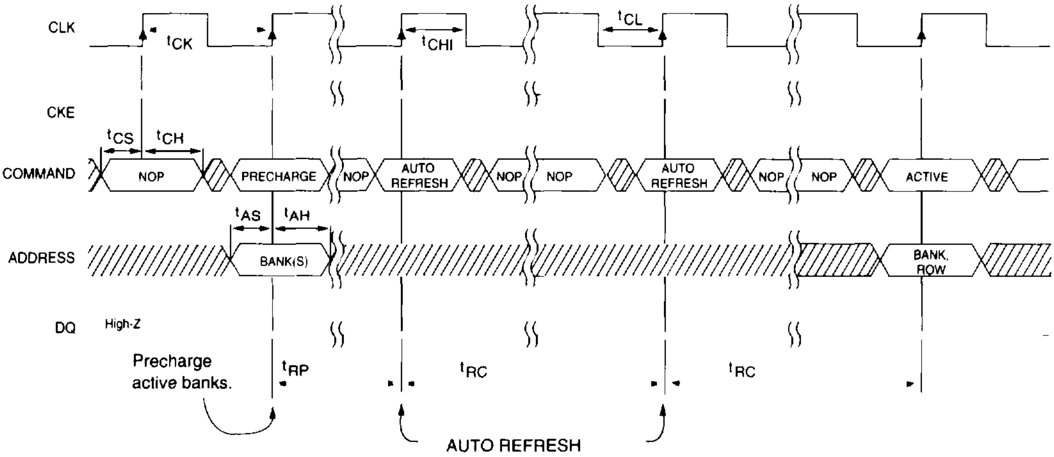
▩ UNDEFINED

NOTE: Violating refresh requirements during power-down may result in a loss of data.

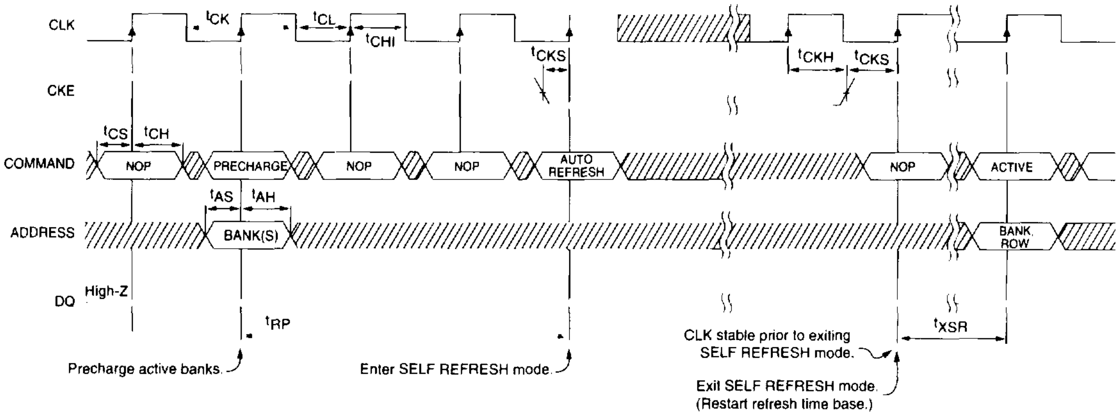
TIMING PARAMETERS

	-10		-12		-15				-10		-12		-15		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
tAH	1		1.5		2		ns	tCKS	3		3.5		4		ns
tAS	3		3.5		4		ns	tCL	3.5		4		5		ns
tCH	1		1.5		2		ns	tCS	3		3.5		4		ns
tCHI	3.5		4		5		ns	tMTC	2		2		2		tCK
tCK	10		12		15		ns	tRC	90		108		135		ns
tCKH	1		1.5		2		ns	tRP	30		36		45		ns

AUTO REFRESH MODE



SELF REFRESH MODE



▨ DON'T CARE

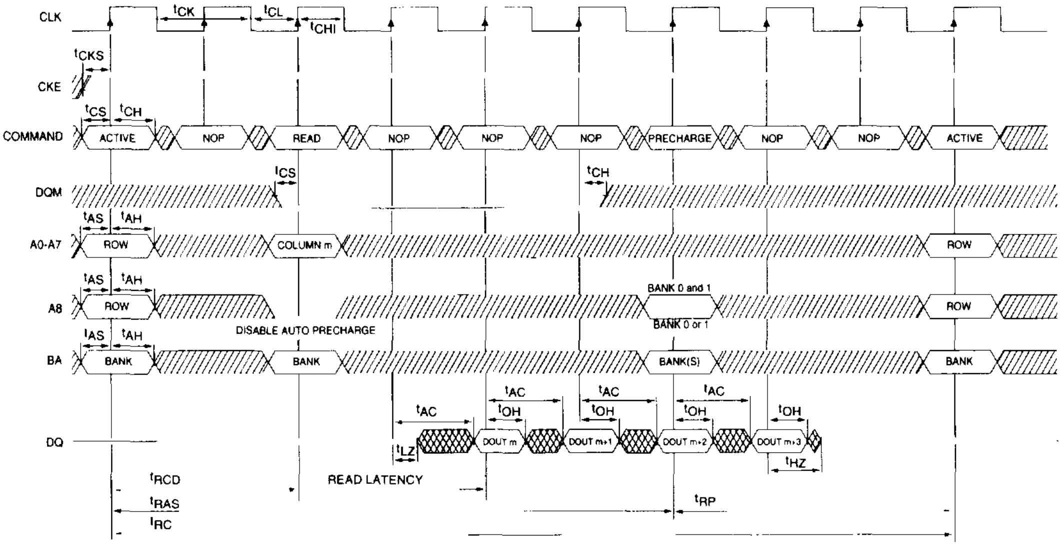
▩ UNDEFINED

TIMING PARAMETERS

	-10		-12		-15		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
^tAH	1		1.5		2		ns
^tAS	3		3.5		4		ns
^tCH	1		1.5		2		ns
^tCHI	3.5		4		5		ns
^tCK	10		12		15		ns
^tCKH	1		1.5		2		ns

	-10		-12		-15		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
^tCKS	3		3.5		4		ns
^tCL	3.5		4		5		ns
^tCS	3		3.5		4		ns
^tRC	90		108		135		ns
^tRP	30		36		45		ns
^tXSR	90		108		135		ns

READ – WITHOUT AUTO PRECHARGE



NOTE: For this example, the BURST LENGTH = 4, the READ LATENCY = 2 and the READ burst is followed by a "manual" PRECHARGE.

▨ DON'T CARE

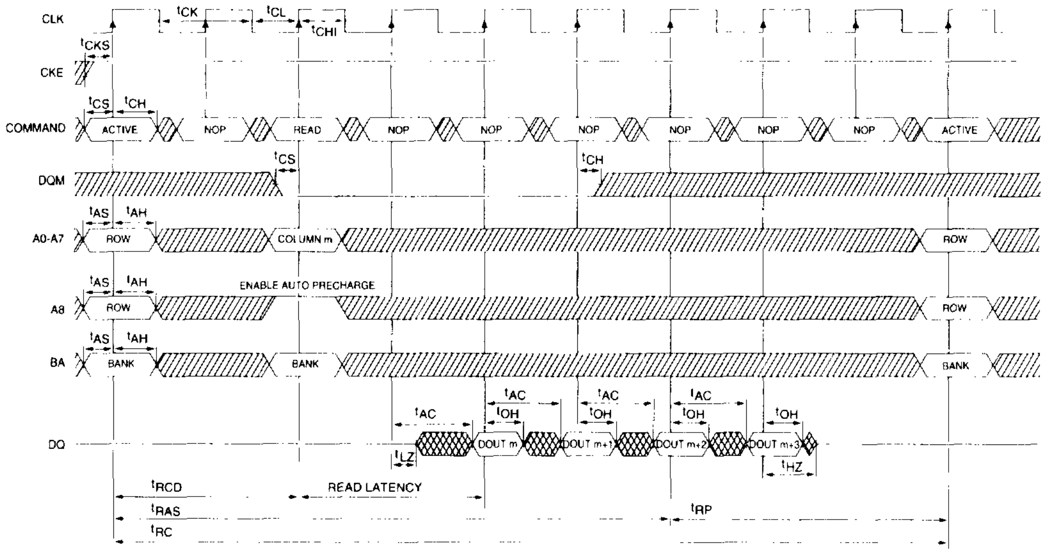
▩ UNDEFINED

TIMING PARAMETERS

SYM	-10 MIN	-10 MAX	-12 MIN	-12 MAX	-15 MIN	-15 MAX	UNITS
^{t}AC		9		11		13	ns
^{t}AH	1		1.5		2		ns
^{t}AS	3		3.5		4		ns
^{t}CH	1		1.5		2		ns
^{t}CHI	3.5		4		5		ns
^{t}CK	10		12		15		ns
^{t}CKS	3		3.5		4		ns
^{t}CL	3.5		4		5		ns

SYM	-10 MIN	-10 MAX	-12 MIN	-12 MAX	-15 MIN	-15 MAX	UNITS
^{t}CS	3		3.5		4		ns
^{t}HZ	4	10	4	10	4	10	ns
^{t}LZ	3		3		3		ns
^{t}OH	4		4		4		ns
^{t}RAS	60	120K	72	120K	90	120K	ns
^{t}RC	90		108		135		ns
^{t}RCD	30		36		45		ns
^{t}RP	30		36		45		ns

READ – WITH AUTO PRECHARGE



NOTE: For this example, the BURST LENGTH = 4, and the READ LATENCY = 2.

▨ DON'T CARE

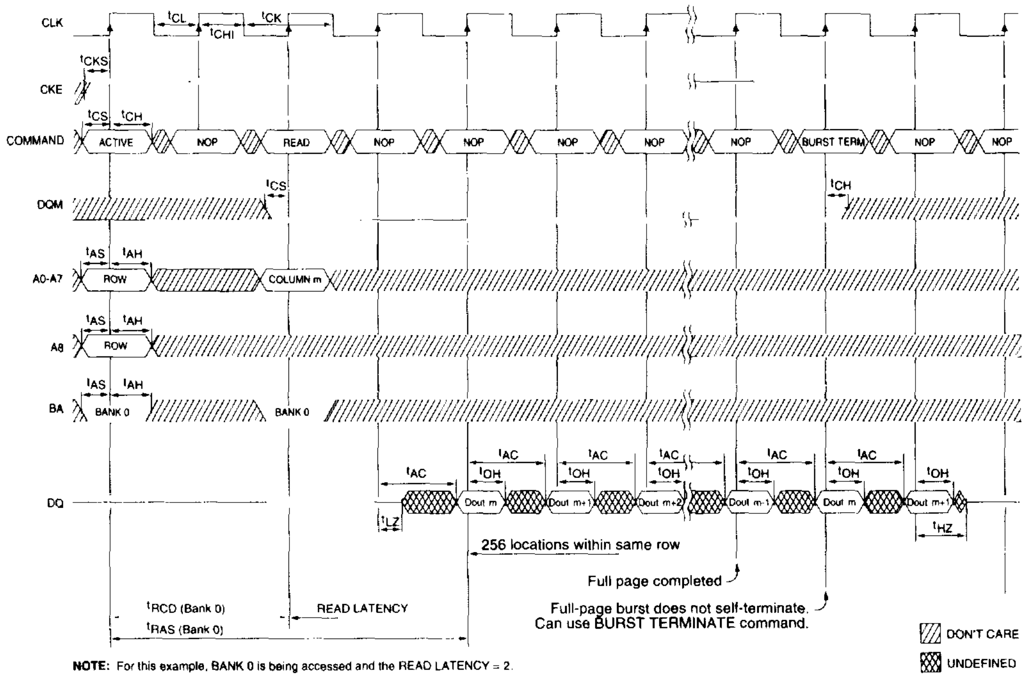
▩ UNDEFINED

TIMING PARAMETERS

SYM	-10 MIN	-10 MAX	-12 MIN	-12 MAX	-15 MIN	-15 MAX	UNITS
^{t}AC		9		11		13	ns
^{t}AH	1		1.5		2		ns
^{t}AS	3		3.5		4		ns
^{t}CH	1		1.5		2		ns
^{t}CHI	3.5		4		5		ns
^{t}CK	10		12		15		ns
^{t}CKS	3		3.5		4		ns
^{t}CL	3.5		4		5		ns

SYM	-10 MIN	-10 MAX	-12 MIN	-12 MAX	-15 MIN	-15 MAX	UNITS
^{t}CS	3		3.5		4		ns
^{t}HZ	4	10	4	10	4	10	ns
^{t}LZ	3		3		3		ns
^{t}OH	4		4		4		ns
^{t}RAS	60	120K	72	120K	90	120K	ns
^{t}RC	90		108		135		ns
^{t}RCD	30		36		45		ns
^{t}RP	30		36		45		ns

READ – FULL-PAGE BURST



256 locations within same row

Full page completed

Full-page burst does not self-terminate. Can use BURST TERMINATE command.

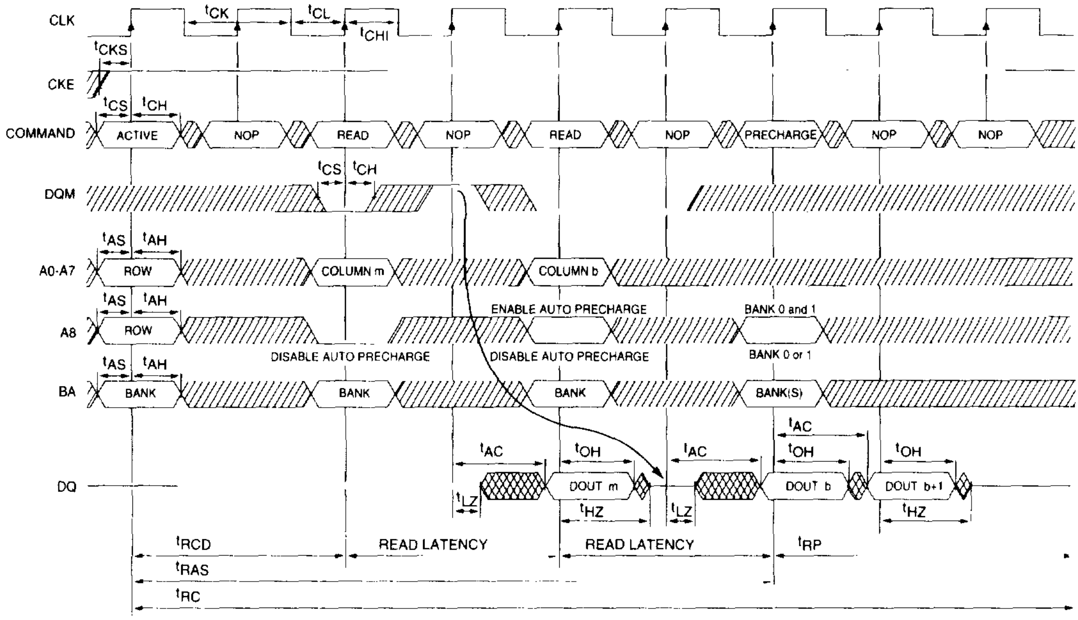
NOTE: For this example, BANK 0 is being accessed and the READ LATENCY = 2.

TIMING PARAMETERS

	-10		-12		-15		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
tAC		9		11		13	ns
tAH	1		1.5		2		ns
tAS	3		3.5		4		ns
tCH	1		1.5		2		ns
tCHI	3.5		4		5		ns
tCK	10		12		15		ns
tCKS	3		3.5		4		ns

	-10		-12		-15		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
tCL	3.5		4		5		ns
tCS	3		3.5		4		ns
tHZ	4	10	4	10	4	10	ns
tLZ	3		3		3		ns
tOH	4		4		4		ns
tRAS	60	120K	72	120K	90	120K	ns
tRCD	30		36		45		ns

READ – DQM OPERATION



NOTE: For this example, the BURST LENGTH = 2 and the READ LATENCY = 2.

▨ DON'T CARE

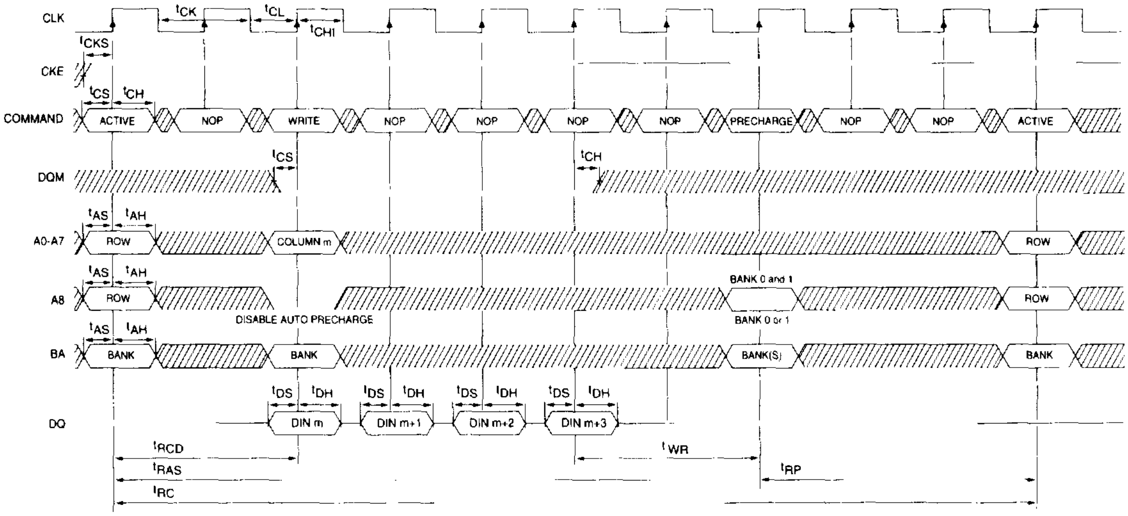
▩ UNDEFINED

TIMING PARAMETERS

	-10		-12		-15		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
^tAC		9		11		13	ns
^tAH	1		1.5		2		ns
^tAS	3		3.5		4		ns
^tCH	1		1.5		2		ns
^tCHI	3.5		4		5		ns
^tCK	10		12		15		ns
^tCKS	3		3.5		4		ns
^tCL	3.5		4		5		ns

	-10		-12		-15		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
^tCS	3		3.5		4		ns
^tHZ	4	10	4	10	4	10	ns
^tLZ	3		3		3		ns
^tOH	4		4		4		ns
^tRAS	60	120K	72	120K	90	120K	ns
^tRC	90		108		135		ns
^tRCD	30		36		45		ns
^tRP	30		36		45		ns

WRITE – WITHOUT AUTO PRECHARGE



NOTE: For this example, the BURST LENGTH = 4 and the WRITE burst is followed by a "manual" PRECHARGE.

▨ DON'T CARE

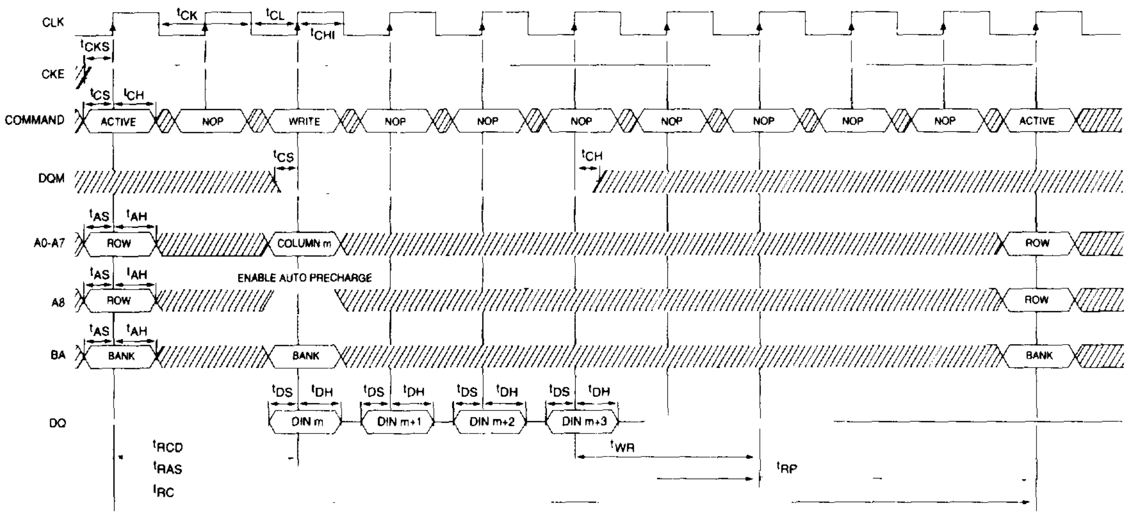
▩ UNDEFINED

TIMING PARAMETERS

	-10		-12		-15		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
tAH	1		1.5		2		ns
tAS	3		3.5		4		ns
tCH	1		1.5		2		ns
tCHI	3.5		4		5		ns
tCK	10		12		15		ns
tCKS	3		3.5		4		ns
tCL	3.5		4		5		ns
tCS	3		3.5		4		ns

	-10		-12		-15		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
tDH	1		1.5		2		ns
tDS	3		3.5		4		ns
tRAS	60	120K	72	120K	90	120K	ns
tRC	90		108		135		ns
tRCD	30		36		45		ns
tRP	30		36		45		ns
tWR	2		2		2		tCK

WRITE – WITH AUTO PRECHARGE



NOTE: For this example, the BURST LENGTH = 4.

▨ DON'T CARE

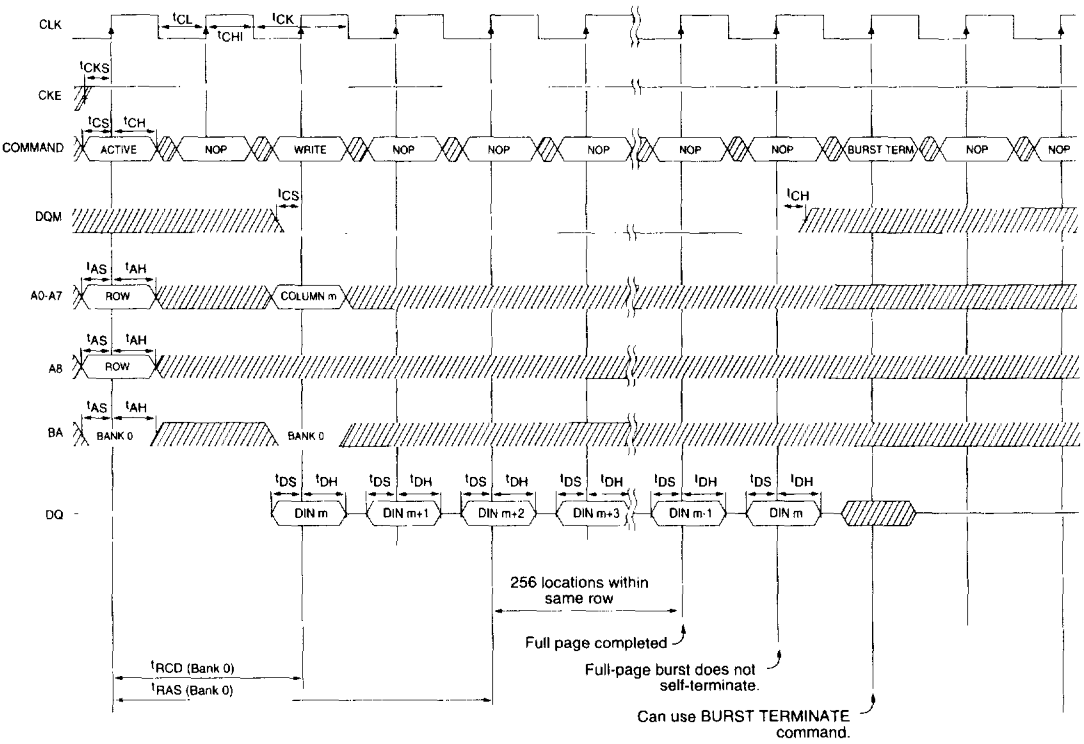
▩ UNDEFINED

TIMING PARAMETERS

	-10		-12		-15		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
^{t}AH	1		1.5		2		ns
^{t}AS	3		3.5		4		ns
^{t}CH	1		1.5		2		ns
^{t}CHI	3.5		4		5		ns
^{t}CK	10		12		15		ns
^{t}CKS	3		3.5		4		ns
^{t}CL	3.5		4		5		ns
^{t}CS	3		3.5		4		ns

	-10		-12		-15		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
^{t}DH	1		1.5		2		ns
^{t}DS	3		3.5		4		ns
^{t}RAS	60	120K	72	120K	90	120K	ns
^{t}RC	90		108		135		ns
^{t}RCD	30		36		45		ns
^{t}RP	30		36		45		ns
^{t}WR	2		2		2		^{t}CK

WRITE – FULL-PAGE BURST



NOTE: For this example, BANK 0 is being accessed.

▨ DON'T CARE

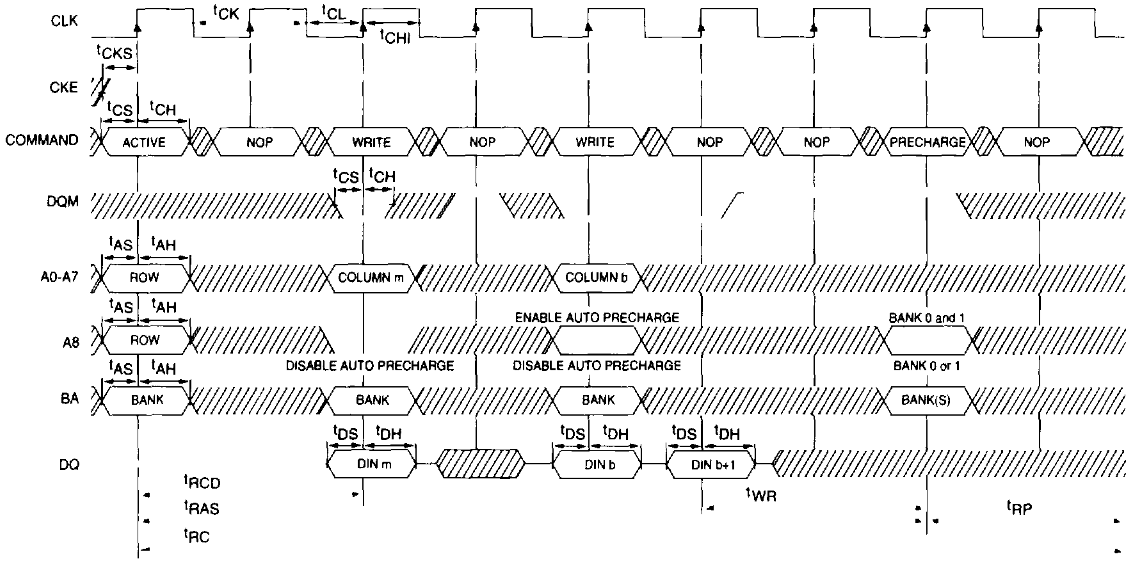
▩ UNDEFINED

TIMING PARAMETERS

	-10		-12		-15		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
^tAH	1		1.5		2		ns
^tAS	3		3.5		4		ns
^tCH	1		1.5		2		ns
^tCHI	3.5		4		5		ns
^tCK	10		12		15		ns
^tCKS	3		3.5		4		ns

	-10		-12		-15		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
^tCL	3.5		4		5		ns
^tCS	3		3.5		4		ns
^tDH	1		1.5		2		ns
^tDS	3		3.5		4		ns
^tRAS	60	120K	72	120K	90	120K	ns
^tRCD	30		36		45		ns

WRITE – DQM OPERATION



NOTE: For this example, the BURST LENGTH = 2.

▨ DON'T CARE

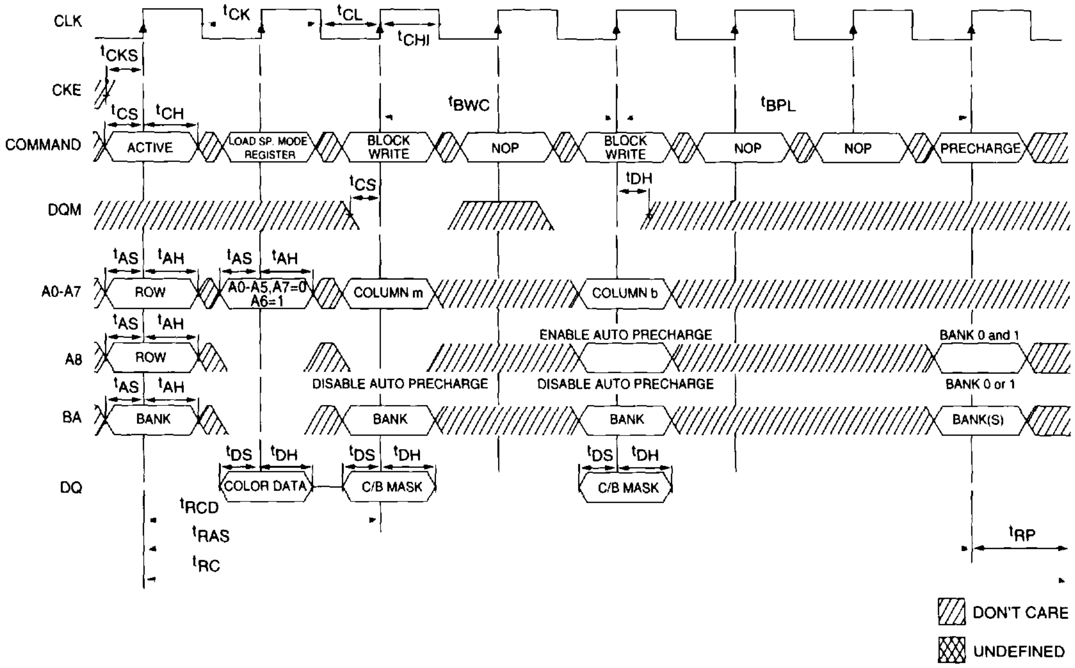
▩ UNDEFINED

TIMING PARAMETERS

	-10		-12		-15		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
^{t}AH	1		1.5		2		ns
^{t}AS	3		3.5		4		ns
^{t}CH	1		1.5		2		ns
^{t}CHI	3.5		4		5		ns
^{t}CK	10		12		15		ns
^{t}CKS	3		3.5		4		ns
^{t}CL	3.5		4		5		ns
^{t}CS	3		3.5		4		ns

	-10		-12		-15		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
^{t}DH	1		1.5		2		ns
^{t}DS	3		3.5		4		ns
^{t}RAS	60	120K	72	120K	90	120K	ns
^{t}RC	90		108		135		ns
^{t}RCD	30		36		45		ns
^{t}RP	30		36		45		ns
^{t}WR	2		2		2		^{t}CK

BLOCK WRITE



TIMING PARAMETERS

	-10		-12		-15		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
tAH	1		1.5		2		ns
tAS	3		3.5		4		ns
tBPL	3		3		3		tCK
tBWC	2		2		2		tCK
tCH	1		1.5		2		ns
tCHI	3.5		4		5		ns
tCK	10		12		15		ns
tCKS	3		3.5		4		ns

	-10		-12		-15		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
tCL	3.5		4		5		ns
tCS	3		3.5		4		ns
tDH	1		1.5		2		ns
tDS	3		3.5		4		ns
tRAS	60	120K	72	120K	90	120K	ns
tRC	90		108		135		ns
tRCD	30		36		45		ns
tRP	30		36		45		ns