National Semiconductor

54ABT/74ABT2952C
Octal Registered Transceiver

General Description

The 'ABT2952C is an octal registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and TRI-STATE® output enable signals are provided for each register. The output pins are guaranteed to source 32 mA (24 mA mil.) and to sink 64 mA (48 mA mil).

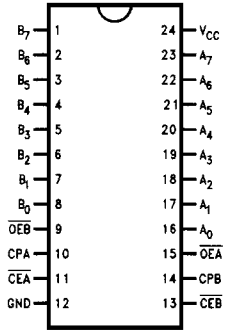
Features

- Separate clock, clock enable and TRI-STATE output enable provided for each register
- A and B output sink capability of 64 mA source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

Ordering Code: See Section 10

Connection Diagrams

Pin Assignment for DIP, SOIC, SSOP and Flatpak



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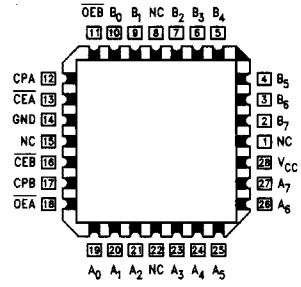
Pin Assignment for LCC



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Pin Descriptions

Pin Names	Description
A_0–A_7	A-Register Inputs/B-Register TRI-STATE Outputs
B_0–B_7	B-Register Inputs/A-Register TRI-STATE Outputs
$\overline{OEA}$	Output Enable A-Register
CPA	A-Register Clock
$\overline{CEA}$	A-Register Clock Enable
$\overline{OEB}$	Output Enable B-Register
CPB	B-Register Clock
$\overline{CEB}$	B-Register Clock Enable

Pin Descriptions (Continued)

Output Control

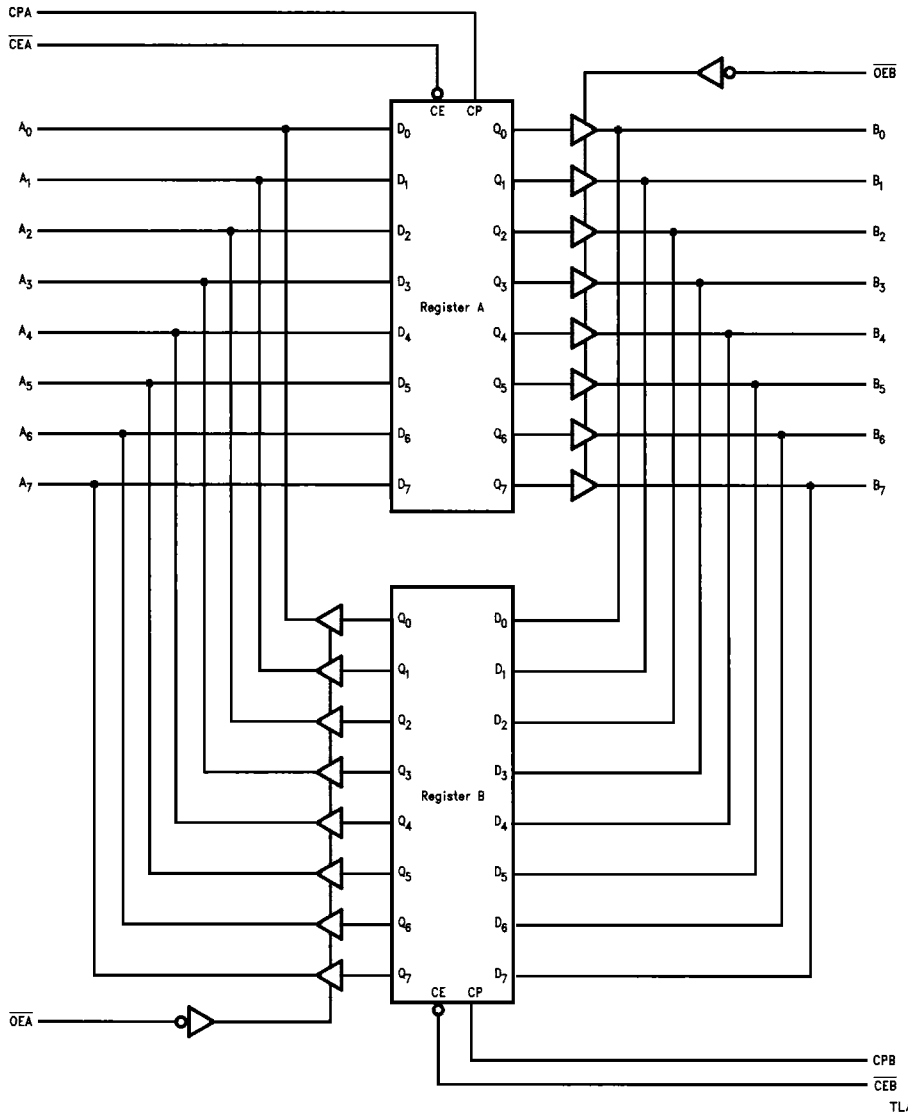
$\overline{OE}$	Internal Q	Output 'ABT2952C	Function
H	X	Z	Disable Outputs
L	L	L	Enable Outputs
L	H	H	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance
⌐‾ = LOW-to-HIGH Transition
NC = No Change

Register Function Table (Applies to A or B Register)

Inputs			Internal Q	Function
D	CP	$\overline{CE}$		
X	X	H	NC	Hold Data
L	⌐‾	L	L	Load Data
H	⌐‾	L	H	

Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

DC Electrical Characteristics

Symbol	Parameter	ABT2952C Min	ABT2952C Typ	ABT2952C Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage 54ABT/74ABT	2.5			V	Min	I_{OH} = −3 mA (A_n, B_n)
	54ABT	2.0					I_{OH} = −24 mA (A_n, B_n)
	74ABT	2.0					I_{OH} = −32 mA (A_n, B_n)
V_{OL}	Output LOW Voltage 54ABT			0.55	V	Min	I_{OL} = 48 mA (A_n, B_n)
	74ABT			0.55			I_{OL} = 64 mA (A_n, B_n)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA (Non-I/O Pins) All Other Pins Grounded
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V (Non-I/O Pins) (Note 2) V_{IN} = V_{CC} (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V (Non-I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	μA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current			−5	μA	Max	V_{IN} = 0.5V (Non-I/O Pins) (Note 2) V_{IN} = 0.0V (Non-I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current			50	μA	0V–5.5V	V_{OUT} = 2.7V (A_n, B_n); $\overline{OEA}$ or $\overline{OEB}$ = 2.0V
I_{IL} + I_{OZL}	Output Leakage Current			−50	μA	0V–5.5V	V_{OUT} = 0.5V (A_n, B_n); $\overline{OEA}$ or $\overline{OEB}$ = 2.0V
I_{OS}	Output Short-Circuit Current	−100		−275	mA	Max	V_{OUT} = 0V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test			100	μA	0.0V	V_{OUT} = 5.5V (A_n, B_n); All Others GND
I_{CCH}	Power Supply Current			250	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current			30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current			50	μA	Max	Outputs TRI-STATE; All Others GND
I_{CCT}	Additional I_{CC}/Input			2.5	mA	Max	V_I = V_{CC} − 2.1V; All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} No Load (Note 2)			0.18	mA/MHz	Max	Outputs Open $\overline{OEA}$ or $\overline{OEB}$ = GND, Non-I/O = GND or V_{CC} One Bit toggling, 50% duty cycle (Note 1)

Note 1: For 8-bit toggling, I_{CCD} < 1.4 mA/MHz.

Note 2: Guaranteed, but not tested.

DC Electrical Characteristics (SOIC package) (Continued)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.6	0.8	V	5.0	T_A = 25°C (Note 1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.2	−1.0		V	5.0	T_A = 25°C (Note 1)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.5	3.0		V	5.0	T_A = 25°C (Note 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.0	1.7		V	5.0	T_A = 25°C (Note 2)
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.2	0.8	V	5.0	T_A = 25°C (Note 2)

Note 1: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at Low. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to theshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics: See Section 2 for Waveforms (SOIC and SSOP Package)

Symbol	Parameter	74ABT T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF			54ABT T_A = −55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Max Clock Frequency	200					200		MHz	
t_{PLH} t_{PHL}	Propagation Delay CPA or CPB to A_n or B_n	1.5 1.5	3.4 3.6	5.3 5.3			1.5 1.5	5.3 5.3	ns	2-3, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	1.5 1.5	3.2 3.5	5.5 5.5			1.5 1.5	5.5 5.5	ns	2-4
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	1.5 1.5	3.6 3.2	6.0 6.0			1.5 1.5	6.0 6.0	ns	2-4

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74ABT T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF		54ABT T_A = −55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n or B_n to CPA or CPB	2.5 2.5				2.5 2.5		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n or B_n to CPA or CPB	1.5 1.5				1.5 1.5		ns	2-6
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CEA}$ or $\overline{CEB}$ to CPA or CPB	2.5 2.5				2.5 2.5		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CEA}$ or $\overline{CEB}$ to CPA or CPB	1.5 1.5				1.5 1.5		ns	2-6
$t_w(H)$ $t_w(L)$	Pulse Width, HIGH or LOW CPA or CPB	3.0 3.0				3.0 3.0		ns	2-3

Extended AC Electrical Characteristics: See Section 2 (SOIC package)

Symbol	Parameter	74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 4)		74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250$ pF (Note 5)		74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 6)		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Progagation Delay	1.5	6.0	2.0	8.0	2.5	10.5	ns	2-4
t_{PHL}	CPA or CPB to A_n or B_n	1.5	6.0	2.0	8.0	2.5	10.5		
t_{PZH}	Output Enable Time	1.5	6.0	2.0	8.0	2.5	11.5	ns	2-4
t_{PZL}	$\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	1.5	6.0	2.0	8.0	2.5	11.5		
t_{PHZ}	Output Disable Time	1.5	6.0	(Note 7)		(Note 7)		ns	2-4
t_{PZL}	$\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	1.5	6.0						

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in plce of the 50 pF load capacitors in the standard AC load. This specificaiton pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: The TRI-STATE delays are dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Skew: See Section 2 (SOIC package)

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$–$5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 3)	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$–$5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 4)	Units	Fig. No.
		Max	Max		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	1.0	1.5	ns	2-13
t_{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	1.0	2.0	ns	2-13
t_{PS} (Note 5)	Duty Cycle LH–HL Skew	2.0	4.5	ns	2-14
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	2.1	4.5	ns	2-17
t_{PV} (Note 2)	Device to Device Skew LH/HL Transitions	2.5	5.0	ns	2-20

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 4: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

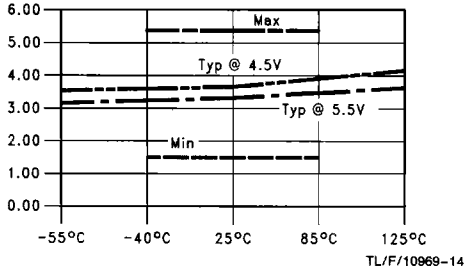
Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0V$ (Non I/O Pins)
$C_{I/O}$ (Note 1)	Output Capacitance	11	pF	$V_{CC} = 5.0V$ (A_n, B_n)

Note 1: $C_{I/O}$ is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

t_{PLH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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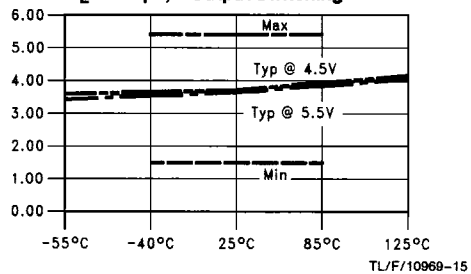
t_{PHL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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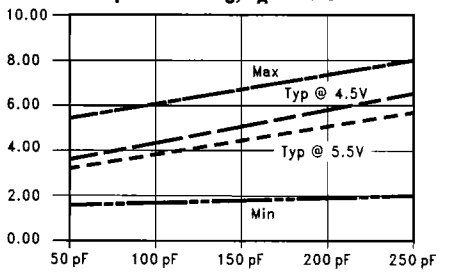
t_{PLH} vs Load Capacitance
1 Output Switching, T_A = 25°C



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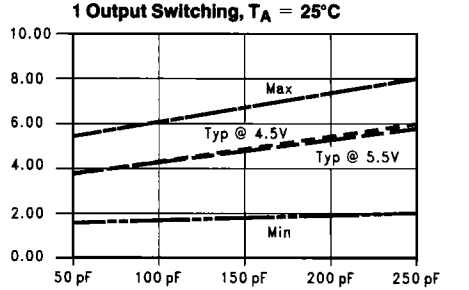
t_{PHL} vs Load Capacitance
1 Output Switching, T_A = 25°C



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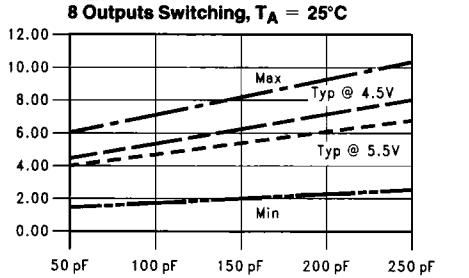
t_{PLH} vs Load Capacitance
8 Outputs Switching, T_A = 25°C



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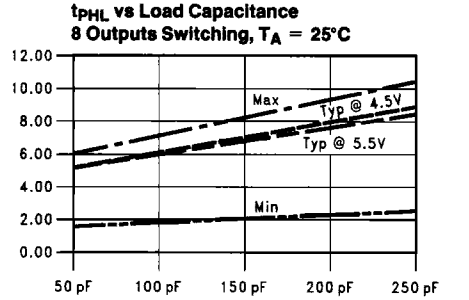
t_{PHL} vs Load Capacitance
8 Outputs Switching, T_A = 25°C



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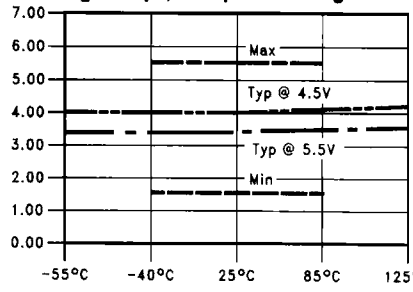
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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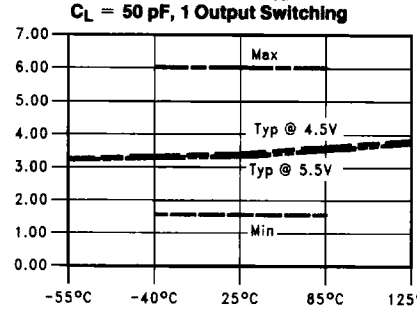
t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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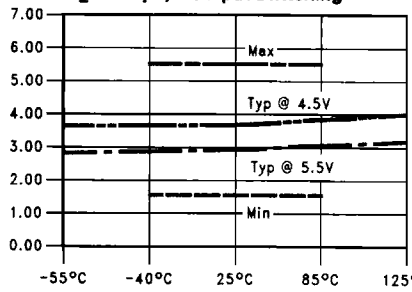
t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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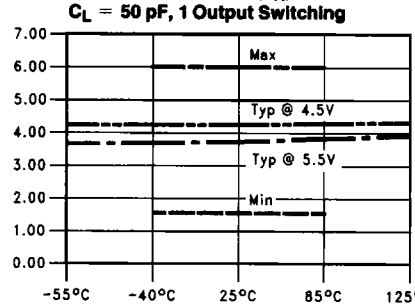
t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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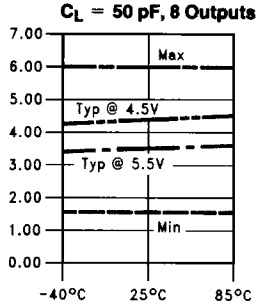
t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



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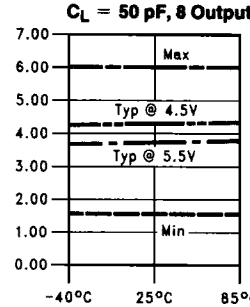
t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



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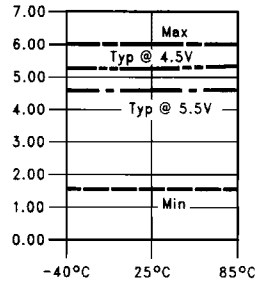
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



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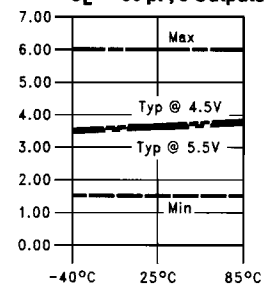
t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



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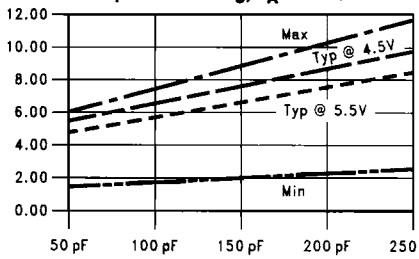
t_{PZL} vs Load Capacitance
8 Outputs Switching, T_A = 25°C



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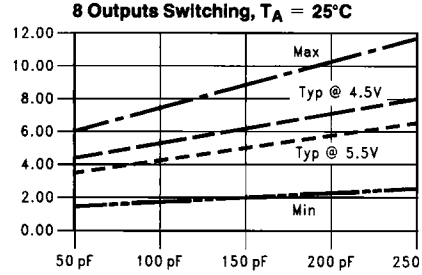
t_{PZH} vs Load Capacitance
8 Outputs Switching, T_A = 25°C



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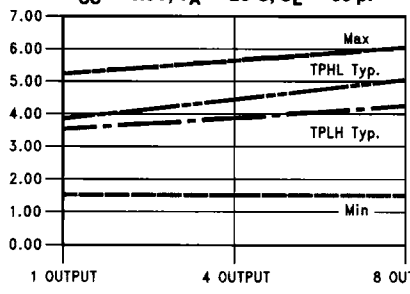
t_{PLH} vs Number Output Switching
V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF



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Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

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