Micro Linear

ML7730
2.4GHz Radio IEEE802.11 Baseband Processor

GENERAL DESCRIPTION

The ML7730 is Micro Linear's wireless local area network (WLAN) baseband controller. The ML7730 integrates the baseband physical layer (PHY) and the media access controller (MAC) into a single device that supports the IEEE802.11 specification. The ML7730 supports frequency hopping spread spectrum (FHSS), on Micro Linear's ML2712 and ML2713 radio systems.

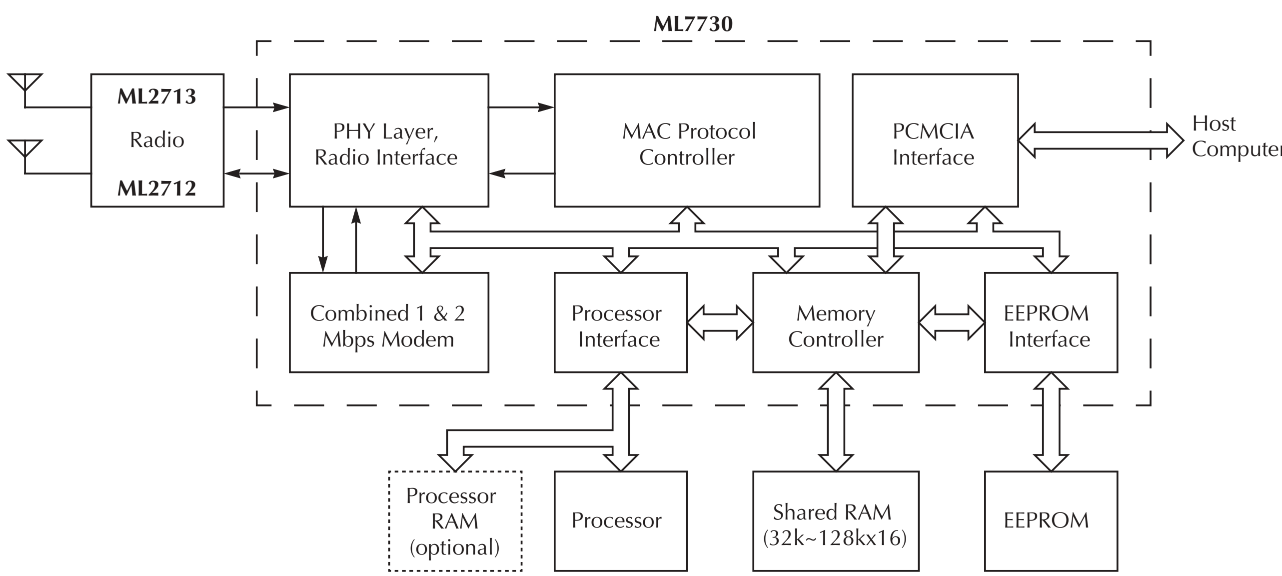
Portable hand-held systems require minimal current dissipation during normal and standby modes. The new hibernate and smart-hibernate power-down modes lowers power consumption to less than 2mA. Two voltages are required for the ML7730; 3.3 volts for the processor core and 5 volts for I/O interface.

Necessary software is available under license from Micro Linear.

FEATURES

- Complies with IEEE802.11 wireless LAN standards
- Smart-hibernate and hibernate power saving modes substantially reduce power consumption in battery applications
- Supports dual antennas
- Suitable for low cost stations and access points
- PCMCIA compliant (Ver. 2.1) – supports 16-bit data transfers
- On-chip radio modem for high-throughput data transfers
- Processor interface support for 80C186

SIMPLIFIED BLOCK DIAGRAM



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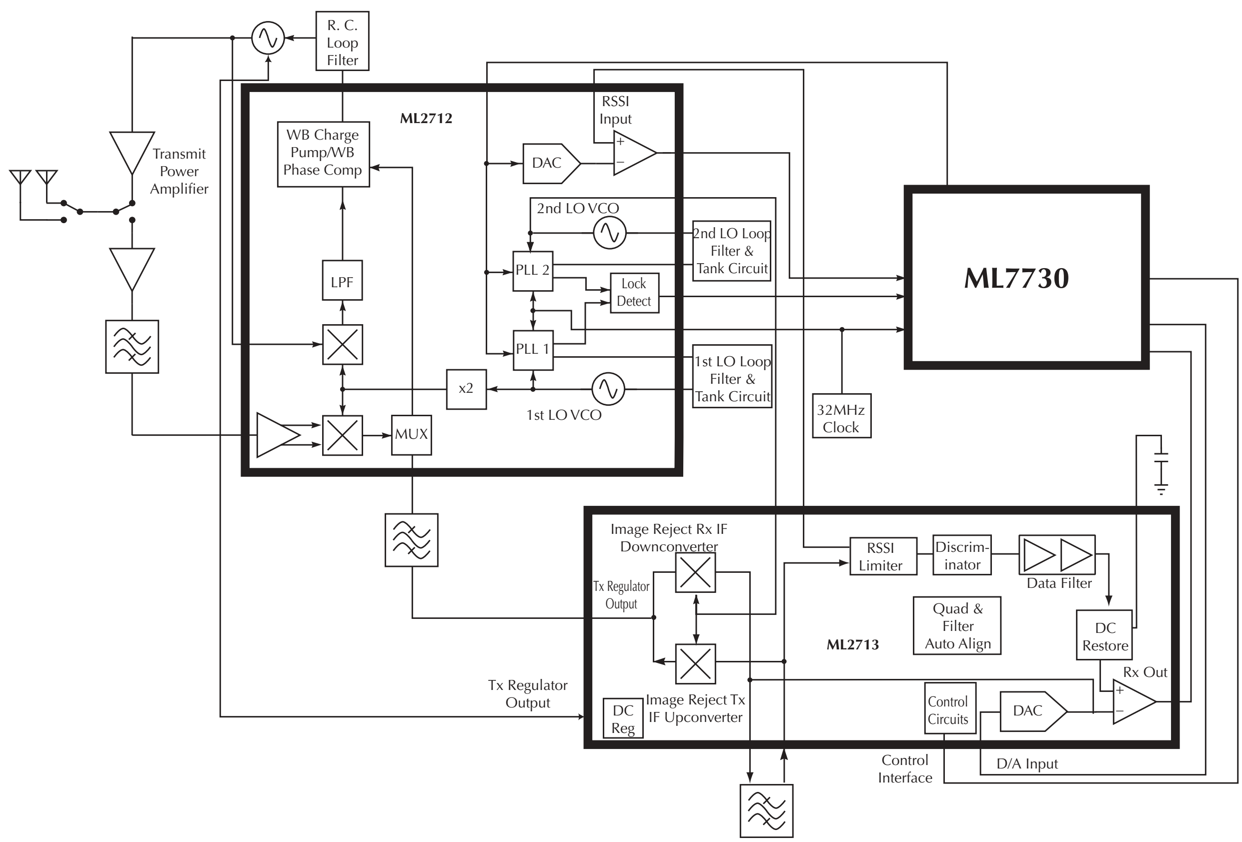
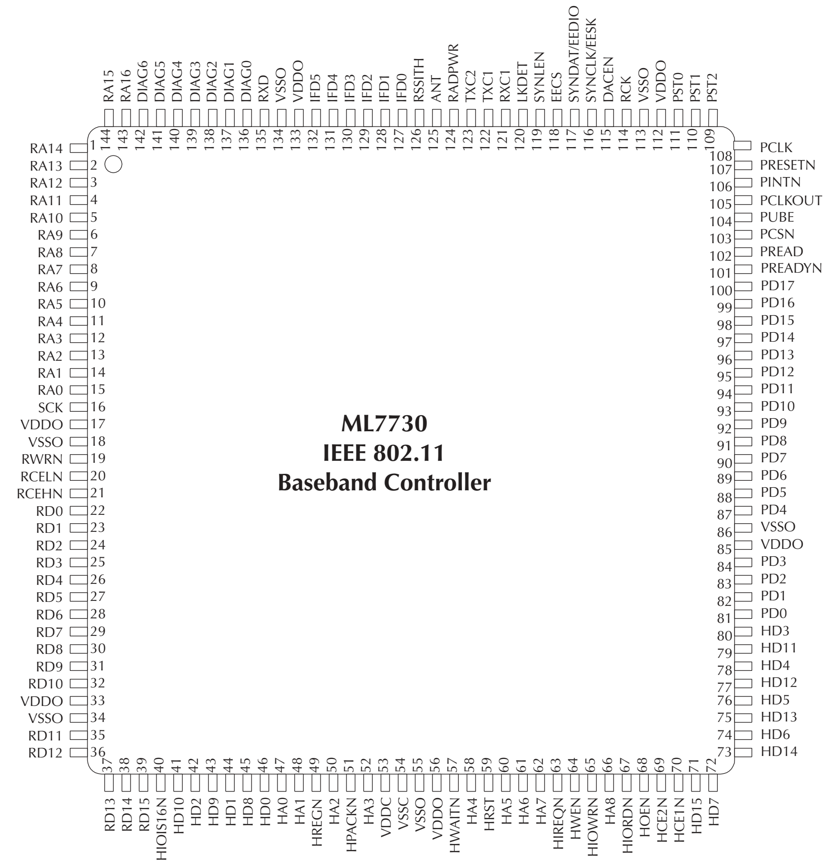
WARRANTY

Products described herein may be covered by one or more of the following U.S. patents: 4,897,611; 4,964,026; 5,027,116; 5,281,862; 5,283,483; 5,418,502; 5,508,570; 5,510,727; 5,523,940; 5,546,017; 5,559,470; 5,565,761; 5,592,128; 5,594,376; 5,652,479; 5,661,427; 5,663,874; 5,672,959; 5,689,167; 5,714,897; 5,717,798; 5,742,151; 5,747,977; 5,754,012; 5,757,174; 5,767,653; 5,777,514; 5,793,168; 5,798,635; 5,804,950; 5,808,455; 5,811,999; 5,818,207; 5,818,669; 5,825,165; 5,825,223; 5,838,723; 5.844,378; 5,844,941. Japan: 2,598,946; 2,619,299; 2,704,176; 2,821,714. Other patents are pending.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTIONS

Pin #	Signal Name	I/O	Description
Host Interface Signal Descriptions (PCI and ISA)			
51	HPACKN	Output	This signal is asserted when the card is selected and can respond to an I/O read cycle at the address on the address bus
40	HIOIS16N	Output	This signal is asserted whenever the access on A[8:0] corresponds to an I/O location which is capable of a 16-bit access
65	HIOWRN	Input	Indicates an I/O write cycle
67	HIORDN	Input	Indicates an I/O read cycle
63	HIREQN	Output	Active low interrupt request and ready/busy indicator prior to I/O card pin replacement
68	HOEN	Input	Outside enable signal asserted during memory read operations. Assertion of this signal causes memory data to be driven onto HD[15:0]
49	HREGN	Input	Assertion of this signal indicates an access to either attribute memory or I/O space

PIN DESCRIPTIONS

Pin #	Signal Name	I/O	Description
47	HA0	Input	Least significant 9 bits of the PC-card address bus. All other address bits are ignored
48	HA1	Input	
50	HA2	Input	
52	HA3	Input	
58	HA4	Input	
60	HA5	Input	
61	HA6	Input	
62	HA7	Input	
66	HA8	Input	
46	HD0	Bidirectional	Bidirectional data bus. Even numbered bytes appear on HD[7:0]. Odd numbered bytes appear on HD [15:8]
44	HD1	Bidirectional	
42	HD2	Bidirectional	
80	HD3	Bidirectional	
78	HD4	Bidirectional	
76	HD5	Bidirectional	
74	HD6	Bidirectional	
72	HD7	Bidirectional	
45	HD8	Bidirectional	
43	HD9	Bidirectional	
41	HD10	Bidirectional	
79	HD11	Bidirectional	
77	HD12	Bidirectional	
75	HD13	Bidirectional	
73	HD14	Bidirectional	
71	HD15	Bidirectional	
59	HRST	Input	Active high reset input
57	HWAITN	Output	Active low wait output. This signal is asserted if an access is requested that cannot complete immediately.
64	HWEN	Input	Active low memory write enable input. Indicates a write to either attribute memory or common memory as determined by the state of the HREGN signal
70	HCE1N	Input	Assertion of this signal indicates that a DMA transfer is in progress
69	HCE2N	Output	Indicates the ISA shared interrupt status Active low card enable signals. HCEN[1] selects even numbered bytes. HCEN[2] selects odd numbered bytes

PIN DESCRIPTIONS

Pin #	Signal Name	I/O	Description
Processor Interface Signal Descriptions (80C186)			
81	PD0	Bidirectional	Bi-Directional multiplexed address/data bus driven during the T1 clock state. PD[17:16] are inputs only
82	PD1	Bidirectional	
83	PD2	Bidirectional	
84	PD3	Bidirectional	
87	PD4	Bidirectional	
88	PD5	Bidirectional	
89	PD6	Bidirectional	
90	PD7	Bidirectional	
91	PD8	Bidirectional	
92	PD9	Bidirectional	
93	PD10	Bidirectional	
94	PD11	Bidirectional	
95	PD12	Bidirectional	
96	PD13	Bidirectional	
97	PD14	Bidirectional	
98	PD15	Bidirectional	
99	PD16	Bidirectional	
100	PD17	Bidirectional	
111	PST0	Input	Processor status code, indicating the current access type. PST inputs must be held in the all ones state while RESET* is asserted
110	PST1	Input	Bus status code that indicates the current cycle type. These inputs must be held HIGH when reset is asserted
109	PST2	Input	
108	PCLK	Input/Output	Clock output of the ML7730 to which all bus interface signals are synchronized. Frequency is 16 MHz during normal operation but is reduced when in hibernate mode. These two pins must be connected together for proper operation
105	PCLKOUT		
106	PINTN	Output	This signal is generated by the host and processor interrupt module
103	PCSN	Input	Processor chip select
101	PREADYN	Output	Active high ready indication from the ML7730
107	PRESETN	Output	This signal is controlled by the host and is asserted based on the state of the PRSTN bit in the H_CTL register
104	PUBE	Input	Upper byte enable. Indicates that a byte of data is to be transferred on PD[15:8]
102	PREAD	Input	Indicates a read cycle when HIGH, and a write cycle when LOW
Shared RAM Interface Signal Descriptions			
15	RA0	Output	The RAM address is provided by these pins. A maximum address size of 128K words is supported
14	RA1	Output	
13	RA2	Output	
12	RA3	Output	
11	RA4	Output	
10	RA5	Output	
9	RA6	Output	
8	RA7	Output	
7	RA8	Output	
6	RA9	Output	
5	RA10	Output	
4	RA11	Output	

PIN DESCRIPTIONS

Pin #	Signal Name	I/O	Description
Shared RAM Interface Signal Descriptions (continued)			
3	RA12	Output	
2	RA13	Output	
1	RA14	Output	
144	RA15	Output	
143	RA16	Output	
22	RD0	Bidirectional	The RAM data is provided by these pins. Word or byte operations are supported. When the shared memory is not in use, the data bus is output to prevent a floating data bus consuming power
23	RD1	Bidirectional	
24	RD2	Bidirectional	
25	RD3	Bidirectional	
26	RD4	Bidirectional	
27	RD5	Bidirectional	
28	RD6	Bidirectional	
29	RD7	Bidirectional	
30	RD8	Bidirectional	
31	RD9	Bidirectional	
32	RD10	Bidirectional	
35	RD11	Bidirectional	
36	RD12	Bidirectional	
37	RD13	Bidirectional	
38	RD14	Bidirectional	
39	RD15	Bidirectional	
20	RCELN	Output	When asserted, a low byte (or word) shared RAM cycle is active
21	RCEHN	Output	When asserted, a high byte (or word) shared RAM cycle is active
19	RWRN	Output	When asserted, a write cycle is required. When deasserted a read cycle is required. This signal remains valid before and while RCELN and RCEHN are asserted
Radio Interface Signal Descriptions			
121	RXC1	Open-collector/ drain Output	When asserted reception is enabled, RXC1 is always asserted during reception. This signal is programmable to be open-collector (active low) or open-drain (active high)
122	TXC1	Open-collector/ drain Output	When asserted transmission is 123 TXC2 enabled, both signals are programmable to be open-collector (active low) or open-drain (active high). Transmit is only activated following a receive (where Clear Channel Assessment is performed). The timing of TXC1 and TXC2 at the start of a transmit is programmable from the deassertion of RXC1. RXC2 is typically used for Tx power amplifier switching, and its assertion depends on the power control mode selected in the ML7730
124	RADPWR	Open-collector/ drain Output	This pin is asserted to power up the radio circuitry (i.e., local oscillators) for reception. The pin is programmable to be open-collector (active low) or open-drain (active high).
125	ANT	Open-collector output	This pin selects one of two antennas for transmission or reception

PIN DESCRIPTIONS

Pin #	Signal Name	I/O	Description
127 128 129 130 131 132	IFD0 IFD1 IFD2 IFD3 IFD4 IFD5	Open-collector/ drain Output	This control pin determines the response time constant of an analog data slicer circuit (options MSEL-0 or 1). This pin is programmable to be open-collector (active low) or open-drain (active high). This pin is asserted when CCA has determined a valid IEEE 802.11 GH signal (preamble is detected)
115 126	DACEN RSSITH	Open-Collector Input	For TX power control, CCA threshold and RSSI measurement, data also is clocked into a serial DAC (10/12 bit type; e.g., MAX515/MAX539) using the SYNCLK and SYNDAT lines as described above, except that DACEN is asserted during the programming, and the data is latched on the rising edge of DACEN. RSSITH is an input from a threshold comparison of the analog RSSI signal from the radio with the DAC output. It is high when the received signal exceeds the programmed threshold. This performs two purposes: A minimum threshold of RSSI can be set before enabling the demodulator for CCA to reduce power. Once a valid receive signal is determined (CCA invalid), the RSSI can be measured with the external comparator/DAC and a SAR within the ML7730. The RSSI measurement is performed for internal and external modem options when CCA is determined. The same DAC can be used for both TX power control, RSSI threshold and RSSI measurement
114	RCK	Output	A clock to the radio is provided on this pin. The clock is derived from SCK when RADPWR is asserted, with fixed division ratio of one or two (selected by post-reset configuration SCK_CONF). RCK is typically 32MHz for the radio synthesizer reference
135	RXD	Input	The function of ths pin depends on the state of the MSEL [3:0] field in the PHY_CONFIG register
Radio/EEPROM Interface			
116	SYNCLK/EESK	Output	This signal is connected to SK of the EEPROM to provide the clock. The clock rate is RCK divided by 64 (500KHz with RCK at 32MHz)
117	SYNDAT/EEDIO	Bidirectional	This is a bi-directional data signal for the EEPROM connected directly to data in (DI) of the EEPROM, and to data out (DO) via a resistor (see EEPROM application notes and figure 2).
119 120	SYNLEN LKDET	Open collector Input	supported by a flexible architecture. The data is output on SYNDAT/EEDIO ready for the rising edge of SYNCLK/EESK. SYNLEN is asserted during the programming, and the data is latched on the rising edge of SYNLEN. SYNCLK/EESK is clocked at RCK divided by 2. SYNCLK/EESK and SYNDAT/ EEDIO are also used to program a serial DAC used for Tx power control, CCA threshold, and RSSI measurement (see below). The synthesizer is programmed when the radio is idle. The RSSI and CCA threshold DAC is used at the start of receiving a packet. The radio provides indication of being in lock with LKDET. This input is active high or low (programmable), pulse sensitive, and latched so that both pulsed and steady out-of-lock signals are recognized. Glitches shorter than 2 RCK periods are ignored. Transmission is prevented when the synthesizer is out-of-lock.

PIN DESCRIPTIONS

Pin #	Signal Name	I/O	Description
118	EECS	Output	This signal is connected to CS of the EEPROM to provide the chip select. These signals provide the interface to the radio synthesizer to select the transmit/receive carrier. Many synthesizers are
Modem Interface Signal Descriptions			
136	DIAG0		Various signals are provided on these pins as diagnostic aids or as a programmable I/O port (see ML7730 Wireless LAN Baseband Controller Datasheet & Programmer's Reference)
137	DIAG1		Various signals are provided on these pins as diagnostic aids or as a programmable I/O port (see ML7730 Wireless LAN Baseband Controller Datasheet & Programmer's Reference)
138	DIAG2		Various signals are provided on these pins as diagnostic aids or as a programmable I/O port (see ML7730 Wireless LAN Baseband Controller Datasheet & Programmer's Reference)
139	DIAG3		Various signals are provided on these pins as diagnostic aids or as a programmable I/O port (see ML7730 Wireless LAN Baseband Controller Datasheet & Programmer's Reference)
140	DIAG4		Various signals are provided on these pins as diagnostic aids or as a programmable I/O port (see ML7730 Wireless LAN Baseband Controller Datasheet & Programmer's Reference)
141	DIAG5		Various signals are provided on these pins as diagnostic aids or as a programmable I/O port (see ML7730 Wireless LAN Baseband Controller Datasheet & Programmer's Reference)
142	DIAG6		Various signals are provided on these pins as diagnostic aids or as a programmable I/O port (see ML7730 Wireless LAN Baseband Controller Datasheet & Programmer's Reference)
General Signal Descriptions			
16	SCK	Input	The system clock to the ML7730 is provided by this pin. The clock must always be active (i.e.,when reset is asserted). The system card operates synchronously to this clock. The ML7730 and radio operate at SCK/2. The internal modem operates at SCK (32MHz). The processor operates from a division of SCK (divide by 1 to divide by 8) depending on a register (GLOB_CTL, see Programmers Reference) in the ML7730. This signal is output as PCK
54	VSSC	Ground	These pins serve as ground for the core logic
18 34 55 86 113 134	VSSO	Power	This pin serves as ground for the I/O pads
53	VDDC	Power	This pin serves as power to the core at 3.3-v nominal
17 33 56 85 112 133	VDDO	Power	This pin serves as power to I/O pads and can either be 3.3V or 5V nominal

FUNCTIONAL DESCRIPTION

INTERFACE DESCRIPTIONS

The ML7730 provides the following interfaces:

- Processor
- Shared RAM
- EEPROM
- Radio
- MODEM
- PHY
- PCMCIA

These interfaces are explained in the following subsections.

Processor Interface

Most applications require a local processor to handle the higher layers of the IEEE 802.11 protocol. The host computer typically runs a network device/driver interface specification (NDIS) or open datalink interface (ODI) driver that communicates to the local processor via shared memory and interrupts. The local processor performs the higher layers of the IEEE 802.11 MAC protocol while the ML7730 performs the lower layers of MAC and the PHY under control of the local processor.

The ML7730 is configured to operate with 80C186 processor. The processor configuration is determined from the P_CONF field in the Device Configuration Register. The following table shows how each processor is selected. No external circuitry is required between the processor and the ML7730.

P_CONF 2:0	Processor Mode
000	Host-only mode. No local processor
001	V30HL local processor mode
010	80C 186 local processor mode
011	Reserved
100	V53A local processor mode

Table 1. Micro Processor Modes

Selecting The Processor Mode

In each processor mode, the bus interface module:

- Interprets the external bus cycles
- Generates the appropriate signals based on the processor mode
- Passes access requests to the host interface module, the shared RAM arbiter, and the baseband registers

The module also synchronizes data and control signals to the internal clocks, and interfaces the external processor to the host interface and processor interrupt control modules.

The 80C186 processor contains a clock generator module and divide-by logic. In these modes, the ML7730 generates a clock (X1) at twice the normal operating frequency. The processor divides this frequency by two (X1/2). Then this clock is used for synchronization of all interface signals. In V30HL processor mode, the ML7730 generates the clocks for internal modules as well as the processor. A 16-MHz clock is used during normal operation. This frequency is reduced when the ML7730 enters either the *Hibernate* or *Smart Hibernate* modes. In *Hibernate* mode the clock frequency is reduced from 16 MHz to 500 KHz. In *Smart Hibernate* mode the frequency is reduced to 125 KHz.

Shared RAM Interface

A shared memory interface is provided for the buffering of packets and the storage of processor code and data. Memory sizes range from 32K words to 128K words in 32 word increments.

Both 16-bit (word) and 8-bit memory accesses are supported. The ML7730 and the host computer support only word accesses to memory. The processor supports both byte and word accesses to memory. Selection of byte or word transfers occurs on a per-cycle basis and depends on the state of the address bit 0 (PD[0]) and the PUBEN signal as shown in Table 2.

PD[0]	PUBEN	Transfer Type
0	0	Word transfer on PD[15:0]
0	1	Even byte transferred on PD[7:0]
1	0	Odd byte transferred on PD[15:8]
1	1	Invalid

Table 2. Data Transfer Size

FUNCTIONAL DESCRIPTION

Selecting the Data Transfer Size

For cost sensitive applications, local processor code may reside in shared memory. However, this may affect processor because accesses to shared memory may contain wait states.

EEPROM INTERFACE

EEPROM support is provided for nonvolatile storage of host interface configuration (e.g., PCMCIA CIS table) and system parameters (e.g., local IEEE address, radio parameters). The ML7730 supports 64-, 128-, or 256-byte EEPROM sizes (e.g., 93C46, 93C56, or 93C66 types).

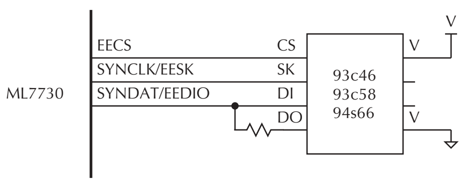


Figure 1. EEPROM Connections to ML7730

The local processor can be used to initialize the EEPROM and control read and write accesses for providing card parameter storage.

Following a reset by the host processor, the EEPROM contents are automatically transferred to shared RAM to provide the configuration information for the host interface. If the device is configured in a PC-Card host mode, either 64 or 128 bytes are downloaded to shared RAM to provide the Configuration Information Structure (CIS). If the device is configured in Industry Standard Architecture (ISA) host mode, a single word is loaded into an internal register to determine the ISA address space mapping and interrupt configuration information.

Host Interface (Between Adapter Card and Computer or Laptop)

The 16-bit PCMCIA interface is fully supported by the ML7730 with no additional logic. Access to attribute memory (CIS configuration data) and I/O memory (host registers) is provided.

During normal operation, I/O addresses are used to access the baseband controller registers and shared memory.

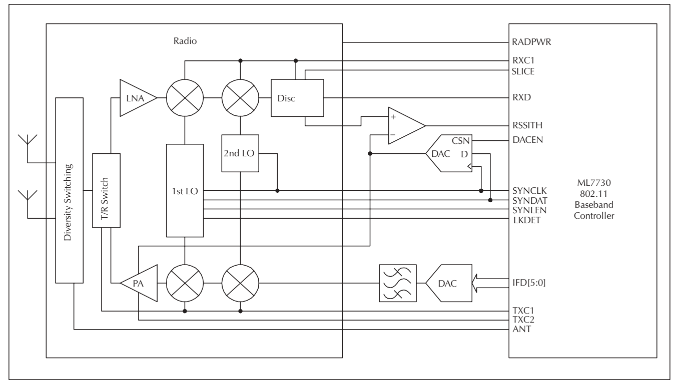


Figure 2. Typical FH Radio Interface

RADIO INTERFACE

The Radio interface supports simple, flexible control of the radio and its synthesizer. The control signal timing is programmable by the processor. Figure 2 shows the connection to a typical radio architecture.

The ML7730 uses the RXC1 and TXC[1:0] pins to control radio timing. The delay between these signals is programmable to support different radio designs.

During a receive operation, the ML2712 DAC is used for RSSI thresholds and measurement. The RSSIA threshold is loaded whenever the receiver is first powered on. Once the RSSIA threshold is exceeded, the demodulator is accessed and the RSSIB, RSSIC, and RSSID thresholds are loaded sequentially during each antenna scan. Once antenna scanning has completed, a successive approximation is started.

MODEM INTERFACE

The ML7730 provides Frequency Hopping Physical Layer Convergence Protocol (FH PLCP) framing and the FH modem as defined by the IEEE 802.11 specification. The radio synthesizer control pins are used for all modem options. A diagnostic port is provided when the internal modem is used. The ML2712 and ML2713 implement delta ADC data recovery.

With MSEL=0 (no modem) an 8MHz square wave is output on IFD4/TXTONE during Tx, and SLICE is output on IFD0/SLICE during Rx. All pins are otherwise tristate.

With MSEL=1 (low cost 1Mbit/s modem), IFD[5:0] are used to drive a 6 bit DAC at 32MHz to provide the modulated transmit IF signal at 24MHz. They are set to the DAC mid value during receive, except IFD0/SLICE which outputs the SLICE signal.

FUNCTIONAL DESCRIPTION

With MSEL=2 or 3 (1/2Mbit/s modem), IFD[5:0] are used to drive a 6 bit DAC at 32MHz to provide the modulated transmit IF signal at 24MHz.

With MSEL=2 (1/2Mbit/s modem, normal ADC) a 4 bit ADC (e.g. CA3304 type) provides digitised demodulated data at 16MHz as input to the baseband controller on pins IFD[3:0] during receive. Additionally, a dithering signal is provided on IFD[5:4]. The ADC outputs must only be enabled during receive (e.g. by connecting RXC1 to the ADC output enable pin).

With MSEL=3 (1/2Mbit/s modem, delta ADC), a comparator is used to compare the value of the transmit IF DAC output to the receive demodulated signal, performing a tracking delta ADC function. The same 6 bit DAC (but at 16MHz) is used on IFD[5:0] as during transmit, and the comparator input is connected to RXD (pin 135).

With MSEL=4 ,5,6 or 7 (external modem) the pins are used to interface with the external modem.

When MSEL=0 (no modem) and MSEL=1 (low cost 1Mbit/s modem), the RXD pin is used for baseband data input from a radio which has a built-in analogue data slicer. The baseband controller has clock recovery circuitry to synchronise to the incoming data. The recovered clock is output on the RXCLK pin for debugging.

When MSEL=2 (1/2Mbit/s modem, 4-bit ADC), this is a reserved input and should tied high or low.

When MSEL=3 (1/2Mbit/s modem, delta ADC), the delta comparator is input on this pin. The recovered clock from the demodulator is output on a diagnostic pin for test purposes.

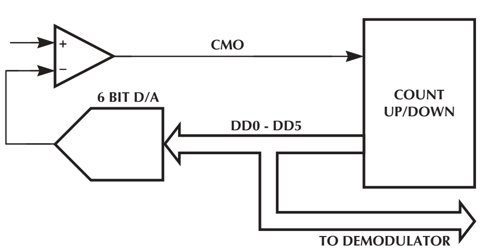


Figure 3. Tracking Delta ADC Block Diagram

Demodulator

The baseband controller in the ML7730 incorporates a digital baseband demodulator designed to demodulate IEEE 802.11 GFSK data packets with 1- and 2-Mbps headers. The demodulator contains the following features:

- 1- and 2-Mbps operation
- Two-antenna diversity control
- Analog discriminator interface
- Flexible clear channel assessment (CCA) options to enhance interference performance
- Tunable or adaptive digital filter and data slicers for performance optimization
- Clock and carrier tracking for demodulation of long data packets

The ML7730 supports two modes:

- 1-Mbps 2-ary FSK
- 2-Mbps 4-ary FSK

The radio requirements for the demodulator are:

- 1Mb: 20dB S/N from discriminator 10^{-5} BER (802.11 specifies sensitivity of 10^{-5} for 80dBm)
- 2Mb: 30dB S/N from discriminator 10^{-5} BER (802.11 specifies sensitivity of 10^{-5} for 75dBm)
- Carrier acquisition for analog slicer option within 4µs, yielding a duty cycle better than 60:40 for a square wave (demodulation provides signal for carrier lock switch once preamble is detected)
- RSSI threshold decision within 4µs of antenna switching

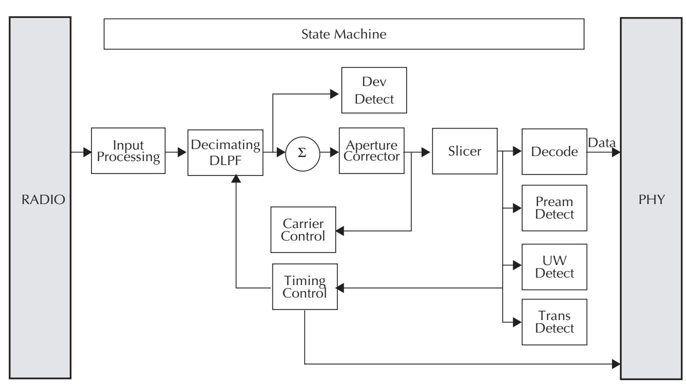


Figure 4. Demodulation Block Diagram

FUNCTIONAL DESCRIPTION

PHY Interface

The PHY section of the ML7730 allows the MAC layers from two different stations to be interconnected via a 2.4 GHz radio signal. Figure 5 shows a block diagram of the PHY interface.

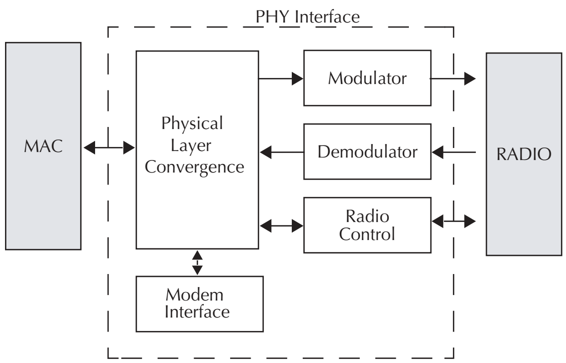


Figure 5. ML7730 Physical Layer Block Diagram

The PHY provides a Frequency Hopping Spread Spectrum (FHSS) radio link at either 1 or 2Mbps. FH is performed over a subset of 1-MHz wide channels with a frequency band of 2.400 to 2.497GHz. The ML7730 is not directly in control of the hopping sequence, but rather provides for reprogramming of the radio channel so that this function can be managed under software control.

The mapping of data between the MAC and the radio link is called the Physical Layer Convergence Protocol (PLCP). This mapping involves the addition and removal of preamble and header information, as well as the whitening and dewhitening of packet data. Figure 6 shows a block diagram of the PLCP.

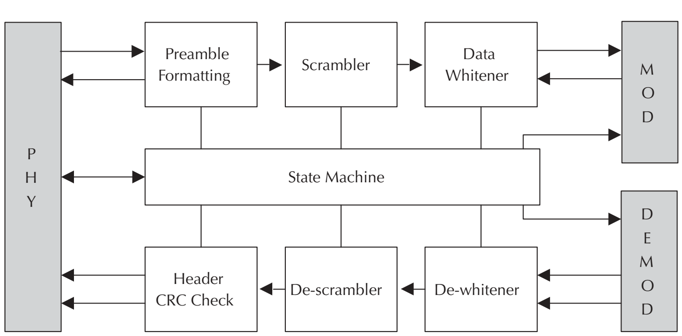


Figure 6. Physical Layer Convergence Protocol Block Diagram

Each frame starts with an 80-bit synchronization sequence or preamble, followed by a 16-bit unique word or start of frame delimiter (SFD).

The Physical Data Unit (PDU) is a data-whitened version of the MAC data at either 1 or 2Mbps.

The PHY is required to perform CCA to determine when to transmit, and for the MAC to control the contention back-off timer.

PCMCIA Interface

The ML7730 provides a PCMCIA host interface mode designed to permit implementation of PC cards for use with host computers compatible with the PCMCIA PC card standard (Revision 2.1). The interface supports 16-bit transfers to maximize overall system throughput. In addition, common memory may be used to access all control registers. This is useful for low-cost card implementations that do not have a local processor.

The ML7730 uses attribute memory to configure the device and card. The device decodes the least-significant 9-bits of PC card address space, allowing for an attribute memory size of 512 bytes located at addresses 0x000 – 0x1FF. The attribute memory stores the PCMCIA registers as well as the card information structure (CIS) table data. The PCMCIA standard defines four configuration registers. However, only the *Configuration Option* and the *Configuration and Status* registers are supported, not the *Pin Replacement* and *Socket and Copy* registers.

The CIS information data is stored in an off-chip serial EEPROM. When the ML7730 is reset, the contents of the EEPROM are downloaded to shared RAM. Then the information is mapped to attribute memory space.

REGISTER MAP

The following table lists the registers in the ML7730.

Byte Offset	Width (bits)	Register Name	Description
Configuration			
0x00	8	Device Configuration	Stores serial EEPROM size and sets host interface and processor interface modes
PCMCIA			
0x10	8	Configuration Option	Stores interrupt, reset, and configuration index information
0x12	8	Configuration and Status	Stores general cycle status information, including interrupts and power-down
ISA Host			
0x00	16	Host Control (H_CTL)	Contains ISA reset, host interface, and processor interface interrupt information
0x02	16	Host Address (H_ADDR)	Contains the address in shared memory to be accessed by the H_DATA register
0x04	16	Host Data (H_DATA)	Stores host data information
Global Control			
0x00	16	Version Number	Contains the ML7730 version number(0xC3). This register is read-only
0x02	16	Global Control	Contains mapping information for baseband control registers and MAC/PHY enables
0x08	16	Processor Interrupt Control	Contains host interrupt, processor interrupt, and interrupt enable information
EEPROM			
0x0C	16	EEPROM Data	This register is a buffer that contains data being transferred to and from the EEPROM
0x0E	16	EEPROM Address Control	Contains EEPROM enable and cycle type information
PHY/Radio			
0x10	16	PHY Configuration	Contains modem and PHY revision information as well as transmit and receive status. The 3-bit MSEL field defines the type of modem information.
0x12	16	Synthesizer Program	Contains the least-significant 16 bits of the 32 bits used for synthesizer programming. This register is used in conjunction with the other SYN register located at 0x14.
0x14	16	Synthesizer Program	Contains the most-significant 16 bits of the 32 bits used for synthesizer programming. This register is used in conjunction with the other SYN register located at 0x12.
0x16	16	Radio Control (RAD_CTL)	Contains radio configuration and transmit and receive status information.
0x18	16	Radio Delay (RAD_DLYS)	Contains the programmable delay parameters between the TXC[1:0] and RXC1 signals.

REGISTER MAP

Byte Offset	Register Group Width (bits)	Register Name	Description
0x1A	16	Radio Power (RAD_PWR)	Determines when the TXC2 signal is asserted if the power control word is selected. Two control bits in the PHY 0x22 I/O port as input or output, and whether values can be read from or written to this register.
0x1C	16	Radio Power (RAD_PWR)	Determines when the TXC2 signal is asserted if the power control word is selected. Two control bits in the PHY control word of a transmit packet determine which one of four 8-bit values is used. This register is used in conjunction with the other PAD_PWR register located at 0x1A
Modem			
0x1E	16	RSSIAB	Contains two 6-bit fields: RSSIA and RSSIB. RSSIA is set to correspond to –65dm the radio input. RSSIB is set to correspond to –85 dBm the radio input
0x20	16	PHY Control (PHY_CTL)	Contains PHY transmit, receive, and Clear Channel Assessment (CCA) status
0x22	16	User I/O port (external)	The external port is selected when the MSEL field in the PHY Configuration registers equals a value between 4 and 7.The bit descriptions are different depending on whether this register is configured for internal or external use (see above register entry). One 6-bit field contains the number of clock periods from TXDRDY or RXDRDY assertion. The other 6-bit field contains the number of RXCLK periods from the length field to the start of the PDU packet
0x26	16	RSSICD	Contains two 6-bit fields: RSSIC and RSSID. RSSIC corresponds to –80 dBm at the radio input. RSSID corresponds to –75 dBm at the radio input
0x28	16	Modem Control 0	Contains two 6-bit fields that set the 1- and 2-Mbps inner symbol modulation index
0x2A	16	Modem Control 1	Contains settings for parameters such as integration time for slow carrier tracking group, antenna scan delay, ramp-up, and ramp-down sequences
0x2C	16	Demodulator Control 0	Contains demodulator control word settings
0x2E	16	Demodulator Control 1	Contains noise threshold and jamming counter settings
MAC Control			
0x30	16	Version Number	Contains the ML7730 MAC version number (0x83).
0x32	16	Buffer Control	Contains the size and address of the receive circular buffer in shared memory.
0x34	16	Rx In Pointer	Contains a word offset from the start of the receive circular buffer in shared memory. The offset indicates the location of the address where the next word to be received will be stored.
0x36	16	Rx Out Pointer	Contains a word offset from the start of the receive circular buffer in shared memory. The offset indicates the first word in the buffer that is available for use by the MAC hardware.
0x40	16	Power Down Control	Contains Hibernate mode request and wakeup information.

REGISTER MAP

Byte Offset	Register Group	Width (bits)	Register Name	Description
0x44		16	MAC Control	Contains filtering mode parameters as well as transmit, receive, PHY, and modem enable information
0x46		16	Tx Pointer	Contains the word offset from the start of the transmit pointer table
0x48		16	Interrupt Enable	Enables interrupts based on the event type
0x4A		16	Interrupt Acknowledge	This register has the exact same format as the Interrupt Enable register. Setting a bit in this register clears the corresponding bit in the Interrupt Enable register
0x4C		16	Interrupt Status	This register has the exact same format as the Interrupt Enable register but is read-only. This register is written by hardware
0x4E		16	Sequencer Status	Indicates current sequencer activity. Most bits are written by hardware and are read-only. However, a global clear bit allows for all of the read-only bits to be cleared at the same time
0x50		16	TSF Timer	This register works in conjunction with the register at address 0x52 to construct a 32-bit microsecond timer used for time stamps in received frames and beacon transmissions
0x52		16	TSF Timer	This register works in conjunction with the register at address 0x50 to construct a 32-bit microsecond timer used for time stamps in received frames and beacon transmissions
0x58		16	TSF Comparator 1	This register contains the least-significant 16 bits of a 24-bit TSF timer value. This register works in conjunction with the register at address 0x5A. The 16 bits of the TSF Comparator 1 register and the 8 bits of the TSF Comparator 2 register compose the 24-bit TSF comparator value
0x5A		16	TSF Comparator 2	This register contains the most-significant 8 bits of a 24-bit TSF timer value. This register works in conjunction with the register at address 0x5A. The 16 bits of the TSF Comparator 1 register and the 8 bits of the TSF Comparator 2 register compose the 24-bit TSF comparator value. This 8-bit value is contained in the lower 8 bits of this register. The upper 8 bits are reserved
0x60		16	Add TSF Time	Hardware uses the lower 10 bits of this register to determine the length of time that the TSF timer is disabled. This value can be modified by software
0x64		16	NAV Timer	This 16-bit register contains a 1-ms resolution timer that maintains the virtual carrier sense mechanism. The timer is automatically loaded by the MAC but can be modified by software
0x66		16	Backoff Timer	This register is loaded automatically by the MAC from transmit frame header structures. If a backoff condition occurs, the counter begins decrementing until it reaches zero
0x68		16	Response Timer	Contains a timeout value, in increments of 32 ms, after which the MAC aborts the transmit frame if it does not receive an acknowledgement
0x6A		16	Tick Timer	Sets the interval time in milliseconds at which interrupts are generated

REGISTER MAP

Byte Offset	Register Group	Width (bits)	Register Name	Description
0x6C		16	Timer Control	Contains enable and status information for each of the timers in the MAC control register group.
0x6E		16	Slot Time	Contains the value used to determine the length of slots required for random backoff.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

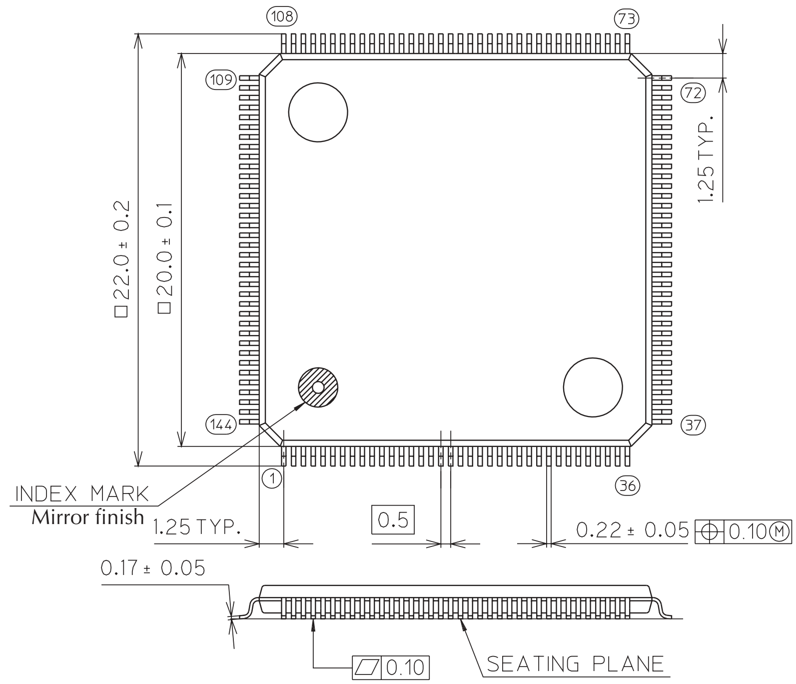
Storage Temperature Range ....-65°C to 150°C
Lead Temperature (Soldering, 10s) .... 240°C
Thermal Resistance) ....
Power Supply Voltage Range ....
.... Ground - 0.3V to VDDC, VDDO +0.3V
Input Voltage Range ....
.... Ground - 0.3V to VDDC, VDDO +0.3V

OPERATING CONDITIONS

VDDO (I/) .... 3.3 to 5V +/- 10%
VDDC (Core) .... 3.3V +/- 10%
Voltage Range ....
All VCC supply pins must be within .1V of each other
Operating Ambient Temperature Range ...... -40°C to 85°C

PHYSICAL DIMENSIONS (millimeters)

144 Pin LQFP



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML7730IM	-40°C - 85°C	144 Pin LQFP

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DS7730-01