

# DN74LS112 *DN74LS112*

## Dual J-K Negative Edge-Triggered Flip-Flops (with Set and Reset)

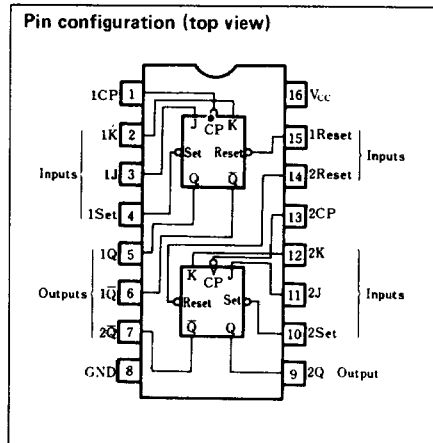
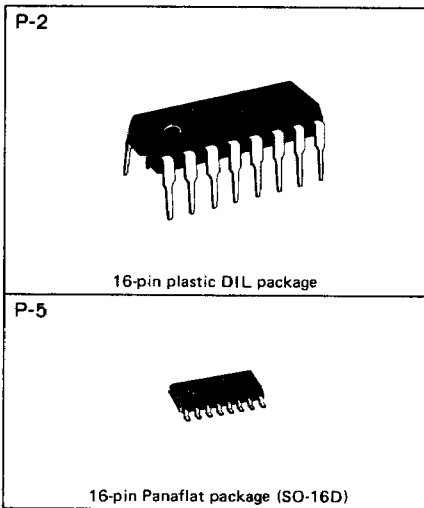
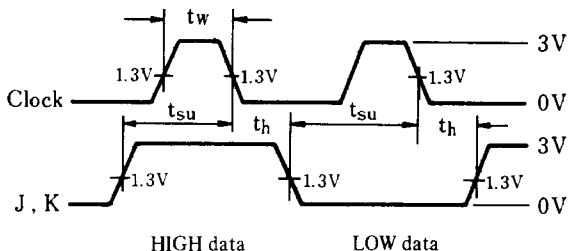
### Description

DN74LS112 contains two negative-edge triggered J-K flip-flop circuits, each with independent clock-CP, J, K, and direct-coupled set and reset input terminals.

### Features

- Negative-edge trigger
- Independent input and output terminals for each flip-flop
- Direct-coupled set and reset inputs
- Q and  $\bar{Q}$  outputs
- Wide operating temperature range ( $T_a = -20$  to  $+75^\circ\text{C}$ )

### Timing definition



### Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.75	5.00	5.25	V
Output current	$I_{OH}$			-400	$\mu\text{A}$
	$I_{OL}$			8	mA
Operating temperature range	$T_{opr}$	-20	25	75	$^\circ\text{C}$
Clock frequency	$f_{clock}$	0		30	MHz
Pulse width	Clock High	$t_w$	25		ns
	Set or Reset Low	$t_w$	25		ns
Set-up time	HIGH data	$t_{su}$	20 ↓		ns
	LOW data	$t_{su}$	20 ↓		ns
Hold time	$t_h$	5 ↓			ns

Notes 1. ↓: Indicates fall edge of standard clock pulse.

■ DC characteristics (Ta = -20 ~ +75°C)

25P

Parameter	Sym	Test conditions	Min	Typ*	Max	Unit
Input voltage	V <sub>IH</sub>		2.0			V
	V <sub>IL</sub>				0.8	V
Output voltage	V <sub>OH</sub>	V <sub>CC</sub> = 4.75V, V <sub>IH</sub> = 2V V <sub>IL</sub> = 0.8V, I <sub>OH</sub> = -400 μA	2.7	3.4		V
	V <sub>OL1</sub>	V <sub>CC</sub> = 4.75V V <sub>IH</sub> = 2V		0.25	0.4	V
	V <sub>OL2</sub>	V <sub>IL</sub> = 0.8V		0.35	0.5	V
Input current	J-K	I <sub>IH</sub>	V <sub>CC</sub> = 5.25V V <sub>I</sub> = 2.7V		20	μA
	Reset			60	μA	
	Set			60	μA	
	Clock			80	μA	
	J-K	I <sub>IL</sub>	V <sub>CC</sub> = 5.25V V <sub>I</sub> = 0.4V		-0.4	mA
	Reset			-0.8	mA	
	Set			-0.8	mA	
	Clock			-0.8	mA	
	J-K	I <sub>I</sub>	V <sub>CC</sub> = 5.25V V <sub>I</sub> = 7V		0.1	mA
	Reset			0.3	mA	
	Set			0.3	mA	
	Clock			0.4	mA	
Output short circuit current**	I <sub>OS</sub>	V <sub>CC</sub> = 5.25V, V <sub>O</sub> = 0V	-15		-100	mA
Input clamp voltage	V <sub>IK</sub>	V <sub>CC</sub> = 4.75V, I <sub>I</sub> = -18mA			-1.5	V
Supply current***	I <sub>CC</sub>	V <sub>CC</sub> = 5.25V		4.0	8.0	mA

\* When constant at V<sub>CC</sub> = 5V, Ta = 25°C.

\*\* Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

\*\*\* Measured with all outputs open, Q and Q̄ outputs alternately HIGH, and clock inputs grounded.

■ Switching characteristics (V<sub>CC</sub> = 5V, Ta = 25°C)

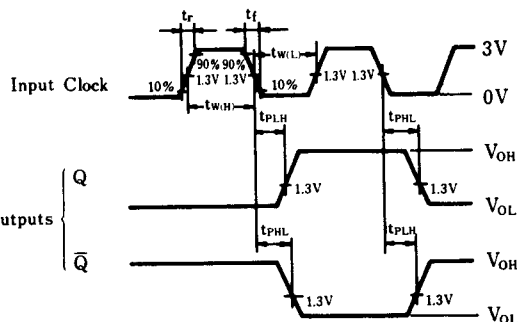
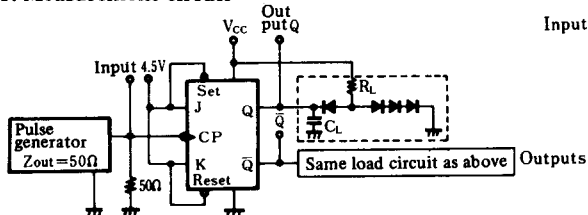
3P

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f <sub>max</sub>				30	45		MHz
Propagation delay time	t <sub>PLH</sub>	Reset Set	Q, Q̄	C <sub>L</sub> = 15pF R <sub>L</sub> = 2kΩ		11	20	ns
	t <sub>PHL</sub>	Clock				15	30	ns

※ Switching parameter measurement information

(1) f<sub>max</sub>, t<sub>PLH</sub>, t<sub>PHL</sub> (Clock → Q, Q̄)

1. Measurement circuit

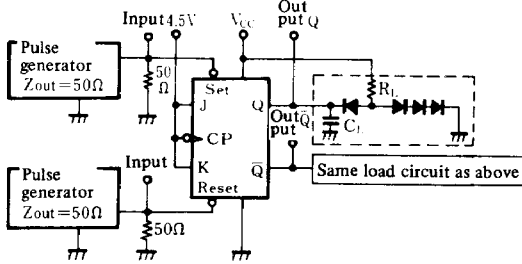


1. Measurement made for each flip flop.
2. C<sub>L</sub> includes probe and tool floating capacitance.
3. Diodes are all MA161 or equivalent.

1. Clock input waveform: t<sub>r</sub> ≤ 15ns, t<sub>f</sub> ≤ 6ns, PRR = 1MHz, duty cycle 50%
2. When measuring f<sub>max</sub>, t<sub>r</sub> and t<sub>f</sub> ≤ 2.5ns.

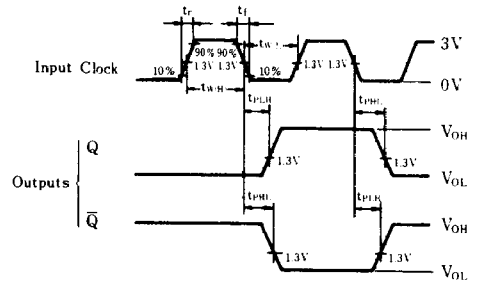
(2)  $t_{PLH}$ ,  $t_{PHL}$ (Reset, Set  $\rightarrow$  Q,  $\bar{Q}$ )

1. Measurement circuit



1. Measurement made for each flip flop.
2.  $C_L$  includes probe and tool floating capacitance.
3. Diodes are all MA161.

2. Waveforms



Notes

1. Reset, Set Input waveform:  $t_r \leq 15ns$ ,  $t_f \leq 6ns$ ,  $PRR=1MHz$

■ Truth tables

Inputs					Outputs	
Set	Reset	Clock	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	$Q_0$	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	$Q_0$	$\bar{Q}_0$

Notes

1. H: HIGH voltage level.
2. L: LOW voltage level.
3. ↓: Change from HIGH to LOW.
4. X: Either HIGH or LOW; doesn't matter.
5.  $Q_0$ : Q level prior to determination of input condition shown in table.
6.  $\bar{Q}_0$ :  $\bar{Q}$  level prior to determination of input condition shown in table.
7. Toggle: With ↓ change, outputs become compliment of previous condition.
8. H\*: When set and reset are LOW, Q and  $\bar{Q}$  are HIGH; however, when set and reset simultaneously change to HIGH, requirements of Q and  $\bar{Q}$  cannot be predicted.

■ Logic diagram (1/2)

