GENERAL PURPOSE PARALLEL PRINTER PORT WITH 83 BYTE FIFO

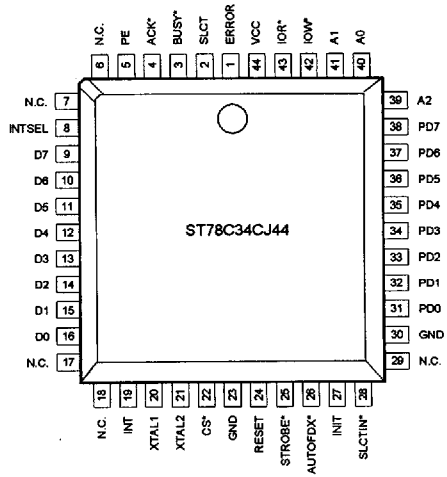
DESCRIPTION

The ST78C34 is a monolithic Bidirectional Parallel port designed to operate as a general purpose I/O port. It contains all the necessary input/output signals to be configured as a CENTRONICS printer port.

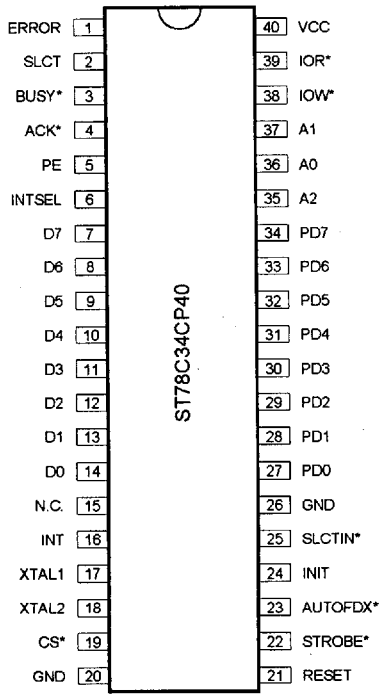
The ST78C34 is a general purpose input/output controller with 83 byte internal FIFO. FIFO operation can be enabled or disabled. For CENTRONICS printer operation, all registers are mapped to IBM printer port registers.

The ST78C34 is designed to operate as normal printer interface without any additional settings. Contents of the FIFO will be cleared after reset or setting the INIT pin to a low state. The auto FIFO operation starts after the first ACK* is received from the printer. Contents of the FIFO transfer to the printer at the printer loading speed.

PLCC Package



Plastic-DIP Package



FEATURES

- 83 bytes of printer output FIFO
- Bi-directional software parallel port
- Bi-directional I/O ports
- Register compatible to IBM XT, AT, compatible 386, 486
- Selectable interrupt polarity
- Selectable FIFO interrupts

ORDERING INFORMATION

Part number	Package	Operating temperature
ST78C34CJ44	PLCC	0° C to + 70° C
ST78C34IJ44	PLCC	-40° C to + 85° C
ST78C34CP40	Plastic-Dip	0° C to + 70° C
ST78C34IP40	Plastic-Dip	-40° C to + 85° C

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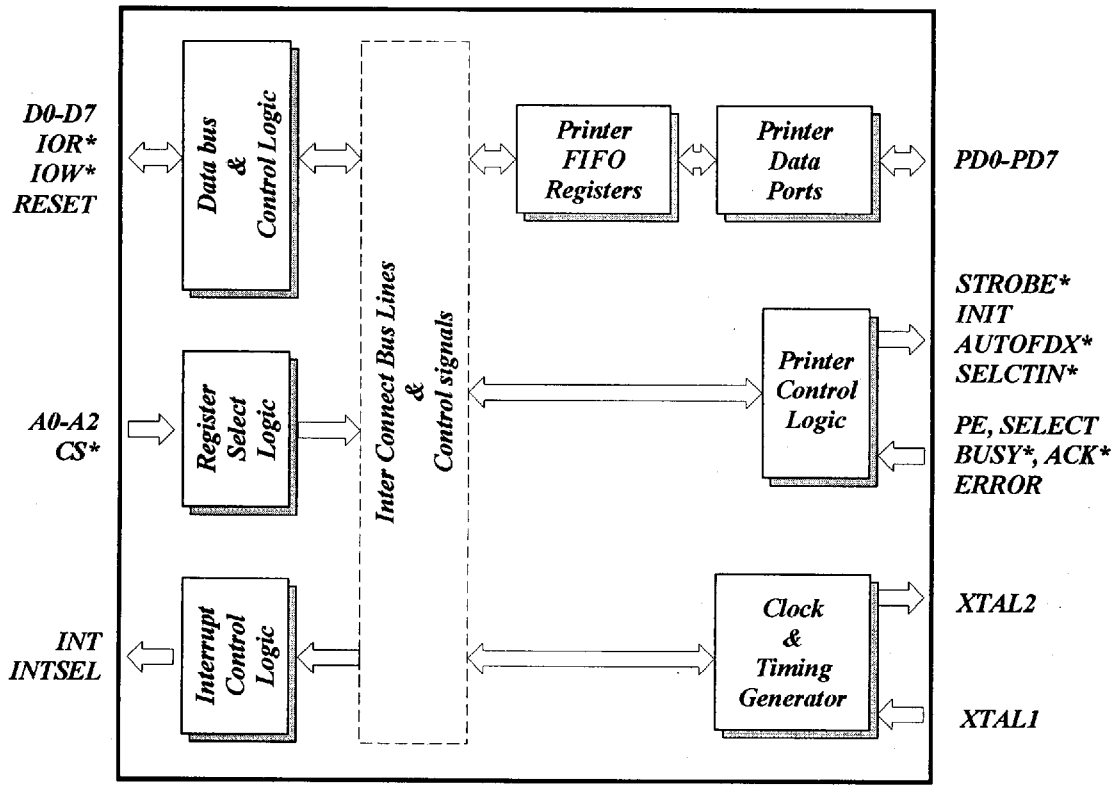
BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Signal Type	Pin Description
ERROR*	1	1	I	General purpose input or line printer error (active low). This is an output from the printer to indicate an error by holding it low during error condition.
SLCT	2	2	I	General purpose input or line printer selected (active high). This is an output from the printer to indicate that the line printer has been selected.
BUSY	3	3	I	General purpose input or line printer busy (active high). An output from the printer to indicate printer is not ready to accept data.
ACK*	4	4	I	General purpose input or line printer acknowledge (active low). An output from the printer to indicate that data has been accepted successfully.
PE	5	5	I	General purpose input or line printer paper empty (active high). An output from the printer to indicate out of paper.
INTSEL	6	8	I	Interrupt select mode (pulled-up). The external ACK* can be selected as an interrupt source by connecting this pin to the VCC or left open. Connecting this pin to GND will set the interrupt to latched mode, reading the status register resets the INT output.
D0-D7	14-7	16-9	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus.
INT	16	19	O	Interrupt output (selectable active low or high). To signal the state of the printer port. This pin tracks the ACK* input pin, When ACK* is low INT is low and when ACK* is high INT is high if selected as active low interrupt.
XTAL1	17	20	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock oscillator circuit.
XTAL2	18	21	O	Crystal input 2 or buffered clock output. See XTAL1.

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SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Signal Type	Pin Description
CS*	19	22	I	Chip select (active low). A low at this pin enables the ST78C34 / CPU data transfer operation.
GND	20	23	O	Signal and power ground.
RESET	21	24	I	Master reset (active high). A high on this pin will reset all the outputs and internal registers.
STROBE*	22	25	I/O	General purpose I/O or strobe output (open drain active low). To transfer latched data to the external peripheral or printer.
AUTOFDXT*	23	26	I/O	General purpose I/O or line printer auto feed (open drain active low). To signal the printer for continuous form feed.
INIT	24	27	I/O	General purpose I/O or line printer initialize (open drain active high). To signal the line printer to enter internal initialization routine.
SLCTIN*	25	28	I/O	General purpose I/O or line printer select (open drain active low). To select the line printer.
GND	26	30	O	Power and signal ground.
PD0-PD7	27-34	31-38	I/O	Bi-directional parallel ports (three state). To transfer data in or out of the ST78C34 parallel port. PD7-PD0 are latched during output mode.
A2	35	39	I	Address line A2. To select internal registers.
A0-A1	36-37	40-41	I	Address lines. To select internal registers.
IOW*	38	42	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR*	39	43	I	Read strobe (active low). A low level on this pin transfers the contents of the ST78C34 data bus to the CPU.
VCC	40	44	I	Power supply input.

PRINTER PORT PROGRAMMING TABLE:

A1	A0	IOW*	IOR*
0	0	PORT REGISTER	PORT REGISTER
0	1		STATUS REGISTER *
1	0	CONTROL REGISTER	COMMAND REGISTER
1	1	ALTERNATE FUNCTION REGISTER	FIFO BYTE COUNT REGISTER

* Reading the status register will reset the INT output.

PRINTER FUNCTIONAL DESCRIPTION

The ST78C34 parallel port is designed to operate as a normal CENTRONICS printer interface. The port contains 83 byte FIFO that may be enabled via bit-7 of the Alternate Function Register (AFR). After reset, the FIFO is disabled and the part will function identical to the ST16C552. Once the FIFO is enabled via AFR bit-7, the port will enter FIFO mode after the first byte of data is strobed to the printer and the printer responds with either an ACK* or BUSY signal.

The ST78C34 will remain in FIFO mode until the part is reset or INIT is brought low. While in FIFO mode, data transfer to the printer will be controlled by the printer without any user intervention. The printer port also contains a FIFO byte counter that maintains a count of the number of bytes remaining in the FIFO. The FIFO and the FIFO byte counter are cleared by a reset or by a change of state of the INIT pin. All FIFO related timing is derived from the clock input to pin 17 of the part.

A special parallel port write / read mode is activated when INIT is held low, either by writing a "0" to Control Register bit-2 or by forcing the INIT pin low. In this mode the FIFO read pointer is advanced by reading the parallel port instead of the ACK* or BUSY signals. The STROBE* output is forced high. This allows the user to perform parallel port write and read from operations without strobing data to the printer.

Following an INIT, the parallel port will not be in the FIFO mode. Control Register bit-0 is used as the STROBE*, Status Register bit-7 is the inverse of the BUSY signal, and INT is derived from ACK*. The transition into FIFO mode will occur after the first STROBE* is generated and the printer responds with either an ACK* or BUSY. In FIFO mode, STROBE* is generated automatically and writing to Control Register bit-0 has no effect on STROBE*. Alternate Function Register bit 0-2 are used to control the delay and width of STROBE*. Handshaking between the printer and the ST78C34 may be controlled by bit-3 of the Alternate Function Register. Setting this bit to a "1" will result in the use of BUSY instead of ACK* for FIFO reading and interrupt control. INT will transition low when a "1" is written to Control Register bit-0 and will transition high when a write to parallel port is performed. In FIFO mode, data transfer to the printer will be controlled by the printer and will occur at the printer's maximum data rate.

The FIFO byte counter is incremented one count for each parallel port write and decremented one count for each FIFO read (data taken by printer). A FIFO read will be generated at the falling edge of either ACK* or BUSY. The byte counter will require two to three clock cycles to update. Hence, a read of FIFO Byte Count Register (FBCR) should only be performed a minimum of three clock after the falling edge of either ACK* or BUSY. The counter is reset whenever the FIFO is reset. If write to parallel port operation is attempted when the FIFO is full, the data

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will not be written into the FIFO and the counter will not increment.

Two interrupt modes are available and are selected with the INTSEL pin. If this pin is tied low, a latched interrupt will result. In this mode, INT will transition low when a "1" is written to Control Register bit-0. A reset or reading the Status Register will clear the interrupt. If INTSEL pin is tied high, INT will transition low when a "1" is written to Control Register bit-0 and will transition high when a write to the parallel port is issued. This (non-latched) interrupt signal is always available in Status Register bit-6 regardless of the state of the INTSEL pin. Status Register bit-2 will always contain the latched interrupt state. The polarity of the INT pin may be inverted by setting Alternate Function Register bit-6 high.

The ST78C34 provides additional programmable interrupt output options by programming the Alternate Function Register bit 4-5. INT output can be selected as FIFO full or FIFO empty interrupt.

REGISTER DESCRIPTIONS

PORT REGISTER
Bi-directional printer port.
Writing to this register during output mode will transfer the contents of the data bus to the PD7-PD0 ports . Reading this register during input mode will transfer the states of the PD7-PD0 to the data bus. This register will be set to the output mode after reset.

PR BIT 7-0:
PD7-PD0 bi-directional I/O ports.

STATUS REGISTER
This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:
This bits are set to "1" normally except when AFR bit 5-4 are both set to "1".

SR BIT-2:
Interrupt condition.
0= an interrupt is pending
This bit will be set to "0" at the falling edge of the ACK* input.
1= no interrupt is pending
Reading the STATUS REGISTER will set this bit to "1".

SR BIT-3:
ERROR input state.
0= ERROR input is in low state
1= ERROR input is in high state

SR BIT-4:
SLCT input state.
0= SLCT input is in low state
1= SLCT input is in high state

SR BIT-5:
PE input state.
0= PE input is in low state
1= PE input is in high state

SR BIT-6:
ACK* input state.
0= ACK* input is in low state
1= ACK* input is in high state

SR BIT-7:
BUSY or FIFO full signal.

0= BUSY input is in high state
1= BUSY input is in low state

FIFO is enabled.
0= FIFO is full
1= One or more empty locations in FIFO

COMMAND REGISTER

The state of the STROBE*, AUTOFDXT*, INIT, SLCTIN* pins, and interrupt enable bit can be read by this register regardless of the I/O direction.

COM BIT-0:
STROBE* input pin.
0= STROBE* pin is in high state
1= STROBE* pin is in low state

COM BIT-1:
AUTOFDXT* input pin.
0= AUTOFDXT* pin is in high state
1= AUTOFDXT* pin is in low state

COM BIT-2:
INIT input pin.
0= INIT pin is in low state
1= INIT pin is in high state

COM BIT-3:
SLCTIN* input pin.
0= SLCTIN* pin is in high state
1= SLCTIN* pin is in low state

COM BIT-4:
Interrupt mask.
0= Interrupt (INT output) is disabled
1= Interrupt (INT output) is enabled

COM BIT 7-5:
Not used. Are set to "1" permanently.

CONTROL REGISTER.

Writing to this register will set the state of the STROBE*, AUTOFDXT*, INIT, SLCTIN pins, and interrupt mask register.

CON BIT-0:
STROBE* output control bit.
0= STROBE* output is set to high state
1= STROBE* output is set to low state

CON BIT-1:
AUTOFDXT* output control bit.
0= AUTOFDXT* output is set to high state
1= AUTOFDXT* output is set to low state

CON BIT-2:
INIT output control bit.
0= INIT output is set to low state
1= INIT output is set to high state

CON BIT-3:
SLCTIN* output control bit.
0= SLCTIN* output is set to high state
1= SLCTIN* output is set to low state

CON BIT-4:
Interrupt output control bit.
0= INT output is disabled (three state mode)
1= INT output is enabled

CON BIT-5:
I/O select. Direction of the PD7-PD0 can be selected by setting or clearing this bit.
0= PD7-PD0 are set for output mode
1= PD7-PD0 are set for input mode

CON BIT 7-6:
Not used.

ALTERNATE FUNCTION REGISTER (AFR)

This register En/Disables FIFO operation and provides additional capabilities to control STROBE*. INT and change interrupt functions.

AFR BIT 0-2:
Timing select.
The STROBE* delay and width can be controlled by these bits.

AFR Bit-2	AFR Bit-1	AFR Bit-0	TSD (clocks)	TSW (clocks)
1	0	0	3	2
1	0	1	5	4
1	1	0	5	4
1	1	1	9	8
0	0	0	6	4
0	0	1	10	8
0	1	0	10	8
0	1	1	18	16

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AFR BIT-3:
Interrupt source.
0= ACK* input pin is selected as printer handshaking source
1= BUSY input pin is selected as printer handshaking source

AFR BIT 4-5:
Interrupt type. State of the INT output pin can be selected for one of the following options.

Bit-5	Bit-4	INT output	SR bit-0	SR bit-6
0	0	Normal mode	1	ACK*
0	1	FIFO empty	1	FIFO empty
1	0	FIFO full	1	FIFO full
1	1	FIFO empty	0	FIFO empty

AFR BIT-6:
INT output polarity.
0= Normal. INT output follows the ACK* input
1= Inverted INT output

AFR BIT-7:
FIFO enable / disable function.
0= FIFO is disabled(default mode).
1= FIFO is enabled. Internal 83 byte of FIFO is enabled.

FIFO BYTE COUNT REGISTER (FBCR)

State and content of the printer FIFO can be monitored by reading this register.

FCBR BIT 0-6:
FIFO byte count. Number of characters left in FIFO. FCRB bit-0 is the LSB bit of the counter and FCRB bit-6 is the MSB bit of the counter.

FBCR BIT-7:
FIFO state.
0= FIFO is enabled
1= FIFO is disabled

ST78C34 EXTERNAL RESET CONDITION

SIGNALS	RESET STATE
PD0-PD7	Unknown, output mode
STROBE*	High
AUTOFDXT*	High
INIT	Low
SLCTIN*	High

ST78C34 REGISTER CONFIGURATIONS

A1	A0	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
0	0	PR	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
0	1	STR	BUSY*/ FIFO full*	None Latched INT	PE	SLCT	ERROR	Latched INT	1	1
1	0	COM	1	1	1	INT enable	SLCTIN*	INIT	AUTO-FDXT*	STROBE*
1	0	CON	X	X	I/O select	INT mask	SLCTIN*	INIT	AUTO-FDXT	STROBE*
1	1	AFR	FIFO enable	INT polarity	INT type bit-1	INT type bit-0	INT source	TIMING select bit-2	TIMING select bit-1	TIMING select bit-0
1	1	FBCR	FIFO* status	FBC-6	FBC-5	FBC-4	FBC-3	FBC-2	FBC-1	FBC-0

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AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	
T_2	Clock low pulse duration	50			ns	External clock
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data setup time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{16}+T_{17}	105			ns	
T_{39}	ACK* pulse width	75			ns	
T_{40}	PD7 - PD0 setup time	10			ns	
T_{41}	PD7 - PD0 hold time	25			ns	
T_{42}	Delay from ACK* low to interrupt low	5			ns	
T_{43}	Delay from IOR* to reset interrupt	5			ns	

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6.0 mA D7-D0 I_{OL}= 15mA PD7-PD0 I_{OL}= 6.0 mA on all other outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6.0 mA D7-D0 I_{OH}= -12.0 mA PD7-PD0 I_{OH}= -150 µA SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{OH}= -6.0 mA on all other outputs
I_{CC}	Avg. power supply current		12	20	mA	
I_{IL}	Input leakage			±10	µA	Except Pins 1-6
I_{IL}	Input leakage			-450	µA	Pins 1-6 @ Vin=0V
R_{IN}	Input pullup resistance	12		40	kΩ	Pins 1-6
I_{CL}	Clock leakage			±10	µA	

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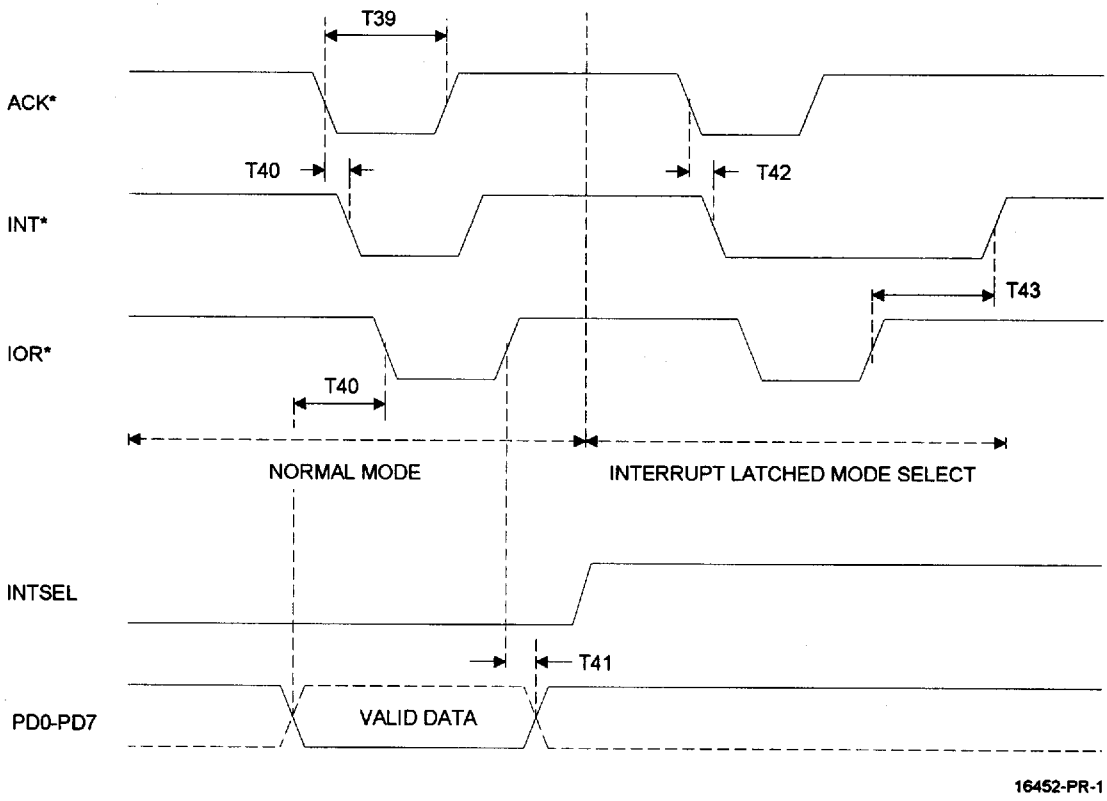
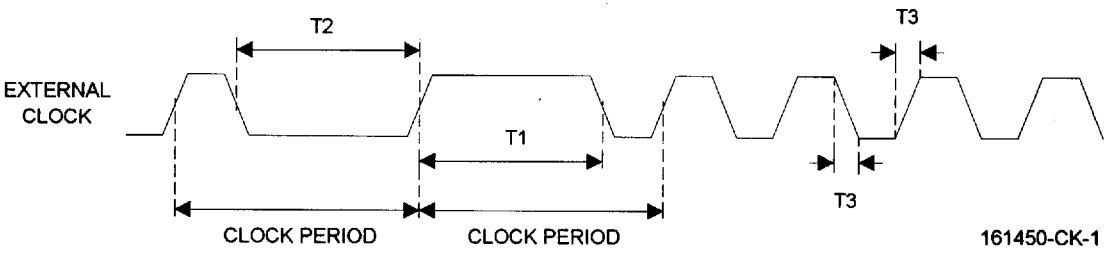
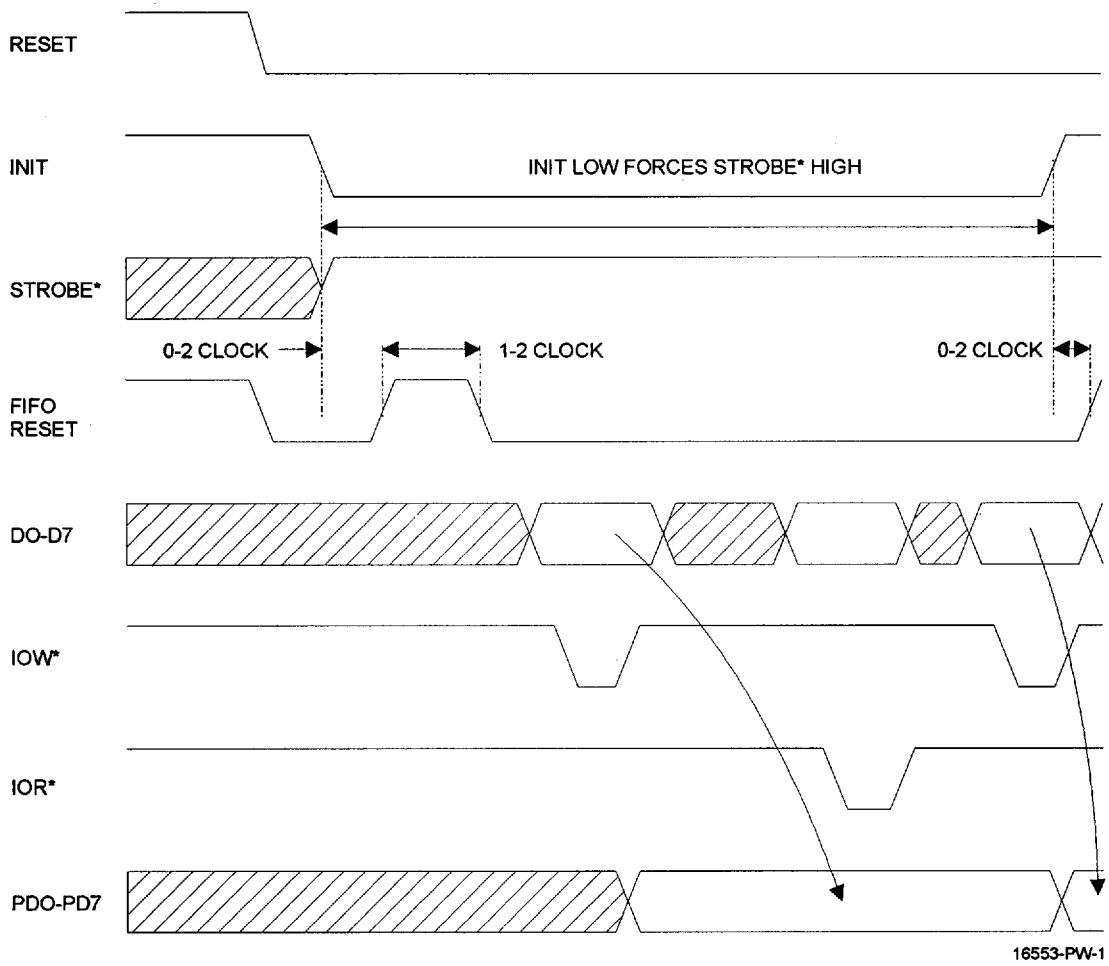
GENERAL READ TIMING



CLOCK TIMING



PRINTER SPECIAL MODE



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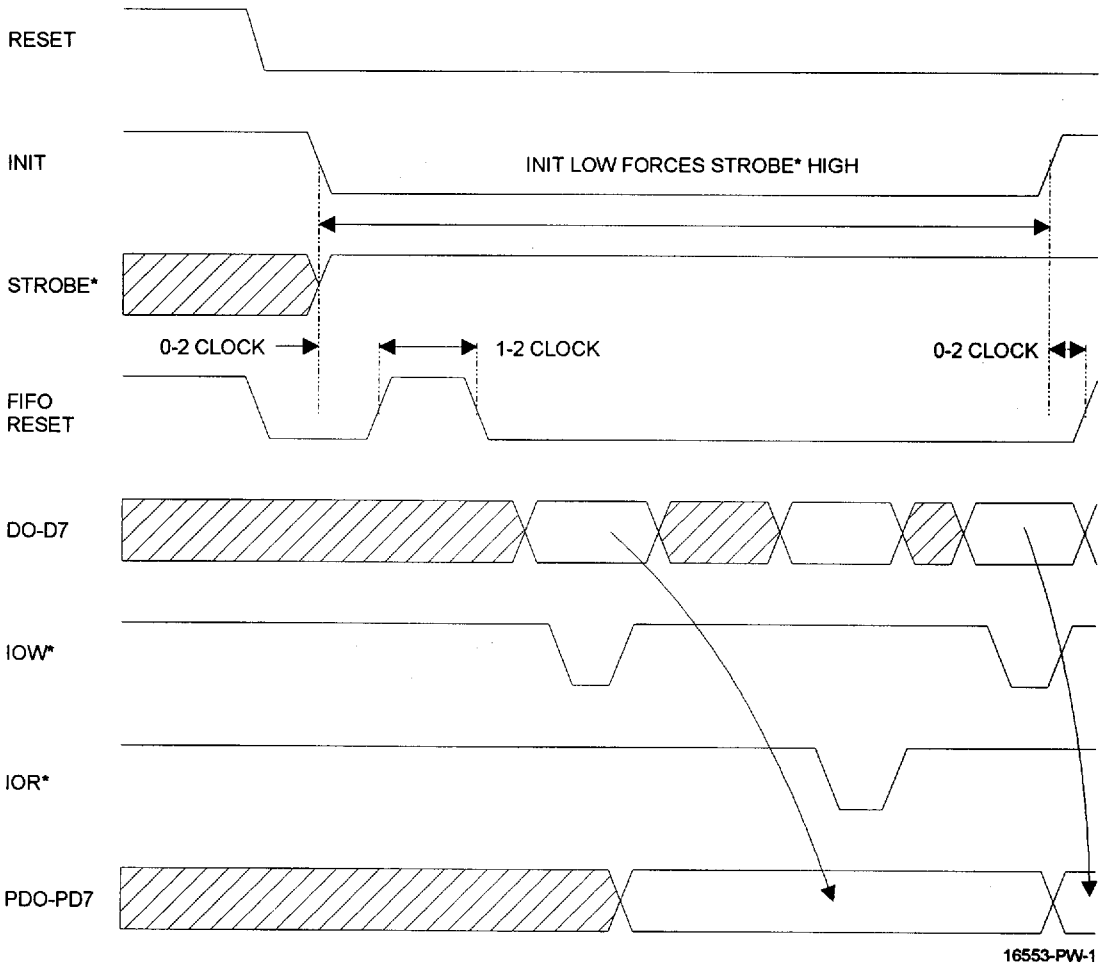
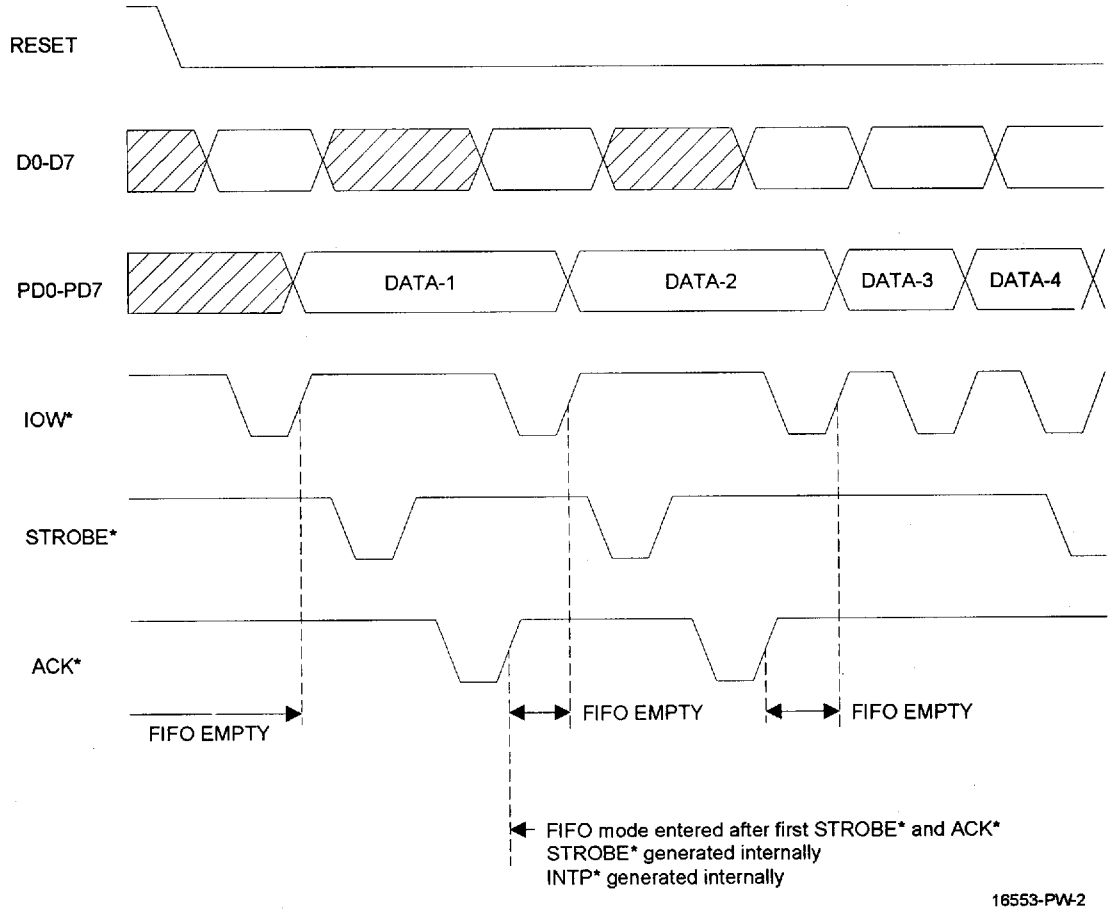
PRINTER SPECIAL MODE



PRINTER AUTO FIFO OPERATION



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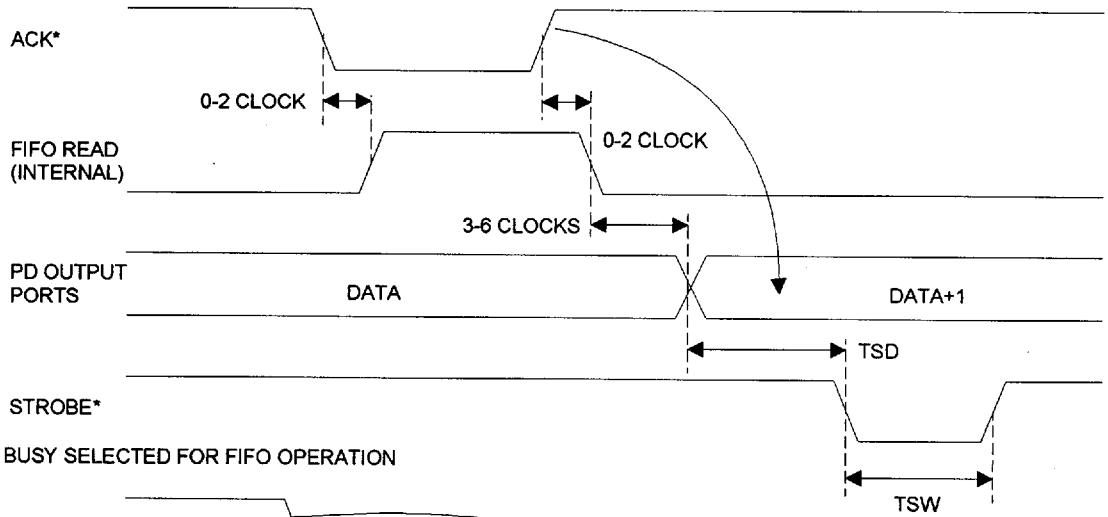
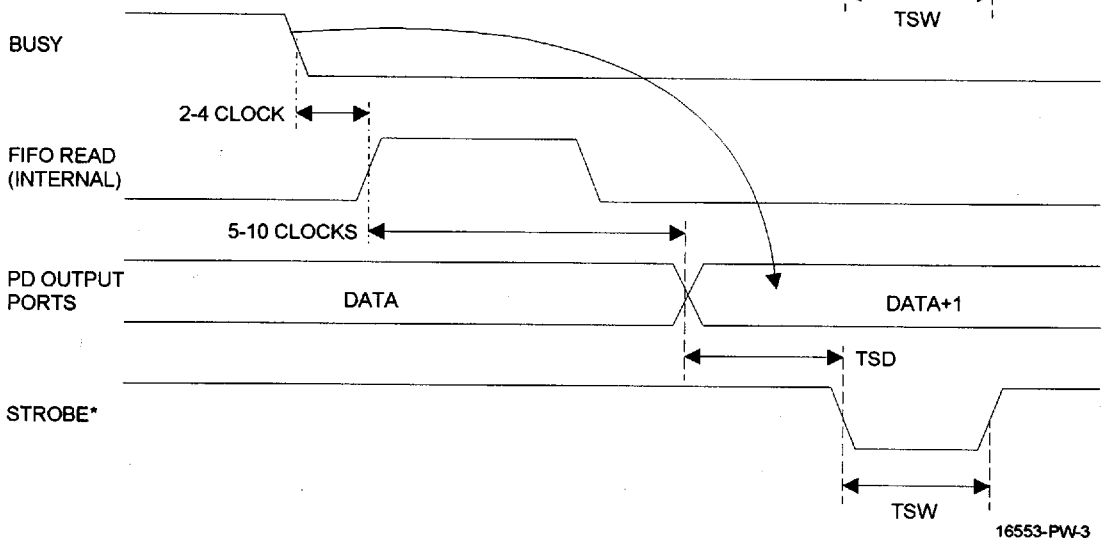
PRINTER FIFO TIMING WITH MORE THAN ONE BYTE IN THE FIFO

ACK SELECTEDFOR FIFO OPERATION



BUSY SELECTED FOR FIFO OPERATION



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PRINTER FIFO, WITH ONE BYTE IN THE FIFO