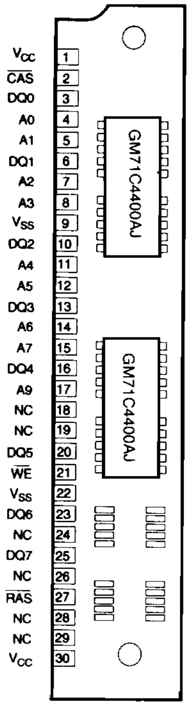
# GMM781000NS-60/70/80

1,048,576 WORDS×8 BIT
CMOS DYNAMIC RAM MODULE

## Description

The GMM781000NS is a 1M×8 bits Dynamic RAM Module, mounted 2 pieces of 4M bit DRAM (GM71C4400AJ, 1M×4) sealed in 20 pin SOJ package. The GMM781000NS is a socket type memory module, suitable for easy interchange or addition of module. The GMM781000NS provides common data inputs and outputs.
It's module board has decoupling capacitors mounted for each DRAM.

## Pin Configuration (Top View)



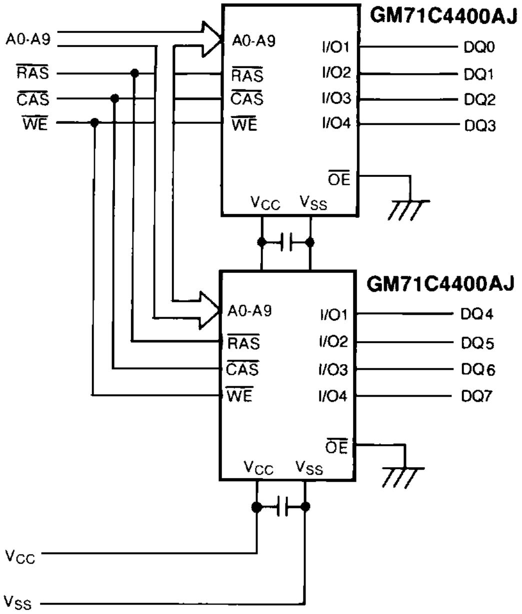
## Features

- High Density Standard 30 pin mounting 2 pcs of 4M DRAM GM71C4400AJ (SOJ)
- Fast Page Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time (Unit: ns)

| | $t_{RAC}$ | $t_{CAC}$ | $t_{RC}$ | $t_{PC}$ |
|---|---|---|---|---|
| GMM781000NS-60 | 60 | 15 | 110 | 40 |
| GMM781000NS-70 | 70 | 20 | 130 | 45 |
| GMM781000NS-80 | 80 | 20 | 150 | 50 |

- Low Power
  Active: 1210/1100/990 mW (MAX)
  Standby: 11mW (CMOS level: MAX)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 1024 Refresh Cycles/16ms

## Block Diagram



## Pin Description

| Pin | Function | Pin | Function |
|---|---|---|---|
| A0 ~ A9 | Address | $\overline{WE}$ | Read/Write Enable |
| DQ0 ~ DQ7 | Data Input/Data Output | $V_{CC}$ | Power (+5V) |
| $\overline{RAS}$ | Row Address Strobe | $V_{SS}$ | Ground |
| $\overline{CAS}$ | Column Address Strobe | NC | No Connection |

Note: 1. Common $\overline{CAS}$ control for eight common data-in and data-out lines.
2. The common control for one separate pair of data-in and data-out lines.
3. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out.

## Absolute Maximum Ratings*

| Symbol | Parameter | Values | Unit |
|---|---|---|---|
| $T_A$ | Ambient Temperature under Bias | 0 ~ 70 | °C |
| $T_{STG}$ | Storage Temperature | −55 ~ 125 | °C |
| $V_{IN}/V_{OUT}$ | Voltage on any Pin Relative to $V_{SS}$ | −1.0 ~ 7.0 | V |
| $V_{CC}$ | Power Supply Voltage | −1.0 ~ 7.0 | V |
| $I_{OUT}$ | Short Circuit Output Current | 50 | mA |
| $P_D$ | Power Dissipation | 2.0 | W |

*Note: Stress greater than above under "Absolute Maximum Ratings" may cause permanent damage to the device.

## Recommended Operating Conditions ($T_A = 0 \sim 70°C$)

| Symbol | Parameter | MIN | TYP | MAX | Unit | Note |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V | 1 |
| $V_{IH}$ | Input High Voltage | 2.4 | — | 6.5 | V | 1 |
| $V_{IL}$ | Input Low Voltage | −1.0 | — | 0.8 | V | 1 |

Note: 1 All voltages referenced to $V_{SS}$

## DC Electrical Characteristics: ($V_{CC}=5V\pm10\%$, $T_A=0\sim70°C$)

| Symbol | Parameter | | Min | Max | Unit | Note |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output Level<br>Output "H" Level Voltage ($I_{OUT}=-5mA$) | | 2.4 | $V_{CC}$ | V | |
| $V_{OL}$ | Output Level<br>Output "L" Level Voltage ($I_{OUT}=4.2mA$) | | 0 | 0.4 | V | |
| $I_{CC1}$ | Operating Current<br>Average Power Supply Operating Current<br>($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC}=t_{RC}$ min) | 60ns | – | 220 | mA | 1,2 |
| | | 70ns | – | 200 | | |
| | | 80ns | – | 180 | | |
| $I_{CC2}$ | Standby Current (TTL)<br>Power Supply Standby Current<br>($\overline{RAS}$, $\overline{CAS}=V_{IH}$) | | – | 4 | mA | |
| $I_{CC3}$ | $\overline{RAS}$ Only Refresh Current<br>Average Power Supply Current<br>$\overline{RAS}$ Only Mode<br>($\overline{RAS}$ Cycling, $\overline{CAS}=V_{IH}$, $t_{RC}=t_{RC}$ min) | 60ns | – | 220 | mA | 2 |
| | | 70ns | – | 200 | | |
| | | 80ns | – | 180 | | |
| $I_{CC4}$ | Fast Page Mode Current<br>Average Power Supply Current<br>Fast Page Mode<br>($\overline{RAS}=V_{IL}$, $\overline{CAS}$ Address Cycling: $t_{PC}=t_{PC}$ min) | 60ns | – | 220 | mA | 1,3 |
| | | 70ns | – | 200 | | |
| | | 80ns | – | 180 | | |
| $I_{CC5}$ | Standby Current (CMOS)<br>Power Supply Standby Current<br>($\overline{RAS}$, $\overline{CAS}=V_{CC}-0.2V$) | | – | 2 | mA | |
| $I_{CC6}$ | $\overline{CAS}$ before $\overline{RAS}$ Refresh Current<br>($t_{RC}=t_{RC}$ min) | 60ns | – | 220 | mA | |
| | | 70ns | – | 200 | | |
| | | 80ns | – | 180 | | |
| $I_{CC7}$ | Standby Current $\overline{RAS}=V_{IH}$<br>$\overline{CAS}=V_{IL}$<br>$D_{OUT}=$ Enable | | – | 10 | mA | 1 |
| $I_{I(L)}$ | Input Leakage Current<br>Any Input ($0V\leq V_{IN}\leq7V$)<br>All Other Pins Not Under Test = 0V | | -20 | 20 | μA | |
| $I_{O(L)}$ | Output Leakage Current<br>($D_{OUT}$ is Disabled, $0V\leq V_{OUT}\leq7V$) | | -10 | 10 | μA | |

Note: 1. $I_{CC}$ depends on output loading condition when the device is selected. $I_{CC}$ (max) is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}=V_{IL}$
3. Address can be changed once or less while $\overline{CAS}=V_{IH}$

## AC Electrical Characteristics

Refer to the GM71C4400A/AL data sheet for AC characteristics.
The GMM781000NS writes data only in early write cycle ($t_{WCS}\geq t_{WCS}$(min)).
Delayed write cycle is not available because of I/O common.

## Capacitance(V$_{CC}$=5V ± 10%, T$_A$=25°C, f=1MHz)

| Symbol | Parameter | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| $C_{I1}$ | Input Capacitance (Address) | – | 20 | pF | 1 |
| $C_{I2}$ | Input Capacitance (Clocks) | – | 20 | pF | 1,2 |
| $C_{I/O}$ | I/O Capacitance (DQ0~DQ7) | – | 17 | pF | 1,2 |

Note 1. Capacitance shall be measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=V$_{IH}$ to disable D$_{OUT}$.

## Package Dimensions

Unit: inches (mm)