Chapter 5
Electrical Specifications

Table 5-1: Absolute Maximum Stress Ratings (Note 1)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
T_{STG}	Storage Temperature	-65	-	+150	°C	
V_{DD}	Supply Voltage	V_{SS} - 0.5	-	7	V	
V_{IN}	Input Voltage	V_{SS} - 0.5	-	V_{DD} + 0.5	V	
I_{LP}	Latch-Up Current	-200	-	+200	mA	(Note 2)
ESD	Electrostatic Discharge	-	-	2000	V	(Note 3)
P_D	Power Dissipation	-	850	1000	mW	@ 266 MHz
		-	600	750	mW	@ 133 MHz

Notes: 1. Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions section of this specification is not implied.

2. $-2V < V_{PIN} < +8V$

3. Measured according to MIL-STD-883C, Method 3015.7.

Table 5-2: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Supply Voltage	4.75	5.0	5.25	V	
T_{OP}	Operating Temperature	0	-	+70	°C	
F_{REF1}	Reference Clock Frequency One	-	13.2813	-	MHz	(Note 1)
F_{REF2}	Reference Clock Frequency Two	-	26.5623	-	MHz	(Note 1)
I_{REF}	Reference Current	180	200	220	µA	

Note 1: User selects either F_{REF1} or F_{REF2} depending on the logical states of the BAUD_SEL [1:0] pins (see the BAUD_SEL [1:0] pin descriptions in Table 3-3). This frequency must be fixed within 100Hz per MHz of the selected Reference Clock Frequency.

DC Characteristics

V_{DD} = 5V + 5%, T_A = 0 to 70°C unless otherwise noted.

Table 5-3: DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{IH}	High Level TTL Input Voltage	2.0	-	-	V	
V_{IL}	Low Level TTL Input Voltage	-	-	0.8	V	
V_{DIFI}	Differential PECL Input Voltage (Peak-to-Peak)	0.2	-	-	V	Note 1
V_{SNGH}	High-Level Single-Ended PECL Input Voltage	$0.74V_{DD}$+ 0.3			V	
V_{SNGL}	Low-Level Single-Ended PECL Input Voltage			$0.74V_{DD}$ - 0.3	V	
V_{OH}	High Level TTL Output Voltage	2.4	-	-	V	I_{OH} = -400µA
V_{OL}	Low Level TTL Output Voltage	-	-	0.4	V	I_{OL} = 4mA
V_{DIFO}	Differential PECL Output Voltage (Peak-to-Peak)	0.8	-	1.4	V	75Ω load to V_{DD} - 2.0V
I_{IH}	High Level TTL Input Current	-	-	30	µA	V_{IN} = 5.25V
I_{IL}	Low Level TTL Input Current	-30	-	-	µA	V_{IN} = 0.0V
I_{OH}	High Level TTL Output Current	-0.4	-	-	mA	
I_{OL}	Low Level TTL Output Current	-	-	4.0	mA	
I_{DD}	Supply Current	-	170	190	mA	@ 266 MHz
		-	120	140	mA	@ 133 MHz

Note 1: The PECL (Pseudo-Emitter Coupled Logic) drivers are compatible with positive-referenced ECL voltage levels.

AC Characteristics

V_{DD} = 5V + 5%, T_A = 0 to 70°C unless otherwise noted. These characteristics are guaranteed by design.

Transmit Parallel Interface

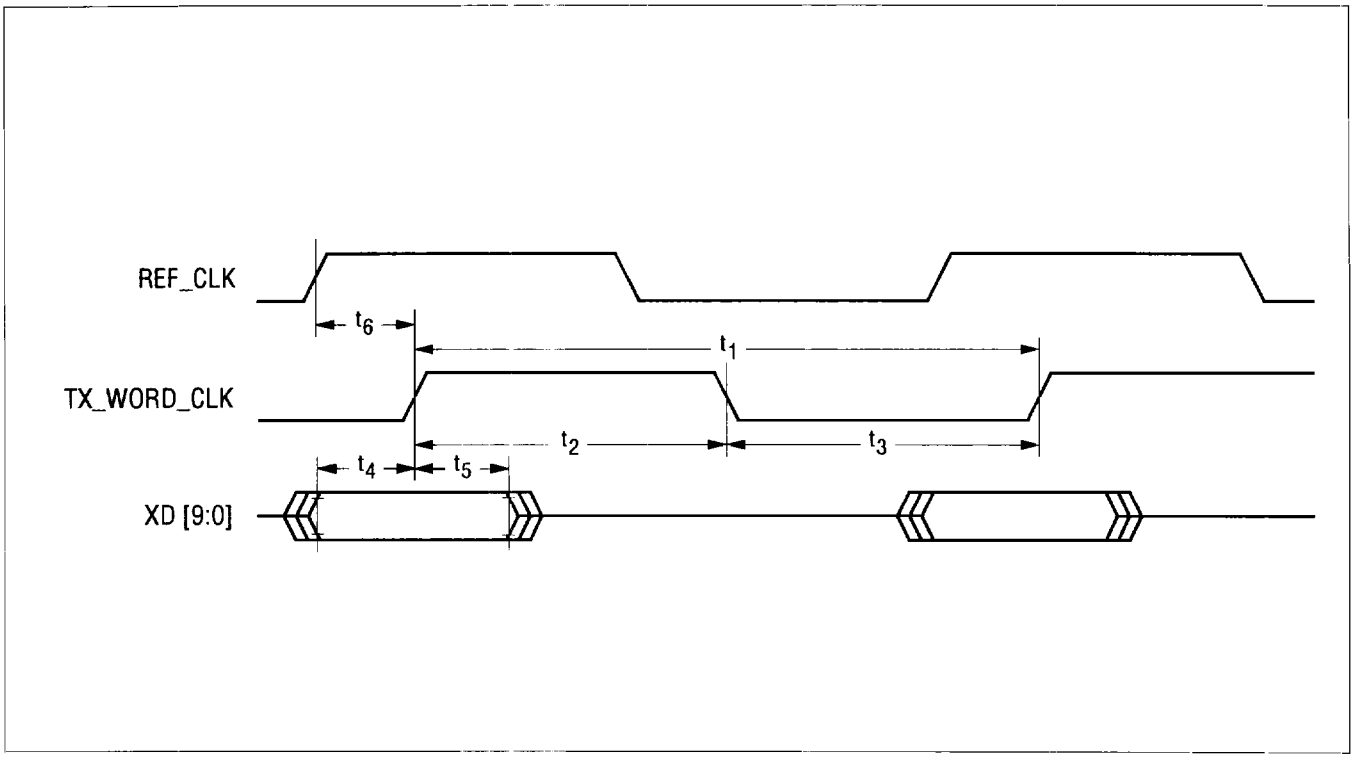

Figure 5-1: Transmit Parallel Interface

Table 5-4: Transmit Parallel Interface Timings

		132.813 Mbit/sec		265.625 Mbit/sec		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
t_1	Clock Cycle Time	-	75.294	-	37.647	ns
t_2	Clock High Time	$0.5t_1 - 2$	-	$0.5t_1 - 2$	-	ns
t_3	Clock Low Time	$0.5t_1 - 2$	-	$0.5t_1 - 2$	-	ns
t_4	Data Setup Time	6	-	6	-	ns
t_5	Data Hold Time	0	-	0	-	ns
t_6	TX_WORD_CLK skew from REF_CLK	0	3	0	3	ns

Receive Parallel Interface

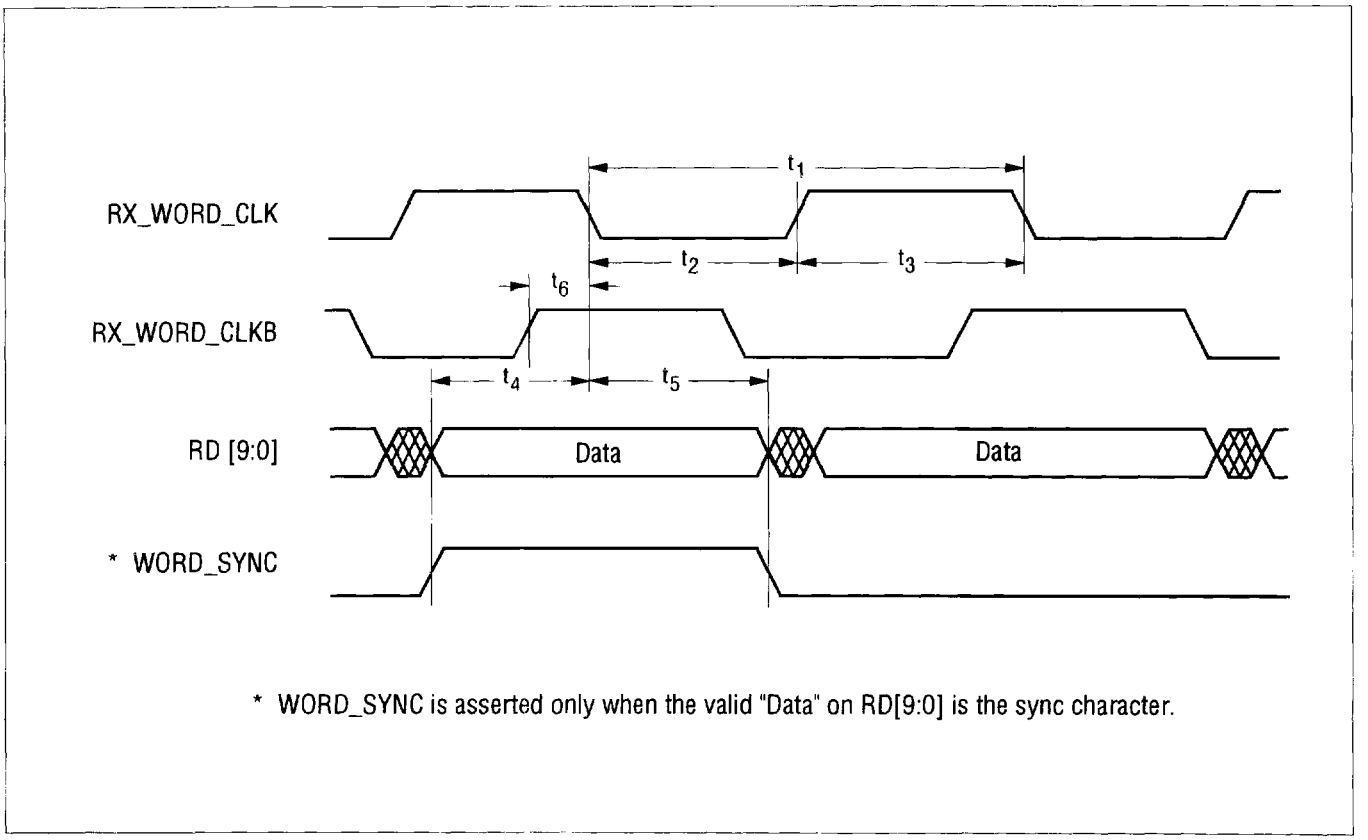

Figure 5-2: Receive Parallel Interface

Table 5-5: Receive Parallel Interface Timings

		132.813 Mbit/sec		265.625 Mbit/sec		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
t_1	Clock Cycle Time	-	75.294	-	37.647	ns
t_2	Clock High Time	$0.5t_1 - 3$	-	$0.5t_1 - 3$	-	ns
t_3	Clock Low Time	$0.5t_1 - 3$	-	$0.5t_1 - 3$	-	ns
t_4	Data Setup Time	32	-	13	-	ns
t_5	Data Hold Time	34	-	16	-	ns
t_6	Clock Skew	-3	3	-3	3	ns

DCT Mode

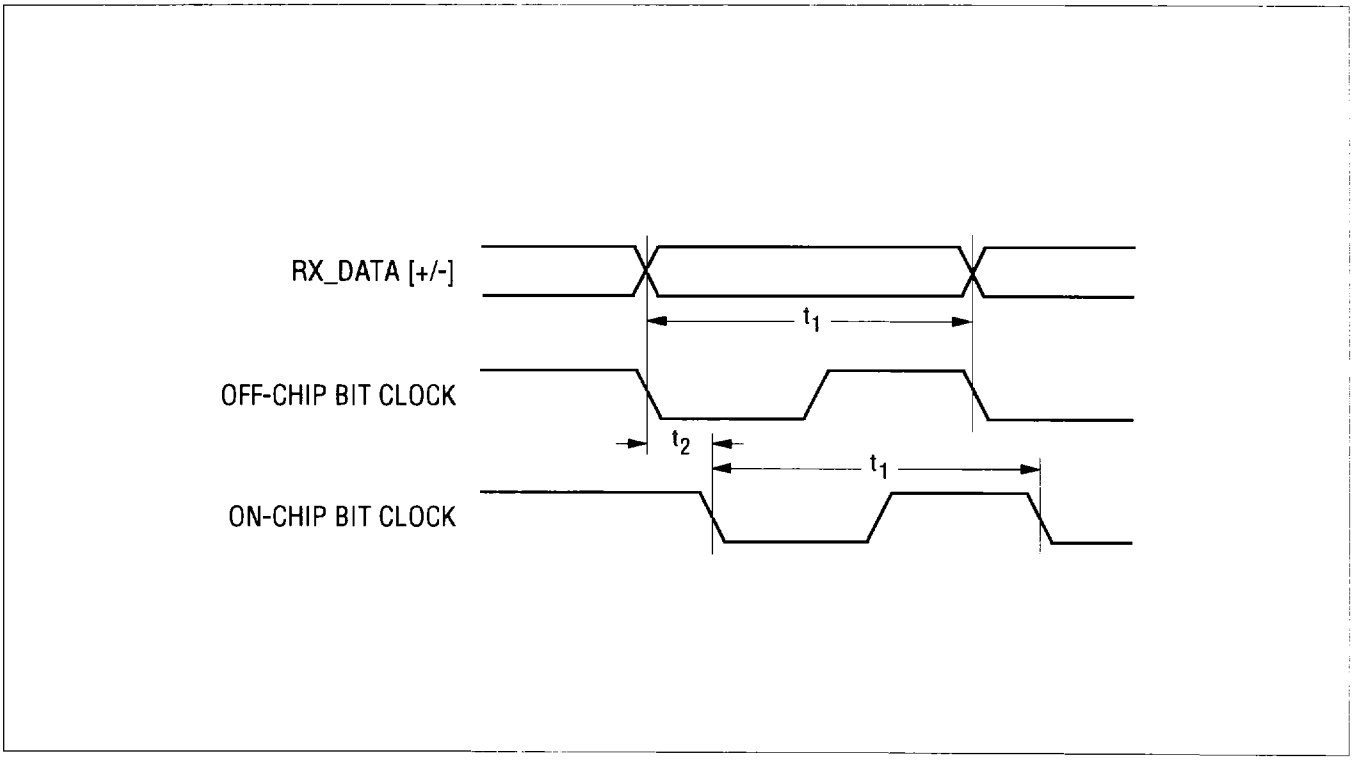

Figure 5-3: Clock Signals in the DCT Mode

Table 5-6: DCT Mode Timing Parameters

Symbol	Parameter	Min	Max	Units	Conditions
t_1	Bit Clock Cycle Time	50	-	ns	
t_2	Bit Clock Skew	-	10	ns	

Note: The skew (t_2) between the off-chip bit clock (provided to the MIC through the LOCK_REFB pin) and the on-chip bit clock can be as much as 10ns under the worst case operating conditions. As a result, the cycle time (t_1) of the bit clock must be longer than 50ns in the DCT mode.

Serial I/O

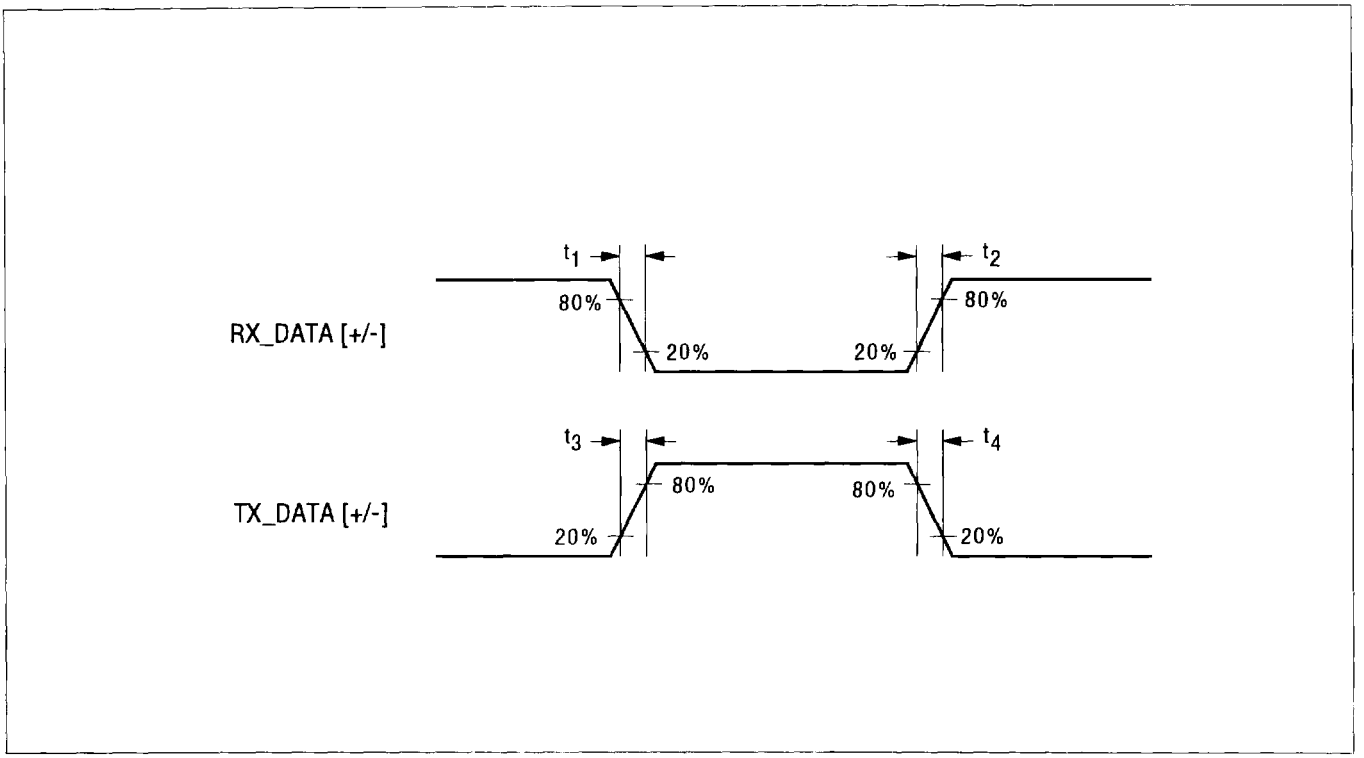

Figure 5-4: Serial Input/Output Waveforms

Table 5-7: Serial Input/Output Rise/Fall Times

		132.813 Mbit/sec		265.625 Mbit/sec		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
t_1	Serial Input Fall Time	-	2.1	-	2.1	ns
t_2	Serial Input Rise Time	-	2.1	-	2.1	ns
t_3	Serial Output Rise Time	-	1.1	-	1.1	ns
t_4	Serial Output Fall Time	-	1.2	-	1.2	ns
	Serial Output Deterministic Jitter	-	0.75	-	0.37	ns (peak-to-peak)
	Serial Output Random Jitter	-	0.60	-	0.30	ns (peak-to-peak)