ICs for Communications

Quad ISDN 2B1Q Echocanceller Digital Front End
DFE-Q V2.1

PEF 24911 Version 2.1

Preliminary Data Sheet 06.99

DS 1

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Preface

This document describes the interfaces, functions and behavior of the QUAD ISDN 2B1Q Echocanceller Digital Front End (DFE-Q V2.1). The PEF 24911 is the digital part of a two-chip solution featuring four times ISDN basic rate access at 144kbit/s. DFE-Q V2.1 supersedes the existing versions, DFE-Q V1.1, V1.2 and V1.3.

The corresponding Analog Front End, the AFE V2.1 (PEF 24902) is described in detail in the Data Sheet V1.1, the Delta Sheet V1.2 and the Delta Sheet V2.1.

Organization of this Document

This Preliminary Data Sheet is divided into 9 chapters. It is organized as follows:

- Chapter 1, Introduction
  Gives a general description of the product and its family, lists the key features, and presents some typical applications.
- Chapter 2, Pin Description
  Lists pin locations with associated signals, categorizes signals according to function, and describes signals.
- Chapter 3, Functional IC Description
  Gives a functional overview of the device, shows a block diagram, specifies the various interfaces and describes the provided U-transceiver functions.
- Chapter 4, Operational Description
  Describes the reset and power-down behavior, illustrates the activation and deactivation procedures, shows how the device is tested and how maintenance data can be retrieved.
- Chapter 5, Monitor Commands
  Lists all available Monitor Commands that can be applied.
- Chapter 6, Register Description
  Lists all register functions that are addressable by the new MON-12 protocol which behaves like a serial microprocessor interface.
- Chapter 7, Electrical Characteristics
  Denotes the operating conditions and gives the exact interface timing.
- Chapter 8, Package Outlines
- Chapter 9, Appendix A: Standards and Specifications

- Chapter 10, Glossary

- Chapter 11, Index

Related Documentation

- DFE-Q V2.1 Delta Sheet 05.98
- AFE V1.1 Data Sheet 05.96
- AFE V1.2 Delta Sheet 06.97
- AFE V2.1 Delta Sheet 09.98

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device name (DFE-Q V2.1), device number (PEF 24911), device version (Version 2.1),

and in the body of your e-mail:
document type (Preliminary Data Sheet), issue date (06.99) and document revision number (DS 1).

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1 Introduction

The Quad ISDN 2B1Q Echocanceller Digital Front End (DFE-Q) is the digital part of an optimized two-chip solution featuring 4x ISDN basic rate access at 144kbit/s. The PEF 24911 is designed to provide in conjunction with the Quad ISDN Echocanceller Analog Front End (PEF 24902 V2.1) full duplex data transmission at the U-reference point according to ANSI T1.601 (1992), ETSI TS 102 080 (1998) and ITU-T G.961 standards.

The DFE-Q 2nd generation has been completely reengineered to guarantee the availability of the well proved DFE-Q/AFE solution over the year 2000. The PEF 24911 V2.1 is downwards pin compatible and functionally equivalent to the DFE-Q V1.x. Thus, line card manufacturers can make use of the most advanced process technology without the need to change their current design (besides the changeover to 3.3V power supply).

No software changes are required if the DFE-Q V2.1 is deployed in existing DFE-Q V1.x solutions. Some new features are provided such as free programmable filteing options for the maintenance bits (M1-6) and enhanced monitoring and test functions. The data rate is programmable from 1Mbit/s to 4Mbit/s.

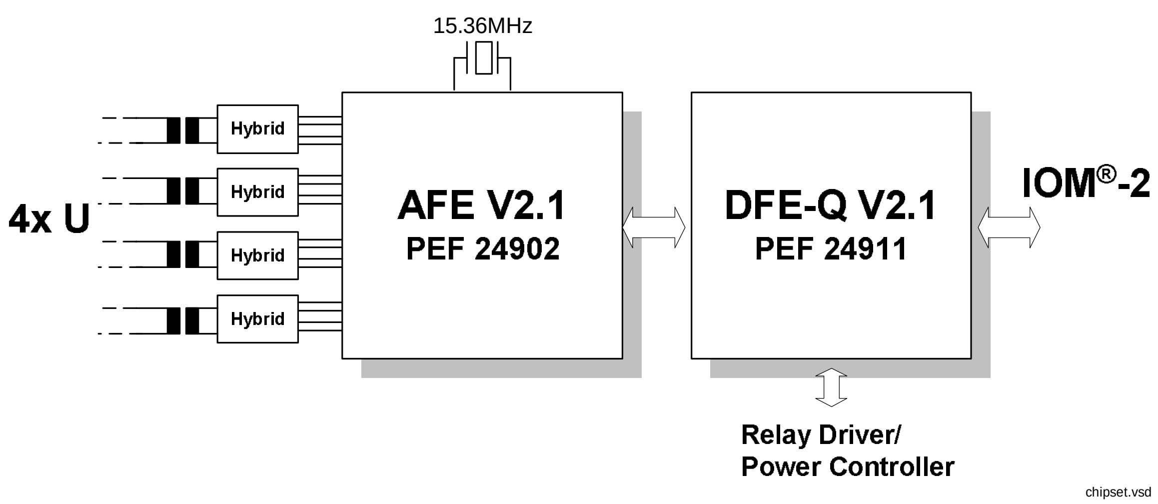


Figure 1-1 DFE-Q/ AFE 2nd Generation Chip Set

The output and input pins are throughout 5V TTL compatible although the PEF 24911 is processed in advanced 3.3V CMOS technology. A power down state with very low power consumption is featured.

The PEF 24911 comes in a P-MQFP-64 package.

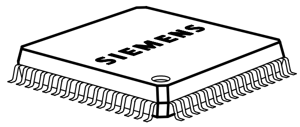
Quad ISDN 2B1Q Echocanceller Digital Front End DFE-Q V2.1

PEF 24911

Version 2.1

CMOS

1.1 Features



P-MQFP-64

U-Interface

- Digital part of a two-chip solution featuring full duplex data transmission and reception over two-wire metallic subscriber loops providing 4x ISDN basic rate access at 144 kbit/s
- Conforms to:
  - ANSI T1.601–1992
  - ETSI TS 102 080 (1998)
  - Recommendation ITU-T G.961
- 2B1Q-block code (2 binary, 1 quaternary) at 80-kHz symbol rate
- LT mode
- Data rate and clock master/slave configuration of the system interface independently programmable from the selected operating mode (LT/NT)
- Activation/ deactivation controller
- 15s start-up guard timer (T1) can be disabled by use in repeater applications
- Adaptive echo cancellation and equalization
- Automatic gain control and polarity adaptation
- Clock recovery (frame and bit synchronization) in all applications
- Built-in wake-up unit for activation from power-down state.

System Interface

- IOM®-2 interface with programmable data rates (1 Mbit/s to 4 Mbit/s)
- SW controlled I/O ports for relay driver and power feeder control
  - 4 relay driver pins per port
  - 2 status pins per port

Type	Package
PEF 24911	P-MQFP-64

Others

- Software compatible to PEF 24911 V1.2 (Quad IEC DFE-Q)
- Inputs and outputs 5V TTL compatible
- DOUT (open drain) accepts pull-up to 3.3V or 5V
- +3.3V ±0.3V Power Supply
- Sophisticated power management for restricted power mode
- Advanced low power CMOS technology
- Extended temperature range (– 40...to 85°C) available
- Boundary-Scan, JTAG IEEE 1149.1

Add-On Features and Differences with Respect to DFE-Q V1.3/V1.2/V1.1

- Max. IOM®-2 data rate 4Mbit/s (DCL= 8MHz)
- +3.3V instead of +5V power supply
- Dedicated pins for SSP and DT test modes
- DOUT configurable either as open drain or push-pull (tristate) output
- Monitor Time-Out (MTO) procedure
- New MON-12 class features internal register access
- Coefficients retrievable by MON-12 commands instead of MON-8 commands
- Information on RANGE bit and receiver phase can be requested by MON-12 instead by MON-8 ’AST’ as introduced in V1.3
- Advanced filter options for MON-0 and MON-2 messages
- Bit Error Rate measurement per port
- Additional digital local loops
- C/I codes ’LTD’ and ’HI’ are no more supported
- Optimized LT-state machine
- JTAG Boundary-Scan with dedicated reset line $\overline{\text{TRST}}$ (replaces power-on reset functionality)

Addressed Applications

- ISDN Line Cards for Central Office
- ISDN Line Cards for Access Networks
- ISDN Line Cards in PBX Systems
- Suited for WLL applications by
  – Constant delay
  – Propagation delay measurement of the U transmission line
  – Means for synchronization of Base Stations

1.2 Logic Symbol

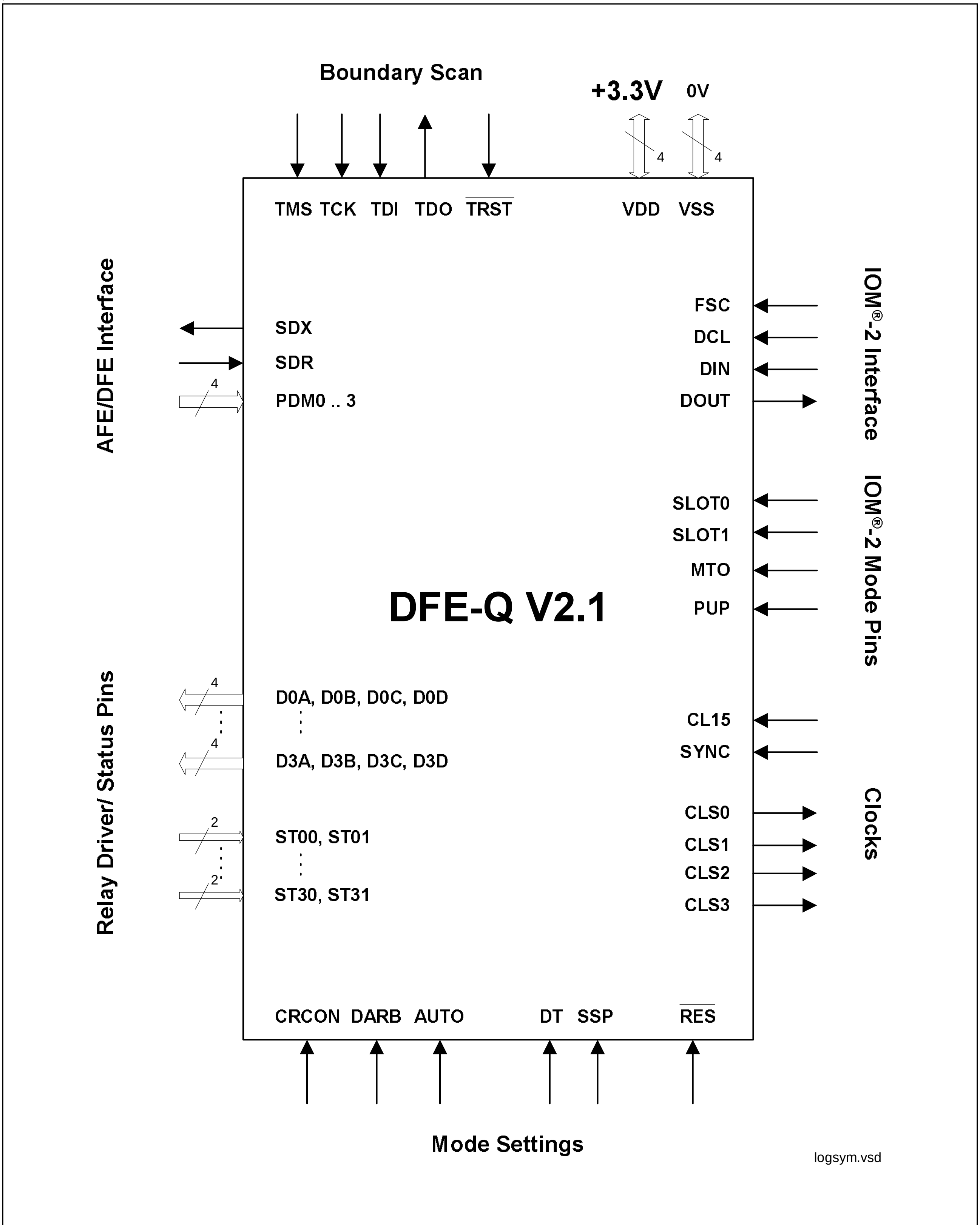


Figure 1-2 Logic Symbol

1.3 System Integration

This paragraph shows how the DFE-Q V2.1 may be integrated in systems using other Infineon ISDN devices. The PEF 24911 DFE-Q is optimized for use in the following applications:

– Digital Line Cards for Central Office
– Digital Line Cards for Access Networks (LT mode only)
– PBX applications (LT mode only)

Figure 1-3 and **Figure 1-4** illustrate line card solutions with various Infineon line card controllers. The DELPHI (PEB 20570) supersedes the ELIC® (PEB 20550) and will feature up to 32 HDLC controllers on-chip.

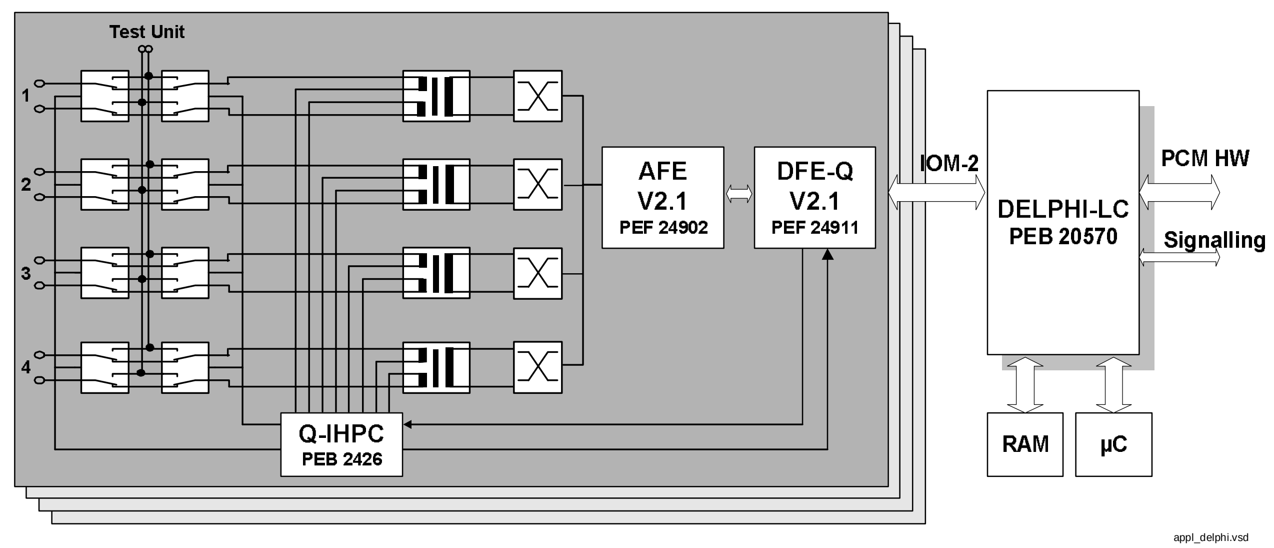


Figure 1-3 16-Line Card Application with DELPHI Solution

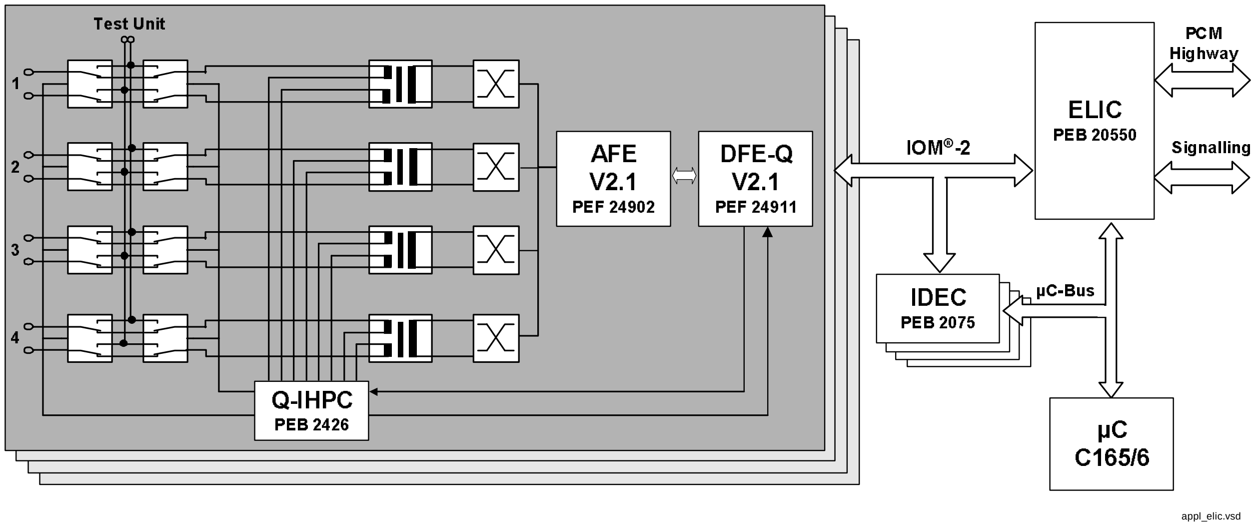


Figure 1-4 16-Line Card Application with ELIC®/ IDEC® Solution

Figure 1-5 shows how a 8 channel line card application is realized by use of two AFE/ DFE-Q chip sets:

One AFE-PLL generates the synchronized 15.36MHz clock and provides the master clock at pin CL15 for the other 3 devices. The internal PLL of the first AFE synchronizes the 15.36 MHz master clock onto a PTT reference clock of either 8 kHz or 2048 kHz. **Infineon recommends to feed the FSC clock input of the DFE-Q V2.1 and the PLL reference clock input (pin CLOCK) of the AFE from the same clock source.**

The PLL of the second AFE is deactivated. The 15.36 MHz master clock is applied at pin CL15. CL15 is configured as input if XIN is clamped either to VDD or to VSS. Pin XOUT has to be left open and CLOCK shall be tied to GND.

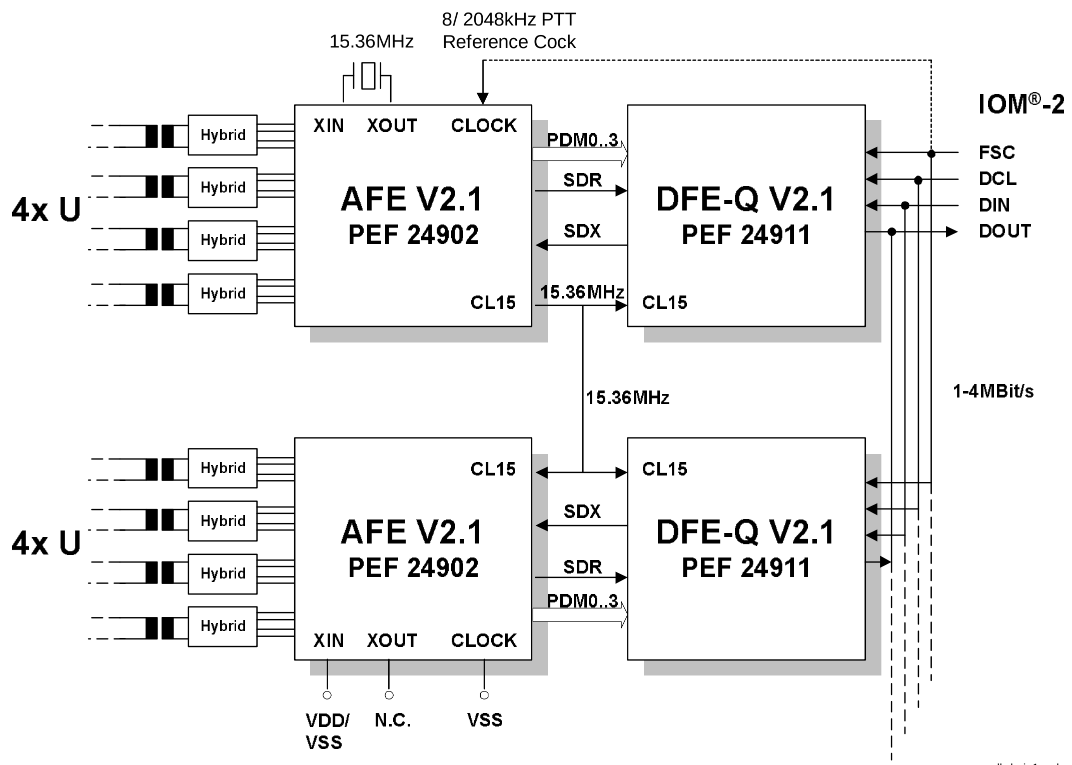


Figure 1-5 Connecting Two AFE/DFE-Q Chip Sets

The DFE-Q devices are supplied by the first AFE at pin CL15 with the synchronized 15.36MHz clock. The IOM®-2 channels the DFE-Q devices are assigned to can be programmed by the two slot pins. Starting from channel no. 0/4/8/12 always four subsequent channels are occupied.

Alternatively the clocking scheme as shown in **Figure 1-6** may be applied if more than 3 devices are to be clocked (e.g. in a 16-channel line card application). Instead to supply the 2nd AFE with the master clock at pin CL15, here the 15.36MHz master clock is input at pin XIN. Thereby pin CL15 is configured as output and passes the 15.36MHz clock on to the attached DFE-Q. If the clock chain is extended in the same way by another two AFE/DFE-Q chip sets a 16-channel line card application can be realized with just one single crystal. Note that the 15.36MHz clock is inverted once by the AFE if it is input at XIN and output at CL15. This way the duty cycle is recovered again.

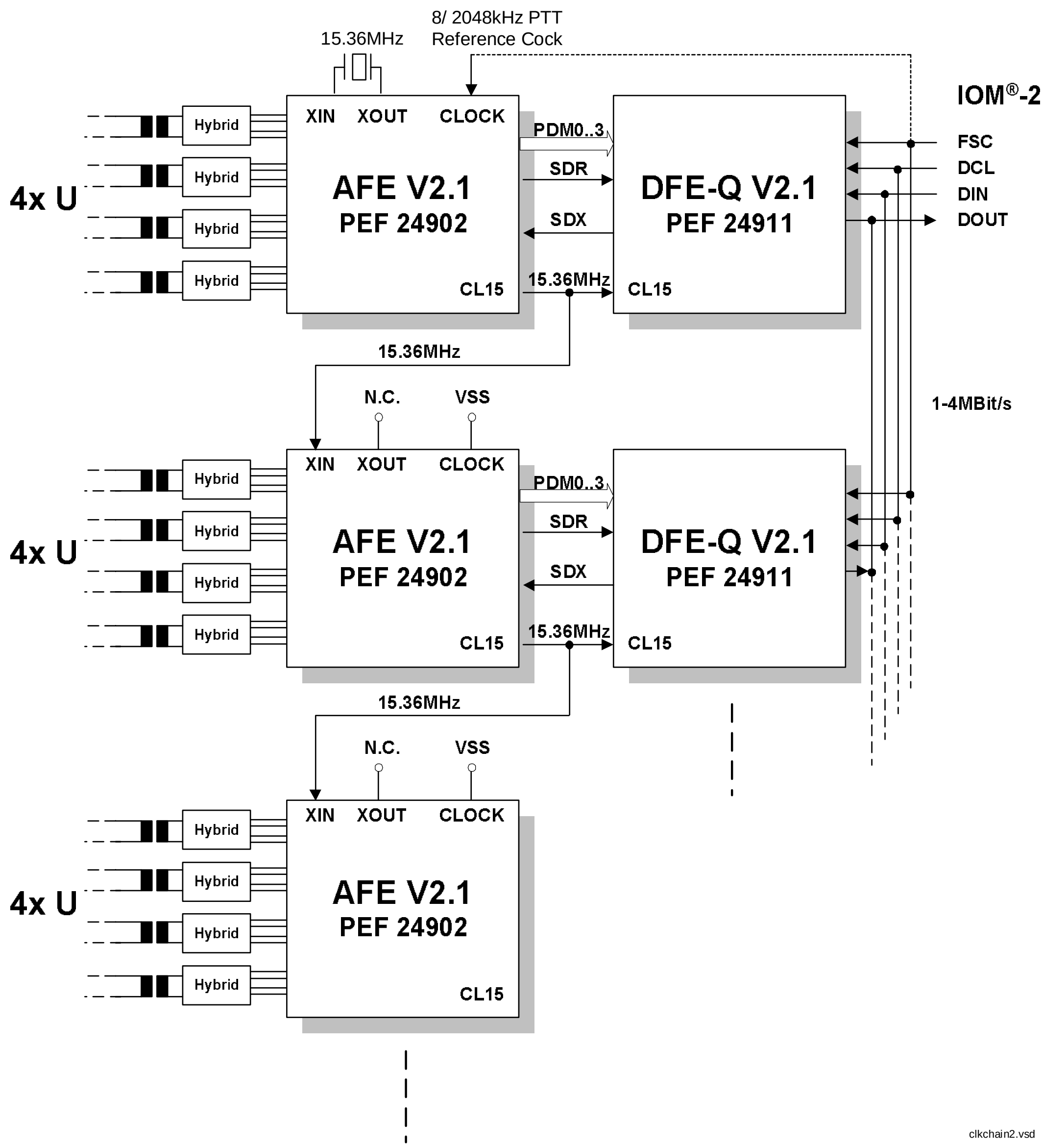


Figure 1-6 Recommended Clocking Scheme for More Than Two DFE-Q/AFE Chip Sets

1.4 Operational Overview

The DFE-Q V2.1 operates always in LT mode. The operating modes known from former versions of the DFE-Q are further supported and can be activated by pin setting as given in **Table 1-1**. For cross reference the corresponding pins of V1.x are additional denoted.

Table 1-1 Operating Modes

V2.1 Mode Pins		V1.x Mode Pins		Operating Mode
DARB	SYNC	PBX	LT	
0	1	0	1	LT mode without WLL/RITL synchronization D-channel arbitration disabled
1	1	1	1	LT mode without WLL/RITL synchronization, D-channel arbitration enabled
0	periodic signal*)	0	periodic signal*)	LT-PBX-mode with WLL/RITL synchronization, D-channel arbitration disabled
1	periodic signal*)	1	periodic signal*)	LT-PBX-mode with WLL/RITL synchronization, D-channel arbitration enabled

*) must be any multiples of 12ms

System Interface Configurations

The following parameters of the system interface are configurable:

- Open Drain/ Push-Pull Mode
  Configured as open drain the output pin DOUT is floating and a pull-up resistor is required. In push-pull mode the output pin is high impedance outside the active time slots.

- IOM®-2 Channel Assignment
  IOM®-2 channels are always assigned in blocks of four.

SLOT1	SLOT0	Assigned IOM®-2 Channels
0	0	0 .. 3
0	1	4 .. 7

1	0	8 .. 11
1	1	12 .. 15

- IOM®-2 Data Rates

DCL Frequency [kHz]	Data Rate [kBit/s]	IOM®-2 Channels
2048	1024	4
3072	1536	6
4096	2048	8
6144	3072	12
8192	4096	16

Send Single Pulses Test Mode

In test mode ’Send Single Pulses’ +/-3 pulses spaced by 1.5ms are transmitted on all U lines. The test mode is activated by pin SSP= set to ’1’. The SSP test function can be as well stimulated by C/I= SSP besides the fact that the HW selection impacts all line ports while the SW selection impacts only the chosen line.

Data Through Mode

In test mode ’Data Through’ the U-transceiver is forced to enter the ’Transparent’ state and to issue U4 independently of the wake-up protocol. The DT test mode is activated by pin DT= set to ’1’. The DT test function can be as well stimulated by C/I= DT besides the fact that the HW selection impacts all line ports while the SW selection impacts only the chosen line.

2 Pin Descriptions

2.1 Pin Diagram

(top view)

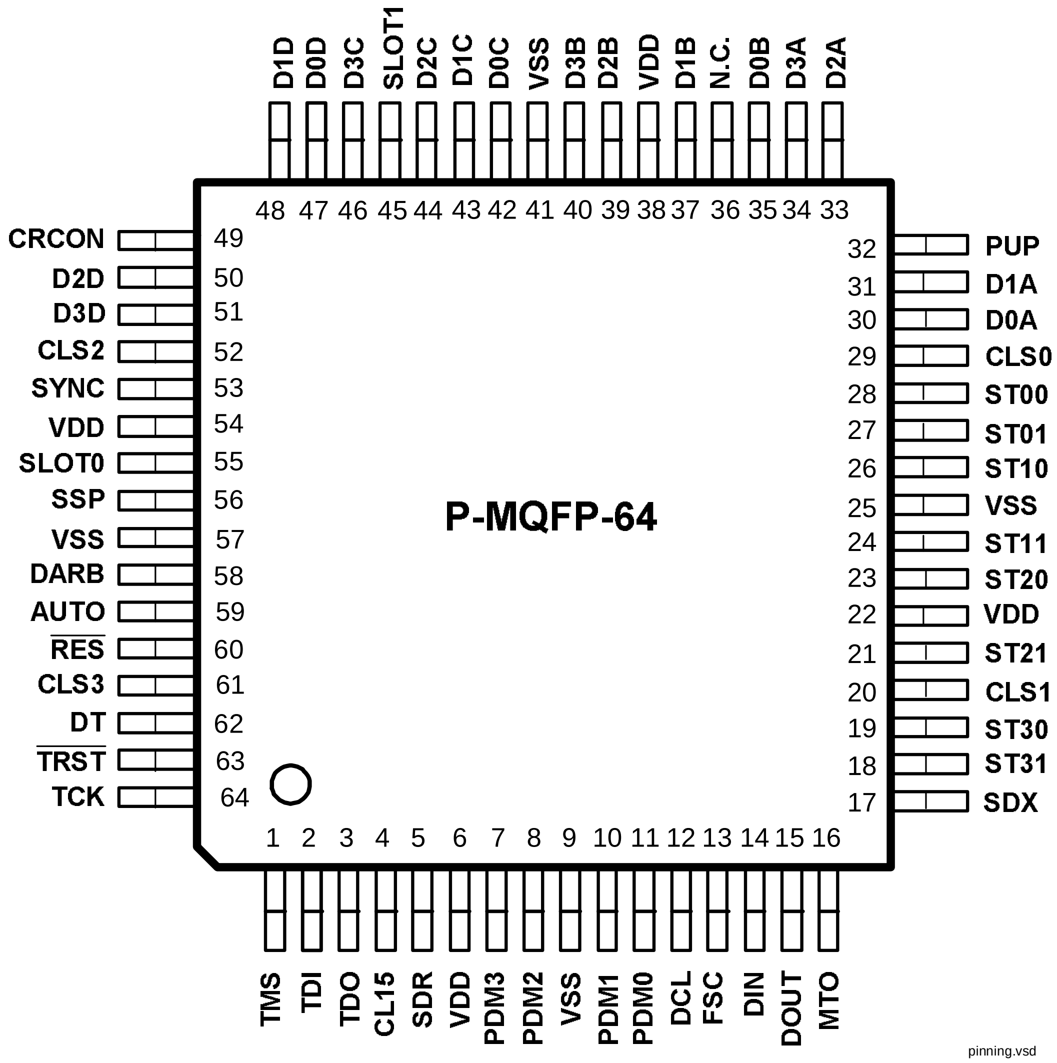


Figure 2-1 Pin Configuration (63 of 64 used)

2.2 Pin Definitions and Functions

Table 2-1 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
IOM®-2 Interface			
13	FSC	I	**Frame Synchronization Clock (8kHz)** the start of the first B1-channel in time-slot 0 is marked, FSC is expected to be ’1’ for at least two DCL periods.
12	DCL	I	**Data Clock** clock rate ranges from 2048 to 8192kHz (1024 to 4096kBit/s)
14	DIN	I	**Data In** input of IOM®-2 data synchronous to DCL clock
15	DOUT	O (OD/ PuP)	**Data Out** output of IOM®-2 data synchronous to DCL clock
Mode Selection Pins			
60	$\overline{\text{RES}}$	I	**Reset** triggers asynchronous HW reset, Schmitt trigger input ’1’= inactive ’0’= active
55	SLOT0	I	**IOM®-2 Channel Slot Selection 0** assigns IOM®-2 channels in blocks of 4 SLOT1, 0: ’00’= IOM®-2 channels 0 to 3 ’01’= IOM®-2 channels 4 to 7 ’10’= IOM®-2 channels 8 to 11 ’11’= IOM®-2 channels 12 to 15
45	SLOT1	I (PD)	**IOM®-2 Channel Slot Selection 1** assigns IOM®-2 channels in blocks of 4

Table 2-1 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
16	MTO	I (PD)	**Monitor Channel Time-Out** if activated the Monitor channel is reset every 6ms ’1’= enables 6ms time-out ’0’= disables the 6ms time-out
32	PUP	I (PD)	**Push Pull Mode** in push pull mode ’0’ and ’1’ is actively driven during an occupied time slot, outside the active time slots DOUT is high impedance (tristate) ’1’= configures DOUT as push/pull output ’0’= configures DOUT as open drain output
49	CRCON	I (PD)	**CRC Check On/Off** defines the condition on which MON-2 messages will be passed on, the setting has effect on all ports ’1’= CRC Check On MON-2 messages are not issued while CRC violations on the U-interface were detected (MFILT= 0001 0xxx) ’0’= CRC Check Off MON-2 messages are issued every time a change in at least one of the overhead bits (M4,5,6) of the U-interface is detected, regardless of the CRC checksum status (MFILT= 0000 0xxx)
53	SYNC	I	**Synchronization Signal** input for a RITL/WLL sync signal which causes the alignment of the U-superframes first edge= RITL/WLL synchronization enabled ’1’= RITL/WLL synchronization disabled

Table 2-1 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
58	DARB	I	**D-Channel Arbitration Signal** enables/disables D-channel arbitration '1'= D-channel arbitration enabled '0'= D-channel arbitration disabled
59	AUTO	I	**EOC Auto Mode** selects auto or transparent mode for EOC channel processing, the setting has effect on all ports '1'= EOC auto mode (MFILT= xxxx x100) '0'= EOC transparent mode (MFILT= xxxx x001)
56	SSP	I	**Send Single Pulses (SSP) Test Mode** '1'= alternating +/-3 pulses are issued at all line ports in 1.5ms intervals '0'= deactivated, clamp to GND if not used *Note: This pin function corresponds to the SW selection by C/I= SSP besides the fact that the HW selection impacts all line ports while the SW selection impacts only the chosen line*
62	DT	I	**Data Through (DT) Test Mode** enables/disables DT test mode '1'= DT test mode enabled, the U-transceiver is forced on all line ports to enter the 'Transparent' state '0'= DT test mode disabled *Note: This pin function corresponds to the SW selection by C/I= DT besides the fact that the HW selection impacts all line ports while the SW selection impacts only the chosen line*

Interface to the Analog Front End

Table 2-1 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
4	CL15	I	**15.36MHz Master Clock Input**
11	PDM0	I	**Pulse Density Modulated Receive Data of Line Port 0** pulse density modulated bit stream from the PEF 24902 Quad AFE that is output from the second-order sigma-delta ADC
10	PDM1	I	**Pulse Density Modulated Receive Data of Line Port 1** pulse density modulated bit stream from the PEF 24902 Quad AFE that is output from the second-order sigma-delta ADC
8	PDM2	I	**Pulse Density Modulated Receive Data of Line Port 2** pulse density modulated bit stream from the PEF 24902 Quad AFE that is output from the second-order sigma-delta ADC
7	PDM3	I	**Pulse Density Modulated Receive Data of Line Port 3** pulse density modulated bit stream from the PEF 24902 Quad AFE that is output from the second-order sigma-delta ADC
5	SDR	I	**Serial Data Receive Line** interface signal from the PEF 24902 Quad AFE that transports level detect information for the wake-up recognition of all 4 lines by use of TDM
17	SDX	O	**Serial Data Transmit Line** interface to the PEF 24902 Quad AFE for the transmit and control data. Transmission is based on clock CL15 (15.36 Mbit/s). For each line port the following bits are exchanged: TD0, TD1: Transmit data RANGE: Range select LOOP: Analog loopback switch PDOW: Power down/power up Synchronization information

Table 2-1 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
Relay Driver/ Status Pins			
30, 35, 42, 47	D0A D0B D0C D0D	O	**Relay Driver Pins of Line Port 0** addressable via MON-8 command in IOM®-2 channel 0/4/8/12. The logic values of the bit positions A,B,C, D of the MON-8 command 'SETD' determine the output setting. Default value after pin-reset is low. C/I-code reset does not affect the current status.
31, 37, 43, 48	D1A D1B D1C D1D	O	**Relay Driver Pins of Line Port 1** addressable via MON-8 command in IOM®-2 channel 1/5/9/13. The logic values of the bit positions A,B,C, D of the MON-8 command 'SETD' determine the output setting. Default value after pin-reset is low. C/I-code reset does not affect the current status.
33, 39, 44, 50	D2A D2B D2C D2D	O	**Relay Driver Pins of Line Port 2** addressable via MON-8 command in IOM®-2 channel 2/6/10/14. The logic values of the bit positions A,B,C, D of the MON-8 command 'SETD' determine the output setting. Default value after pin-reset is low. C/I-code reset does not affect the current status.
34, 40, 46, 51	D3A D3B D3C D3D	O	**Relay Driver Pins of Line Port 3** addressable via MON-8 command in IOM®-2 channel 3/7/11/15. The logic values of the bit positions A,B,C, D of the MON-8 command 'SETD' determine the output setting. Default value after pin-reset is low. C/I-code reset does not affect the current status.
28, 27	ST00 ST01	I	**Status Pin of Line Port 0** change of status is passed to IOM®-2 channel 0/4/8/12 via MON-8 message 'AST' at bit positions $S_{0,}$ S_1. Connect to either VDD or VSS if not used.

Table 2-1 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
26, 24	ST10 ST11	I	**Status Pin of Line Port 1** change of status is passed to IOM®-2 channel 1/5/9/13 via MON-8 message 'AST' at bit positions $S_{0,}$ S_1. Connect to either VDD or VSS if not used.
23, 21	ST20 ST21	I	**Status Pin of Line Port 2** change of status is passed to IOM®-2 channel 2/6/10/14 via MON-8 message 'AST' at bit positions $S_{0,}$ S_1. Connect to either VDD or VSS if not used.
19, 18	ST30 ST31	I	**Status Pin of Line Port3** change of status is passed to IOM®-2 channel 3/7/11/15 via MON-8 message 'AST' at bit positions $S_{0,}$ S_1. Connect to either VDD or VSS if not used.

Test Pins

29	CLS0	O	**80kHz Transmit Baud Clock of Port 0** can be used for monitoring and test purposes
20	CLS1	O	**80kHz Transmit Baud Clock of Port 1** can be used for monitoring and test purposes
52	CLS2	O	**80kHz Transmit Baud Clock of Port 2** can be used for monitoring and test purposes
61	CLS3	O	**80kHz Transmit Baud Clock of Port 3** can be used for monitoring and test purposes

JTAG Boundary Scan

64	TCK	I	**Test Clock**
1	TMS	I (PU)	**Test Mode Select** internal pullup resistor (160kΩ)
2	TDI	I (PU)	**Test Data Input** internal pullup resistor (160kΩ)
3	TDO	O	**Test Data Output**

Table 2-1 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
63	$\overline{\text{TRST}}$	I (PU)	**JTAG Boundary Scan Disable** resets the TAP controller state machine (asynchronous reset), active low, internal pullup (160kΩ) *Note: Clamp $\overline{\text{TRST}}$ to GND if the Boundary Scan logic is not used* ’1’= reset inactive ’0’= reset active
Power Supply Pins			
6, 22, 38, 54	VDD		3.3V ±0.3V supply voltage
9, 25, 41, 57	VSS		0V ground

OD: Open Drain
PuP: Push Pull
PD: Internal Pull Down
PU: Internal Pull Up

2.3 Pinning Changes from DFE-Q V1.3 to DFE-Q V2.1

Table 2-2 Pinning Changes

Pin No.	V2.1	V1.3	Comment
16	MTO	TPD	activates the Monitor Time-Out procedure
32	PUP	N.C.	additional push-pull mode for pin DOUT eases interface adaptation
36	N.C.	DSYNC	obsolete, replaced by signal ’SYNC’ , see pin no. 53
45	SLOT1	N.C.	increased max data rate requires additional SLOT pin
53	SYNC	LT	input signal is used for RITL/WLL synchronization, dedicated LT mode pin is obsolete

Table 2-2 Pinning Changes

Pin No.	V2.1	V1.3	Comment
55	SLOT0	SLOT	renamed
56	SSP	TSP	dedicated pin for 'Send Single Pulses' test mode
58	DARB	PBX	renamed
62	DT	TP	dedicated pin for 'Data Through' test mode
63	$\overline{\text{TRST}}$	TP1	BScan power-on-reset is replaced by a dedicated reset line

3 Functional Description

3.1 Functional Overview

A functional overview of the DFE-Q V2.1 is given in **Figure 3-1**. Besides the signal processing and frame formatting blocks the PEF 24911 features an on-chip activation/ deactivation controller and programmable general purpose I/O pins for the control of test relays and power feeding circuits. An application specific DSP core services the four U-lines and cuts chip size to a minimum.

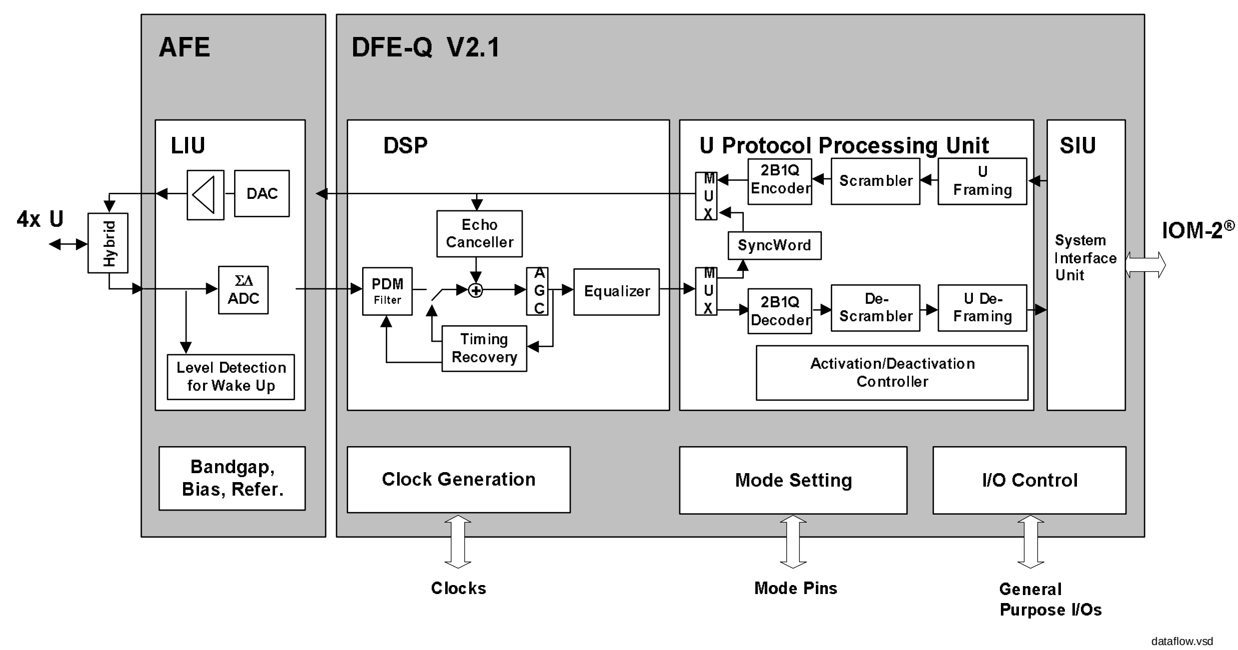


Figure 3-1 Data Flow Diagram (DFE-Q V2.1 + AFE)

3.2 Block Diagram

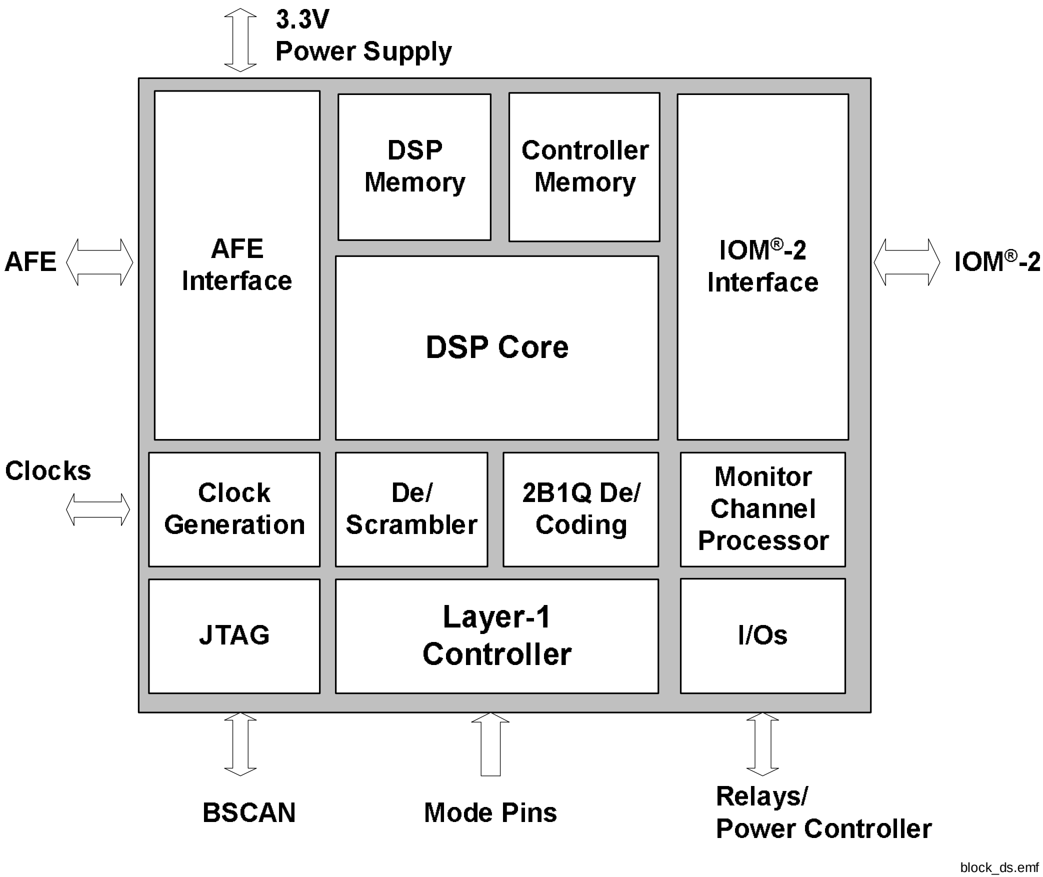


Figure 3-2 DFE-Q V2.1 Block Diagram

3.3 IOM®-2 Interface

The IOM®-2 interface is a four-wire serial interface providing a symmetrical full-duplex communication link to layer-1 and layer-2 backplane devices. It transports user data, control/programming and status information via dedicated time multiplexed channels.

The structure used follows the 2B + 1 D-channel structure of ISDN. The ISDN-user data rate of 144 kbit/s (B1 + B2 + D) on the U-interface is transmitted transparently in both directions (U <=> IOM®) over the interface.

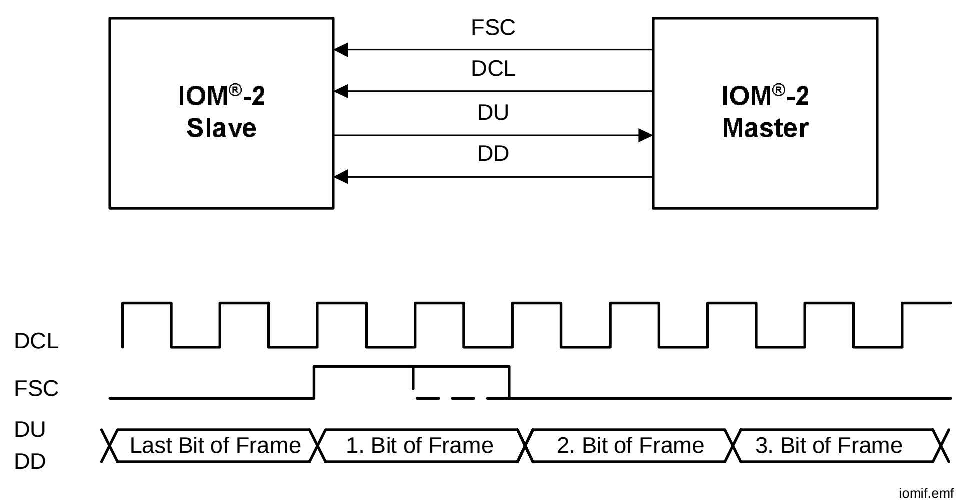


Figure 3-3 Clock Supply and Data Exchange between Master and Slave

The **Frame Sync Signal FSC** is a 8 kHz signal delimiting the frames. This signal is used to determine the start of a frame.

The data is clocked by a **Data Clock (DCL)** which operates at twice the data rate. The data clock is a square wave signal with a duty cycle ratio of typically 1:1. Incoming data is sampled on the falling edge of the DCL-clock.

Data is carried over **Data Upstream (DD)** and **Data Downstream (DU)** signals. The upstream and downstream directions are always defined with respect to the exchange: Downstream refers to information flowing from the exchange to the subscriber, upstream is defined vice versa.

The output line is operating either as open drain or push-pull output. Both modes are selected by signal “PUP”. In open drain mode an external pull-up resistor is required. The absence of a pull-up resistor is not automatically recognized (i.e. no push-pull detection).

Within one FSC-period, 128 to 512 bit are transmitted, corresponding to DCL-frequencies ranging from 2048 kHz up to 8192 kHz. The following table shows possible operating frequencies of the IOM®-2-interface.

Table 3-1 IOM®-2 Data Rates

DCL Frequency [kHz]	Data Rate [kBit/s]	IOM®-2 Channels
2048	1024	4
3072	1536	6
4096	2048	8
6144	3072	12
8192	4096	16

3.3.1 IOM®-2 Interface Frame Structure

The typical IOM®-2 line card application comprises a DCL-frequency of 4096 kHz with a nominal bit rate of 2048 kbit/s. Therefore eight channels are available, each consisting of the basic frame with a nominal data rate of 256 kbit/s. The downstream data (DD) is transferred on signal DIN, the upstream data (DU) on signal DOUT. The IOM®-2 channel assignment is programmable by pin strapping (SLOT1,0).

The basic IOM®-2 frame and clocking structure consists of:

channel	B1	B2	Monitor	D	Command / Indicate	MR	MX
bits	8	8	8	2	4	1	1

- Two 64-kbit/s channels B1 and B2
- The monitor channel for transferring maintenance information between layer-1 and layer-2 devices
- Two bits for the 16-kbit/s D-channel
- Four command / indication (C/I) bits for controlling of layer-1 functions (activation/ deactivation and additional control functions) by the layer-2 controller
- Two bits MR and MX for handling the monitor channel

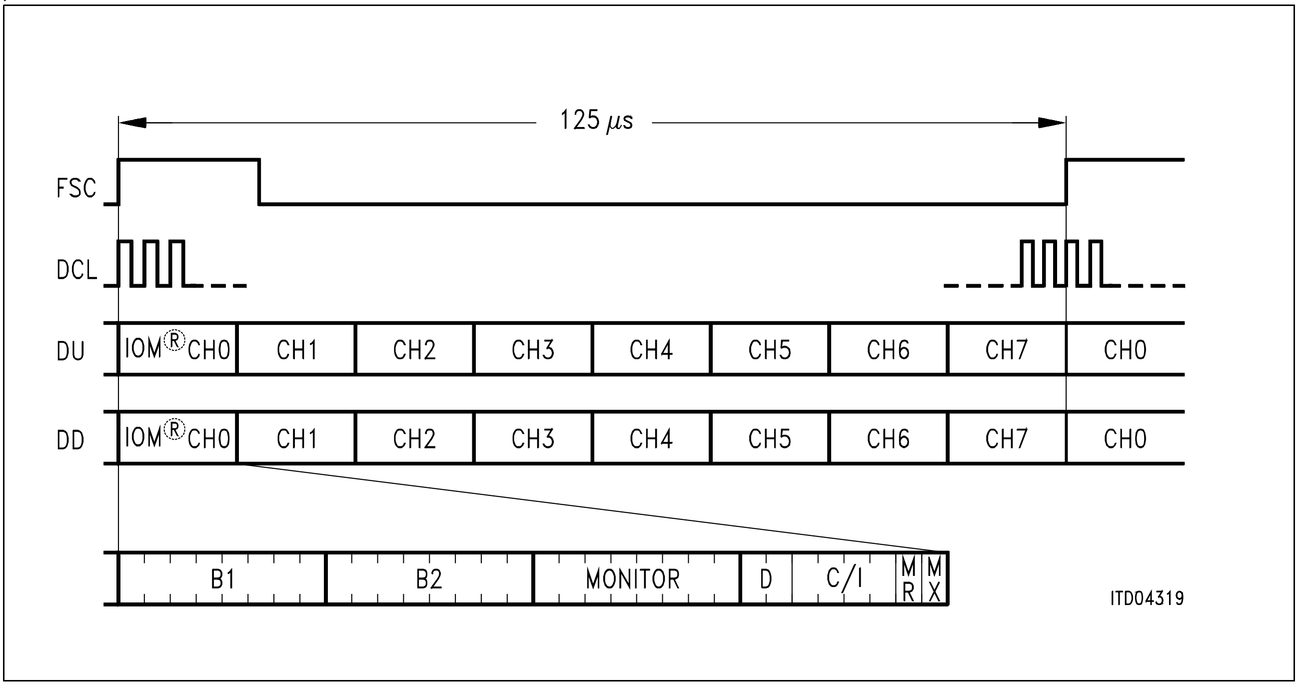


Figure 3-4 Multiplexed Frame Structure of the IOM®-2 Interface

3.3.2 Superframe Marker Function

The start of a new superframe is programmed by a FSC high-phase lasting for one single DCL-period. A FSC high-phase of two (or more) DCL-periods is transmitted for all other IOM®-2-frame starts.

It is optional to include superframe markers in every 96th “frame synchronization” signal. The remaining 95 FSC-clocks must be of at least two DCL-periods duration. If no superframe marker is to be used all FSC high-phases need to be of at least two DCL-periods duration.

With the SF function enabled the next outgoing basic frame on U defines the start of the U superframe by an inverted sync word (see **Figure 3-5**). This way the positions of the IOM®-2 and the U superframe are no more arbitrary but definite within a tolerance of 1.5ms.

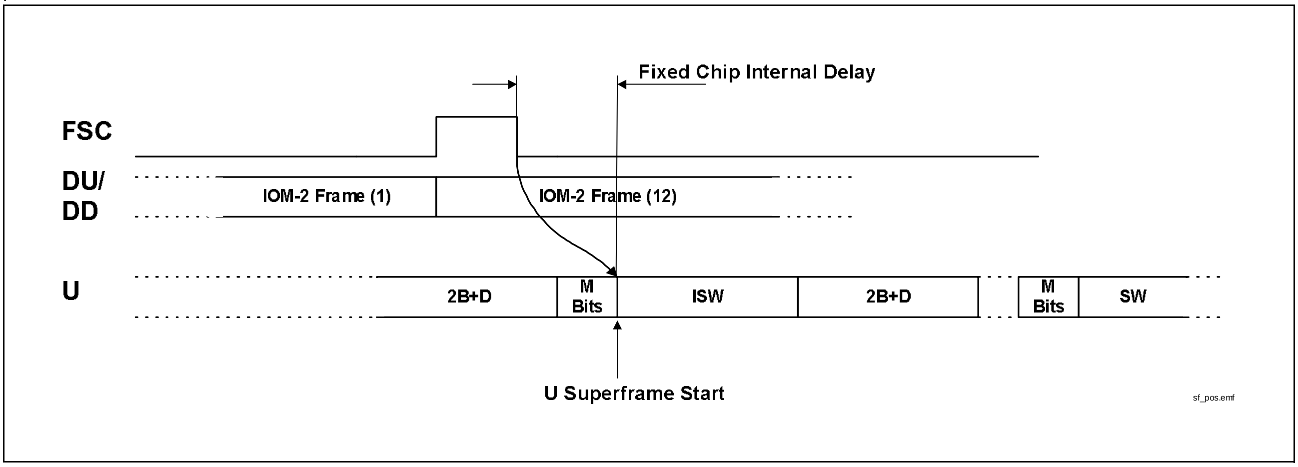


Figure 3-5 Superframe Marker

If no superframe marker is to be used, all FSC high-phases need to be of at least two DCL-periods duration.

The relationship between the IOM®-2-superframe on the LT-side, the U-frame and the IOM®-2-superframe on the NT-side is fixed after activation of the U-interface. I.e. data inserted on LT-side in the first B1-channel after the IOM®-2-slave superframe marker will always appear on NT-side with a fixed offset, e.g. in the 5th B1-channel after the master superframe marker. After a new activation this relationship (offset) may be different.

3.3.3 IOM®-2 Command/ Indicate Channel

The Command/Indication (C/I) channel carries real-time control and status information between the DFE-Q V2.1 and a layer-1 control device. A new C/I code must be detected in two consecutive IOM®-2 frames to be considered valid (double last look criterion). An indication is issued permanently by the DFE-Q V2.1 on DOUT until a new indication needs to be forwarded.

The C/I code is 4 bit wide and located at bit positions 27–30 in each time-slot. A listing and explanation of the U-transceiver C/I codes can be found on page 3-37.

3.3.4 IOM®-2 Monitor Channel

The Monitor channel represents a second method of initiating and reading U-transceiver specific information. Features of the monitor channel are supplementary to the command/indicate channel. Unlike the command/indicate channel with an emphasis on status control, the monitor channel provides access to internal bits (maintenance, overhead) and test functions (local loop-backs, block error counter etc).

Besides the known MON-0/2/8 commands a new MON class, MON-12 is introduced in the DFE-Q V2.1:

New MON-12 Class

By use of MON-12 commands the DFE-Q V2.1 provides the ability to address parts of the device internal register map and thus to address functions that have been added with version 2.1. MON-12 commands are always prioritized and processed first if other Monitor commands are outstanding. See **Chapter 3.3.5** for the details.

This means that Monitor commands are split into four categories. Each category derives its name from the first nibble (4 bits) of the two byte long message. These are:

- MON-12 (Internal Register Map)
- MON-0 (Transparent Channel)
- MON-2 (Overhead Bits)
- MON-8 (Local Functions)

The order of the list above corresponds to the priority attributed to each category. MON-12 commands are always processed first. MON-0 messages will be transmitted before MON-2 messages in case several messages are initiated simultaneously. The various MON-0, MON-2 and MON-8-commands are discussed in detail in chapter "Monitor Commands" on page 5-1.

Structure

The structure of the Monitor channel is 8 bit wide, located at bit position 17 – 24 in every time-slot. Monitor commands/messages sent to/from the U-transceiver are always 2 bytes long.

Transmission of multiple monitor bytes is specified by IOM®-2 (see next section “Handshake Procedure” for details). For handshake control in multiple byte transfers, bit 31, monitor read “MR”, and bit 32, monitor transmit “MX”, of every time-slot are used.

Verification

A double last-look criterion is implemented for the monitor channel. If the monitor message that was received consecutively after a change has been detected is not identical to the message that was received before the message will be aborted.

Handshake Procedure

IOM®-2 provides a sophisticated handshake procedure for the transfer of monitor messages. For handshake control two bits, MX and MR, are assigned to each IOM®-2 frame (on DIN and DOUT). The monitor transmit bit (MX) indicates when a new byte has been issued in the monitor channel (active low). The transmitter postpones transmitting the next information until the correct reception has been confirmed. A correct reception will be confirmed by setting the monitor read bit (MR) to low.

The monitor channel is full duplex and operates on a pseudo-asynchronous base, i.e. while data transfer on the bus takes place synchronized to frame synchronization, the flow of monitor data is controlled by the MR- and MX-bits. Monitor data will be transmitted repeatedly until its reception is acknowledged.

Figure 3-6 illustrates a monitor transfer at maximum speed. The transmission of a 2-byte monitor command followed by a 2-byte response requires a minimum of 15 IOM®-2 frames (reception 7 frames + transmission 8 frames = 1.875 ms). In case the controller is able to confirm the receipt of first response byte in the frame immediately following the MX-transition on DOUT from high to low (i.e. in frame No. 9), 1 byte may be saved (7 frames + 7 frames).

Transmission and reception of monitor messages can be performed simultaneously by the U-transceiver. In the procedure depicted in **Figure 3-6** it would be possible for the U-transceiver to transmit monitor data in frames 1–5 (excluding EOM-indication) and receive monitor data from frame 8 onwards.

M 1/2: Monitor message 1. and 2. byte
R 1/2: Monitor response 1. and 2. byte

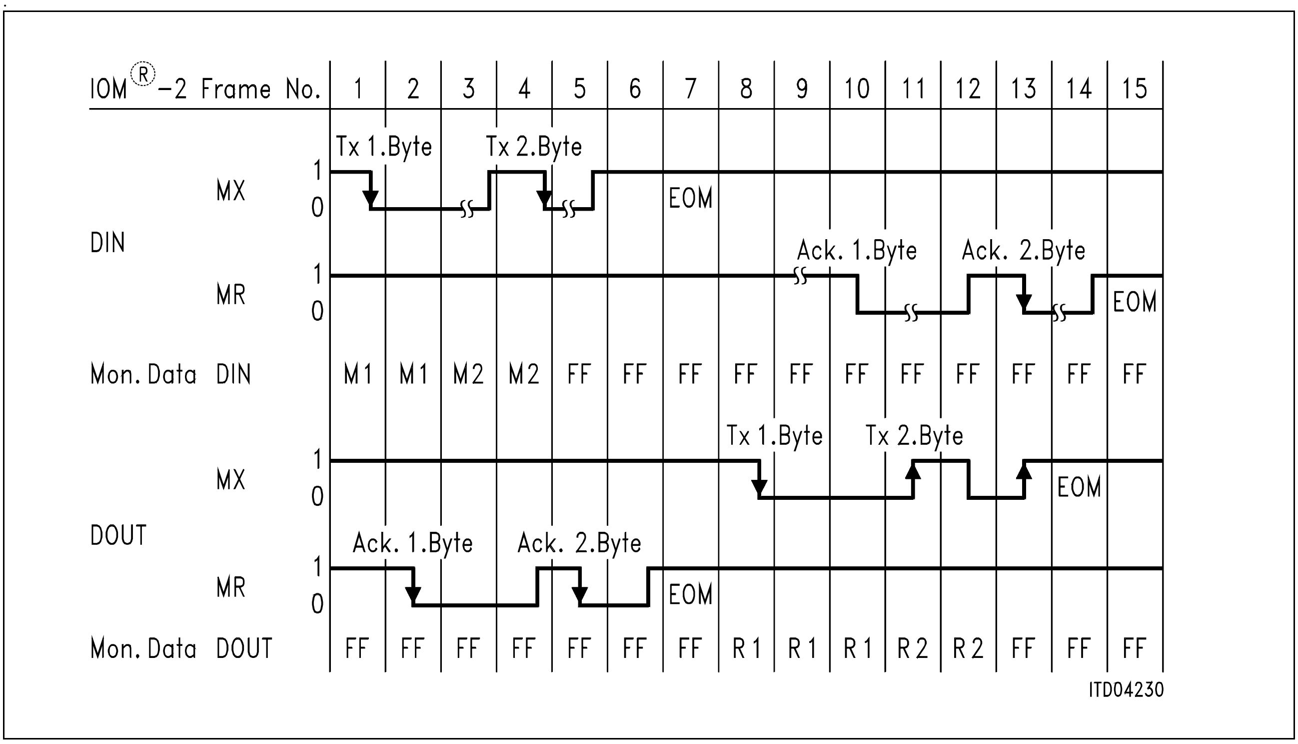


Figure 3-6 Handshake Protocol with a 2-Byte Monitor Message/Response

Idle State

After the bits MR and MX have been held inactive (i.e. high) for two or more successive IOM®-frames, the channel is considered idle in this direction.

Standard Transmission Procedure

1. The first byte of monitor data is placed by the external controller on the DIN line of the DFE-Q V2.1 and MX is activated (low; frame No. 1).
2. The DFE-Q V2.1 reads the data of the monitor channel and acknowledges by setting the MR-bit of DOUT active if the transmitted bytes are identical in two received frames (frame No. 2 because data are already read and compared while the MX-bit is not activated).
3. The second byte of monitor data is placed by the controller on DIN and the MX-bit is set inactive for one single IOM®-frame. This is performed at a time convenient to the controller.
4. The DFE-Q V2.1 reads the new data byte in the monitor channel after the rising edge of MX has been detected. In the frame immediately following the MX-transition active-to-inactive, the MR-bit of DOUT is set inactive. The MR-transition inactive-to-active exactly one IOM®-frame later is regarded as acknowledgment by the external controller (frame No. 4–5).
   The acknowledgment by the DFE-Q V2.1 will always be sent two IOM®-frames after the activation of a new data byte.
5. After both monitor data bytes have been transferred to the DFE-Q V2.1, the controller transmits “End Of Message” (EOM) by setting the MX-bit inactive for two or more IOM®-frames (frame No. 5–6).
6. In the frame following the transition of the MX-bit from active to inactive, the DFE-Q V2.1 sets the MR-bit inactive (as was the case in step 4). As it detects EOM, it keeps the MR-bit inactive (frame No. 6). The transmission of the monitor command by the controller is complete.
7. If the DFE-Q V2.1 is requested to return an answer it will commence with the response as soon as possible. In case the “monitor time out” function is enabled it may have to postpone the answer until after the internal reset (see section Monitor Procedure Time-out for details). **Figure 3-6** illustrates the case where the response can be sent immediately.
   The procedure for the response is similar to that described in points 1 – 6 except for the transmission direction. It is assumed that the controller does not latch monitor data. For this reason one additional frame will be required for acknowledgment.
   Transmission of the 2nd monitor byte will be started by the DFE-Q V2.1 in the frame immediately following the acknowledgment of the first byte. The U-transceiver does not delay the monitor transfer.

Transmission Abortion

If no EOM is detected after the first two monitor bytes, or received bytes are not identical in the first two received frames, transmission will be aborted through receiver by setting the MR-bit inactive for two or more IOM®-2-frames. The controller reacts with EOM. This situation is illustrated in **Figure 3-7**.

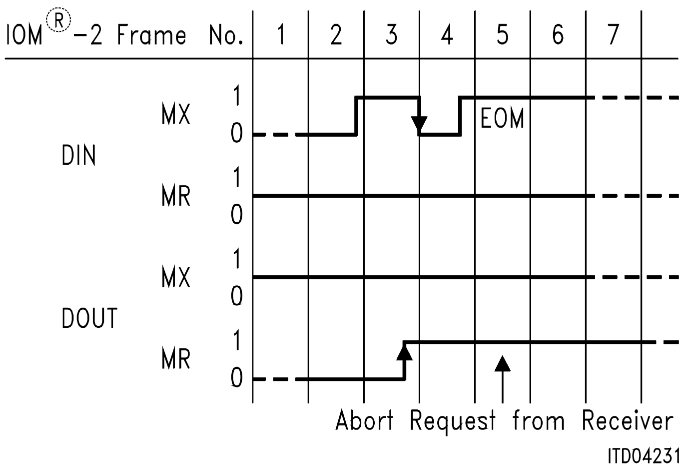


Figure 3-7 Abortion of Monitor Channel Transmission

MONITOR Procedure Time-Out (MTO)

The DFE-Q offers an internal reset (monitor procedure “Time-out”) for the monitor routine. This reset function transfers the monitor channel into the idle state (MR and MX set to high) thereby resolving possible lock-up situations. It therefore is to be used in all systems where no µP is capable of detecting and solving hang-up situations in the monitor procedure.

The reset procedure is started in 6 ms intervals. In order to avoid the loss of transmitted or received data the DFE-Q V2.1 commences a monitor transfer only when enough time is available before the next reset will be initiated. If this is not the case transmission is postponed until after the reset.

Once a message has been issued on IOM®, its transfer needs to be completed before the next reset. If this is not accomplished, the message can be lost without notice. For this reason the control software should be able to transfer monitor messages as quickly as possible.

Signal “MTO” set to ’1’ enables the MTO-function, signal “MTO” set to ’0’ disables it.

With the MTO-function enabled, the monitor routine is reset twice per U-superframe. The resets are performed at the start of the 1st and 49th IOM®-2-frame (see **Figure 3-8**). Due to the relationship of the reset timing to the U-frame the 6ms reset procedure is only executed in active states (Line Active, Pend. Transparent, Transparent, S/T Deactivated).

Every reset sets both handshake bits of DOUT to the idle state (MR and MX set to high) thereby preventing lock-up situations. The DFE-Q-transmitter and -receiver are reset synchronously.

With the MTO-function disabled no internal resets are performed. This eliminates the restrictions described in the following paragraphs, requires however an external controller to prevent lock-up situations in the monitor channel.

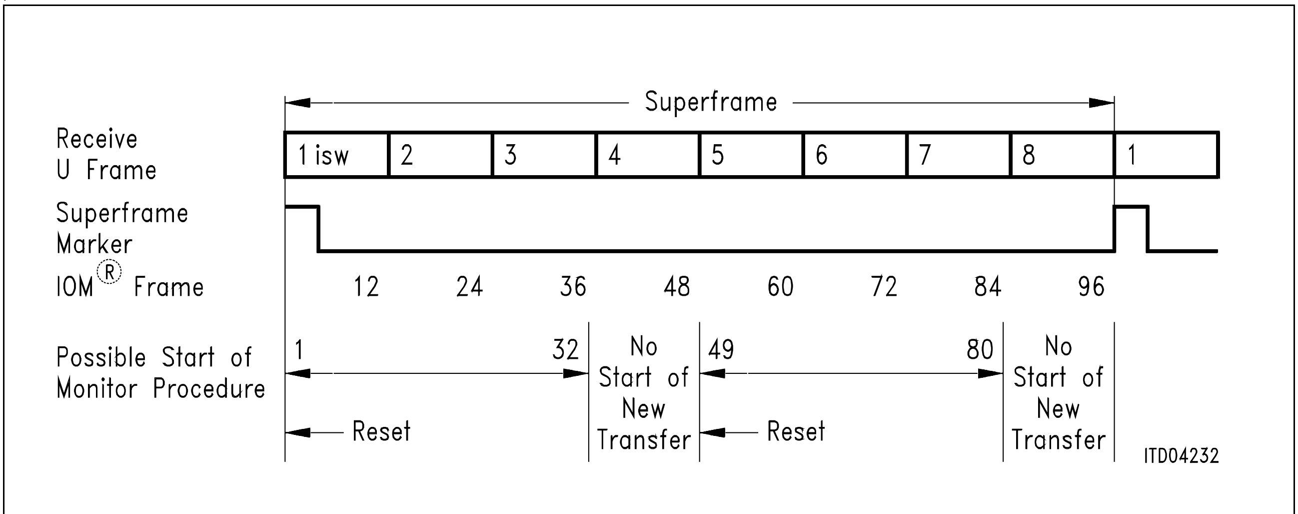


Figure 3-8 Monitor Access with MTO Enabled

DFE-Q V2.1 operates as Transmitter with MTO Enabled

The transmitter is reset in 6 ms intervals in the frames shown above. In case the transmission of a monitor message has not been completed before the transmitter is reset, the complete message will be lost. A message that has been lost due to the interruption of a monitor reset will not be retransmitted.

To prevent this loss of monitor messages, the DFE-Q V2.1 will only commence a monitor transmission if more than 16 IOM®-2 frames will be available for transmission before the next reset occurs. Transmission thus does not start during frame numbers 33 … 48 and 81 … 96. To ensure correct transmission the receiver must not delay the receive procedure for more than the following value:

2-byte transmission: max. speed = 8 frames => max. controller (receive) delay = 8 frames

DFE-Q V2.1 operates as Receiver with MTO Enabled

The receiver is reset in 6 ms intervals in the frames shown above. In case the reception of a monitor message has not been completed before the receiver is reset, the complete message can be lost because the generation of an abort request can not be guaranteed.

To prevent this loss of monitor messages the DFE-Q will only commence a monitor reception (i.e. acknowledge the 1st received byte) if more than 16 IOM®-2 frames will be available for reception before the next reset occurs. Reception thus does not start during frame numbers 33 … 48 and 81 … 96. To ensure correct reception, the transmitter must not delay the receive procedure for more than the following value:

2-byte reception: max. speed = 7 frames => max. controller (transmit) delay = 9 frames

3.3.5 MON-12 Protocol

MON-12 commands feature direct access to the device internal register map via the Monitor channel. This means that although the DFE-Q V2.1 features no microcontroller interface internal register functions can be directly addressed by use of MON-12 commands.

A MON-12 read request command must be first acknowledged by the DFE-Q V2.1 before a subsequent read request can be triggered. In case of a failure condition the DFE-Q V2.1 repeats the last outstanding MON-12 answer. MON-12 commands are prioritized over the other MON classes.

If U-interface functions are addressed then the value of register LP_SEL determines the register bank of the channel that is referred to. As a result the desired line port number must be programmed first in register LP_SEL before any U-interface register can be accessed. For this reason MON-12 commands may not be issued simultaneously on different IOM®-2 channels, but must be issued consecutively if they address U-interface functions.

For registers that are addressable by MON-12 commands please refer to the register map in **Chapter 6.4** on page 6-6.

MON-12 commands are of the following format:

- A MON-12 **write command** comprises 3 bytes, the first byte contains the MON-12 header, the second byte the register address, the third byte the register value.

1. Byte		2. Byte		3. Byte	
1100	w=1 0 0 0	A A A A	A A A A	D D D D	D D D D
MON-12		Register Address		Register Value	

- A MON-12 **read request command** comprises 2 bytes, the first byte contains the MON-12 header, the second byte the register address of the data that is requested.

1. Byte		2. Byte	
1100	r=0 0 0 0	A A A A	A A A A
MON-12		Register Address	

- After a read request the DFE-Q V2.1 reacts with a 3-byte message. A MON-12 **read answer** comprises 3 bytes, the first byte contains the MON-12 header, the second byte the register address, the third byte the register value.

1. Byte		2. Byte		3. Byte	
1100	r=0 0 0 0	A A A A	A A A A	D D D D	D D D D
MON-12		Register Address		Register Value	

3.4 Interface to the Analog Front End

The interface to the PEF 24902 AFE V2.1 is a 6-wire interface (see **Figure 3-9**). On SDX and SDR transmit and receive data is exchanged as well as control information for the start-up procedure by means of time division multiplexing.

On **SDX** transmit data, power-up/down information, range function and analog loopback requests are transferred.

On **SDR** level status information is received for all line ports.

On **PDM0..PDM3** the ADC output data from the AFE is transferred to the DFE-Q V2.1. The timing of all signals is based on the 15.36MHz master clock which is provided by the AFE.

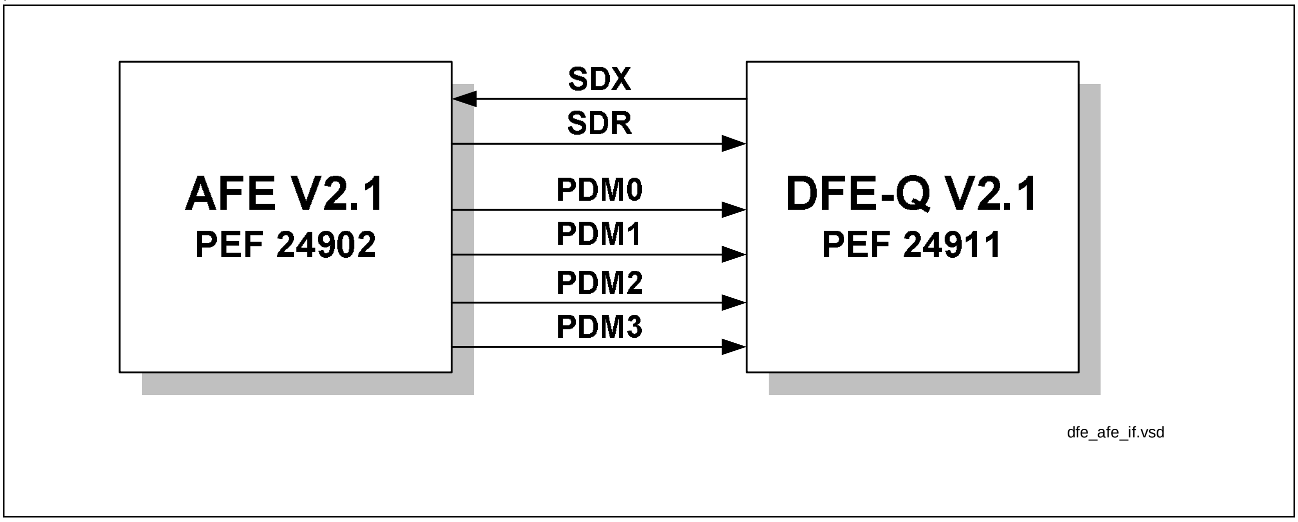


Figure 3-9 Interface to the Analog Front End

The 192 available bits (related to the 15.36 MHz clock) on SDR/SDX during a 80 kHz period are divided into 9 time-slots. 8 time-slots are 21 bits long and are reserved for data transmission, 1 time-slot is 24 bits long and used for synchronization purposes. The DFE-Q V2.1 uses four of them, time-slots no. 1, 3, 5 and 7. **Table 3-2** shows the assignment of the IOM®-2 channels to the time-slots on SDX/SDR and the assignment of the time-slots to the line ports.

Table 3-2 Assignments of IOM® Channels to Time-Slots No. on SDX/SDR and Line Ports No.

IOM®-2 Channel No.	Time-Slot No.	Line Port No.
0/4/8/12	1	0
1/5/9/13	3	1
2/6/10/14	5	2
3/7/11/15	7	3

The status on SDR is synchronized to SDX. Each time-slot on SDR carries the corresponding LD bit during the last 20 bits of the slot.

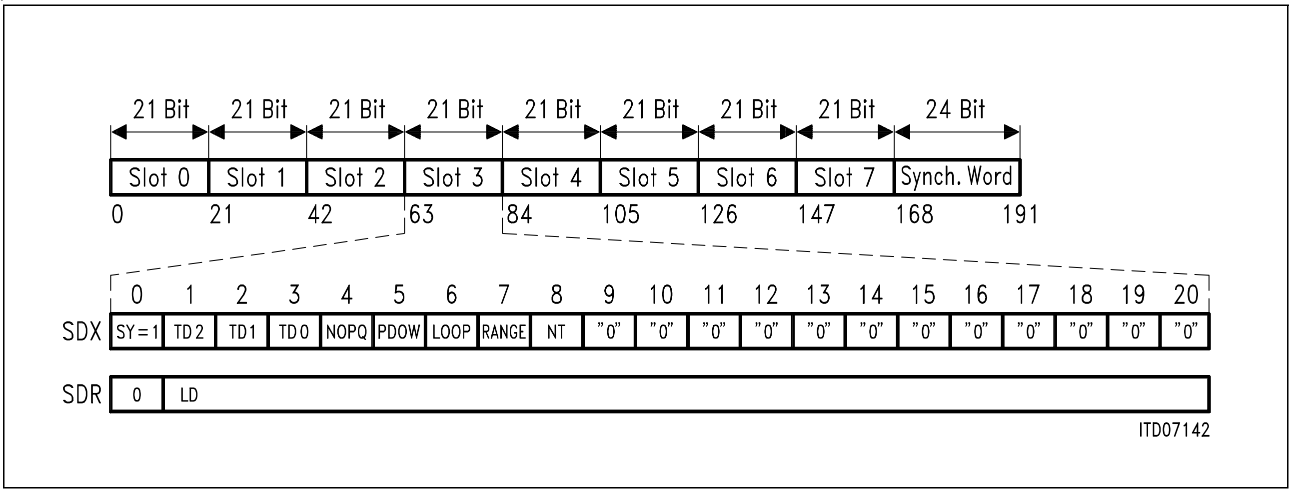


Figure 3-10 Frame Structure on SDX/SDR

The data on **SDX** is interpreted as follows:

NOP: The no-operation-bit is set to '0' if none of the control bits (PDOW, RANGE and LOOP) shall be changed. The values of the control bits of the assigned line port is latched. The states of the control bits on SDX are ignored, they should be set to '0' to reduce any digital cross-talk to the analog signals.

The NOPQ bit is set to '1' if at least one of the control bits shall be changed. In this case all control bits are transmitted with their current values.

PDOW: If the PDOW bit is set to '1', the assigned line port is switched to power-down. Otherwise it is switched to power-up.

RANGE: RANGE activates the range function which attenuates the received U-signal
'1'= RANGE function is activated (short line)
'0'= RANGE function is deactivated (long line)

LOOP: LOOP = ’1’ activates the loop function, i.e. the loop is closed. Otherwise the line port is in normal operation.

SY: First bit of the time-slots with transmission data. For synchronization and bit allocation on SDX, SY is set to ’1’ on SDX and ’0’ on SDR.

"0": Reserved bit. Reserved bits are currently not defined and shall be set to ’0’. Some of these bits may be used for test purposes or can be assigned to a function in later versions.

The 2B1Q data is coded with the bits TD2, TD1, TD0:

Table 3-3 2B1Q Coding Table

2B1Q Data	TD2	TD1	TD0
0	1	don´t care	don´t care
– 3	0	0	0
– 1	0	0	1
+ 3	0	1	0
+ 1	0	1	1

The data on **SDR** is interpreted as follows:

LD: The level detect information is communicated to the DFE-Q V2.1 on SDR. If the signal amplitude reaches the wake-up level, the LD bit toggles with the signal frequency. If the input signal at the U-interface is below the wake-up level, the LD bit is tied to either low or high.

SY: First bit of the time-slots with transmission data. For synchronization and bit allocation on SDX, SY is set to ’1’ on SDX and ’0’ on SDR.

3.5 General Purpose I/Os

The DFE-Q V2.1 features 6 general purpose I/O pins per line port. This way transparent control of test relays and power feeding circuits is possible via the IOM®-2 Monitor channel. Four of the six pins are outputs, two are inputs.

Setting Relay Driver Pins

Four relay driver output pins Dij (where i = 0, 1, 2, 3 denotes the line port no. and j = A, B, C, D specifies the pin) are available per line port. The logic state of the four relay driver outputs which are assigned to the same line port can be set by a single MON-8 command, called ’SETD’. The value is latched as long as no other SETD command with different relay driver settings is received.

The state of the relay driver pins is not affected by any software reset (C/I= RES). The state of all relay driver pins after hardware reset is „low“.

Reading Status Pins

Each line port owns two status pins ST_{ij} (where i = 0,1, 2, 3 denotes the line port no. and j = 0, 1 specifies the pin) whose logical value is reported in the associated Monitor channel. Any signal change at one of the status pins ST1..4 causes automatically the issue of a two-byte MON-8 message ’AST’ whose two least significant bits reflect the status of pin STij.

However, this automatic mechanism is only enabled again, if the previous status pin message has been transferred and acknowledged correctly according to the Monitor channel handshake protocol. It takes the DFE-Q V2.1 at least 8x IOM®-2 frames (1ms) to transmit the 2-byte MON-8 message. Thus, repeated changes within periods shorter than 8x IOM®-2 frames will overwrite the status pin register information. For this reason only the value of the last recent status change will be reported. Note that the MON-8 transfer time depends also on the reaction time (acknowledge by MR-bit) of the DFE-Q counterpart.

Besides this automatic report the DFE-Q V2.1 will issue the status pin Monitor message ’AST’ upon the MON-8 request ’RST’ .

The ST_{ij} pins have to be tied to either VDD or GND, if they are not used.

3.6 Clock Generation

The U-transceiver has to synchronize onto an externally provided PTT-master clock. A phase locked loop (PLL) is integrated in the AFE (PEF 24902) to generate the 15.36MHz system clock. A synchronized system clock guarantees that U-interface transmission will be synchronous to the PTT-master clock.

The AFE is able to synchronize onto a 8 kHz or a 2048 kHz system clock. **Infineon recommends however to feed the FSC clock input of the DFE-Q V2.1 and the PLL reference clock input (pin CLOCK) of the AFE from the same clock source.** Please refer to the PEF 24902 Data Sheet for further details on the PLL.

For the connection of the AFE clock output line with the DFE-Q V2.1 clock input line (CL15) please refer to page 1-5.

3.7 U-Transceiver Functions

The U-interface establishes the direct link between the exchange and the terminal side. It consists of two copper wires. The Quad IEC AFE uses four differential outputs (AOUT, BOUT) and four differential inputs (AIN, BIN) for transmission and reception. These differential signals are coupled via four hybrids and four transformers to the four two-wire U-interfaces. The nominal peak values of ± 3 correspond to a 3.2 Vpp chip output and 2.5 Vpp on the U-interface.

Direct access to the U-interface is not possible. 2B + D user data can be inserted and extracted via the IOM®-2 interface. Control of maintenance bits is partly provided via IOM®-2 monitor commands. The remaining maintenance bits are fully controlled by the DFE-Q V2.1 itself and allow no external influence (e.g. CRC-checksum).

3.8 2B1Q Frame Structure

Transmission over the U_{2B1Q}-interface is performed at a symbol rate of 80 kBaud. The code used reduces two binary informations to one quaternary symbol (2B1Q) resulting in a total bit rate of 160 kbit/s. 144 kbit/s are user data (B1 + B2 + D), 16 kbit/s are used for maintenance and synchronization information.

Data is grouped together into U-superframes of 12 ms each. The beginning of a new superframe is marked by an inverted synchronization word (ISW). Each superframe consists of eight basic frames (1.5ms) which begin with a standard synchronization word (SW) and contain 222 bits of information. The structure of one U-superframe is illustrated in **Figure 3-11** and **Figure 3-12**.

ISW	**1. Basic Frame**	**SW**	**2. Basic Frame**	**. . .**	**SW**	**8. Basic Frame**
<---			12 ms			--->

Figure 3-11 U-Superframe Structure

(I) SW **(Inverted) Synch Word** **18 Bit (9 Quat)**	**12 × 2B + D** **User Data** **216 Bits (108 Quat)**	**M1 – M6** **Maintenance Data** **6 Bits (3 Quat)**
<---	1,5 ms	--->

Figure 3-12 U-Basic Frame Structure

Out of the 222 information bits 216 contain 2B + D data from 12 IOM®-frames, the remaining 6 bits are used to transmit maintenance information. Thus 48 maintenance bits are available per U-superframe. They are used to transmit two EOC-messages (24 bit), 12 Maintenance (overhead) bits and one checksum (12 bit).

Table 3-4 2B1Q U-Frame Structure

		Framing	2B + D	Overhead Bits (M1 – M6)					
	Quat Positions	1 – 9	10 – 117	118 s	118 m	119 s	119 m	120 s	120 m
	Bit Positions	1 – 18	19 – 234	235	236	237	238	239	240
Super Frame #	Basic Frame #	Sync Word	2B + D	M1	M2	M3	M4	M5	M6
1	1	ISW	2B + D	EOCa1	EOCa2	EOCa3	ACT/ ACT	1	1
	2	SW	2B + D	EOCd m	EOCi1	EOCi2	DEA / PS1	1	FEBE
	3	SW	2B + D	EOCi3	EOCi4	EOCi5	1/ PS2	CRC1	CRC2
	4	SW	2B + D	EOCi6	EOCi7	EOCi8	1/ NTM	CRC3	CRC4
	5	SW	2B + D	EOCa1	EOCa2	EOCa3	1/ CSO	CRC5	CRC6
	6	SW	2B + D	EOCd m	EOCi1	EOCi2	1	CRC7	CRC8
	7	SW	2B + D	EOCi3	EOCi4	EOCi5	UOA / SAI	CRC9	CRC 10
	8	SW	2B + D	EOCi6	EOCi7	EOCi8	AIB / NIB	CRC11	CRC12
2,3…									
						LT- to NT dir. >	/	< NT- to LT dir.	

– ISW Inverted Synchronization Word (quad): – 3 – 3 + 3 + 3 + 3 – 3 + 3 – 3 – 3
– SW Synchronization Word (quad): + 3 + 3 – 3 – 3 – 3 + 3 – 3 + 3 + 3
– CRC Cyclic Redundancy Check
– EOC Embedded Operation Channel
  a = address bit
  d/m = data / message bit
  i = information (data / message)
– ACT Activation bit — ACT = (1) –> Layer 2 ready for communication
– DEA Deactivation bit — DEA = (0) –> LT informs NT that it will turn off
– CSO Colt Start Only — CSO = (1) –> NT-activation with cold start only
– UOA U-Only Activation — UOA = (0) –> U-only activated
– SAI S-Activity Indicator — SAI = (0) –> S-interface is deactivated
– FEBE Far-end Block Error — FEBE = (0) –> Far-end block error occurred
– PS1 Power Status Primary Source — PS1 = (1) –> Primary power supply ok ?
– PS2 Power Status Secondary Source — PS2 = (1) –> Secondary power supply ok ?
– NTM NT-Test Mode — NTM = (0) –> NT busy in test mode
– AIB Alarm Indication Bit — AIB = (0) –> Interruption (according to ANSI)
– NIB Network Indication Bit — NIB = (1) –> no function (reserved)

3.9 Maintenance Channel

The last three symbols (6 bits) form the 4kbit/s M(Maintenance)-channel used for exchange of operations and maintenance data between the network and the NT. Approved M-bit data is first processed and then reported to the system by Monitor channel messages (MON-0, MON-2).

MON-0/ MON-2 - M Bit mapping

The M1-3 bits over four basic frames constitute one complete EOC word. EOC words are exchanged across the IOM®-2 interface via MON-0 messages. The overhead bits (M4,M5,M6) of one U-superframe are collected and transported in a MON-2 message. **Figure 3-13** shows in detail how the maintenance bits of one received U-superframe are mapped to MON-0 and MON-2 messages.

M1-6 Filtering Options

To reduce processor load the DFE-Q V2.1 provides several programmable filters for the issue of MON-0 and MON-2 messages. In the following paragraphs the various verification algorithms and the provided control mechanism for the overhead bits (M4,M5,M6) are presented.

The verification method of received M-channel data can be programmed in the MFILT register using the MON-12 protocol. The following options are provided:

U-Frame Structure

Super Frame	Basic Frame	M1	M2	M3	M4	M5	M6
1	1	EOC 1			ACT	1	1
	2				DEA/PS1	1	FEBE
	3				SCO/PS2	CRC1	CRC2
	4				1/NTM	CRC3	CRC4
	5	EOC 2			1/CSO	CRC5	CRC6
	6				1	CRC7	CRC8
	7				UOA/SAI	CRC9	CRC10
	8				AIB/NIB	CRC11	CRC12
2,3 ...							

LT to NT > / < NT to LT

MON-0/2 Correspondence

Super Frame	Basic Frame	M1	M2	M3	M4	M5	M6
1	1	A1	A2	A3	D11	D10	D9
	2	D/M	I1	I2	D8	D7	D6
	3	I3	I4	I5	D5	CRC1	CRC2
	4	I6	I7	I8	D4	CRC3	CRC4
	5	A1	A2	A3	D3	CRC5	CRC6
	6	D/M	I1	I2	D2	CRC7	CRC8
	7	I3	I4	I5	D1	CRC9	CRC10
	8	I6	I7	I8	D0	CRC11	CRC12
2,3 ...							

MON-0 **MON-2**

MON-0 Format

1. Byte								2. Byte							
MON-0				Address			D/M	EOC Code							
0	0	0	0	A1	A2	A3	D/M	I1	I2	I3	I4	I5	I6	I7	I8

MON-2 Format

1. Byte								2. Byte							
MON-2				Single Bits (M4, M5, M6 except CRC)											
0	0	1	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

mon02corrsp.emf

Figure 3-13 MON-0/2 - M-Bit Correspondence

EOC (M1-M3) Filtering

The first three M-bits (M1-M3) in each basic U-frame constitute an EOC command/ message. For the different EOC commands and their meaning see the next paragraph. Via register MFILT the following operating modes can be set:

- **Automode** (MFILT.EOC= '100' = **default setting**)
  In automode received EOC messages are checked by 'triple-last-look' (TLL) before they are signalled to the system by a MON-0 message. The Return Message Reception Function is activated (see "EOC Auto Mode" on page 3-31).
- **Transparent** mode (MFILT.EOC= '001')
  In transparent mode received EOC messages are forwarded via MON-0 to the system interface. This means that every 6ms a MON-0 message is issued.
- **Transparent** mode **with On Change** function active (MFILT.EOC= '010')
  Only if a change in the EOC message has been detected the received EOC message is reported via a MON-0 message.
- **Transparent** mode **with TLL** active (MFILT.EOC= '011')
  A change is only reported via MON-0 if the new EOC command has been detected in at least three consecutive EOC messages.

For more details on EOC commands and messages and its processing please refer to chapter 3.10 on page 29.

Overhead Bit (M4, M5, M6) Filtering

M4 bits are used to communicate status and maintenance functions between the transceivers. The meaning of a bit position depends on the direction of transmission (upstream/downstream) and the operation mode (NT/LT). See **Table 3-4** for the different meaning of the M4 bits.

To reflect a change of the system status a new value for M4 bits shall be repeated in at least three consecutively transmitted superframes. All overhead bits are set to binary '1' when leaving a power-down state. No further processing is performed by the U-transceiver.

Four different validation modes can be selected and take effect on a **per bit base**. Only if the received M4 bit change has been approved by the programmed filter algorithm the corresponding MON-2 message is issued. The following filter algorithms are provided:

- **On Change** (MFILT.M4= 'X00')
- **Triple-Last-Look (TLL)** coverage (MFILT.M4= 'X01')
- **CRC** coverage (MFILT.M4= 'X10' = **default setting**)
- **CRC and TLL** coverage (MFILT.M4= 'X11')

Some M4 bits, ACT, DEA and UOA, have two destinations, the state machine and the system interface. Regarding these bits Triple-Last-Look (TLL) is applied by default before the changed status is input to the state machine. Via bit no. 5 of the MFILT register the user can decide whether the M4 bits which are input to the state machine shall be approved

- by **TLL** (MFILT.M4= ’0XX’) (**default setting**, since TLL is a Bellcore requirement) or
- by the same verification mode (MFILT.M4= ’1XX’) as selected for the issue of a MON-2 message.

The spare bits **M51, M52 and M61** are set by default to ’1’ unless they are not explicitly set by MON-2 commands otherwise. By default M56 bit changes are reported via MON-2 messages only if no CRC violation has been detected (same mode as for M4 bits). However the user has the choice to program one of the following two options:

- Same validation algorithm is applied to M5 and M6 bits as programmed for M4 bits (MFILT.M56= ’X0’ = **default setting**)
  Note that unlike the M4 bits the M56 bits are not included in the CRC generation!
- **On Change** (MFILT.M56= ’X1’)

Note: The issue of the corresponding Monitor messages is delayed for 12ms (= U-superframe) if received M-bits are CRC covered. This way the M-bit data is checked with the actual CRC sum which is received one U-superframe later.

Filter Setting via Pin AUTO and Pin CRCON

Besides the MFILT register the verification method for the maintenance bits can be as well programmed by pin AUTO and pin CRCON. The setting of **pin AUTO** determines the operational mode of the Embedded Operations Channel:

- Pin AUTO set to ’1’ selects automode for all line ports and corresponds to the following register setting of MFILT = xxxx x100.
- Pin AUTO set to ’0’ selects transparent mode for all line ports and corresponds to the following register setting of MFILT = xxxx x001.

Via **pin CRCON** the CRC mode for the overhead bits can be activated or deactivated:

- Pin CRCON set to ’1’ enables the CRC mode for all line ports and corresponds to the following register setting of MFILT = 0001 0xxx.
- Pin CRCON set to ’0’ disables the CRC mode for all line ports and corresponds to the following register setting of MFILT = 0000 0xxx.

Note that the pin setting is only evaluated once after reset. This fact allows to reprogram the verification modes later on by a MON-12 command. The MFILT register setting is evaluated each time the U-transceiver enters the DEACTIVATED state.

Figure 3-14 summarizes the various filtering options that are provided for the several bits of the Maintenance channel .

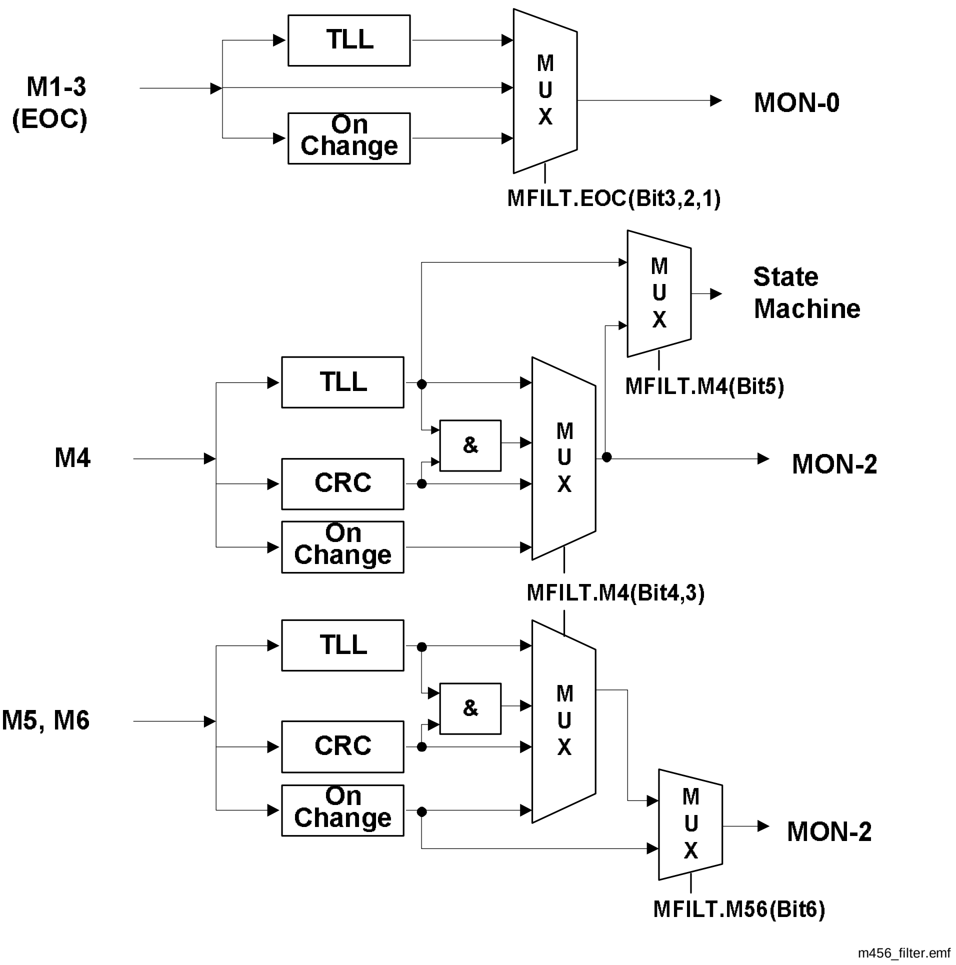


Figure 3-14 Maintenance Channel Filtering Options

3.9.1 M4 Bit Reporting to State Machine

Figure 3-15 illustrates the point of time when a detected M4 bit change is reported to the system interface and when it is reported to the state machine:

- **towards the system interface** MON-2 messages might be sent after one complete U-superframe was received,
- whereas **towards the state machine** M4-bit changes (ACT, SAI) are instantly passed on as soon as they were approved by TLL (default setting in register register MFILT, see "MFILT - M-Bit Filter Options" on page 6-8).
  In context to **Figure 3-15** this means that a verified ACT bit change is already reported at the end of basic frame #1 instead at the end of basic frame #8.

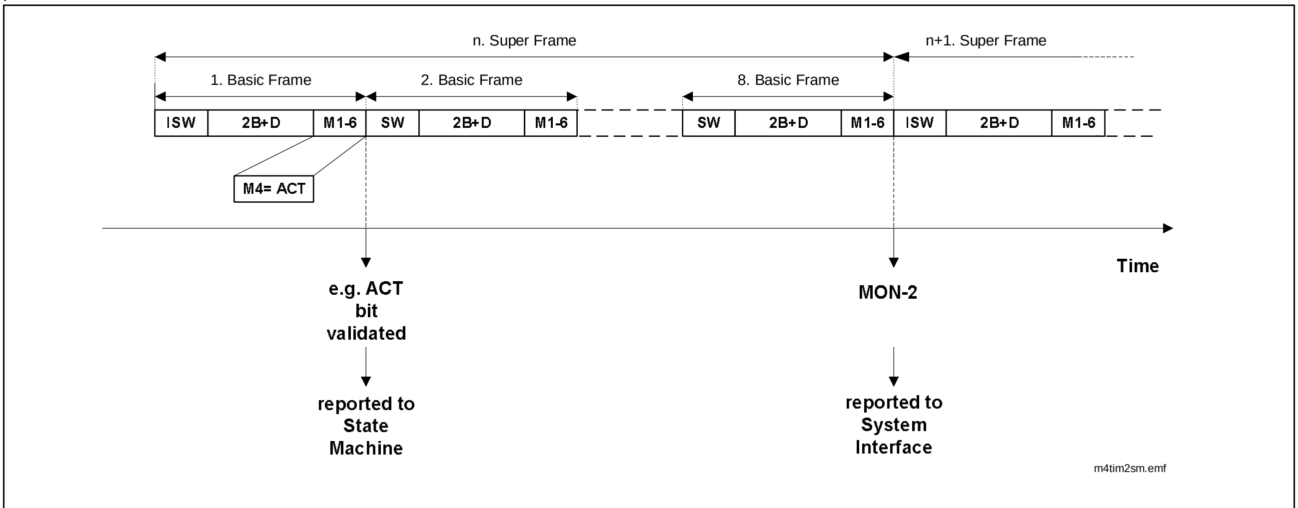


Figure 3-15 M4 Bit Report Timing

However, if the same filter is selected towards the state machine as programmed towards the system interface (by Bit5= '1' in register MFILT) the user has to be aware that if CRC mode is active the state machine is informed at the end of the next U-superframe.

3.9.2 M4, M5, M6 Bit Control Mechanisms

Figure 3-16 to **Figure 3-17** show the control mechanisms that are provided for M4, M5 and M6 bit data:

Via the **M4WMASK** register the user can selectively program which M4 bits are externally controlled and which are set by the internal state machine. If one M4WMASK bit is set to ’0’ then the M4 bit value in the U-transmit frame is determined by the bit value at the corresponding bit position of the MON-2 command.
Note that the MON-8 command PACE/PACA corresponds to bit 6 in the M4WMASK register. By bit 6 it can be selected whether SAI is set by the state machine or by MON-2 commands.
Via the **M4RMASK** register the user can selectively program which M4 bit changes shall cause a MON-2 message. With respect to the SAI bit the corresponding bit (no. 6) in the M4RMASK bit decides in addition whether the value of the received SAI bit is reported to the state machine or SAI= ’1’ is signalled.

Access to M4WASK and M4RMASK is provided by the MON-12 protocol. By MON-2 commands the M4 bits can be set that are sent with the next available U-superframe. By MON-2 messages the status of the last validated M4 bit data is reported.

Also the default values of the spare bits, M51, M52 and M61 can be overwritten at any time by a MON-2 command. A MON-2 messages reports the last received and verified M5, M6 bit data.

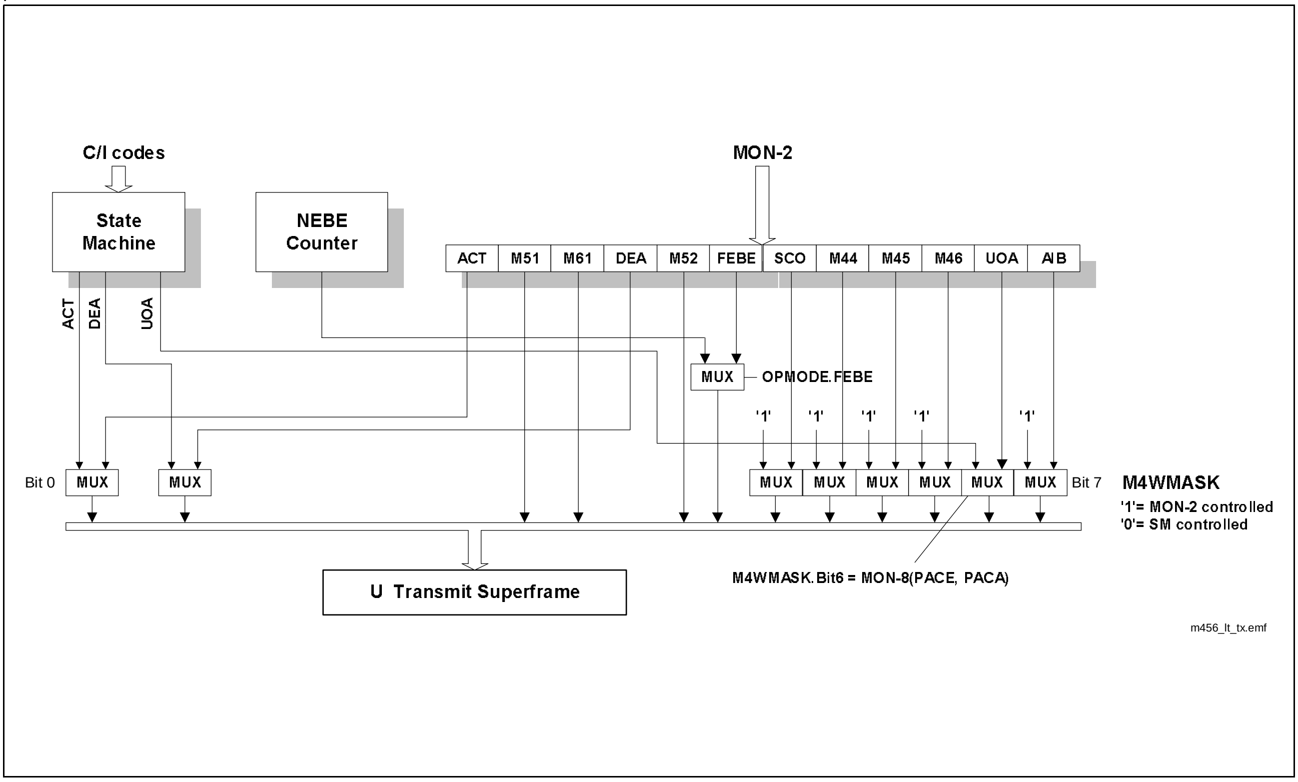


Figure 3-16 M4, M5, M6 Bit Control in Transmit Direction

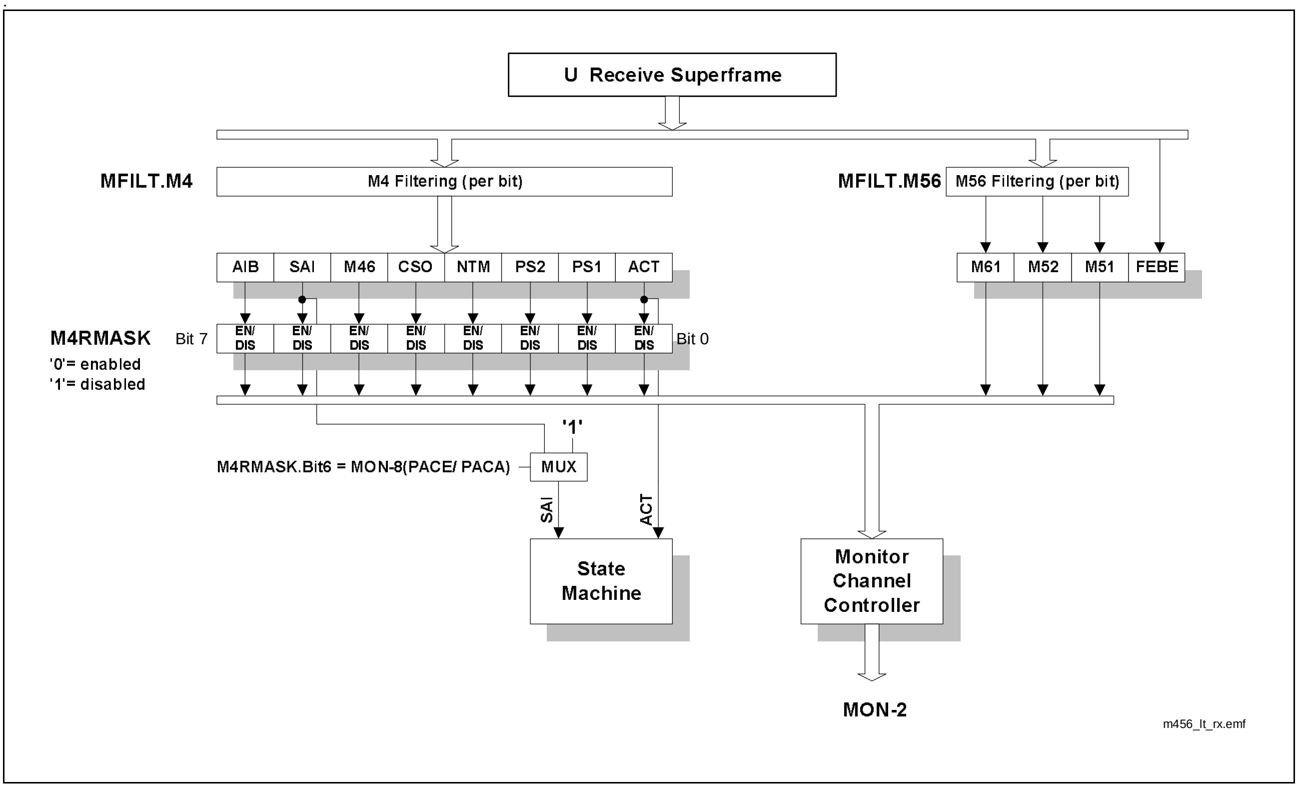


Figure 3-17 M4, M5, M6 Bit Control in Receive Direction

3.9.3 Start of Maintenance Bit Evaluation

MON-0/2 messages will be issued only if the receiver is synchronized. This is done to avoid meaningless MON-0/2 messages if data transmission is not synchronized.

In other words, MON-0/2 messages will be issued **only** in the following states:

States
Line Active
Pending Transparent
S/T Deactivated
Pending Deactivation
Transparent

3.10 Embedded Operations Channel (EOC)

The Embedded Operations Channel (EOC) is used to transfer data from the exchange to the terminal side and vice versa without occupying B- or D-channels. It is used to transmit diagnostic functions and signaling information.

EOC-data is inserted into the U-frame at the positions M1, M2 and M3 thereby permitting the transmission of two complete EOC-messages (2x 12bits) within one U-superframe. With a MON-0-command a complete EOC-message (address field, data/message indicator and information field) can be passed to the U-transceiver.

The EOC contains an address field, a data/message indicator and an eight-bit information field. With the address field the destination of the transmitted message/data is defined. Addresses are defined for the NT, 6 repeater stations and broadcasting.

The data/message indicator needs to be set to (1) to indicate that the information field contains a message. If set to (0), numerical data is transferred to the NT. Currently no numerical data transfer to or from the NT is required.

From the 256 codes possible in the information field 64 are reserved for non-standard applications, 64 are reserved for internal network use and eight are defined by ANSI for diagnostic and loopback functions. All remaining 120 free codes are available for future standardization.

Table 3-5 Supported EOC-Commands

EOC					
Address Field	Data/ Message Indicator	Information	O (rigin) D (estination)		Message
a1 a2 a3	d/m	i1 i2 i3 i4 i5 i6 i7 i8	LT	NT	
0 0 0	x				NT
1 1 1	x				Broadcast
0 0 1 1 1 0	x				Repeater stations No. 1 – No. 6
	0				Data
	1				Message
	1	0 1 0 1 0 0 0 0	O	D	LBBD
	1	0 1 0 1 0 0 0 1	O	D	LB1
	1	0 1 0 1 0 0 1 0	O	D	LB2
	1	0 1 0 1 0 0 1 1	O	D	RCC
	1	0 1 0 1 0 1 0 0	O	D	NCC
	1	1 1 1 1 1 1 1 1	O	D	RTN
	1	0 0 0 0 0 0 0 0	D/O	O/D	H
	1	1 0 1 0 1 0 1 0	D	O	UTC

The EOC protocol operates in a repetitive command/response mode. Three identical properly-addressed consecutive messages shall be received by the NT before an action is initiated. In order to cause the desired action the Line Card controller continues to send the message until it receives three identical consecutive EOC frames from the NT that agree with the transmitted EOC frame.

The response of the NT is the echo of the received EOC frame. Any reply or echoed EOC frame is sent upstream in the next available returning EOC frame. All actions to be initiated at the NT shall be latching, permitting multiple EOC-initiated actions to be in effect simultaneously. Latched functions are resolved by the RTN (return-to-normal) command.

Access to the EOC is only possible when a superframe is transmitted. This is the case in the following states:

– Line Active
– Pend. Transparent
– S/T Deactivated
– Pend. Deactivation
– Transparent

In other states than the listed above all EOC-bits on the U-interface are clamped to high.

3.11 EOC Processor

The on-chip EOC-processor is responsible for the correct insertion and extraction of EOC-data on the U-interface. MON-0-messages provide the access to the device internal EOC-registers. The EOC processor performs code repitition. This means that a MON-0 message transporting the EOC command needs to be transferred only once

The EOC-processor can be programmed to automode or transparent mode:

EOC Auto Mode

– **Acknowledgment:** There is no acknowledgment in LT mode.

– **Latching:** No latching is performed.

– **Transfer to IOM®:** ’Return Message Reception Function’ is enabled as soon as the LT has transmitted an EOC command. It causes the U-transceiver in LT mode to compare the received and verified (by TLL) EOC messages with the last downstream transmitted EOC command. A MON-0 message is issued if they prove to be equal. For this particular received EOC message the ’different from previous’ rule is **NOT** applied. This means that a MON-0 message is even issued if the received EOC message is not different to the one previously accepted.

  All other incoming EOC messages besides the echo of the one transmitted downstream will be evaluated by TLL **and** the ’different from previous’ verification.

  New received EOC messages will be passed independently of the address used, i.e. not only messages addressed with (000) or (111) but all received EOC-messages will be transmitted with MON-0-messages or indicated by an interrupt request.

– **Execution:** No execution in LT mode

EOC Transparent Mode

Every 6 ms a MON-0-message is issued on IOM®. It contains the last received EOC-message. This occurs even if no change occurred in the EOC-channel. No “triple-last-look” is performed before a MON-0-message is sent.

Figure 3-18 summarizes the different processing of EOC/MON-0 commands/messages in LT and NT mode.

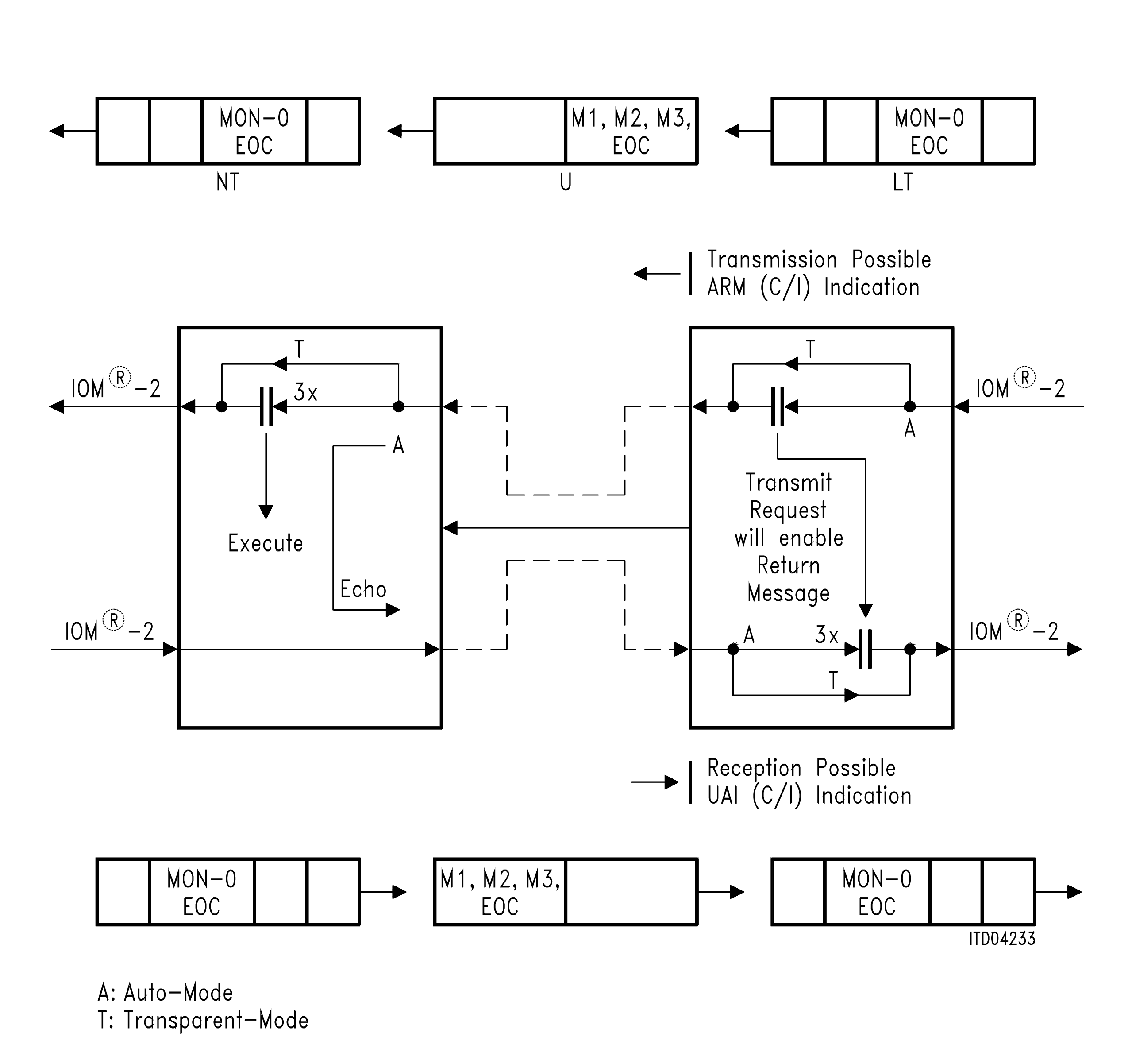


Figure 3-18 EOC-Procedure in Auto- and Transparent Mode

3.12 Cyclic Redundancy Check

An error monitoring function is implemented covering the 2B + D and M4 data transmission of a U-superframe by a Cyclic Redundancy Check (CRC).

The computed polynomial is:

$$G(u) = u^{12} + u^{11} + u^{3} + u^{2} + u + 1$$

(+ modulo 2 addition)

The check digits (CRC bits CRC1, CRC2, …, CRC12) generated are transmitted in the U-superframe. The receiver will compute the CRC of the received 2B + D and M4 data and compare it with the received CRC-bits generated by the transmitter.

A CRC-error will be indicated to both sides of the U-interface, as a NEBE (Near-end Block Error) on the side where the error is detected, as a FEBE (Far-end Block Error) on the remote side. The FEBE-bit will be placed in the next available U-superframe transmitted to the originator.

Far-end or near-end error indications increment the corresponding block error counters of exchange and terminal side. **Figure 3-19** illustrates the CRC-process.

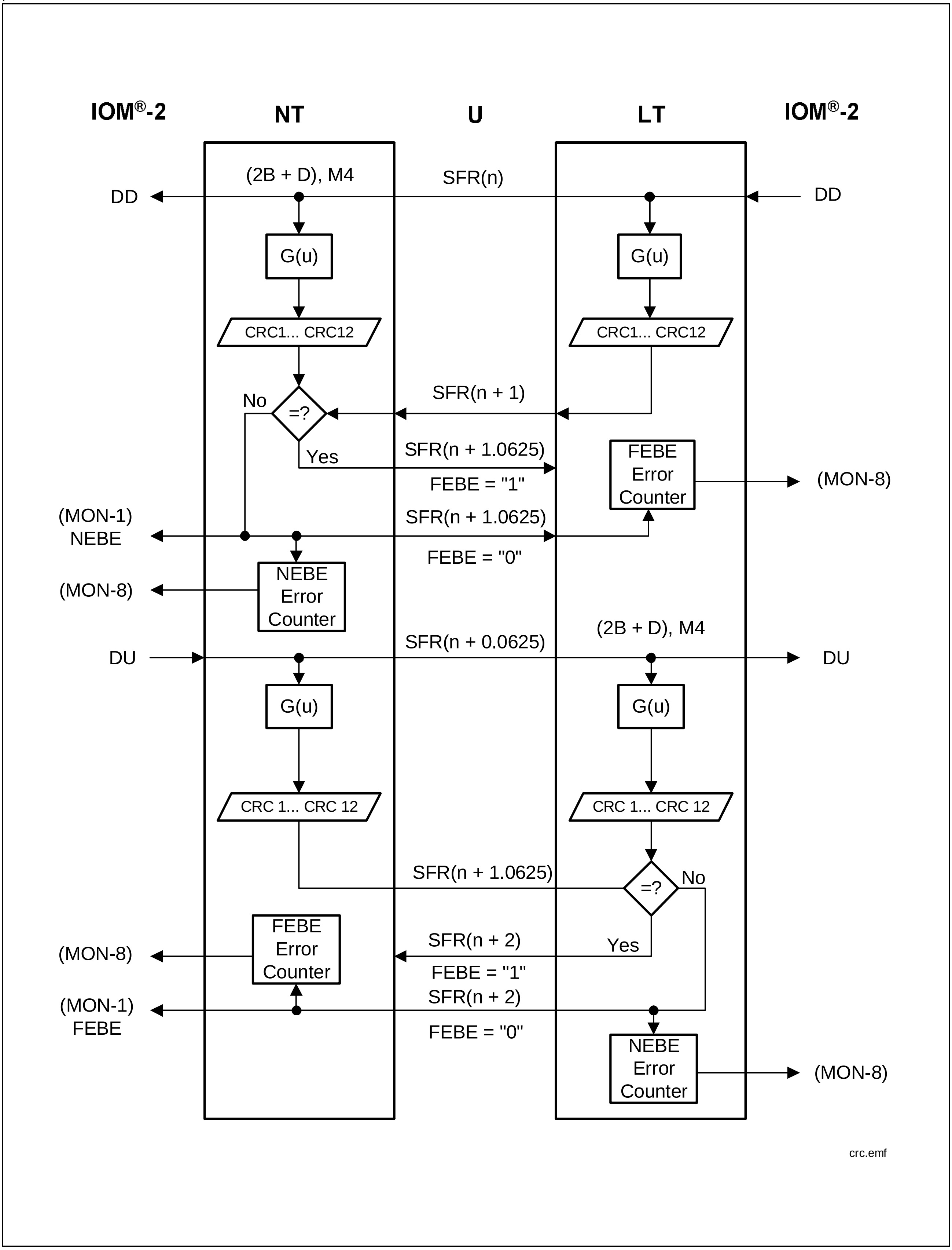


Figure 3-19 CRC-Process

3.13 Scrambling/ Descrambling

The scrambling algorithm ensures that no sequences of permanent binary 0s or 1s are transmitted. It is defined in ETSI TS 102 080 and ANSI T1.601. The algorithms used for scrambling and descrambling in LT- and NT-mode are given in **Figure 3-20**.

Note that one wrong bit decision in the receiver automatically leads to at least three bit errors. Whether all of these are recorded by a bit error counter depends on the fact whether all faulty bits are part of the monitored channels or not.

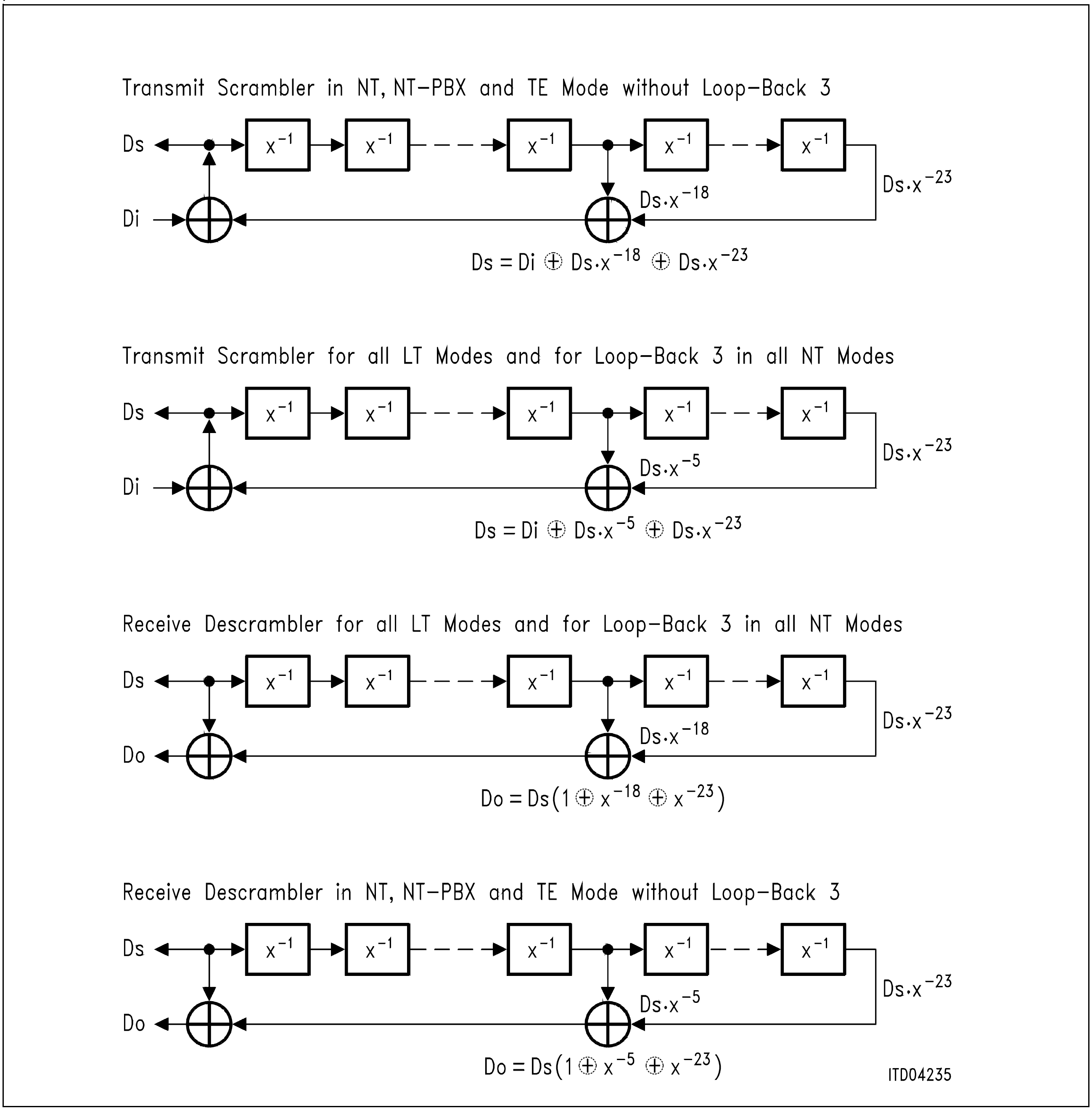


Figure 3-20 Scrambler/ Descrambler Algorithms

3.14 Encoding/ Decoding (2B1Q)

The 2B1Q line code is a 4-level pulse amplitude modulation (PAM) code without redundancy. 2B1Q stands for 2 Binary, 1 Quaternary. In transmit direction two-bit binary pairs are converted into quaternary symbols that are called quats. In each pair of bits the first bit is called the sign bit and the second is called the magnitude bit. **Table 3-6** shows the relationship of the bits to quats.

Table 3-6 2B1Q Coding Table

First bit (sign)	Second bit (magnitude)	Quaternary Symbol (quat)
1	0	+3
1	1	+1
0	1	-1
0	0	-3

The four values listed under 'Quaternary symbol' in the table above should be understood as symbol names, not numerical values.

At the receiver, each quaternary symbol is converted to a pair of bits by reversing the table, descrambled and finally formed into the original bit stream.

3.15 C/I Codes (2B1Q)

The operational status of the DFE-Q V2.1 is controlled by the Control/Indicate channel (C/I-channel). The four C/I channels operate completely independently.

Table 3-7 presents the existing C/I codes. A new command or indication will be recognized as valid after it has been detected in two successive IOM®-frames (double last-look criterion). Indications are strictly state oriented. Refer to the state diagrams in the following sections for commands and indications applicable in various states.

Commands have to be applied continuously on DIN until the command is validated by the DFE-Q V2.1 and the desired action has been initiated. Afterwards the command may be changed.

An indication is issued permanently by the DFE-Q V2.1 on DOUT until a new indication needs to be forwarded. Because a number of states issue identical indications it is not possible to identify every state individually.

Table 3-7 Command / Indicate Codes (2B1Q)

Code	LT-Mode	
	DIN	DOUT
0000	DR	–
0001	RES	DEAC
0010	–	FJ
0011	–	–
0100	RES1	RSY
0101	SSP	EI2
0110	DT	–
0111	UAR	UAI
1000	AR	AR
1001	ARX	ARM
1010	ARL	–
1011	–	EI3
1100	–	AI
1101	AR0	LSL
1110	–	–
1111	DC	DI

AI Activation Indication
AR Activation Request
AR0 Activation Request with act bit = 0
EI2 Error Indication 2 (error on S/T)
LSL Loss of Signal Level on U
DC Deactivation Confirmation

ARL	Activation Request Local Loop
ARM	Activation Request Maintenance bits
ARX	Activation Request without 15 sec limit
DR	Deactivation Request
DEAC	Deactivation Accepted
DI	Deactivation Indication
DT	Data-Through test mode
EI3	Error Indication 3 (time-out T1 [15 s], error on U)
RES	Reset
RES1	Reset receiver
RSY	Loss of Synchronization
SSP	Send-Single-Pulses test mode
UAI	U-Activation Indication
UAR	U-Activation Request
FJ	Frame Jump

3.16 State Machine Notation

The state machines control the sequence of signals at the U-interface that are generated during the start-up procedure. The informations contained in the following state diagrams are:

- State name
- U-signal transmitted
- Overhead bits transmitted
- C/I-code transmitted
- Transition criteria
- Timers

Figure 3-21 shows how to interpret the state diagrams.

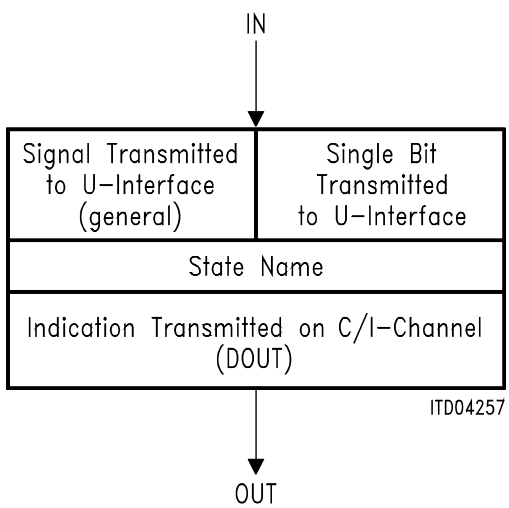


Figure 3-21 Explanation of the State Diagram

The following example explains the use of a state diagram by an extract of the LT-state diagram. The state explained is the “Deactivated” state in LT-mode.

The state may be entered by either of three methods:

– From state “Receive Reset” after time T7 has expired (T7 E*xpired*)
– From state “Tear Down” after the internal transition criterion “LSU” is fulfilled
– From state “Reset” or “Test” after the C/I-command “DR” has been sent on DIN

The following information is transmitted:

– SL0 is sent on the U-interface
– No overhead bits are sent
– C/I-message “DI” is issued on DOUT

The state may be left by either of the following methods:

– Leave for state “Awake” after NT wake up tone (TN) was detected and the C/I-code DC is present on DIN
– Leave for state “Alerting” after C/I-commands “AR”, “ARX”, “AR0” or “UAR” were received
– Leave for state “Reset for Loop” after C/I-command “ARL” was received

Combinations of transition criteria are possible. Logical “AND” is indicated by “&” (TN & DC), logical “OR” is written “or” and for a negation “/” is used. The start of a timer is indicated with “TxS” (“x” being equivalent to the timer number). Timers are always started when entering the new state. The action resulting after a timer has expired is indicated by the path labelled “TxE”.

The sections following the state diagram contain detailed information on all states and signals used. These details are mode dependent and may differ for identically named signals/states. They are therefore listed for each mode.

3.17 LT Mode State Diagram

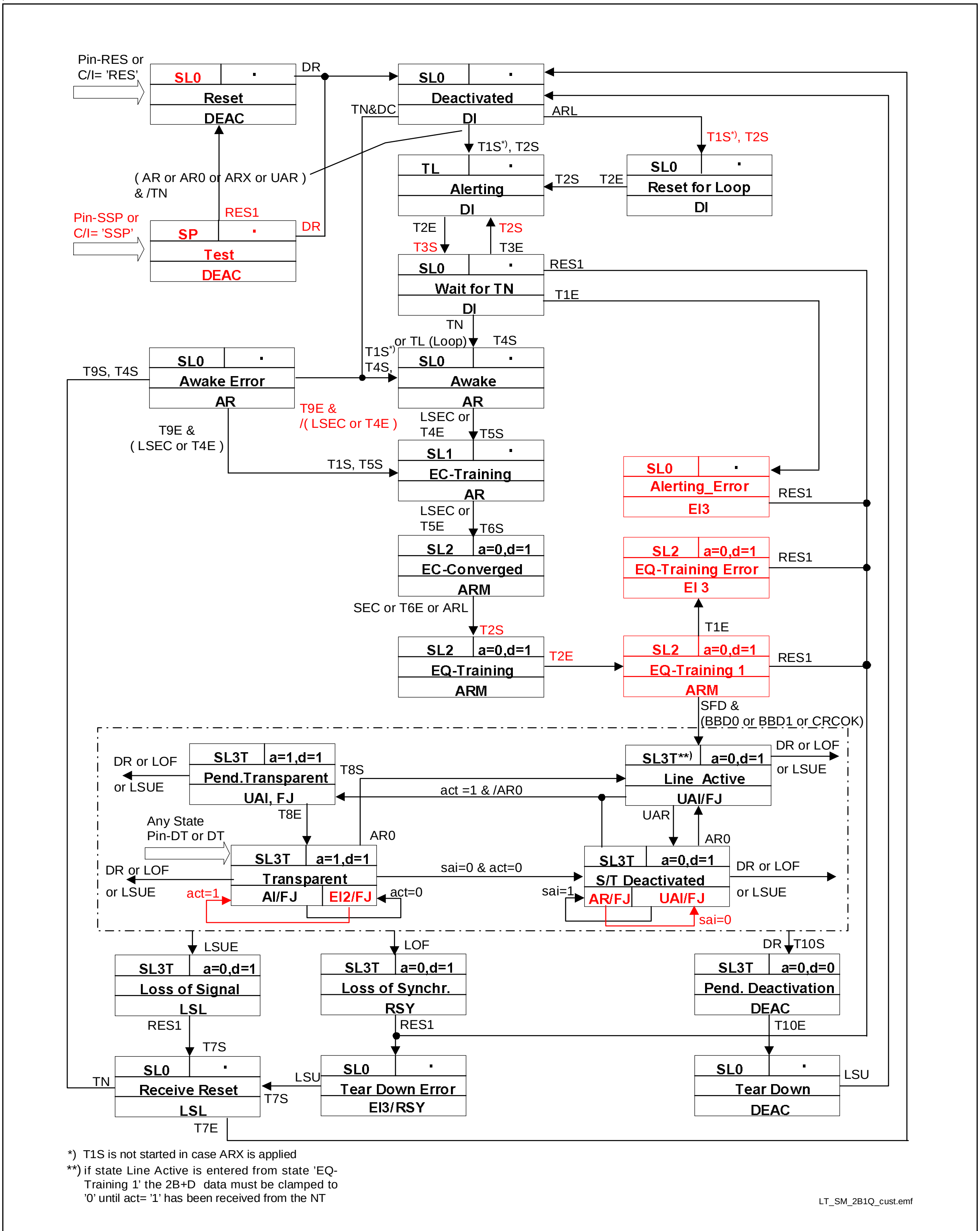


Figure 3-22 State Transition Diagram in LT-Mode

3.17.1 Inputs to the U-Transceiver in LT-Mode

The transition criteria are described in the following sections. They are grouped into:

– C/I-commands
– Pin settings
– Events related to the U-interface
– Timers

C/I-Commands

AR Activation Request
The U-transceiver is requested to enter the power-up state and to start an activation procedure by sending the wake-up signal TL. In case the U-transceiver is in state "Deactivated" it is recommended always to apply DC before AR to resolve the situation if a TN tone has been detected before.

AR0 Activation Request with “ACT” bit = (0)
The U-transceiver is requested to enter the power-up state and to start an activation procedure by sending the wake-up signal TL. After “EQ Training” the state “Line Active” will be entered independent of the “ACT” bit. Evaluation of the “ACT” bit is disabled when AR0 is received and enabled when AR is received.
In case the U-transceiver is in state "Deactivated" it is recommended always to apply DC before AR0 to resolve the situation if a TN tone has been detected before.

ARL Activation Request Local Loop-back
The U-transceiver is requested to operate an analog loop-back (close to the U-interface) and to start the start-up sequence by sending the wake-up tone TL. This command may be issued only after the U-transceiver has been set to the “Deactivated” state (C/I-channel code DI issued on DOUT) and has to be issued continuously as long as loop-back is requested.

ARX Activation Request Extended
The DFE-Q is requested to enter the power-up state and to start an activation procedure by sending the wake-up signal TL. The difference to the command AR is that the Timer T1 is disabled. The activation duration may exceed 15 sec.
In case the U-transceiver is in state "Deactivated" it is recommended always to apply DC before ARX to resolve the situation if a TN tone has been detected before.

DC Deactivation Confirmation
If ’DC’ is applied in state “Deactivated” the DFE-Q transitions to state "AWAKE" as soon as it receives a wake-up tone from the NT. If ’DR’ is applied in state “Deactivated” the wake up request of the NT is not acknowledged. This way the linecard is able to reject an activation attempt by the NT e.g. during a service procedure.

By means of the ’DC’ command the LT is also during an U-only activation capable to control the point of time when the complete transmission line is set transparent in case a terminal initiated activation request has occurred. In state ’S/T Deactivated’ with applied C/I code ’UAR’ the DFE-Q issues ’UOA= 0’ and receives ’SAI= 0’ from the deactivated S interface. If the terminal requests an activation with ’AR’ issued in the NT the SAI bit is set to ’1’ and the LT indication ’UAI’ switches to ’AR’. As soon as ’DC’ is applied instead of ’UAR’ on the LT side the line is set transparent, since the UOA bit reflects the polarity of SAI and is thus set to ’1’.

DR Deactivation Request
This command requests the U-transceiver to start a deactivation procedure by setting the DEA bit to “0” and to cease transmission afterwards. The DR-code is a conditional command causing the U-transceiver only to react in the states “Reset”, “Test”, “S/T Deactivated”, “Line Active”, “Pending Transparent” and “Transparent”, i.e. when the C/I-channel codes DEAC, UAI, AR, AI, FJ or EI2 are issued on DOUT.

DT Data Through
This unconditional command is used for test purposes only and forces the U-transceiver into the transparent state independent of the wake-up protocol. A far-end transceiver needs not to be connected; in case a far-end transceiver is present it is assumed to be in the same condition.

RES Reset
Unconditional command which resets the whole chip; note that on contrary to the pin reset a clock signal must be provided for the C/I code processing.

RES1 Reset 1
The reset 1 command resets all receiver functions; especially the EC- and EQ-coefficients and the AGC are set to zero. The RES1-code does not reset any other than receiver functions (e.g. IOM®-functions or relay driver settings). The RES1-code should be used when the U-transceiver has entered a failure condition (expiry of timer T1, loss of framing or loss of signal level) indicated by the C/I-channel EI3, RSY or LSL on DOUT. Besides resetting the receiver, this command stops transmission on the U-interface. The DEA bit is not set to “0” by RES1.

SSP Send Single Pulses
Unconditional command which requests the transmission of single pulses on the U-interface. The pulses are issued at 1.5 ms intervals and have a duration of 12.5 µs. The chip is transferred to the “Test” state; the receiver will not be reset.

UAR Partial Activation Request (U only)
The U-transceiver is requested to enter power-up state and to start an activation procedure of the U-interface only.

Pins

Pin-RES Pin-Reset
The function of this pin is the same as the C/I-code RES. C/I-message DEAC will be issued. The duration of the reset pulse must be 10 ns minimum.

Pin-SSP Send Single Pulses
The function of this pin is the same as for the C/I-code SSP. The C/I-message DEAC will be issued. The high level needs to be applied continuously for the transmission of single pulses.

Pin-DT Data Through
The function is identical with the C/I-code DT.

U-Interface Events

ACT = 0/1 "ACT" bit received from the NT-side.

- ACT = 1 signals that the NT has detected INFO3 on the S/T-interface and indicates that the complete basic access system is synchronized in both directions of transmission. The LT-side is requested to provide transparency of transmission in both directions and to respond with setting the ACT-bit to "1". In the case of loop-backs (loop-back 2 or single-channel loop-back in the NT), however, transparency is required even when the NT is not sending ACT = 1. Transparency is achieved in the following manner:
- The U-transceiver performs transparency in both directions of transmission after the receiver has achieved synchronization (state EQ-training is left) independent of the status of the received ACT-bit.
- The status "ready for sending" is reached when the state transparent is entered i.e. when the C/I-channel indication AI is issued. This is valid in the case of a normal activation procedure for call control. In the case of loop-backs (loop-back 2 or single-channel loop-back in the NT and analog loop-back in the LT) however, the status "ready for sending" is reached when the state line active is entered i.e. when the C/I-channel indication UAI is issued. Until the status "ready for sending" is reached, binary "0s" have to be passed in the B- and D-channels on DIN.
- ACT = 0 indicates the loss of transparency on the NT-side (loss of framing or loss of signal level on the S/T-interface). The U-transceiver informs the LT-side by issuing the C/I-channel indication EI2, but performs no state change or other actions.

CRCOK Cyclic Redundancy Check OK
This input is used as a criterion that the receiver has acquired frame synchronization and both its EC and EQ coefficients have converged.

LOF Loss of Framing on the U-interface
This condition is fulfilled if framing is lost for 576 ms. 576 ms are the upper limit. If the correlation between synchronization word and input signal is not optimal, LOF can be issued earlier.

LSEC Loss of Signal Level behind the Echo Canceler
In the "Awake" state, this input is used as indication that the NT has ceased the transmission of signal SN1. In the EC-training state, this input is used as an internal signal indicating that the EC in the LT has converged.

LSU Loss of Signal Level on the U-interface
This signal indicates that a loss of signal level for the duration of 3 ms has been detected on the U-interface. This short response time is relevant in all cases where the LT waits for a response (no signal level) from the NT-side, i.e. after a deactivation procedure has been started or after loss of framing in the LT occurred.

LSUE Loss of Signal Level on the U-interface (error condition)
After a loss of signal level has been noticed, a 492 ms timer is started. After this timer has elapsed, the LSUE-criterion is fulfilled. This long response time (see also LSU) is valid in all cases where the LT is not prepared to lose signal level. Note that 492 ms

represent a minimum value; the actual loss of signal might have occurred earlier, e.g. when a long loop is cut at the LT-side, the echo coefficients need to be readjusted to new parameters. Only after the adjusted coefficient cancel the echo completely, the loss of signal is detected and the timer can be started (if the long loop is cut at the remote end, the coefficients are still correct and a loss of signal will be detected immediately).

SEC Signal Level behind the echo canceler
This signal indicates that a signal level corresponding to SN2 from the NT has been detected on the U-interface.

SFD Superframe Detected

TN Tone (wake-up signal) received from the NT.
When in the “Deactivated” state, the U-transceiver is requested to start an activation procedure and to inform the LT-side making use of the C/I-channel code AR. When in the “Wait for TN” state, the signal TN sent by the NT acknowledges the receipt of a wake-up signal TL from the LT.
When an analog loop-back is operated, the wake-up signal TL sent by the LT-transmitter is detected by the LT-receiver.
The TN-criteria is fulfilled when 12 consecutive periods of the 10 kHz wake-up tone were detected.

BBD0/1 Binary “0” or “1s” detected in the B- and D-channels
This internal signal indicates that for a period of time of 6–12 ms a continuous stream of binary “0s” or “1s” has been detected. It is used as a criterion that the receiver has acquired frame synchronization and both its EC- and EQ-coefficients have converged. BBD1 corresponds to the signals SN2 or SN3 in the case of a normal activation and BBD0 corresponds to the internally received signal SL2 in the case of an analog loop-back or possibly a loop-back 2 in the NT.

Timers

The start of timers is indicated by TxS, the expiry by TxE. The following **Table 3-8** shows which timers are used in LT-modes:

Table 3-8 Timers Used in LT-Modes

Timer	Duration (ms)	Function	State
T1	15000	Supervisor for start-up	
T2	3	TL-transmission Receiver reset	Alerting Reset for loop
T3	40	Re-transmission of TL	Wait for TN
T4	6000	Supervisor SN0 detect	Awake
T5	1000	Supervisor EC converge	EC training
T6	6000	Supervisor SN2 detect	EC converge
T7	40	Hold time	Receiver reset

Timer	Duration (ms)	Function	State
T8	24	Delay time for AI detection	Pend. transparent
T9	40	Hold time	Awake error
T10	40	“DEA” = (0) transmission	Pend. Deactivation

3.17.2 Outputs of the U-Transceiver in LT-Mode

Signals and indications are issued on the IOM®-2-interface (C/I-codes) and U-interface (predefined U-signals).

C/I-Indications

AI — Activation Indication
This indication signals that “ACT” = 1 has been received and that timer T8 has elapsed. This indication is not issued in case AR0 is applied to DOUT or an analog loop-back is operated.

AR — Activation Request
The AR-code signals that a wake-up signal has been received and that a start-up procedure has commenced. Receiver synchronization has not yet been achieved. When already partially active (U only activation), AR indicates that the “SAI” bit was set to (1), i.e. the S/T-interface has become active.

DEAC — Deactivation
This indication is issued in response to a DR-code (Pend. Deactivation, Tear Down) and in the “Reset” and “Test” states.

DI — Deactivation Indication
Idle code on the IOM®-interface. Normally the U-transceiver stays in the “Deactivated” state unless an activation procedure is started by the NT-side.

EI2 — Error Indication 2
EI2 is issued if the received ACT-bit is (0). The NT receiver indicates a loss of signal or framing on the S/T-interface by setting the upstream ACT-bit to (0). The U-transceiver remains in the “Transparent” state. After a signal level or framing is detected again, the C/I-indication AI will be issued anew.

EI3 — Error Indication 3
This indication is issued when the U-transceiver has not been able to activate successfully (expiry of timer T1).

LSL — Loss of Signal Level
The U-transceiver has entered a failure condition after loss of signal level (LSUE).

RSY — Re-Synchronization indication after a loss of framing (LOF)
For EI3, LSL and RSY indication the LT-side should react by applying the C/I-channel code RES1 to allow the U-transceiver to enter the “Receive reset” state and to reset the receiver functions.

FJ — Frame Jump
This indication signals that either a data buffer overflow/underflow has been detected or a phase jump of one of the IOM®-timing signals DCL or FSC has occurred. The FJ-code is issued for a period of 1.5 ms.

UAI — U-Activation Indication
The UAI-code signals that the line system is synchronized in both directions of transmission (see also the input ACT = 1). Maintenance bits are transmitted normally.

ARM — Activation Request Maintenance
Transmission of maintenance bits is possible.

Signals on U-Interface

The signals SLx, TL and SP transmitted on the U-interface are defined in **Table 4-1 on page 3**. The polarity of the overhead bits ACT and DEA is indicated as follows:

a = 0/1 corresponds to ACT bit set to binary “0/1”.
d = 0/1 corresponds to DEA bit set to binary “0/1”.

The polarity of the transmitted UOA-bit depends on the received C/I-channel code:

– UAR sets UOA-bit to binary 0.
– AR sets UOA-bit to binary 1.
– Any other C/I-codes sets the UOA to the same value as the received SAI bit. After deactivation the UOA-bit is set to binary 0 until a valid SAI-bit is received.

3.17.3 LT-States

This section describes the functions of all states defined in LT-mode.

Alerting

The wake-up signal TL is transmitted for 3 ms (T2) in response to an activation request from the LT side (AR or ARL). In the case of an analog loop-back, the signal TL is forwarded internally to the wake-up signal detector and stored.

Alerting Error

When timer T1 (15s) is expired in state "Alerting" before TN has been detected then the DFE-Q transits from state "Alerting" to state "Alerting Error". Once "Alerting Error" has been entered the receiver must be reset by C/I RES1.

Awake

The “Awake” state is entered upon the receipt of a wake-up or an acknowledge signal TN from the NT. In the case of an activation started by the LT-side, timer T1 is restarted when the “Awake” state is entered.

Awake Error

The “Awake Error” state is equivalent to the “Awake” state, but is entered only when a wake-up signal is received while being in the “Receive reset” state. As the “Receive reset” state was entered upon the application of the C/I-channel code RES1, the “Awake error” state assures that a minimum amount of time elapses between the application of the RES1-code and the U-transceiver entering a state (EQ training) in which it again reacts on the RES1-code. The LT-side is requested to stop issuing the command RES1 within T9 after the receipt of the C/I-channel code AR on DOUT and to replace it by another command such as the idle code DC for instance.

Deactivated (Full Reset)

In the “Deactivated” state the device may enter the low power consumption condition. The power-down mode is entered if no monitor messages are to be expected. In power-down the receiver and parts of the interface are deactivated while functions related to the IOM®-2-interface and the wake-up detector are still active.
No signal is sent on the U-interface, the differential outputs AOUT and BOUT are set to 0 V. The U-transceiver waits for a wake-up signal TN from the NT-side or an activation request (AR, AR0, UAR or ARL) from the LT-side to start an activation procedure. Note that in state "Deactivated" no activation can be initiated by AR, ARX, AR0 or UAR if a TN tone has been recognized before. This situation can be only resolved by applying DC. Therefore it is recommended to apply always DC before AR, ARX, AR0 or UAR.

For the recognition of the wake-up signal TN the following procedure applies:

– TN detected for 8 periods –> transfer within the “Deactivated” state into power-up
– In power-up both differential outputs, AOUTx and BOUTx, are set to the common mode DC level of VDDmin/2

– TN detected for a total of 12 consecutive periods –> transition criterion TN fulfilled, change to next state, if in addition the C/I-command DC is given on DIN.
– TN detected for more than 8 but less than 12 periods –> return to power-down

The input sensitivity is stated in the AFE V1.1 Data Sheet. There the minimum level required is specified to meet the TN transition criterion. The power-up condition may thus already be entered at a lower level.

EC Converged

Upon the EC-coefficients having converged, the U-transceiver starts the transmission of signal SL2 and waits for the receipt of signal SN2 from the NT (SEC). If no signal is detected within T6, nevertheless the start-up procedure will be continued. In the case of an analog loop-back, this state is left immediately because the EC compensates for the looped back transmit signal.

EC-Training

The signal SL1 is transmitted on the U-interface to allow the LT-receiver to update its EC-coefficients. The “EC-training” state is left when the EC has converged (LSEC) or when timer T5 has elapsed. Timer T5 allows the start-up procedure to proceed even if LSEC due to a high noise level on the U-interface for instance, could not be detected.

EQ-Training

In state “EQ-Training” the equalizer coefficients are trained for a minimum period of 3ms. Upon expiry of timer T2 state “EQ-Training 1” is entered.

EQ-Training 1

The “EQ-Training 1” state is left after the receiver has achieved synchronization and the superframe indication has been detected (SFD). In case RES1 is applied “EQ-Training 1” the U-transceiver transits to “Tear Down Error” and finally gets reset. Refer to state “EQ-Training 1” in case an error condition occurred.

EQ-Training Error

Upon expiry of timer T1 the DFE-Q leaves state “EQ-Training 1”, enters state “EQ-Training Error” and issues the C/I-channel indication EI3. The error condition can only be resolved by applying RES1.

Line Active

In the “Line Active” state, the U-transceiver transmits transparently in both directions. The U-Interface is synchronized and the maintenance channel is operational. The U-transceiver stays in the line-active state

– during a normal activation procedure while the “ACT” bit = (0) is received
– when an analog loop-back is established
– while C/I-command AR0 is applied to DIN

In the case of normal activation with call control, binary “0s” have to be applied to the B and D channels on the IOM®-interface. After the C/I-channel indication UAI has been issued, the layer-2 receiver should be fully operational to prevent the first layer-2 message issued by the NT-side upon the receipt of the AI-code in the TE, to be lost.

Loss of Signal

The “Loss of Signal” state is entered upon the detection of a failure condition i.e. loss of receive signal (LSUE). The ACT bit is set to “0” and the C/I-channel indication LSL is issued. The U-transceiver waits for the C/I-channel command RES1 to enter the “Receive Reset” state.

Loss of Synchronization

The “Loss of Synchronization” state is entered upon the detection of a failure condition i.e. loss of framing by the LT-receiver (LOF). The ACT-bit is set to “0” and the C/I-channel indication RSY is issued. The U-transceiver waits for the C/I-channel command RES1 to enter the “Tear Down Error” state and subsequently the “Receive Reset” state.

Pending Deactivation

“Pending Deactivation” is a transient state entered after the receipt of a DR-code. The DEA-bit is set to “0”. Timer T10 assures that the DEA-bit is set to “0” in at least three consecutive superframes before the transmit level is turned off.

Pending Transparent

“Pending Transparent” is a transient state entered upon the detection of ACT = 1 and left by T8. The ACT-bit is set to “1”. The purpose of this state is to issue the C/I-channel indication AI (corresponding to “ready for sending”) 24 ms after the ACT-bit has been set to “1” by the LT-transceiver. This assures that under normal operating conditions the AI-indication is issued first on the TE-side and only afterwards on the LT-side. Thus the layer-2 receiver in the TE is already operational when the first layer-2 message is issued by the LT-side.

Reset

The “Reset” state is entered with the unconditional command RES, respectively Pin-RES. It is left when pin RESQ is inactive and the C/I-channel code DR is received. SL0 and DEAC are output in “Reset” state. The U-transceiver does not react to the receipt of a wake-up signal TN.

Reset for Loop

“Reset for Loop” resets the receiver in order to guarantee a correct adaption of the echo- and equalizer coefficients.

Receive Reset

The “Receive Reset” state assures that for a period of T7 no signal, especially no wake-up signal TL, is sent on the U-interface, i.e. no activation procedure is started from the LT-side. A wake-up signal TN, however, from the NT-side is acknowledged.

S/T Deactivated

The state "S/T Deactivated" will be entered if the received ACT- and SAI-bits are set to (0). In this state the signal SL3T, ACT = (0), DEA = (1) and UOA = (0) are transmitted downstream. On the IOM®-2-bus the C/I-code UAI is issued while the received SAI = (0).
In order to initiate a complete activation from the S/T deactivation state, the LT needs to set the UOA-bit to (1). This will occur if either of the following three conditions are met:

– C/I = AR(LT-activation)
– SAI = (1) & AR(TE-activation with exchange control [DIN = C/I UAR])
– SAI = (1)(TE-activation without exchange control [DIN = C/I DC])

"S/T deactivated" will be left if the received ACT bit is (1), or the C/I code AR0 is applied.

Tear Down

In "Tear Down" state, transmission ceases in order to deactivate the basic access, and the U-transceiver waits for a response (no signal level, LSU) from the NT-side.

Tear Down Error

"Tear Down Error" state is entered after loss of framing has been detected. Transmission ceases in order to deactivate the basic access and the U-transceiver waits for a response (no signal level, LSU) from the NT-side. EI3-indication is transmitted after a transition forced by RES1 from the wait-for-TN or EQ-training states. In the case of transition from the "Loss of synchronization" state RSY is sent.

Test

This "Test" mode is entered when the unconditional commands SSP or Pin-SSP is applied. It is left when pin SSP is set inactive again and the C/I-channel code DR or RES1 is received. Single pulses (SP) and DEAC are output in "Test" state. The U-transceiver does not react to the receipt of a wake-up signal TN.

Transparent

This "Transparent" state corresponds to the fully active state in the case of a normal activation for call control. It may also be entered in the case of a loop-back #2 if the NT issues ACT = 1 or in case of a single-channel loop-back in the NT. The LT-side is informed that the status "ready for sending" is reached (indication AI). If the NT-side loses transparency (receipt of ACT = 0), the LT-side is informed by making use of the C/I-channel indication EI2, but no state change is performed. Upon reception of ACT= (1) the C/I indication AI is issued again. If the S/T-interface is deactivated (SAI = (0) & ACT = (0)), the device is transferred to the S/T deactivated state.

Wait for TN

In "Wait for TN" the U-transceiver waits for a response (tone TN from the NT or tone TL in case of an analog loop-back) to the transmission of the wake-up signal TL. If no response is received within T3, the state is left for re-transmission of a wake-up tone TL. This procedure is repeated until the detection of tone TN or until expiry of timer T1. In this case the C/I-channel indication EI3 is issued, but no state change is performed.

4 Operational Description

The scope of this section is to describe how the DFE-Q V2.1 works and behaves in the system environment. Activation/ deactivation control procedures are exemplary given for SW programmers reference.

4.1 Reset

There are two different ways to apply a reset,

- either as a hardware reset by setting pin $\overline{\text{RES}}$ to low
- or as a software reset by applying 'C/I= RES'

Hardware Reset

A hardware reset affects all design components and takes effect immediately (asynchronous reset style). No clock signal other than the 15.36MHz master clock is required for reset execution.

Software Reset

C/I 'RES' resets the receiver and the activation/deactivation state machine. Transmission on U is stopped. It is an unconditional command and is therefore applicable in any state.

Unlike a hardware reset, a software reset triggered by 'C/I= RES' or 'C/I= RES1' has only effect on the addressed line port.

– C/I= RES resets the receiver and the activation/deactivation state machines. It is an unconditional command.
– C/I= RES1 resets all receiver functions. Transmission on U is stopped. EC-, and EQ-coefficients and AGC are set to zero. It is a conditional command.

The remaining line ports, the system interface, the relay driver/ status pins and other global functions are not affected. Note that a clock signal must be provided for the C/I code processing.

4.2 Power Down

Each building block of the DFE-Q V2.1 is optimized with respect to power consumption and support a power down mode. See chapter 7.6.2 page 7-8 for the specified max. power consumption.

The DFE-Q V2.1 goes in power down mode if the U-transceiver is in state DEACTIVATED. The DFE-Q V2.1 leaves power down mode when a wake up tone (TN) has been detected on the U-interface for at least 800µs.

- as the internal control logic of the activation/deactivation procedures are event driven power is saved as soon as one of the four lines transits in the ’Deactivated’ state

Regarding the **DFE-Q V2.1** power down mode means that

- the DSP clock is turned off
- all digital circuits (excluding the IOM®-2 interface) go in power down mode
- no timing signals are delivered (CLS0, ... , CLS3)
- as the internal control logic of the activation/deactivation procedures are event driven power is saved as soon as one of the four lines transits in the DEACTIVATED state

Regarding a connected **AFE** power down mode means that

- no signal is sent on the U-interface
- only functions that are necessary to detect the wake up conditions are kept active
- transmit path, receive path and auxiliary functions of the analog line port are switched to a low power consuming mode when the power down function is activated. This implies the following:
- the ADC, the relevant output is tied to GND.
- the DAC and the output buffer; the outputs AOUTx/ BOUTx are tied to GND.
- the internal DC voltage reference is switched off.
- the range and the loop functions are deactivated.

4.3 Layer 1 Activation/ Deactivation Procedures

This chapter illustrates the interactions during activation and deactivation between the LT and NT station. An activation can be initiated by either of the two stations involved. A deactivation procedure can be initiated only by the exchange.

This chapter shows the user how to activate and deactivate the device under various circumstances. Two types of start-up procedures are supported by the U-transceiver:

- cold starts and
- warm starts.

Cold starts are performed after a reset and require all echo and equalizer coefficients to be recalculated. This procedure typically is completed after 1-7 seconds depending on the line characteristic. Cold starts are recommended for activations where the line characteristic has changed considerably since the last deactivation.

A warm start procedure uses the coefficient set saved during the last deactivation. It is therefore completed much faster (maximum 300ms). Warm starts are however restricted to activations where the line characteristic has not changed significantly since the last deactivation.

Both start-up procedures differ only in the fact that the device has been transferred into the RESET state (= cold start) prior to activation. Activation initialization and procedure is in both cases identical. The following sections thus apply to both warm and cold start-ups.

The table below summarizes the existing U-interface signals as specified by ETSI/ ANSI.

Table 4-1 U-Interface Signals

Signal	Synch. Word (SW)	Superframe (ISW)	2B + D	M-Bits
NT-Modes (NT –> LT)				
TN [1)]	± 3	± 3	± 3	± 3
SN0	no signal	no signal	no signal	no signal
SN1	present	absent	1	1
SN2	present	absent	1	1
SN3	present	present	1	normal
SN3T	present	present	normal	normal
LT-Modes (LT –> NT)				
TL [1)]	± 3	± 3	± 3	± 3
SL0	no signal	no signal	no signal	no signal
SL1	present	absent	1	1
SL2	present	present	0	normal

Signal	Synch. Word (SW)	Superframe (ISW)	2B + D	M-Bits
SL3 [2)]	present	present	0	normal
SL3T[3)]	present	present	normal	normal
Test Mode				
SP [4)]	no signal	no signal	± 3	no signal

Notes:[1)] Alternating ± 3 symbols at 10 kHz

[2)] Must be generated by the exchange

[3)] If state 'Line Active' is entered from state 'EQ-Training 1' the 2B+D data must be clamped to '0' by the exchange until act= '1' has been received from the NT-side

[4)]Alternating ± 3 single pulses of 12.5 µs duration spaced by 1.5 ms

4.3.1 Complete Activation Initiated by LT

Figure 4-1 depicts the procedure if the activation has been initiated by the exchange side.

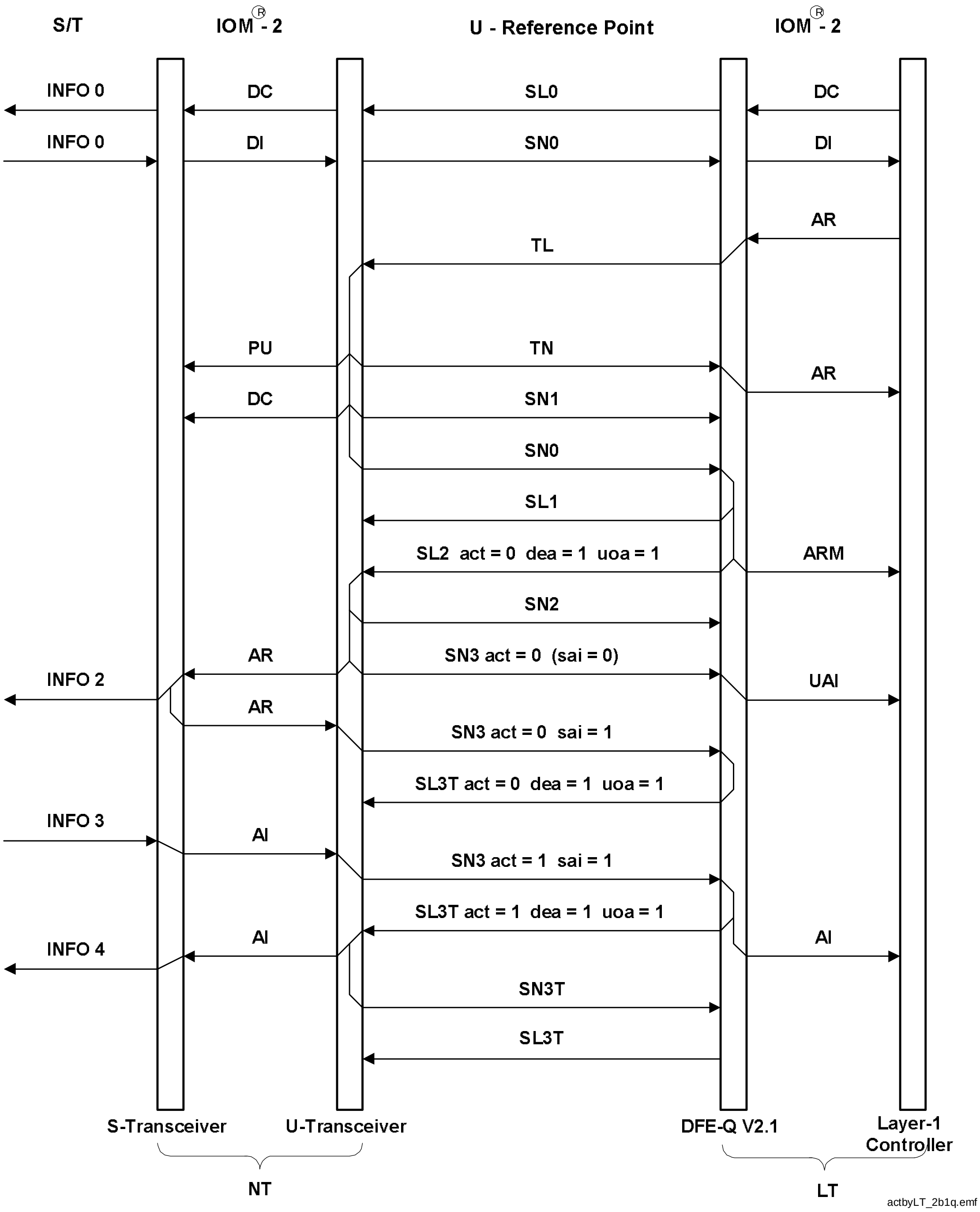


Figure 4-1 Complete Activation Initiated by LT

The activation protocol and the user interactions are summarized below:

	NT IOM®-2		LT IOM®-2			
<———	C/I DC	(1111_B)	CI/DC	(1111_B)	<———	; Initial state is “Deactivated”
———>	C/I DI	(1111_B)	C/IDI	(1111_B)	———>	;
<———	C/I PU	(0111_B)	**C/I AR**	**(1000_B)**	**<-----**	; Start activation
<———	C/I DC	(1111_B)	C/I AR	(1000_B)	———>	; Activation proceeds
			C/I ARM	(1001_B)	———>	; :
<———	C/I AR	(1000_B)	C/I UAI	(0111_B)	———>	; :
----->	**C/I AI**	**(1100_B)**				; Confirm that terminal is ; active
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	; Activation complete

4.3.2 Activation with ACT-Bit Status Ignored by the Exchange Side

The LT ignores the ACT-bit transmitted upstream from the NT if the LT-activation has been initiated with „AR0“ instead of „AR“. Activation with C/I-command “AR0” forces the state machine into the state “Line Active” independently of the ACT-bit status transmitted upstream from the network.

Because the activation with AR0 is performed with the UOA-bit set to “0”, initially only a partial activation is started. By setting UOA = 1 via a MON-2 message the S-interface is activated as well. Activation may be completed after the ACT-bit evaluation has been enabled with C/I-command “AR”.

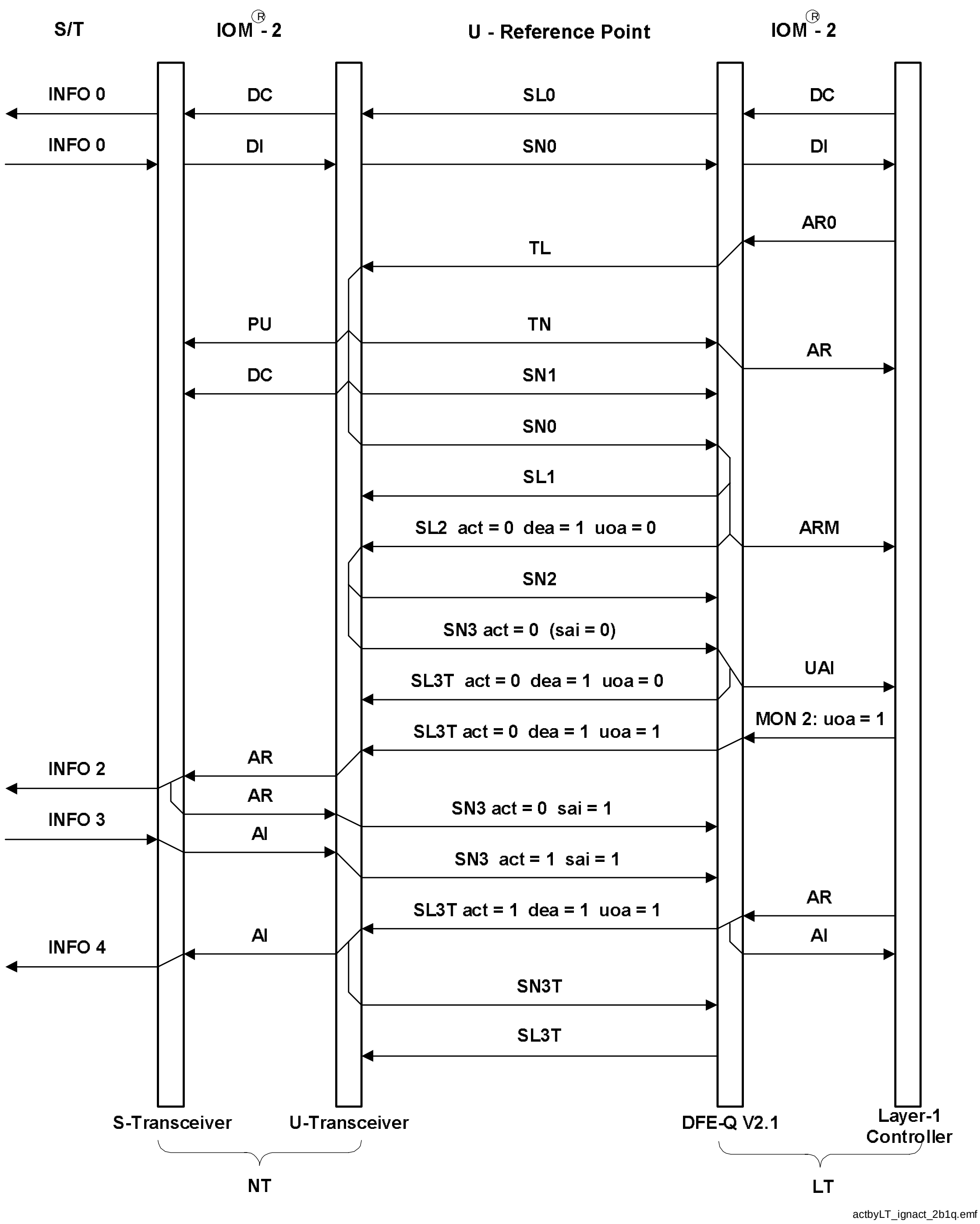


Figure 4-2 Activation with ACT-Bit Status Ignored by the Exchange

The activation protocol and the user interaction is summarized below:

	NT IOM®-2		LT IOM®-2			
<———	C/I DC	(1111_B)	C/I DC	(1111_B)	<———	; Initial state is “Deactivated”
———>	C/I DI	(1111_B)	C/I DI	(1111_B)	———>	;
			C/I AR0	**(1101_B)**	**<-----**	; Start activation
<———	C/I PU	(0111_B)	C/I AR	(1000_B)	———>	;
<———	C/I DC	(1111_B)	C/I ARM	(1001_B)	———>	;
			C/I UAI	(0111_B)	———>	;
			MON8 PACE	**(80 BE_H)**	**<-----**	; Enable control of UOA-bit
			MON2 UOA	**(2F FF_H)**	**<-----**	; and set UOA = 1
<———	C/I AR	(1000_B)				
----->	**C/I AI**	**(1100_B)**				: Confirm that terminal is ; active
<———	C/I AR	(1000_B)	C/I UAI	(1100_B)	———>	; ACT-bit status ignored
			C/I AR	**(1000_B)**	**<-----**	; Enable ACT-bit evaluation
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	; Activation complete
			C/I AR0	**(1101_B)**	**<-----**	: Disable ACT-bit evaluation
<———	C/I AR	(1000_B)	C/I UAI	(0111_B)	———>	: ACT-bit status ignored

4.3.3 Complete Activation Initiated by TE

Figure 4-3 depicts the procedure if the activation has been initiated by the terminal side.

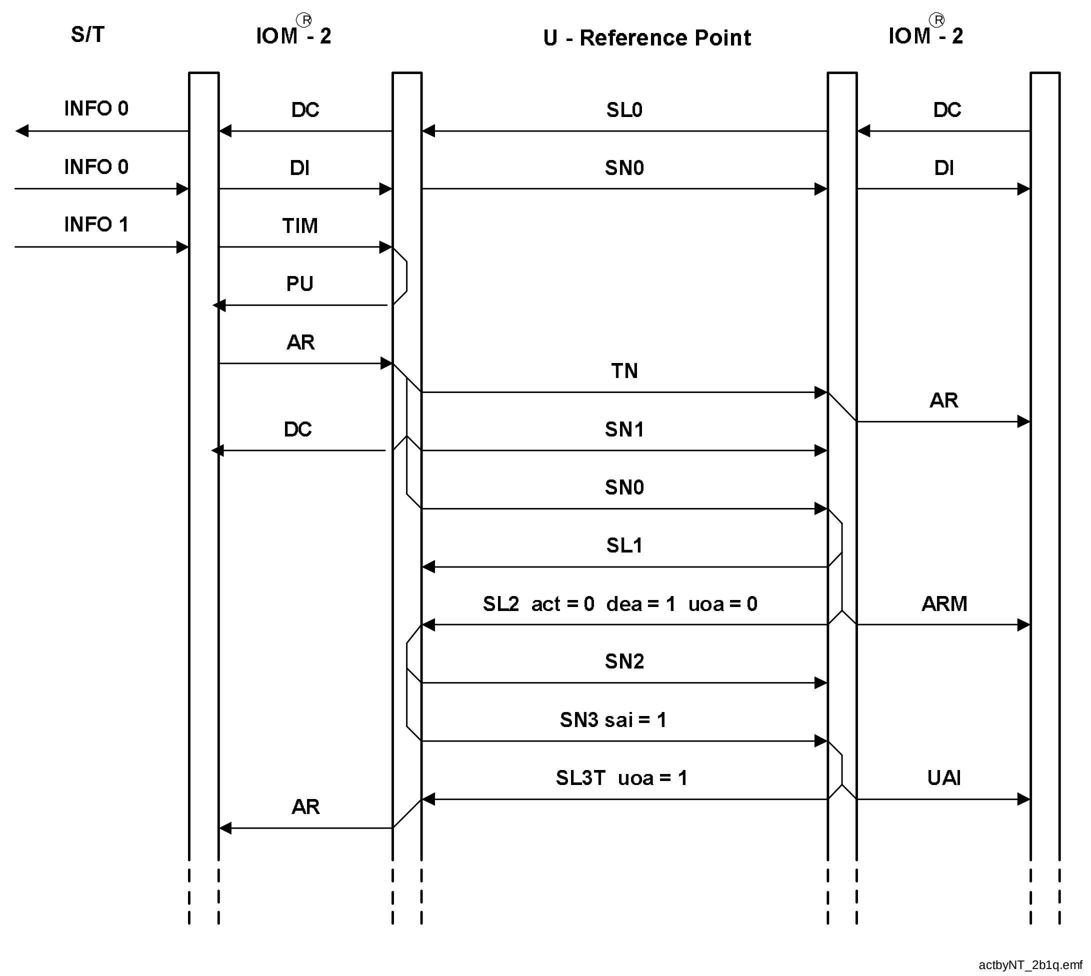


Figure 4-3 Complete Activation Initiated by TE

When initiating an activation from the terminal side, the LT must be in the DEACTIVATED state. For a TE initiated activation to be successful the downstream LT C/I-code must be DC. This is not the case if the DEACTIVATED state has been entered from the RESET or TEST state (the last code is DR in this case).

	NT IOM®-2		LT IOM®-2			
<———	C/I DC	(1111_B)	C/I DC	(1111_B)	<———	; Initial state is “Deactivated”
———>	C/I DI	(1111_B)	C/I DI	(1111_B)	———>	
----->	**C/I TIM**	**(0000_B)**				; Start IOM®-clocks
<———	C/I PU	(0111_B)				; U-transceiver is in power-up
----->	**C/I AR**	**(1000_B)**				
----->	**TIM release**[2)]					; Start activation
<———	C/I DC	(1111_B)	C/I AR	(1000_B)	———>	; Activation proceeds
			C/I ARM	(1001_B)	———>	; :
<———	C/I AR	(1000_B)	C/I UAI	(0111_B)	———>	; :
----->	**C/I AI**	**(1100_B)**				; Confirm that terminal is ; active
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	; Activation complete

4.3.4 Complete Deactivation

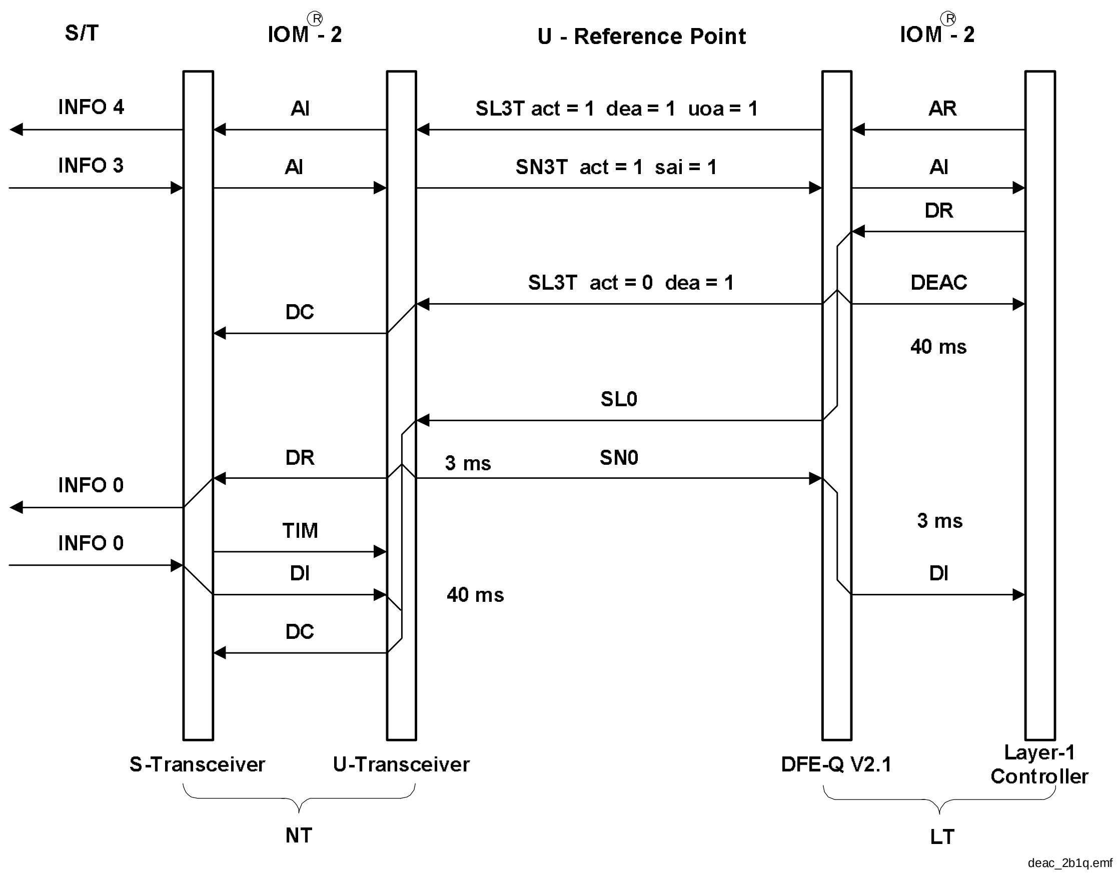


Figure 4-4 Complete Deactivation

Deactivating the U-interface can be initiated only by the exchange. A deactivation can be started when the device is in the states LINE ACTIVE, PEND. TRANSPARENT or TRANSPARENT.

	NT IOM®-2		LT IOM®-2			
			C/I DR	(0000_B)	<———	; Start deactivation
<———	C/I DR	(0000_B)	C/I DEAC	(0001_B)	———>	; Deactivation proceeds
			C/I DI	(1111_B)	———>	; Deactivation complete on
						; LT
———>	C/I DI	(1111_B)				; Power down NT
<———	C/I DC	(1111_B)				; Deactivation complete on
						; NT

4.3.5 Partial Activation (U Only)

If the U-transceiver is only partially activated the S-interface remains deactivated. When the partial activation is initiated by the LT-side, the exchange has two options:

- First, in case the C/I-command DC is not issued after the partial activation is complete, the exchange has to issue AR before a terminal initiated complete activation request is accepted. This allows the exchange to retain full control, even in case of terminal initiated activation requests.
- Secondly the exchange can issue DC after UAI has been received. This allows the terminal to activate the S-interface independently of the exchange. In this case the exchange has no control of the S-interface activation procedure.

The NT U-transceiver is in the “Synchronized 1” state after a successful partial activation. On DOUT the C/I-message “DC” as well as the LT-user data is sent.

While the C/I-messages “DI” (1111_B) or “TIM” (0000_B) are received on DIN, the U-transceiver will transmit “SAI” = (0) upstream. Any other code results in “SAI” = (1) to be sent. On the U-interface the signal SN3 (i.e. 2B + D = (1)) will be transmitted continuously regardless of the data on DIN.

The LT will transmit all user data transparently downstream (signal SL3T). In case the last C/I-command applied to DIN was “UAR”, the LT retains activation control when an activation request comes from the terminal (confirmation with C/I = “AR” required. With C/I “DC” applied on DIN, TE initiated activations will be completed without the necessity of an exchange confirmation.

	NT IOM®-2		LT IOM®-2			
<———	C/I DC	(1111_B)	C/I DC	(1111_B)	<———	; Initial state is “Deactivated”
———>	C/I DI	(1111_B)	C/I DI	(1111_B)	———>	
			C/I UAR	**(0111_B)**	**<–––––**	; Start partial activation
<———	C/I PU	(0111_B)	C/I AR	(1000_B)	———>	; Activation proceeds
<———	C/I DC	(1111_B)	C/I ARM	(1001_B)	———>	; :
			C/I UAI	(0111_B)	———>	; Partial activation complete
			[C/I DC	(1111_B)]	<———	; Exchange retains no ; control of S-interface activation

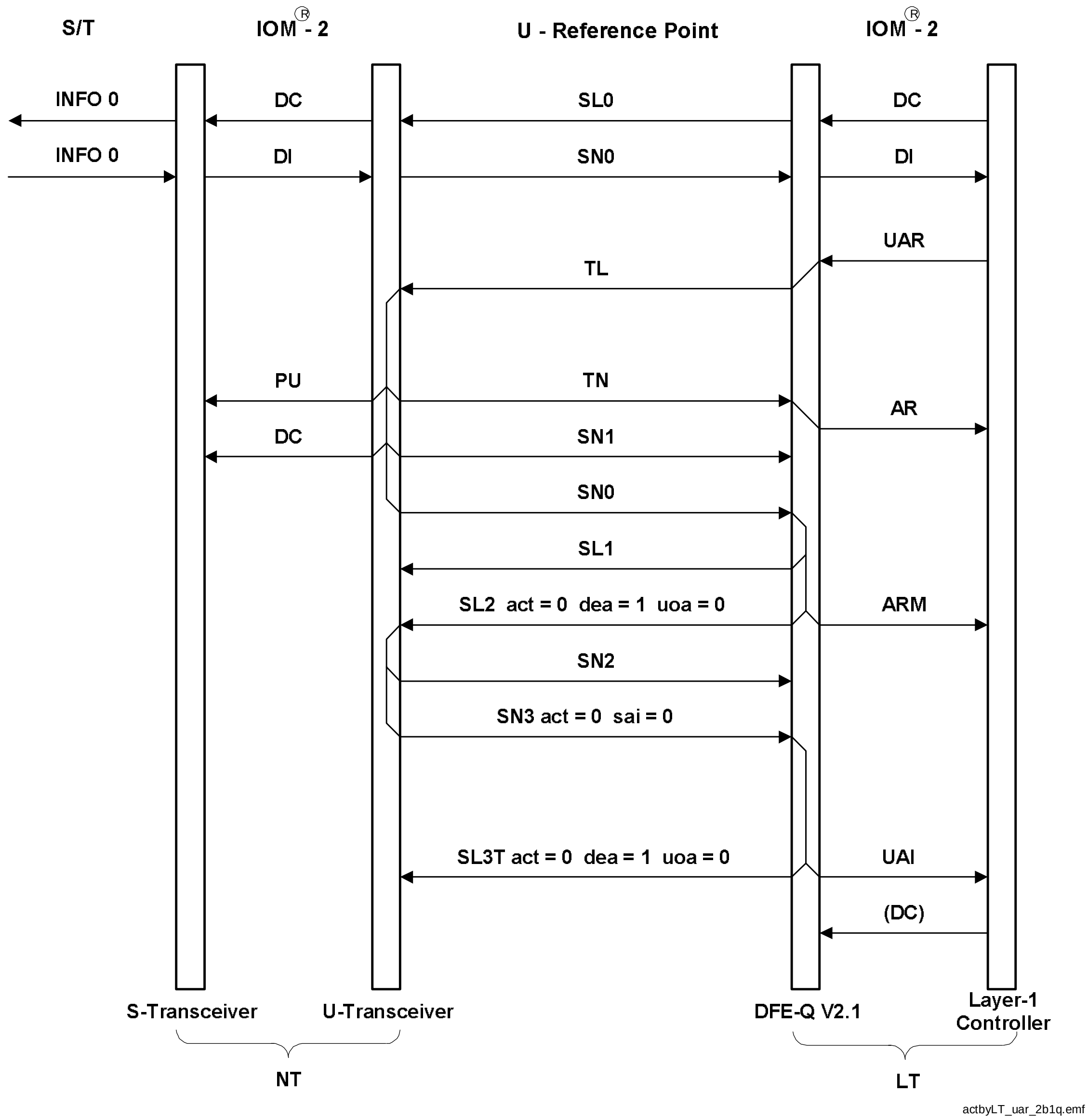


Figure 4-5 U Only Activation

4.3.6 Activation Initiated by LT with U Active

When U is already active, the S-interface can be activated either by the exchange or by the terminal. The first case is described here, the second in the next section.

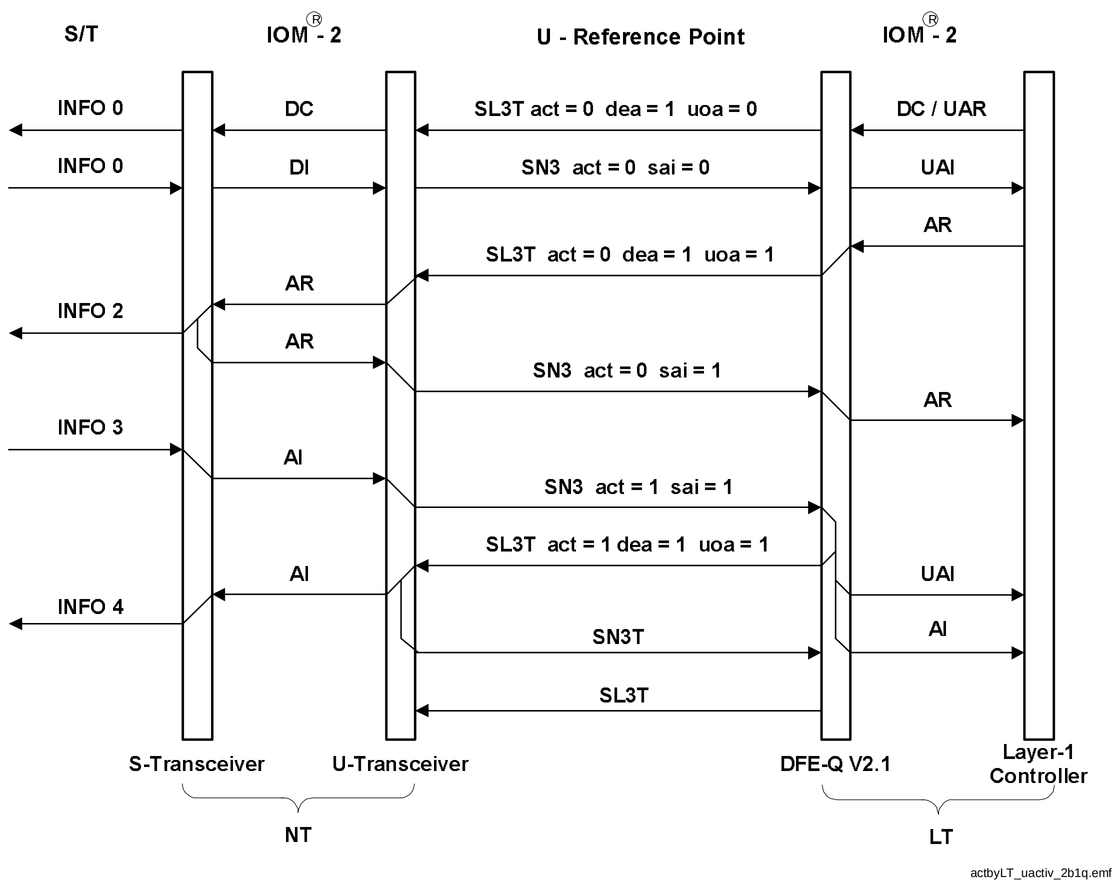


Figure 4-6 LT Initiated Activation with U-Interface Active

The S-interface is activated from the exchange with the command “AR”. Bit “UOA” changes to (1) requesting S-interface activation.

	NT IOM®-2		LT IOM®-2			
<———	C/I DC	(1111_B)	C/I UAR [DC]		<———	; U only is activated
———>	C/I DI	(1111_B)	C/I UAI	(0111_B)	———>	; [exchange retains no ; control]
			C/I AR	**(1000_B)**	**<–––––**	; Start complete activation
<———	C/I AR	(1000_B)				
–––––>	**C/I AR**	**(1100_B)**				
			C/I AR	(1000_B)	———>	; Activation proceeds
–––––>	**C/I AI**	**(1100_B)**				; Confirm that terminal is ; active
			C/I UAI	(0111_B)	———>	
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	; Activation complete

4.3.7 Activation Initiated by TE with U Active

When the terminal requests to activate the S-interface (U-interface already active) two cases can occur:

In the first case the exchange has retained control over the S-interface activation. Then S-activation can proceed only after the explicit permission by the exchange with AR. This situation is discussed in this section under “case 1”.

In the second case the exchange is not requested to send AR in order to continue activation. This situation is described in “case 2” of this section.

The TE initiates complete activation with INFO 1 leading to “SAI” = (1). Case 1 requires the exchange side to acknowledge the TE-activation by sending C/I = “AR”, Case 2 activates completely without any LT-confirmation. The TE recognizes no difference between the two types, the procedure on NT-side consequently is identical in both cases.

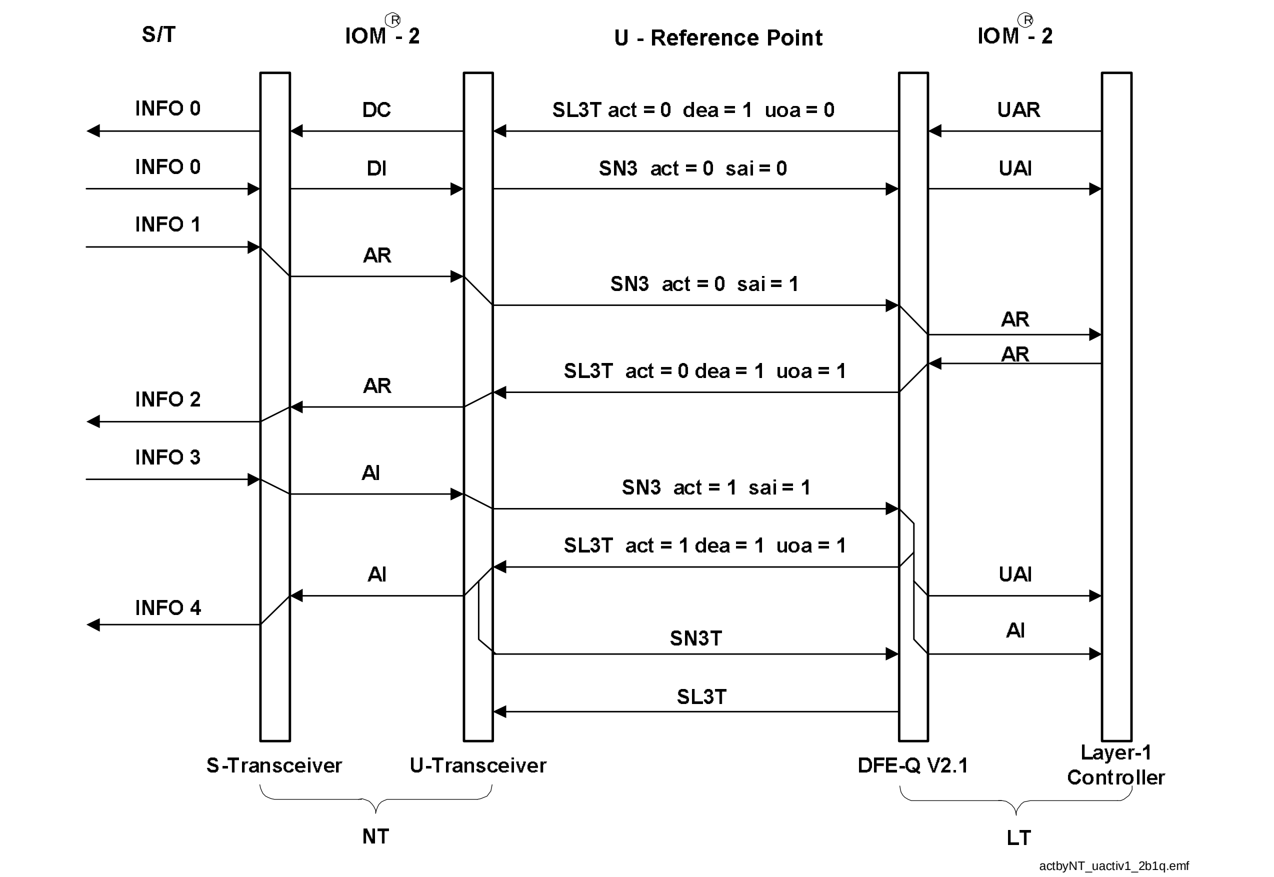


Figure 4-7 TE-Activation with U Active and Exchange Control (case 1)

Case 1 (controlled by exchange)

	NT IOM®-2		LT IOM®-2			
<———	C/I DC	(1111_B)	C/I UAR	(0111_B)	<———	; U only is activated
———>	C/I DI	(1111_B)	C/I UAI	(0111_B)	———>	
----->	**C/I AR**	**(1000_B)**				; Terminal requests ; activation
			C/I AR	(1000_B)	———>	; Exchange is notified of ; request
			C/I AR	**(1000_B)**	**<-----**	; Exchange permits ; S-activation
<———	C/I AR	(1000_B)				
----->	**C/I AI**	**(1100_B)**				; Confirm that terminal is ; active
			C/I UAI	(0111_B)	———>	
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	; Activation complete

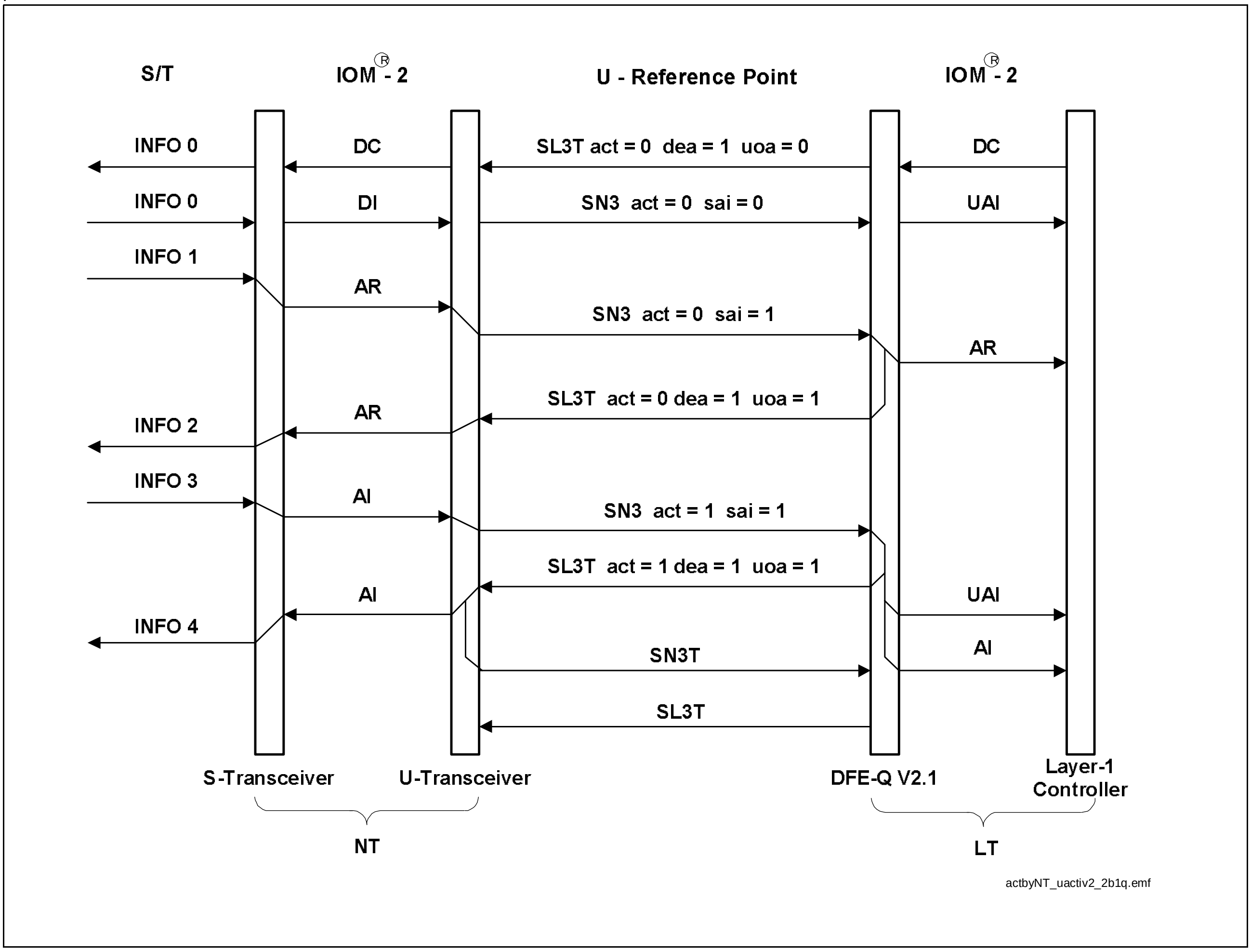


Figure 4-8 TE-Activation with U Active and no Exchange Control (case 2)

Case 2 (no control by exchange)

	NT IOM®-2		LT IOM®-2			
<———	C/I DC	(1111_B)	C/I DC		<———	; U only is activated
———>	C/I DI	(0011_B)	C/I UAI	(0111_B)	———>	
----->	**C/I AR**	**(1000_B)**				; Terminal requests
						; activation
			C/I AR	(1000_B)	———>	; Exchange is notified of
<———	C/I AR	(1000_B)				; proceeding S-activation
----->	**C/I AI**	**(1100_B)**				; Confirm that terminal is
						; active
			C/I UAI	(0111_B)	———>	
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	; Activation complete

4.3.8 Deactivating S/T-Interface Only

The following shows the procedure for deactivating the S-interface only while leaving the U-interface active. Deactivation of the S-interface only is initiated from the exchange by setting the “UOA” bit = (0).

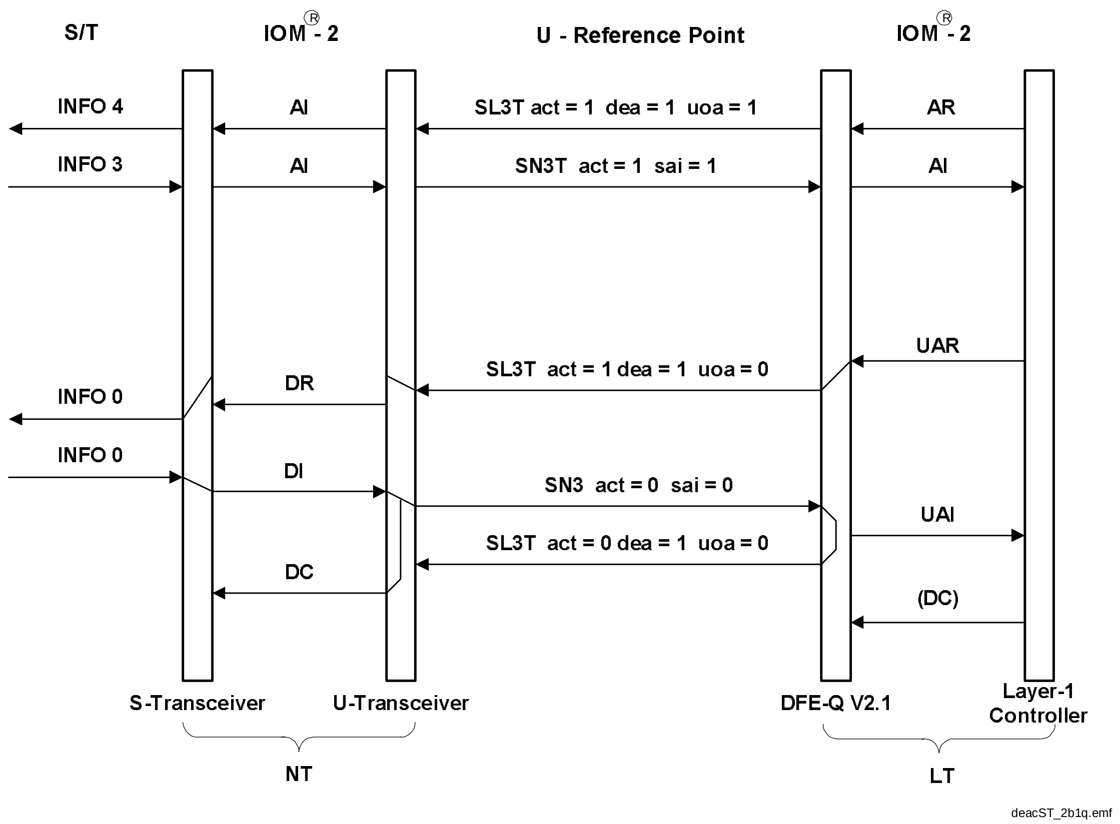


Figure 4-9 Deactivation of S/T Only

	NT IOM®-2		LT IOM®-2			
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	; Initial state: layer 1 activated
———>	C/I AI	(1100_B)	C/I AR	(1000_B)	<———	
<———	C/I DR	(0000_B)	**C/I UAR**	**(0111_B)**	**<-----**	; Deactivate S-interface only
----->	**C/I DI**	**(1111_B)**	C/I UAI	(0111_B)	———>	; S-interface is deactivated
<———	C/I DC	(1111_B)	[C/I DC	(1111_B)]	<———	; Exchange retains no control

4.4 Maintenance and Test Functions

This chapter summarizes all features provided by the DFE-Q V2.1 to support maintenance functions and system measurements. Three main groups may be distinguished:

– maintenance functions to close and open test loopbacks
– features facilitating the recognition of transmission errors
– test modes required for system measurements

The next sections describe how these test and maintenance functions are implemented and used in applications.

4.4.1 Test Loopbacks

Test loopbacks are specified by the national PTTs in order to facilitate the location of defect systems. Four different loopbacks are defined. The position of each loopback is illustrated in **Figure 4-10**.

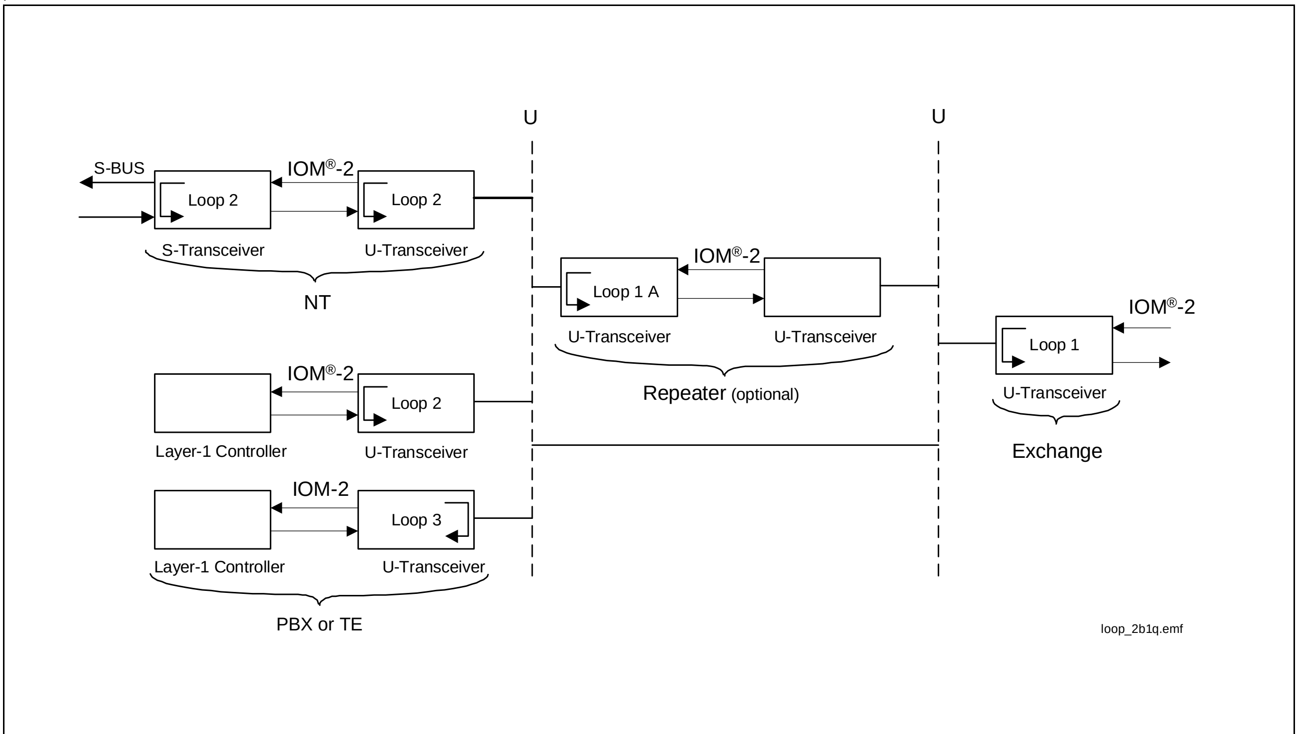


Figure 4-10 Test Loopbacks

Loopbacks #1, #1A and #2 are controlled by the exchange. Loopbacks #1 is closed by the DFE-Q V2.1 itself whereas loopbacks #1A and #2 are remote controlled and closed in the repeater and NT. Loopback #3 is closed and controlled by the terminal.

All four loopback types are transparent. This means all bits that are looped back will also be passed onwards in the normal manner. The propagation delay of B- and D-channel data is identical in all loopbacks.

Beside the remote loopback stimulation via the EOC- and MON-channel the DFE-Q V2.1 features also direct loopback control via its register set. The next sections describe how these loopbacks are closed and opened using C/I- and MON-commands.

4.4.1.1 Analog Loopback (No.1)

Loopback #1 is closed by the DFE-Q V2.1 as near to the U-interface as possible. For this reason it is called analog loopback. The 6 dB range attenuation in the receive path is active.

Transparent

All analog signals will still be passed on to the U-interface. As a result the NT-station will be activated as well. Only the internal loopback signal is processed. Signals on the receive pins are ignored. For this reason the device stays in the “Line Active” state (upstream ACT-bit cannot be received).

Loopback Activation

Before an analog loopback is closed the device should have been reset and put into state “Deactivated” first before Loop-back #1 is closed. Then the C/I-command ARL (activation request loopback) must be applied continuously as long as the loopback is requested.

Loopback Deactivation

In order to open an analog loopback again the device should be reset by applying the C/I-command RES (or by pin reset). This ensures that the echo coefficients and equalizer coefficients will converge correctly when activating the next time.

The example below demonstrates the control of loopbacks #1.

	NT IOM®-2		**LT IOM®-2**			
<———	C/I DC	(1111B)	C/I DI	(1111B)	———>	
			C/I ARL	**(1010B)**	<———	; Close loopback #1
<———	C/I AR	(1000B)	C/I AR	(1000B)	———>	; Activation proceeds in NT
			C/I ARM	(1001B)	———>	; and LT
			C/I UAI	(0111B)	———>	; Activation complete, ; #1 closed
			C/I RES	**(0001B)**	<———	; Open loopback #1, ; reset the U-transceiver

4.4.1.2 Loopback No.2 - Overview

For loopback #2 several alternatives exist. Both the type of loopback and the location may vary. Three loopback types belong to the loopback #2 category:

- Complete loopback, in the NT U-transceiver or in a downstream device
- B1-channel loopback, always performed in the NT U-transceiver
- B2-channel loopback, always performed in the NT U-transceiver

All loop variations are closed as near to the IOM®-interface as possible.

Complete Loopback

The complete loopback comprises both B-channels and the D-channel. It may be closed either in the U-transceiver itself or in a downstream device. The propagation delay of B and D-channel data is identical.

Single Channel Loopback

Single channel loopbacks are always performed within the U-transceiver. In this case the digital data of DOUT will be directly fed back into DIN. This also applies if the complete loopback is closed in the U-transceiver.

Normally loopback #2 is controlled from the exchange by the MON-0 commands LBBD, LB1 and LB2. The loop requests are recognized and executed automatically by the NT U-transceiver if automode is selected.

All loopback functions are latched in the NT. This allows channel B1 and channel B2 to be looped back simultaneously. All loopbacks are opened again upon reception of the EOC command RTN.

Transparency

Data sent downstream will be passed on transparent independently of closed loopbacks.

4.4.1.3 Loopback No.2 - Complete Loopback

Upon receiving the EOC-command LBBD in EOC automode, the NT U-transceiver does not close the loopback immediately. Because the intention of this loopback is to test the complete NT, the U-transceiver passes the complete loopback request on to the next downstream device (e.g. S-Transceiver). This is achieved by issuing the C/I-code AIL in the “Transparent” state or C/I = ARL in states different than “Transparent”.

If the downstream device is not able to close the complete loopback, a MON-8-message LBBD may be returned to the NT U-transceiver. This in turn will close the complete loopback within the NT U-transceiver itself (B1 + B2 + D-channels).

All remaining IOM®-information (monitor, C/I-channel as well as the bits MR and MX) are still read from the IOM®-2-interface. For this reason it is still possible for a layer-2 device to deactivate the NT despite the fact that the loopbacks are controlled by the exchange.

Figure 4-11 illustrates these two options.

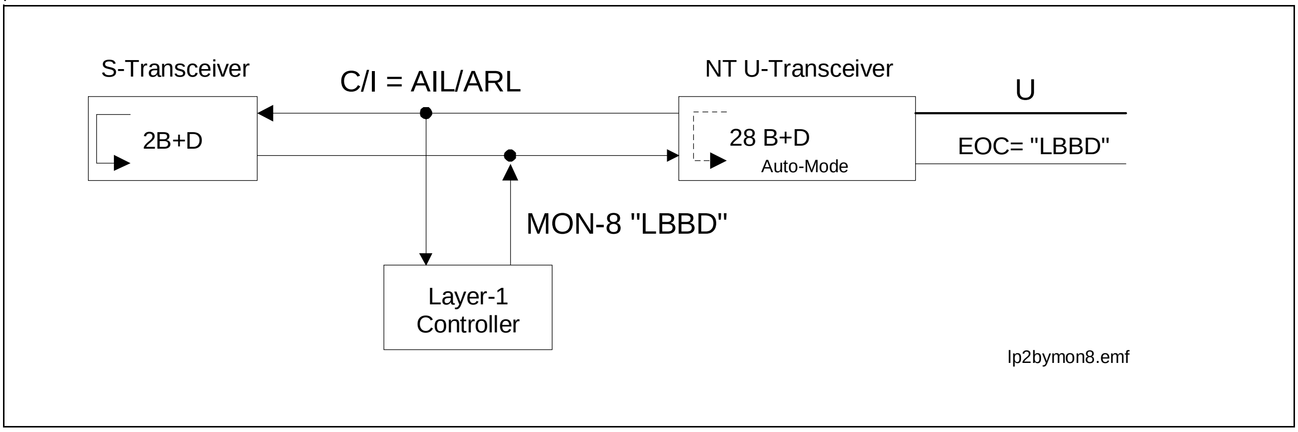


Figure 4-11 Complete Loopback Options in the NT

The complete loopback is opened again by the NT U-transceiver (e.g. IEC-Q, PEB 2091) when the EOC command RTN or the MON-8-command NORM is received. No reset is required for loopback #2. The line stays active and is ready for data transmission. The typical procedure for closing and opening a complete loopback is demonstrated in the examples below. There the LT is always operated in EOC automode.

Complete Loopback in EOC Automode (NT-side):

	NT IOM®-2		**LT IOM®-2**			
			C/I AR	(1000_B)	<——	; U-interface is activated
<——	C/I AR	(1000_B)	C/I UAI	(0111_B)	——>	; without terminal
						; confirmation
(——>	C/I AI	(1100_B)				; or with

	NT IOM®-2		LT IOM®-2			
<——	C/I AI	(1100_B)	C/I AI	(1100_B)	——>	; terminal confirmation)
			MON-0 LBBD	**(50_H)**	**<----**	; Close complete loop (EOC)
<——	C/I AIL	(1110_B)				; Request for downstream
<——	MON-0 LBBD	(50_H)				; device to close complete ; loopback
			MON-0 LBBD	(50_H)	——>	; Receive acknowledgment
---->	**MON-8 LBBD**	**($F1_H$)**				; If downstream device can't ; close, loop is closed in the NT U-transceiver
			MON-0 RTN	**(FF_H)**	**<----**	; Open all loopbacks
<——	MON-0 RTN	(FF_H)				; All loopbacks opened
			MON-0 RTN	(FF_H)	——>	; Receive acknowledgment

Complete Loopback in EOC Transparent Mode (NT side):

	NT IOM®-2		LT IOM®-2			
——>	C/I AI	(1100_B)	C/I AR	(1000_B)	<——	; U-interface is activated
<——	C/I AI	(1100_B)	C/I AI	(1100_B)	——>	
			MON-0 LBBD	**(50_H)**	<——	; Close complete loop (EOC)
<——	MON-0 LBBD	(50_H)				; Request passes ; transparently the NT U-transceiver
--->	**MON-0 LBBD**	**(50_H)**	MON-0 LBBD	(50_H)	——>	; Transmit acknowledgment
--->	**MON-8 LBBD**	**($F1_H$)**				; Close complete loop in IEC
<——	MON-0 RTN	(FFH)	**MON-0 RTN**	**(FF_H)**	<——	; Request to open all loops
--->	**MON-0 RTN**	**(FF_H)**	MON-0 RTN	(FF_H)	——>	; Receive acknowledgment
--->	**MON-8 NORM**	**(FF_H)**				; Open all loopbacks

4.4.1.4 Loopback No.2 - Single Channel Loopbacks

Single channel loopbacks are always performed directly in the NT U-transceiver. No difference between the B1-channel and the B2-channel loopback control procedure exists. They are therefore discussed together.

- In **EOC automode** the B1-channel is closed by the EOC-command LB1. LB2 causes the channel B2 to loopback. Because these functions are latched, both channels may be looped back simultaneously by sending first the command to close one channel followed by the command for the remaining channel.
- In **EOC transparent mode** single channels are closed by the corresponding MON-8-commands.

Single channel loopbacks are resolved in the same manner as described for the complete loopback, either by the EOC command RTN or by the MON-8 command NORM. The NT may be deactivated while single loopbacks are closed.

Typical procedures for closing and opening single channel loopbacks are given in the examples below. There the LT is always operated in EOC automode.

Single-Channel Loopback in EOC Automode (NT-side):

	NT IOM®-2		**LT IOM®-2**			
——>	C/I AI	(1100_B)	C/I AR	(1000_B)	<——	; U-interface is activated
<——	C/I AI	(1100_B)	C/I AI	(1100_B)	——>	
			MON-0 LB1	**(51_H)**	<——	; Close B1 loop (EOC)
<——	MON-0 LB1	(51_H)				; Loop B1 closed
			MON-0 LB1	(51H)	——>	; Receive acknowledgment
			MON-0 LB2	**(52_H)**	<——	; Close B2 loopback (EOC)
<——	MON-0 LB2	(52_H)				; Loop-back B1 and B2 ; closed
			MON-0 LB2	(52_H)	——>	; Receive acknowledgment
			MON-0 RTN	**(FF_H)**	<——	; Open all loopbacks
<——	MON-0 RTN	(FF_H)				; All loopbacks opened
			MON-0 RTN	(FF_H)	——>	; Receive acknowledgment

Single-Channel Loopback in EOC Transparent Mode (NT-side):

	NT IOM®-2		LT IOM®-2			
——>	C/I AI	(1100_B)	C/I AR	(1000_B)	<——	; U-interface is activated
<——	C/I AI	(1100_B)	C/I AI	(1100_B)	——>	
			MON-0 LB1	**(51_H)**	<——	; Close B1 loop (EOC)
<——	MON-0 LB1	(51_H)				; Request passes IEC ; transparent
–––>	**MON-0 LB1**	**(51_H)**	MON-0 LB1	(51_H)	——>	; Transmit acknowledgment
–––>	**MON-8 LB1**	**($F4_H$)**				; Close B1 loop in IEC
			MON-0 LB2	**(52_H)**	<——	; Close B2 loop (EOC)
<——	MON-0 LB2	(52_H)				; Request passes IEC ; transparent
–––>	**MON-0 LB2**	**(52_H)**	MON-0 LB2	(52_H)	——>	; Transmit acknowledgment
–––>	**MON-8 LB2**	**($F2_H$)**				; Close B2 loop in IEC ; B1 and B2 closed
			MON-0 RTN	**(FF_H)**	<———	; Request to open all loops
–––>	**MON-0 RTN**	**(FF_H)**	MON-0 RTN	(FF_H)	———>	; Receive acknowledgment
–––>	**MON-8 NORM**	**(FF_H)**				; Open all loopbacks

4.4.1.5 Local Loopbacks Featured By Register LOOP

Besides the standardized remote loopbacks the DFE-Q V2.1 features additional local loopbacks for enhanced test and debugging facilities. The local loopbacks that are featured by the internal register LOOP are shown in **Figure 4-12**. They are closed in the DFE-Q V2.1 itself and can be activated regardless of the current operational status.

By register LOOP it can be configured whether the digital local looback is closed only for the B1 and/or B2 or for all ISDN-BA channels and whether the loopback is closed towards the IOM®-2 interface or towards the U-Interface.

By default the loopbacks are set to transparent mode. In transparent mode the data is both passed on and looped back. In non-transparent mode the data is not forwarded but substituted by 1s (idle code).

Besides the loopbacks in the system interface a further digital loopback, the Framer/ Deframer loopback, is provided. It allows to test all digital functions of the 2B1Q U-transceiver besides the signal processing blocks.

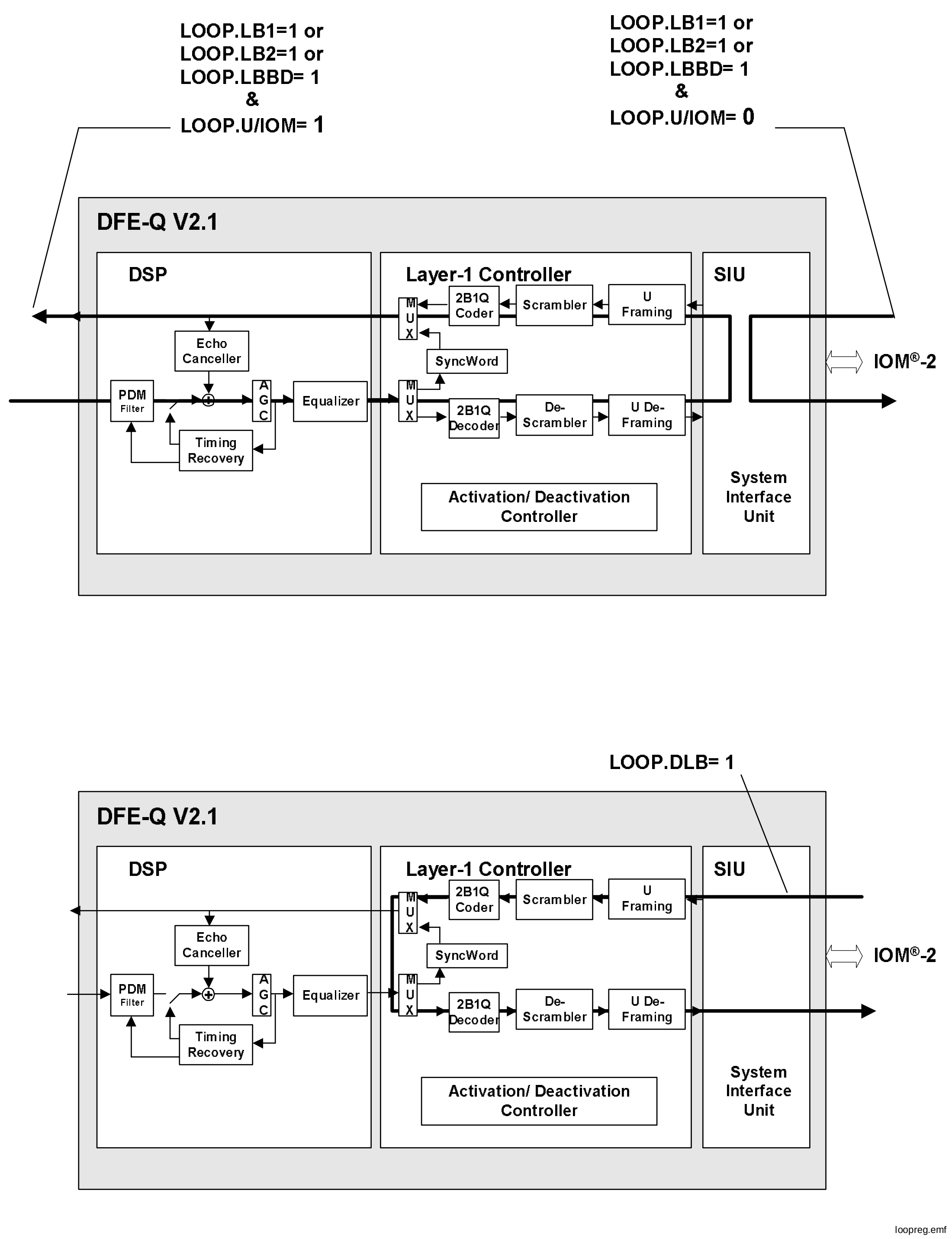


Figure 4-12 Loopbacks Featured by Register LOOP

4.4.2 Bit Error Rate Counter

For bit error rate monitoring the DFE-Q V2.1 features a 16-bit Bit Error Rate counter (BERC) per line. The function is channel selective. The user can direct that the measurement is performed only for the B1 or for the B2 or for the B1-, B2- and the D-channel. Prerequisite is that the corresponding loop #2 of the addressed channel(s) has been closed on the NT side before by an EOC command.

The measurement is initiated by the two BER control bits in the TEST register. As soon as the BER function is enabled zeros are sent in the selected channel(s) and incoming ones are counted until the BER function has been disabled again by the user.

4.4.3 Block Error Counters

The DFE-Q V2.1 provides internal counters for far-end and near-end block errors. This allows a comfortable surveillance of the transmission quality on the U-interface. In addition MON-messages indicate the occurrence of near-end errors, far-end errors and the simultaneous occurrence of both error types.

A block error is detected each time when the calculated checksum of the received data does not correspond to the control checksum transmitted in the successive superframe. One block error thus indicates that one U-superframe has not been transmitted correctly. No conclusion with respect to the number of bit errors is therefore possible.

The following two sections describe the operation of near and far-end block error counters as well as the commands available to test them.

4.4.3.1 Near-End and Far-End Block Error Counter

A near-end block error (NEBE) indicates that the error has been detected in the receive direction (i.e. NEBE = NT => LT error). Each detected NEBE-error increments the 8-bit NEBE-counter. The NEBE counter stops at its maximum value FF_H and does not overflow.

The current value of the NEBE counter can be read by the MON-8-command RBEN. The response comprises two bytes: the first byte always indicates that a MON-8-message is replied (80_H), the second represents the counter value (00_H) … (FF_H). Each read operation resets the counter to (00_H).

A far-end block error identifies errors in transmission direction (i.e. FEBE = LT => NT error). FEBE errors are processed in the same manner as NEBE-errors. The FEBE counter is read and reset by the MON-8-command RBEF.

Near-End Errors - Summary:

- Definition

A near-end block error (NEBE) indicates errors that occurred in the receive direction, i.e. an detected error during transmission from NT to LT. A near-end block error is considered detected when the calculated check-sum of the received U-superframe does not correspond to the check-sum sent in the following U-superframe.

- Indications

Each detected NEBE causes the NEBE counter to be incremented (maximum count is FF_H, no overflow). The U-maintenance bit "FEBE" is set to zero in the next U-superframe (for a duration of one superframe).

- Read Out and Reset

The counter value may be read out by the MON-8-command RBEN

MON-8				RBEN				Read Block Errors Near-end							
1	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1

MON-8				ABEN				Answer Block Errors Near-end							
1	0	0	0	0	0	0	0	C7	C6	C5	C4	C3	C2	C1	C0

C0 … C7: 8-bit counter value

Each read operation resets the NEBE-counter to 00_H. The counter is also reset in all states except the following ones:

- Line Active
- Pend. Transparent
- Transparent
- S/T Deactivated

Far End Errors - Summary:

- Definition

A far-end block error (FEBE) indicates errors that occurred in the transmit direction, i.e. an detected error during transmission from LT to NT. A far-end block error is detected when the U-maintenance bit “FEBE” is set to zero.

- Indications

Each detected FEBE will cause the FEBE-counter to be incremented (maximum count is FF_H, no overflow)

- Read Out and Reset

The counter value may be read out by the MON-8-command RBEF

MON-8 **RBEF**

1	0	0	0	0	0	0	0

Read Block Errors Far-end

1	1	1	1	1	0	1	0

MON-8 **ABEN**

1	0	0	0	0	0	0	0

Answer Block Errors Far-end

C7	C6	C5	C4	C3	C2	C1	C0

C0 … C7: 8-bit counter value

Each read operation resets the FEBE-counter to 00_H. The counter is also reset in all states except the following ones:

- Line Active
- Pend. Transparent
- Transparent
- S/T Deactivated

The following section illustrates how block error counters are tested.

4.4.3.2 Testing Block Error Counters

Figure 4-13 illustrates how near- and far-end block error counters can be tested. Transmission errors are simulated with artificially corrupted CRCs. With two commands the cyclic redundancy checksum can be inverted. A third command offers the possibility to invert single FEBE-bits.

- **MON-8 CCRC** causes the DFE-Q V2.1 to permanently transmit inverted CRCs. With CCRC issued on LT-side, near-end block errors will be observed at the NT and far-end errors are noticed at the LT.
- **MON-0 RCC** requests the NT to send corrupt CRCs. Again the CRC will be permanently inverted. After issuing RCC (NT in EOC automode) near-end block errors will be registered on the LT-side.
- **MON-0 NCC** requests the NT to disable the NEBE-detection. However, the NCC command shows only effect if the NT U-transceiver operates in EOC automode. The different behavior of the NT U-transceiver is summarized below

Auto-mode	NEBE-detection stopped, no MON-1 NEBE messages and NEBE-counter disabled
Transparent mode	NEBE-detection enabled, MON-1-message NEBE issued and NEBE-counter enabled

- **MON-8 SFB** causes the DFE-Q V2.1 to invert single FEBE-bits. Because this command does not provoke permanent FEBE-bit inversion but sets only one FEBE-bit to (0) per SFB command it is possible to predict exactly the FEBE-counter value.
- **MON-0 RTN** and **MON-8 NORM** disable again activated test functions

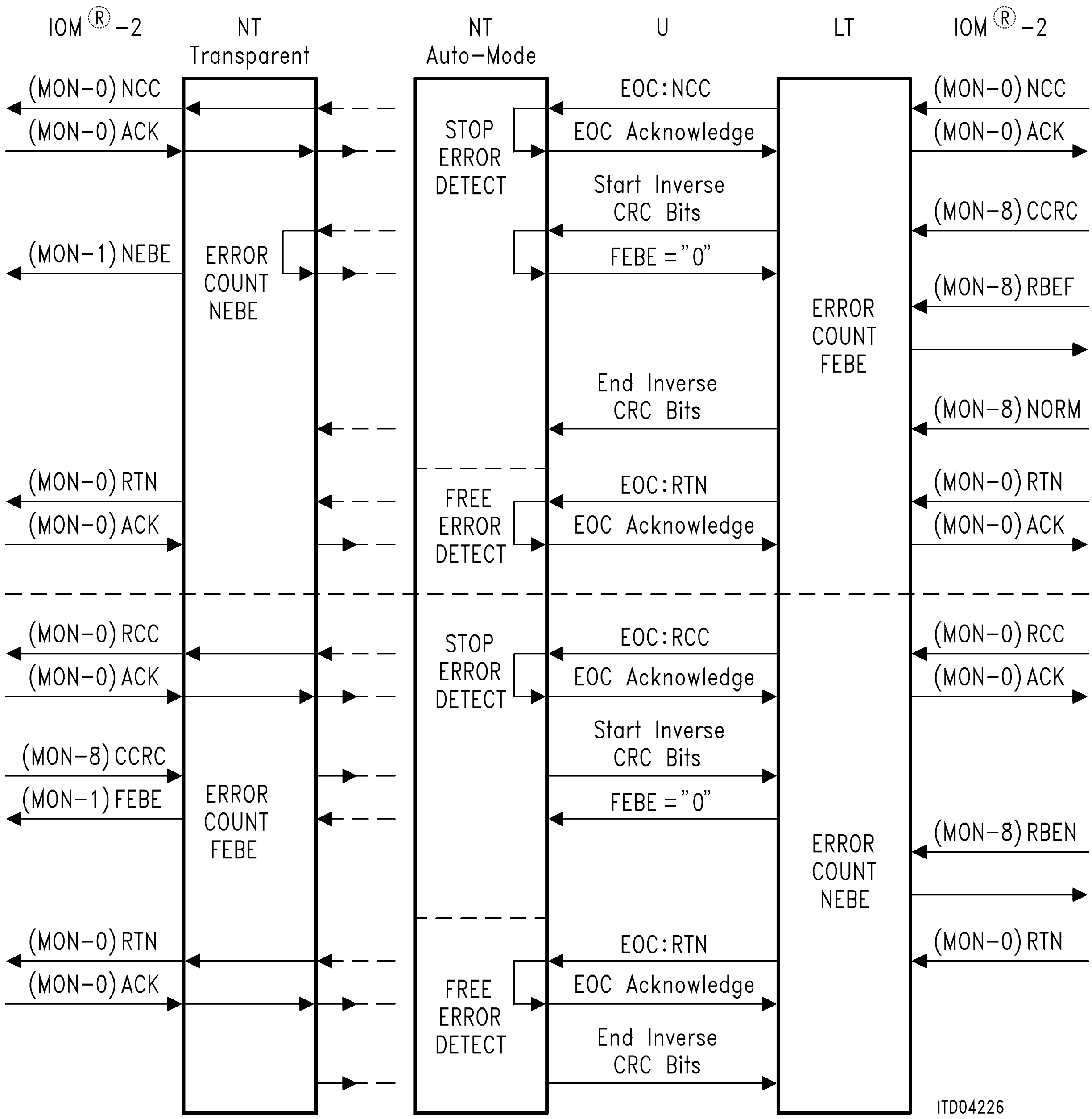


Figure 4-13 Block Error Counter Test

4.4.4 System Measurements

The DFE-Q V2.1 features dedicated test modes to enable and ease system measurements. How these test modes can be used to conduct the most frequently needed system measurements is described in the following sections.

4.4.4.1 Single-Pulses Test Mode (SSP)

In the send single pulses test mode the U-transceiver transmits on the U-interface alternating ± 3 pulses spaced by 1.5 ms. Two options exist for selecting the “Send-Single-Pulses” (SSP) mode:

– hardware selection: Pin-SSP= ’1’
– software selection: C/I code= SSP (0101_B)

Both methods are fully equivalent besides the fact that the HW selection impacts all line ports while the SW selection impacts only the chosen line. In SSP-mode the C/I-code transmitted by the DFE-Q V2.1 is DEAC.

The SSP-test mode is required for pulse mask measurements.

4.4.4.2 Data Through Mode (DT)

When selecting the data-through mode the DFE-Q V2.1 is forced directly into the “Transparent” state. This is possible from any state in the state diagram.

The Data-Through option (DT) provides the possibility to transmit a standard scrambled U-signal even if no U-interface wake-up protocol is possible. This feature is of interest when no counter station can be connected to supply the wake-up protocol signals.

As with the SSP-mode, two options are available.

– hardware selection: Pin-DT= ’1’
– software selection: C/I code= DT (0110_B)

Both methods are fully equivalent besides the fact that the HW selection impacts all line ports while the SW selection is channel selective..Note that the hardware selection offers in addition the option to initiate further actions via C/I-code (e.g. simultaneous stimulation of an analog loop-back by C/I ’ARL’).

The DT-mode is required for power spectral density and total power measurements.

4.4.4.3 Master Reset Mode

In the master reset mode the DFE-Q V2.1 does not transmit any signals. The chip is in RESET state. All echo canceller and equalizer coefficients are reset.

For measurements two methods are recommended in order to transfer the U-transceiver into the master reset mode:

– hardware selection: Pin-$\overline{\text{RES}}$= ’0’
– software selection: C/I-code= RES (0001_B)

Both alternatives are fully compatible besides the fact that the SW selection is channel selective. The C/I-code DEAC is output by the DFE-Q V2.1 in the RESET state.

The master reset test mode is used for return-loss measurements.

4.4.4.4 Pulse Mask Measurement

- Pulse mask is defined in ANSI T1.601 and ETSI TS 102 080
- U-interface has to be terminated with 135 Ω
- DFE-Q V2.1 is in Send Single Pulses test mode (C/I = 'SSP' or Pin SSP= '1')
- Measurements are done using an oscilloscope

4.4.4.5 Power Spectral-Density Measurement

- PSD is defined in ANSI T1.601 and ETSI TS 102 080
- U-interface has to be terminated with 135 Ω
- DFE-Q V2.1 is in Data Through test mode (C/I = 'DT' or Pin DT= '1')
- For measurements a spectrum analyzer is employed

4.4.4.6 Total Power Measurement

- Total power is defined in ANSI T1.601 and ETSI TS 102 080
- Total power must be between 13 dBm and 14 dBm
- U-interface has to be terminated with 135 Ω
- DFE-Q V2.1 is in Data Through test mode (C/I= 'DT' or Pin DT= '1')
- Measurements are done using an 80 kHz high-impedance low-pass filter and true RMS-voltmeter

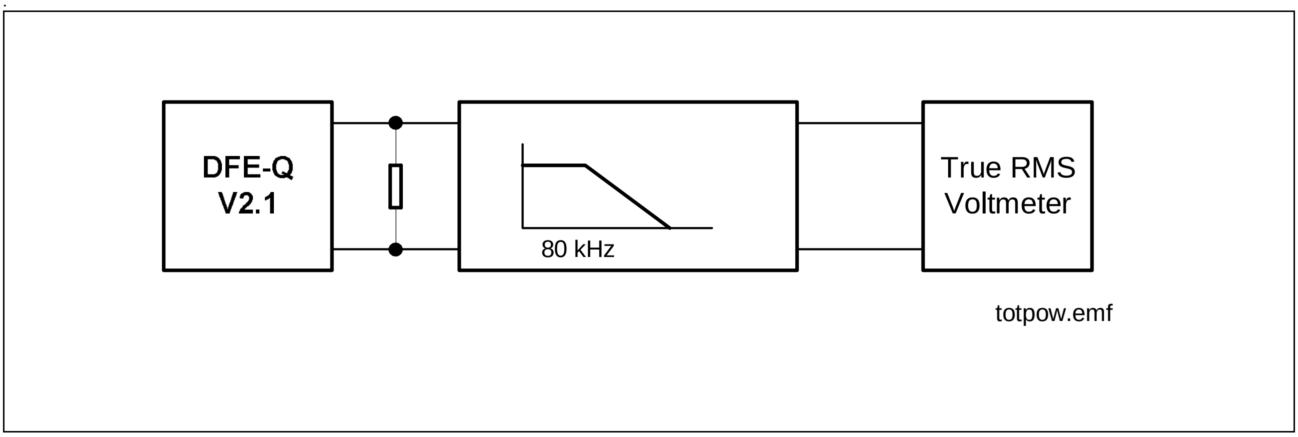


Figure 4-14 Total Power Measurement Set-Up

4.4.4.7 Return-Loss Measurement

- Return loss is defined in ANSI T1.601 and ETSI TS 102 080
- DFE-Q V2.1 is in RESET state (C/I = 'RES' or Pin $\overline{\text{RES}}$= '0')
- Measure complex impedance “Z” from 1 kHz – 200 kHz

– Calculate return loss with formula:
RL(dB) = 20log (abs((Z + 135) / (Z –135)))

4.4.4.8 Quiet Mode Measurement

– Quite mode is defined in ANSI T1.601 and ETSI TS 102 080
– DFE-Q V2.1 is in the “Reset” state (C/I = ’RES’ or Pin $\overline{\text{RES}}$= ’0’)
– Trigger and exit criteria have to be realized externally

4.4.4.9 Insertion Loss Measurement

– Insertion loss is defined in ANSI T1.601 and ETSI TS 102 080
– DFE-Q V2.1 is in Data Through test mode (C/I = ’DT’ or Pin DT= ’1’)
– Trigger and exit criteria have to be realized externally

4.4.5 Retrieving DSP Data

Beyond the test and maintenance features described in the previous sections, the DFE-Q V2.1 permits access to specific DSP data. Access is provided via the MON-12 protocol. The data transfer between the DSP and an external device is synchronized by two handshake signals, ’DATA_REQ’ and ’DATA_ACK’.

In the following text the technical term ’read’ stands for the process of sending a read request via the Monitor channel using the MON-12 protocol.

DSP Data Exchange via Handshake Signals

The handshake signal DATA_REQ is accommodated at bit position 0 in register DSP_DREQ, the handshake signal DATA_ACK at bit position 0 in register DSP_DACK.

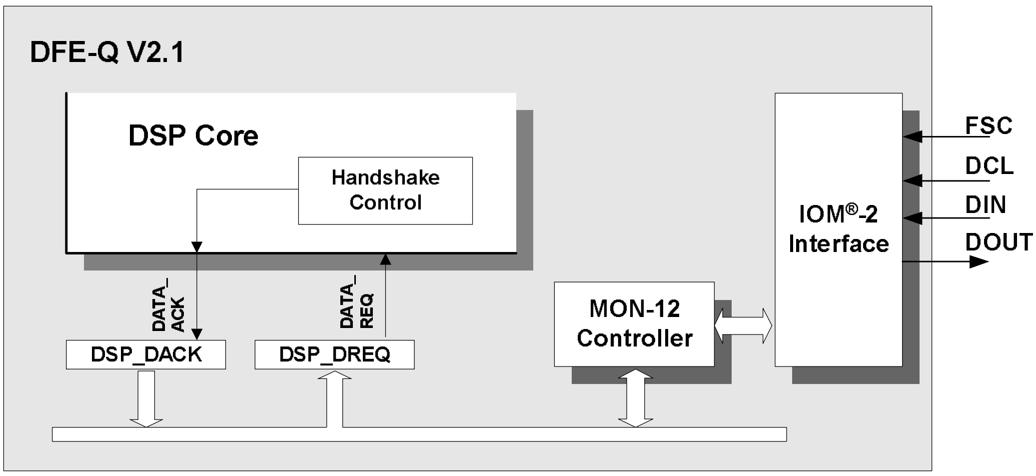


Figure 4-15 DSP Data Transfer Synchronization by Handshake Signals

Significance of DATA_REQ

Via DATA_REQ an external device is able to control the data exchange and to adapt the data rate to its needs.

- During a read access the layer-1 controller indicates with an active DSP_REQ signal (=’1’) that it requests new data.
- DATA_REQ set to ’0’ signals that the layer-1 controller is busy.

Significance of DATA_ACK

Signal DATA_ACK is controlled by the DSP.

- During a read access the DSP informs an external controller by DATA_ACK set to ’0’ that the data in the DSP Read Registers (DSP_RD1..3) has been updated.
- An active DATA_ACK bit (= ’1’) signals that the DSP is busy.

Below the single steps of the handshake protocol in the course of a read access is given.

Read direction (DSP -> Layer-1 controller):

1. Layer-1 controller polls if DATA_ACK bit is set to ’0’
2. Layer-1 controller signals its readiness for a read access by DATA_REQ= ’1’
3. DSP signals with DATA_ACK= ’0’ that the DSP_RD1..3 registers have been loaded
4. Layer-1 controller reads the DSP Read Registers, DSP_RD1..3

For subsequent read accesses this procedure has to be repeated

4.4.5.1 Reading Coefficient Values

By means of the DSP_RD1..3 registers it is possible to read coefficient values. The coefficient subsets of the various filter banks are addressable by the 3-bit DAT_TYP field in register DSP_CR2. Below the accessible coefficient clusters are listed:

'100'	Coefficient Set 1
'110'	Coefficient Set 2
'001'	Coefficient Set 3
'011'	Coefficient Set 4

Figure 4-16 shows the register structure that is provided for the access to coefficient values.

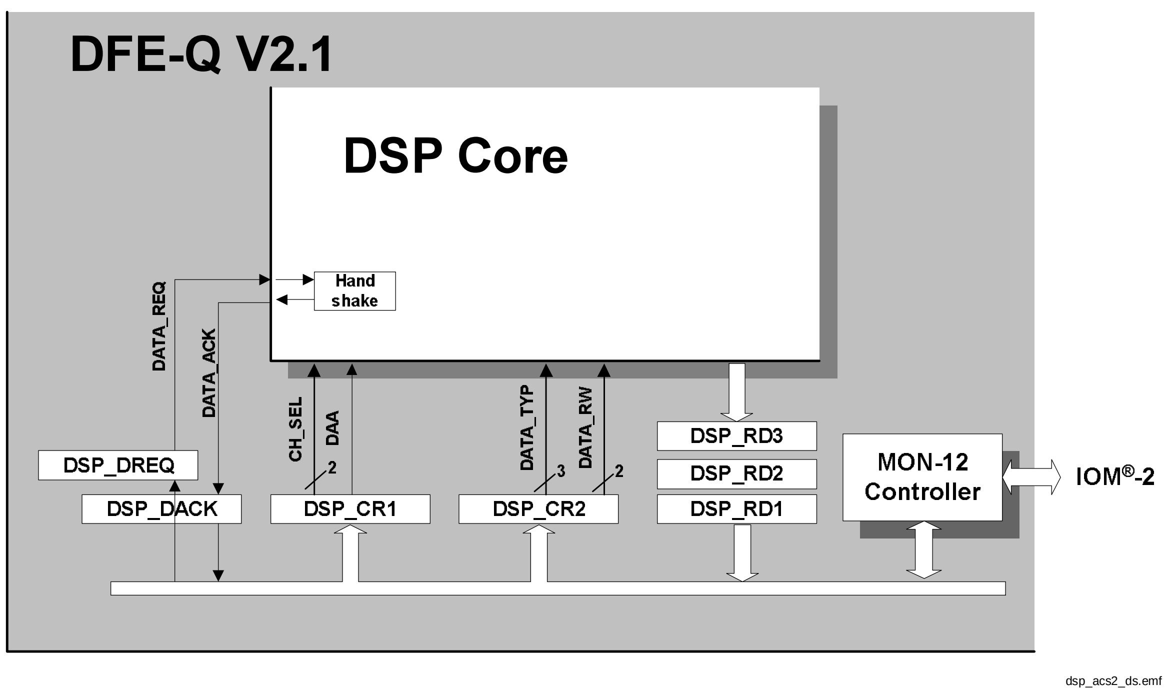


Figure 4-16 Provided DSP Registers for Access to Coefficient Data

To read out coefficient data the following programming sequence must be carried out

1. Select the addressed line port by CH_SEL in register DSP_CR1
2. Set DAA to ’1’ in register DSP_CR1. Thereby all coefficients are freezed.
3. Program the DSP Control Register No.2, DSP_CR2 as follows:
   - Select the proper coefficient type by DATA_TYP (e.g. coefficient set= ’100’)

     If the same coefficient set is repeatedly read out DSP_TYP must be set to another value and then reset again to the desired coefficient type. This is required to reset internal counters.

   - Set COM_MOD to ’1’ to enable the handshake mechanism
4. Trigger the read procedure by setting DATA_RW to ’01’ in register DSP_CR2.
5. Read out DSP_RD1..3 registers using either the handshake procedure as described in the chapter before.

4.4.6 Boundary Scan

The DFE-Q V2.1 provides a boundary scan support for a cost effective board testing. It consists of:

- Boundary scan according to IEEE 1149.1 specification
- Test Access Port controller (TAP)
- Five dedicated pins (TCK, TMS, TDI, TDO, $\overline{\text{TRST}}$)
- Pins $\overline{\text{TRST}}$, TDI and TMS are provided with an internal pullup resistor
- One 32-bit IDCODE register
- Pin $\overline{\text{TRST}}$ tied to low resets the Boundary Scan TAP Controller (recommended setting for normal operation if the Boundary Scan logic is not used)
- Instructions CLAMP and HIGHZ were added, instructions SSP and DT were removed in V2.1

Boundary Scan

All pins except the power supply pins, the "Not Connected" pins and the pins TDI, TDO, TCK, TMS, and $\overline{\text{TRST}}$ are included in the boundary scan chain. Depending on the pin functionality one, two or three boundary scan cells are provided.

Table 4-2 Boundary Scan Cells.

Pin Type	Number of Boundary Scan Cells	Usage
Input	1	input
Output	2	output, enable
I/O	3	input, output, enable

When the TAP controller is in the appropriate mode data is shifted into or out of the boundary scan via the pins TDI/TDO using the 6.25 MHz clock on pin TCK.

The pins are included in the following sequence in the boundary scan chain:

Boundary Scan Number TDI ––>	Pin Number	Pin Name	Type	Number of Scan Cells
1.	62	**DT**	I	1
2.	61	CLS3	I/O	3
3.	60	$\overline{\text{RES}}$	I	1
4.	59	AUTO	I	1
5.	58	**DARB**	I	1

Boundary Scan Number TDI -->	Pin Number	Pin Name	Type	Number of Scan Cells
6.	56	**SSP**	I	1
7.	55	**SLOT0**	I	1
8.	53	**SYNC**	I	1
9.	52	CLS2	I/O	3
10.	51	D3D	I/O	3
11.	50	D2D	I/O	3
12.	49	CRCON	I	1
13.	48	D1D	I/O	3
14.	47	D0D	I/O	3
15.	46	D3C	I/O	3
16.	45	**SLOT1**	I	1
17.	44	D2C	I/O	3
18.	43	D1C	I/O	3
19.	42	D0C	I/O	3
20.	40	D3B	I/O	3
21.	39	D2B	I/O	3
22.	37	D1B	I/O	3
23.	35	D0B	I/O	3
24.	34	D3A	I/O	3
25.	33	D2A	I/O	3
26.	32	**PUP**	I	1
27.	31	D1A	I/O	3
28.	30	D0A	I/O	3
29.	29	CLS0	I/O	3
30.	28	ST00	I	1
31.	27	ST01	I	1
32.	26	ST10	I	1
33.	24	ST11	I	1
34.	23	ST20	I/O	3
35.	21	ST21	I/O	3

Boundary Scan Number TDI –->	Pin Number	Pin Name	Type	Number of Scan Cells
36.	20	CLS1	I/O	3
37.	19	ST30	I/O	3
38.	18	ST31	I/O	3
39.	17	SDX	I/O	3
40.	16	**MTO**	I	1
41.	15	DOUT	I/O	3
42.	14	DIN	I	1
43.	13	FSC	I	1
44.	12	DCL	I	1
45.	11	PDM0	I	1
46.	10	PDM1	I	1
47.	8	PDM2	I	1
48.	7	PDM3	I	1
49.	5	SDR	I	1
50.	4	CL15	I	1

TAP Controller

The *Test Access Port* (TAP) controller implements the state machine defined in the JTAG standard IEEE 1149.1. Transitions on pin TMS cause the TAP controller to perform a state change. Before operation the TAP controller has to be reset by $\overline{\text{TRST}}$. According to the IEEE 1149 standard 7 instructions are executable. The instructions 'CLAMP' and 'HIGHZ' were added. Instructions 'SSP' and 'DT' are no more supported since its function is identical to that of the SSP and DT pins.

Table 4-3 TAP Controller Instructions:

Code	Instruction	Function
0000	EXTEST	External testing
0001	INTEST	Internal testing
0010	SAMPLE/PRELOAD	Snap-shot testing

Code	Instruction	Function
0011	IDCODE	Reading ID code
0100	CLAMP	Reading outputs
0101	HIGHZ	Z-State of all boundary scan output pins
1111	BYPASS	Bypass operation

EXTEST is used to examine the board interconnections.

When the TAP controller is in the state "update DR", all output pins are updated with the falling edge of TCK. When it has entered state "capture DR" the levels of all input pins are latched with the rising edge of TCK. The in/out shifting of the scan vectors is typically done using the instruction SAMPLE/PRELOAD.

INTEST supports internal chip testing.

When the TAP controller is in the state "update DR", all inputs are updated internally with the falling edge of TCK. When it has entered state "capture DR" the levels of all outputs are latched with the rising edge of TCK. The in/out shifting of the scan vectors is typically done using the instruction SAMPLE/PRELOAD.

0001 (INTEST) is the default value of the instruction register.

SAMPLE/PRELOAD provides a snap-shot of the pin level during normal operation or is used to preload (TDI) / shift out (TDO) the boundary scan with a test vector. Both activities are transparent to the system functionality.

IDCODE Register

The 32-bit identification register is serially read out via TDO. It contains the version number (4 bits), the device code (16 bits) and the manufacturer code (11 bits). The LSB is fixed to "1".

Version	Device Code	Manufacturer Code		Output
0001	0000 0000 0111 0010	0000 1000 001	1	--> TDO

Note: In the state "test logic reset" the code "0011" is loaded into the instruction code register.

CLAMP allows the state of the signals included in the boundary scan driven from the PEF 24911 to be determined from the boundary scan register while the bypass register is selected as the serial path between TDI and TDO. These output signals driven from the DFE-Q V2.1 will not change while CLAMP is selected.

HIGHZ sets all output pins included to the boundary scan path into a high impedance state. In this state, an in-circuit test system may drive signals onto the connections normally driven by the DFE-Q V2.1 outputs without incurring the risk of damage to the DFE-Q V2.1.

BYPASS, a bit entering TDI is shifted to TDO after one TCK clock cycle, e.g. to skip testing of selected ICs on a printed circuit board.

4.5 D-Channel Arbitration

In order to facilitate the simultaneous serving of multiple D-channels with one HDLC-controller (e.g. ELIC®), the DFE-Q V2.1 uses the EOC-Channel of the U-interface to forward the stop/go information to the terminal. A 6 ms cycle time is possible. As there is no bit in the U-interface frame structure reserved for this application, the EOC-channel is used to transmit the information. The function is as follows:

In LT-Mode with D-channel arbitration enabled (by pin DARB= '1') the C/I-command AR (1000_b) triggers the transmission of the associated EOC message 27_H to the NT side in the next available half superframe. This will only be done once.

The PEB 2091 IEC-Q V5.3 translates this message then into a continuous series of '1's. The '1's are output on the S/G-bit of the IOM®-2 channel or at pin S/G indicating that D-channel access is not provided.

As soon as the C/I-code AR is switched to C/I-code AI (1100_b), the EOC-message 25_H is sent to the NT-side and the S/G-bit will be set to '0' indicating access permission to the D-channel. **Figure 4-17** illustrates the relation of the C/I-code at DIN on LT-side and the S/G-bit on NT-side.

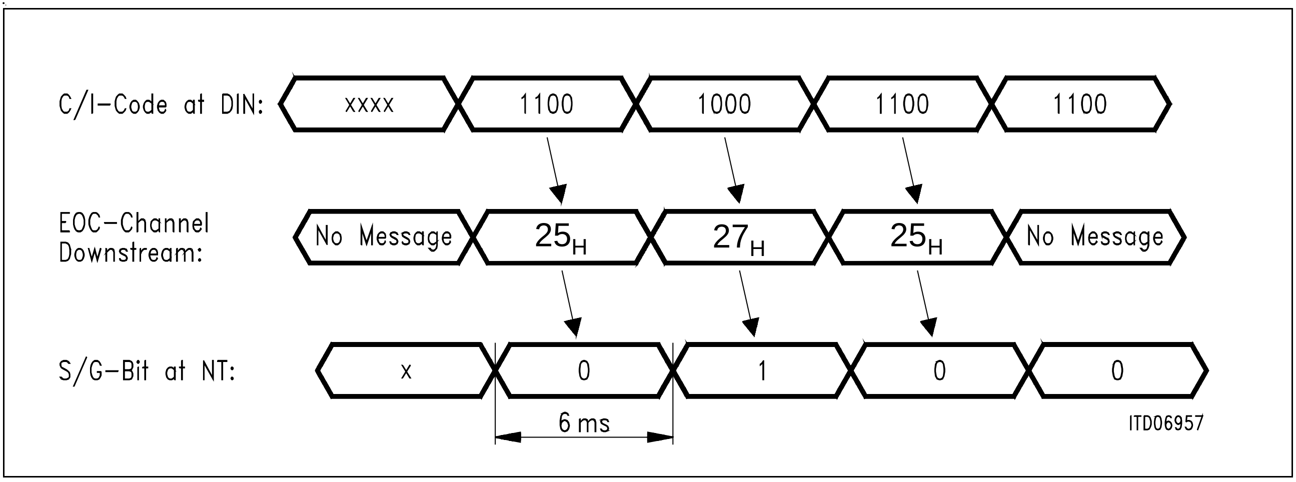


Figure 4-17 Passing D-channel arbitration to the Terminal via the EOC-Channel

This behavior is compatible to the operation of the PEB 2096 OCTAT-P, except the fact, that the OCTAT-P can set the S/G bit in 0.5ms intervals and the DFE-Q V2.1 only in 6 ms intervals. Note however, that the PEB 2091 IEC-Q V5.3 on the NT side provides a method to safely assign the HDLC-controller to the terminal before it actually sends the HDLC-frame to the line module. Hence, complete D-channel arbitration is provided. Refer to the PEB 2091 IEC-Q Data Sheet for version 5.3 for a detailed description.

4.6 Operation in RITL/WLL Systems

In this section the procedures are outlined that are performed if the DFE-Q V2.1 is operated in a 'Radio in the Loop' (RITL) application or 'Wireless Local Loop' (WLL) system.

4.6.1 Alignment and Synchronization of the U-Superframes

Alignment and synchronization of the U-frames that are issued in LT-mode on the four line ports is achieved by applying a synchronization signal at the SYNC input pin. The sync signal must meet the following requirements:

- the sync signal must be phase synchronous to the IOM®-2 clocks, FSC and DCL
- the sync signal must have a period that is any multiple of 12ms
  (= 1x U-superframe period)
- for proper synchronization one sync signal period has to be awaited before an activation is initiated

For RITL/WLL applications the U-frames of the active line ports must be aligned for overall synchronization of the base stations. The U-superframes are synchronized by an externally provided sync signal which must be any multiple of a 12ms period and which must be phase synchronous to FSC, e.g. the 2.4s DECT signal (see **Figure 4-18**).

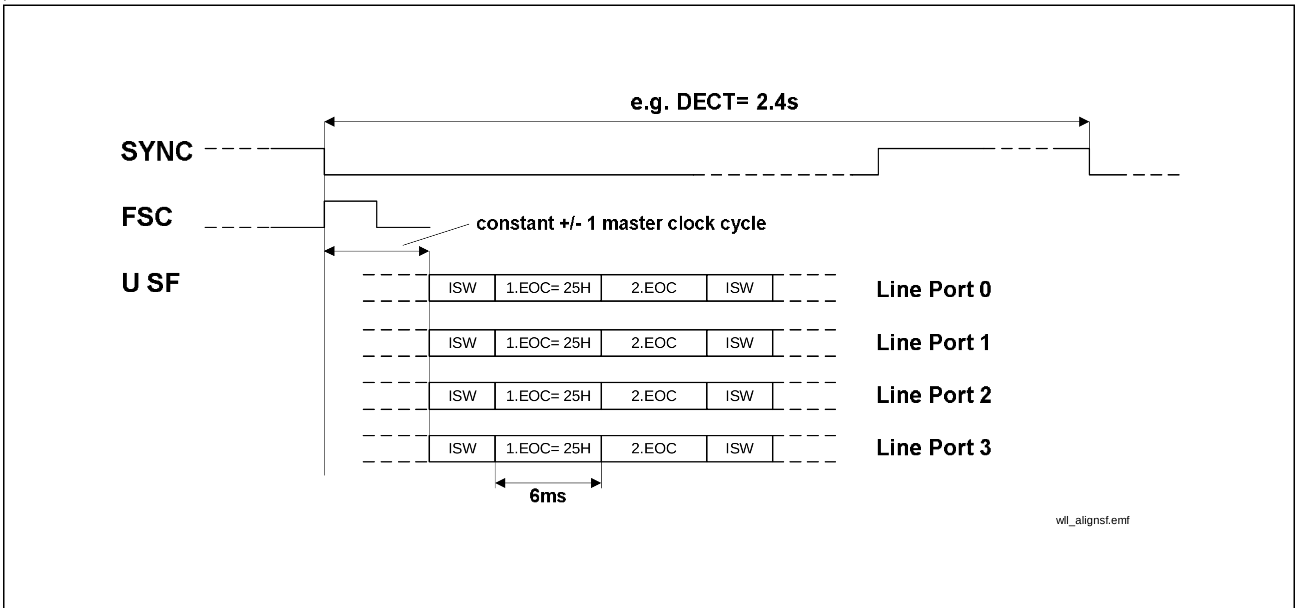


Figure 4-18 U-Frame Alignment/Synchronization in RITL/WLL Mode

The negative edge of the sync signal defines the start of the transmit U-superframe with a tolerance of +/-65ns. **Note that every negative edge takes effect and that thus jitter on the sync signal may reposition the U-superframe and cause bit errors on the U-interface!** After deactivation the U-superframe position must be maintained (this is because the warm start time may be shorter than the sync signal period and thus no sync edge may occur during a warm start activation). Therefore an internal 12 ms counter which stays active during power down mode is provided.

The status of synchronism can be monitored by the output signals, CLS0, CLS1, CLS2 and CLS3. In the active state they issue the 12ms transmit frame clocks. If they are aligned it is the evidence for synchronism.

4.6.2 Propagation Delay Measurement

Once the four U-interfaces are synchronized and activated the line lengths can be measured for propagation delay compensation in the base stations.

The propagation delay can be requested by the MON-8 command RPDU (Request Propagation Delay on U) and will be answered by the MON-8 message APDU. The propagation delay that is measured is the time between the transmission of the U-frame at the LT-side and the reception of the associated U-frame at the LT side (see **Figure 4-19**).

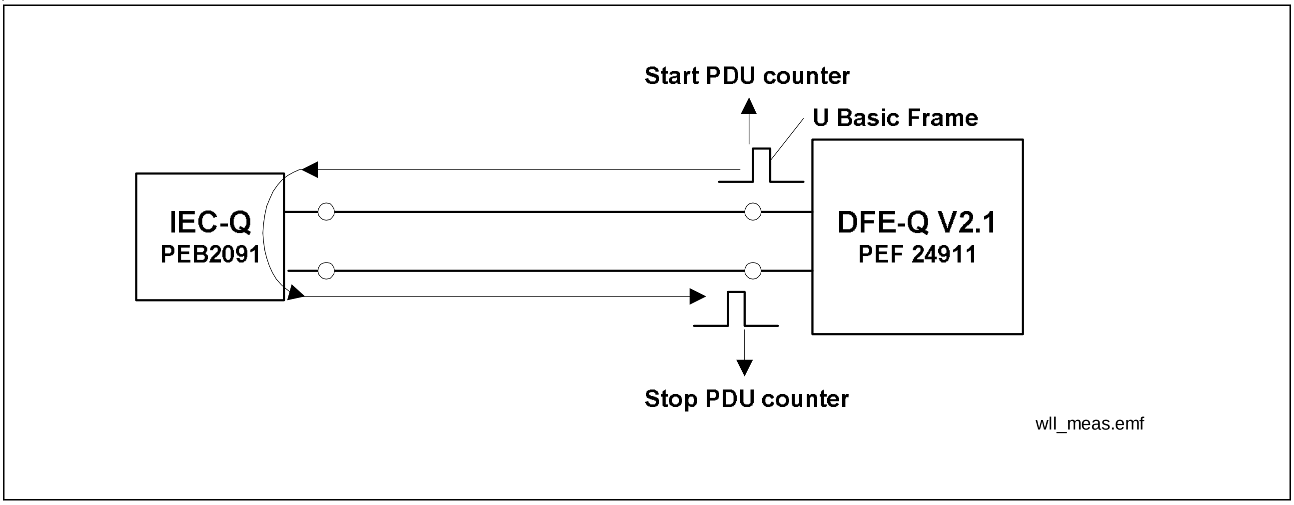


Figure 4-19 Measurement Principle

The propagation delay value is updated every 1.5ms (duration of 1 U-basic frame). Transmitting it to the terminal allows to adopt an appropriate delay in the base station in order to synchronize signal flow on the air interface.

The monitor message reporting the delay is of the format 1000 $1a_{10}a_9a_8\,a_7$ .. a_0. The PDU counter is clocked with 15.36Mhz which results in a resolution of +/-33ns.

Propagation delay measurements can be performed while the activation/deactivation state machine resides in one of the transparent states. That is, during transmission of data, the measurement can be repeated to cope with delay variations which may occur due to a temperature shift of the line.

4.6.3 Measurement Data Interpretation

There is a linear interdependency between the physical delay value (µs) and the binary result value. The conversion algorithm can be easily implemented in software by use of simple linear equations. The range from the shortest to the longest measurable propagation delay reaches up to 165µs.

An adequate way to achieve the reference line equations is to perform a sufficient number of propagation delay measurements on various line lengths. By means of statistical methods, such as Linear Regression, it is possible to retrieve a reference line equation out of a set of measured propagation delay values. Though Infineon Technologies will supply the reference line equations, which are based on a large number of measurements and an existing set of lab equipment, it is recommended that customers do additional evaluations using their own equipment and possibly using real telecom lines in order to minimize possible errors due to equipment tolerances.

Further detailed information about the conversion of the binary result in microseconds will be delivered by Infineon Technologies as soon as first measurement results are available. For a better understanding of the interpretation of measurement data the application note „A Dedicated Chip Set Features Synchronization of DECT Base stations Interfacing the U-Reference Point“ which was written for the DFE-Q V1.x / AFE chip set may help provisionally.

For compensation of chip internal effects that may influence the propagation delay value the following parameters must be read out by SW via the IOM®-2 interface:

RITL/WLL Parameters	DFE-Q V2.1: Access via	DFE-Q V1.3: Access via
Phase Information	MON-12 access to register PHI	MON-8 ’AST’
Range Bit	MON-12 access to register PDU (bit RANGE)	MON-8 ’AST’
Polarity	MON-12 access to register PDU (bit POL)	MON-8 ’88_H, $D9_H$’
AGC Value	MON-12 access to DSP Read registers DSP_RD1..3	MON-8 ’Read Coefficients’

Since the AGC or Range bit values of both sides must be known for correction its value must be transmitted either from line card to base station or vice versa, depending on where the processor power is best utilized. The D-channel or user accessable bits, which are contained within the maintenance channel of the U-interface may be used for this purpose. Since on the maintenance channel of the U-interface there is only a limited number of user accessible bits available, the AGC-value may be encoded.

Investigations have shown that two bits are sufficient for the encoding. The maintenance channel bits referred to as M51 and M52 may be used. They can be accessed via MON-2 messages.

If the parameters listed above are taken into account for the data conversion the remaining tolerance sources are restricted to a phase-in tolerance of the transmit path (position 1 in **Figure 4-20**). Positions 3 + 4 are compensated by parameter evaluation, position 2 is not covered in this document. The tolerance introduced by the transmit path accounts to +/-33ns.

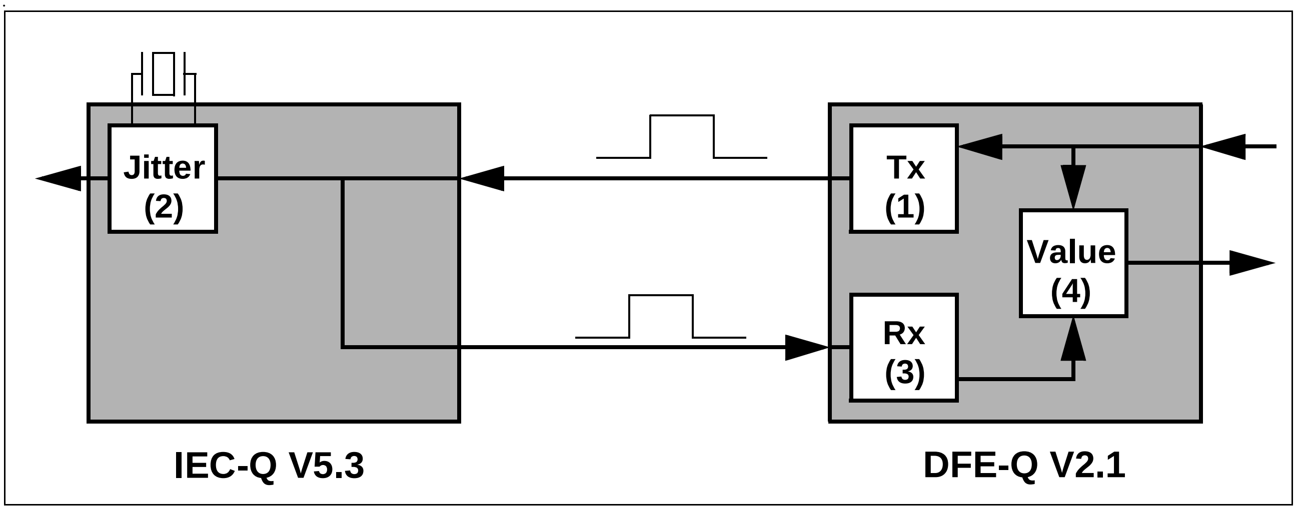


Figure 4-20 Sources of Measurement Tolerances

The compensation values must be transferred via EOC- or D-channel from the base station controller to the base stations. In the base stations the frame counters of the air interface are delayed by the preloaded compensation value. Thus, the air interfaces of all base stations are synchronized.

4.6.4 Synchronization of Base Stations

Similar to the D-channel arbitration procedure the DFE-Q V2.1 provides a control mechanism that generates a specific pattern (Infineon Technologies chipsets: 25_H) in the EOC channel, which prompts the synchronization process in the NT device, e.g. S/G bit activity of the IEC-Q V5.3. The S/G bit signal change in turn is used as sync event to synchronize different base stations among one another.

The sync process is initiated per line port by the MON-8 command BSYN (8125_H) which enables the transmission of the snyc pattern 25_H via the EOC-channel on U. The point of time for transmission of the sync pattern EOC 25H is triggered by the next falling edge at pin SYNC. The DFE-Q V2.1 issues the associated EOC message 25_H simultaneously on all the channels, which previously have been enabled by means of the BSYN command.

The PEB 2091 IEC-Q V5.3 - if programmed appropriately in TE mode - will interpret this EOC message such, that four "1" bits will appear at the S/G-bit followed by 44 "0" bits or vice versa. These 48 IOM®-frames constitute a period of 6 ms. A non Infineon device on the NT side must be able to interpret the 25H EOC command in an appropriate form.

In order to terminate again the synchronization procedure the EOC-channel must be reset to an idle state by explicitly sending the RTN (return to normal) MON-0 command. Otherwise the IEC-Q V5.3 will repeatedly send bursts of ones at the S/G bit position, as long as it is receiving super frames on U with EOC channel contents equal to 25H.

Note: It has to be ensured that the Monitor channel is in idle state in downstream direction, i.e. there should be no other Monitor channel activity before the BSYN command is applied to the DFE-Q V2.1. Moreover the echo of an issued EOC= 25H command has to be received before a new eoc command may be sent.

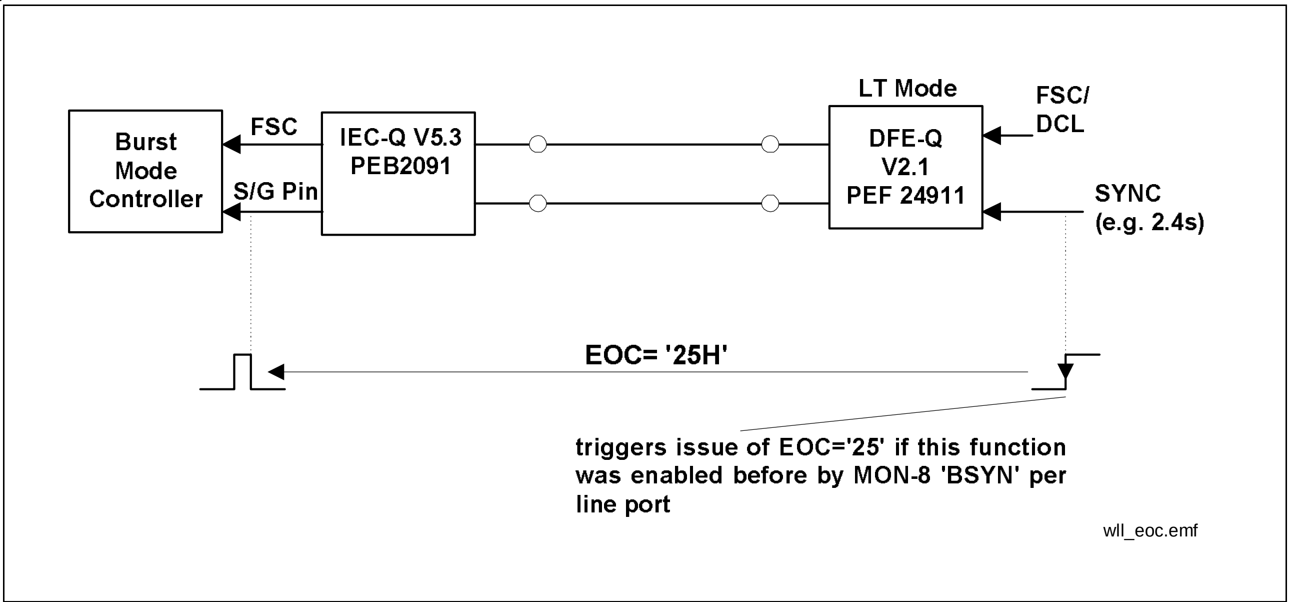


Figure 4-21 Transmission of a Synchronizing Pattern via the EOC Channel

The S/G bit is defined in channel 2 of the IOM®-2 terminal mode as is depicted in **Figure 4-22**.

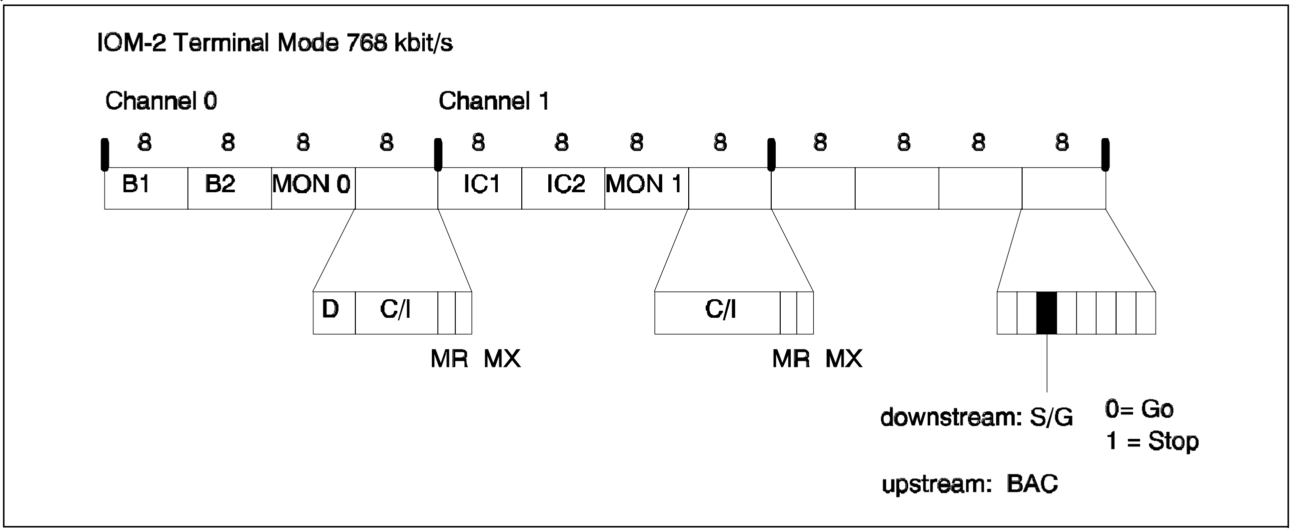


Figure 4-22 S/G Bit in IOM®-2 Terminal Mode

5 Monitor Commands

The registers of the DFE-Q V2.1 are accessed via the Monitor channel of the IOM®-2 interface. This chapter summarizes the available Monitor commands and messages. Please refer to section "IOM®-2 Monitor Channel" on page 3-6 for a detailed description of the Monitor handshake procedure.

Monitor commands supported by the DFE-Q V2.1 are divided into three categories. Each category derives its name from the first nibble (4 bits) of the two byte long message. These are MON-0, MON-2 and MON-8. All monitor messages representing similar functions are grouped together.

A special Monitor class are MON-12 commands which exist beside the known classes listed above. By MON-12 commands it is possible to address internal registers directly. MON-12 commands are always prioritized and are acknowledged first. See “MON-12 Protocol” on page 12. for the details on MON-12 commands and messages.

5.1 MON-0 - Exchanging EOC Information

MON-0 messages are used to write and read the registers containing the information of the EOC-channel on the U-interface. It is important to note that MON-0 messages provide only access to the device internal EOC-registers. The insertion and extraction of a message on the U-frame is handled automatically by the EOC-processor of the device.

The EOC is controlled and monitored via MON-0 commands and messages in the IOM®-2 Monitor channel. MON-0 commands may be passed at any instant and need to be transferred only once (applicable for auto and transparent mode). Code repetition is performed within the chip by the EOC-processor. For more information about the EOC processor and a detailed description of EOC auto/ transparent mode please see paragraph 3.10 on page 29.

The structure of a MON-0 message is shown below. The structure is identical in EOC auto and transparent mode.

MON-0 Structure

1. Byte		**2. Byte**	
0 0 0 0	A A A | 1	i1 i2 i3 i4	i5 i6 i7 i8
MON-0	Addr. | d/m	EOC Code	

Addr:	Address	– 0 = NT – 1 … 6 = Repeater – 7 = Broadcast
d/m:	Data/Message	– 0 = Data – 1 = Message
E:	EOC Code	– 00 … FF_H = coded EOC command/indication

Nine MON-0 commands are defined and can be interpreted. MON-0 commands are applied at DIN, MON-0 messages are issued at DOUT for confirmation. MON-0 messages have the highest priority among MON-0,2,8 and are issued first if i.e. a MON-2 or a MON-8 message is simultaneously outstanding.

Table 5-1 MON-0 Functions

Hex-code	LT		Function
i1-i8	**D**	**U**	
00	H	H	**Hold** Provokes no change. It may be used as a preliminary message in configurations where the acknowledgment is delayed. E.g. in a repeater configuration the NT-RP could answer with H while the EOC-acknowledgment is passed upstream. Thereby it can be avoided that the LT-control unit misinterprets the delayed ACK as a malfunction. The device issues Hold if no NT or broadcast address is used or if the d/m indicator is set to (0).
50	LBBD		**Close complete loop-back (B1, B2, D)** The NT does not close the complete loop-back immediately after receipt of this code. Instead it issues the C/I-command AIL (in “Transparent” state and auto mode) or ARL in the states “Error S/T” and “Synchronized”. This allows the downstream device to close the loop-back if desired (e.g. S-transceiver). If the downstream device does not close the loop a MON-8 command (LBBD) must be returned and the loop-back is closed within the U-transceiver.
51	LB1		**Closes B1 loop-back in NT** All B1-channel data will be looped back within the NT U-transceiver.
52	LB2		**Closes B2 loop-back in NT** All B2-channel data will be looped back within the NT U-transceiver.
53	RCC		**Request corrupt CRC** Upon receipt the NT transmits corrupted (= inverted) CRCs upstream. This allows to test the near end block error counter on the LT-side. The far end block error counter at the NT-side is stopped and NT-error indications (MON-1) are retained.
54	NCC		**Notify of corrupt CRC** Upon receipt of NCC the NT-block error counters (near-end only) are disabled and error indications are retained. This prevents wrong error counts while corrupted CRCs are sent (MON-8 CCRC).
AA		UTC	**Unable to comply** Message sent instead of an acknowledgment if an undefined EOC-command was received by the NT.
FF	RTN		**Return to normal** With this command all previously sent EOC-commands will be released. The EOC-processor is reset to its initial state (FF_H).
XX		ACK	**Acknowledge** If a defined and correctly addressed EOC-command was received by the NT, the NT replies by echoing back the received command.

5.2 MON-2 - Exchanging Overhead Bits

MON-2 indications are used to transfer all overhead bits except those representing EOC- and CRC-bits. Starting with the ACT-bit, the order is identical to the position of the bits on the U-interface.

The first MON-2 message is issued immediately after reaching the 'Line Active' state in LT-mode. Thereby the control system is informed about the initial U-interface status after a successful activation.

Later on MON-2 messages will only be sent if the system status has been changed. No MON-2 messages are issued while CRC-violations are detected (default setting). This prevents the system of being overloaded by faulty monitor indications. Alternative validation modes besides CRC are provided by the MFILT register which can be accessed via the MON-12 protocol (see chapter 3.3.5 on page 12 for the details).

MON-2 monitor messages have the second highest priority after MON-0 commands. Via the MON-8 command "PACE" bit D1, SAI/UOA, can be controlled by a MON-2 command. By use of register M4WMASK the user can also gain control on all other overhead bits via MON-2 commands (see again paragraph 3.9.2 on page 27 for the details).

Latching

MON-2 data that is received from IOM® is latched and transmitted on U. MON-2 data received from U is just forwarded on IOM® and is not latched.

MON-2 Structure

1. Byte		2. Byte
0 0 1 0	D11 D10 D9 D8	D7 D6 D5 D4 D3 D2 D1 D0
MON-2	Overhead Bits	Overhead Bits

D0 … 11: Overhead bits

The bit positions in the MON-2 message correspond to the following overhead bits:

Table 5-2 MON-2 and Overhead Bits

Position	LT –> NT	
MON-2/ U-Frame	Bit	Control
D11/M41	ACT	U-Trans/MON-2
D10/M51	1	MON-2
D9/M61	1	MON-2

D8/M42	DEA	U-Trans/MON-2
D7/M52	1	MON-2
D6/M62	FEBE	U-Trans/MON-2
D5/M43	1	MON-2
D4/M44	1	MON-2
D3/M45	1	MON-2
D2/M46	1	MON-2
D1/M47	UOA	U-Trans/MON-2
D0/M48	1	MON-2

Control via U-Transceiver

– ACT (Activation bit).ACT = (1) –> Layer 2 ready for communication
– DEA (Deactivation bit).DEA = (0) –> LT informs NT that it will turn off
– UOA (U-Only Activation).UOA = (0) –> U-activation only
– FEBE (Far-end Block Error).FEBE = (0) –> Far-end block error occurred

Control via MON-2

– by default the undefined bits marked with binary ’1’
– SAI (S Activity Indicator) = (0) –> S-interface is deactivated; can be controlled via MON-2 after MON-8 ’PACE’
– all M4 bits by programming register M4WMASK via MON-12 command

Control via other MON-Commands

– FEBE (Far-end Block Error) MON-8 message ’SFB’ sets a single FEBE bit to ’0’

For more details about the meaning of the overhead bits please refer to ETSI TS 102 080 and ANSI T1.601.

Transmission on U-Interface

– In transmit direction register M4WMASK decides which M4, M5 and M6 bits are controlled automatically by the internal logic or by a MON-2 message.
– The DFE-Q V2.1 transmits a given bit polarity as long as it is not changed by a new MON-2 message.
– The spare bits (M51, M52, M61) are set to binary ’1’ when leaving a power-down state. No further processing is performed by the U-transceiver.

Reception on U-Interface

– In the receive direction (on DOUT), the incoming M4, M5 and M6 bits are checked by the selected validation mode. A MON-2 message defining all 12 bits is issued if a change of at least one single bit other than the FEBE bit has been approved valid. Therefore a MON-2 message is sent not more often than once per superframe (12 ms interval).

– In order to notify the controller of the initial system status, one MON-2 message is issued immediately after reaching the “Line Active” state in LT-mode.
– The DFE-Q V2.1 will not issue MON-2 messages while the programmed validation criterion (CRC, TLL, ...) is not fulfilled.

5.3 MON-8 - Local Functions

Local functions are controlled via MON-8-commands. Local functions comprise e.g. reading block error counters, stimulating test functions, etc. MON-8-commands have the lowest priority and may be passed at any time and need to be transferred only once.

Latching

Latched commands in the NT must be disabled explicitly with the “NORM” command. Internal transfer commands (RBEN/F, RID) are not latched. Test and activation control commands (PACE, PACA, CCRC, LB1/2, LBBD) will be latched.

The following tables give an overview of structure and features of commands belonging to this category.

MON-8 Structure

1. Byte		2. Byte
1 0 0 0	r | 0 0 0	D7 D6 D5 D4 D3 D2 D1 D0
MON-8	Register | Addr.	Local Command (Message/Data)

r:	Register address	– 0 = local function register – 1 = internal register
D0…7	Local command	– 00 … FF_H = local function code – 00 … FF_H = internal register address

The following local commands are defined. If a response is expected, it will comprise 2 bytes. In the two-byte response the first byte will indicate that a MON-8 answer is transmitted, the second byte contains the requested information.

Table 5-3 MON-8-Local Function Commands

MON-8-Functions				
1.Byte	**2.Byte**	**LT**		**Function**
2nd nibble	**Code (Bin)**	D	U	
0000	1011 1110	PACE		**Partial Activation Control External** the PACE-command causes the DFE-Q V2.1 to ignore the actual status of the SAI-bit and to behave as if SAI = (1) is received. The SAI-bit is then controlled by MON-2 commands.
0000	1011 1111	PACA		**Partial Activation Control Automatic** PACA enables the device to interpret and control the SAI-bit automatically.
0000	1111 0000	CCRC		**Corrupt CRC** this command causes the device to send inverted (i.e. corrupted) CRCs. Corrupted CRCs are used to test block error counters.
0000	1111 1111	NORM		**Return to Normal** the NORM-command requests the device to stop the transmission of corrupted CRCs.
0000	1111 1011	RBEN		**Read Near-End Block Error Counter** the value of the near-end block error counter is returned and the counter is reset to zero. The maximum value is FF_H.
0000	1111 1010	RBEF		**Read Far-End Block Error Counter** The value of the far-end block error counter is returned and the counter is reset to zero. The maximum value is FF_H.
0000	r r r r r r r r		ABEC	**Answer Block Error Counter** The value of the requested block error counter (FEBE/NEBE) is returned (8 bit).
0000	0000 0000	RID		**Read Identification**
0000	**** ****		AID	**Answer Identification**. The DFE-Q V2.1 will reply with its ID upon a RID request
0000	1111 1001	SFB		**Set FEBE-Bit to ’0’** FEBE is set to ’0’ for one single U-superframe
0001	0111 DCBA	SETD		**Set status of relay driver pins** four driver pins (DxA, DxB, DxC, DxD, x= line port no.) can be set to either low or high.
0001	0000 0000	RST		**Read status pin** the logic state of the status pins STx0, STx1 is requested.

MON-8-Functions				
0001	xxxxxxS_1S_0		AST	**Answer 'RST' request** also issued without explicit request - issued upon signal change at the pins STx0, STx1
0001	1000 0000	RPDU		**Read Propagation Delay on U-Interface**
1aaa	aaaa aaaa		APDU	**Answer Propagation Delay on U-Interface** 11-bit APDU value corresponds to 14-bit PDU register value without the last 3 least significant bits
0001	0010 0101	BSYN		**Synchronize Base Stations** triggers EOC message „25H“ which in turn issues a sync impulse in the NT. Note that the EOC must be explicitly reset by MON-0(FF_H)

Notes: a … a propagation delay value
r … r result from block error counter

6 Register Description

In this section the complete register map is described that is provided with the new MON-12 protocol. For the protocol details please refer to page 3-12.

The register address arrangement is given in **Figure 6-1**. The U-interface registers are provided per line port. By register LP_SEL it can be determined which U register bank and by that which line port number is addressed. LP_SEL adds an offset value to the current address. The offset value is latched as long as register LP_SEL is overwritten again.

For access to DSP registers the MSB of the 8-bit wide address must be set to '1'.

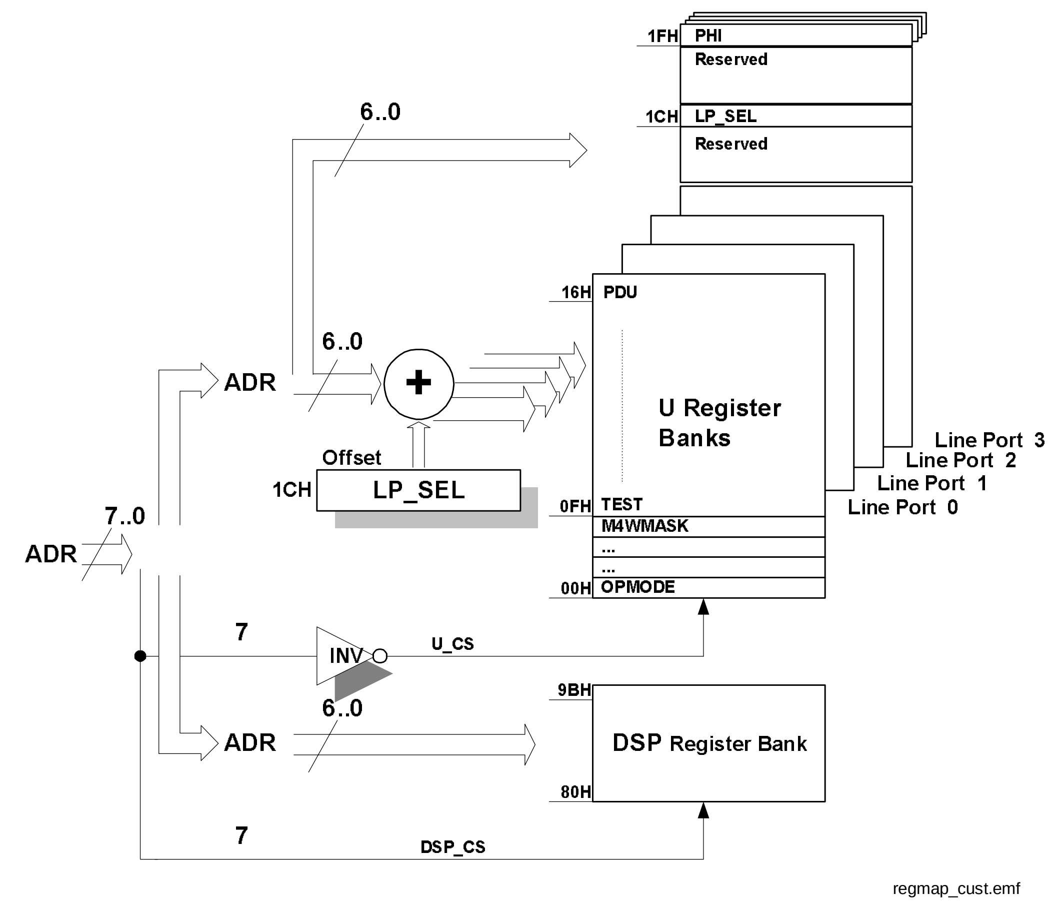


Figure 6-1 DFE-Q V2.1 Register Map

6.1 Register Summary

	ADR	7	6	5	4	3	2	1	0	WR/RD	1/4 Ch.
LP_SEL	**$1C_H$**	0	0	0	0	0	0	LN2	LN1	**WR/RD***	1

U-Interface Registers

	ADR	7	6	5	4	3	2	1	0	WR/RD	1/4 Ch.
OPMODE	**00_H**	0	0	FEBE	0	0	0	1	0	**WR/RD***	1
MFILT	**01_H**	M56 FILTER		M4 FilLTER			EOC FILTER			**WR/RD***	1
EOC_CR	**02_H**	0	0	0	0	0	0	BSYN	DARB	**WR/RD***	1
M4RMASK	**07_H**	M4 Read Mask Bits								**WR/RD***	1
M4WMASK	**08_H**	M4 Write Mask Bits								**WR/RD***	1
TEST	**$0F_H$**	0	MPDU	BER		CCRC	+-1 Tones	333 Hz	40KHz	**WR/RD***	4
LOOP	**10_H**	0	DLB	TRANS	U/IOM®	1	LBBD	LB2	LB1	**WR/RD***	4
FEBE	**11_H**	FEBE Counter Value								**RD**	4
NEBE	**12_H**	NEBE Counter Value								**RD**	4
BERC	**13_H**	BERC Counter Value (Bit 15-8)								**RD**	4
	14_H	BERC Counter Value (Bit 7-0)									
PDU	**15_H**	RANGE	POL	PDU Counter Value (Bit 13-8)						**RD**	4
	16_H	PDU Counter Value (Bit 7-0)									
PHI	**$1F_H$**	Phase Adjust Value								**RD**	4

DSP Registers

	ADR	7	6	5	4	3	2	1	0	WR/RD	1/4 Ch.
DSP_CR1	**80_H**	0	CH_SEL		DAA	0	0	0	0	**WR/RD***	1
DSP_CR2	**81_H**	0	0	1	DATA_TYP			DATA_RW		**WR/RD***	1
DSP_DREQ	**82_H**	0	0	0	0	0	0	0	DATA _REQ	**WR**	1
DSP_DACK	**90_H**	0	0	0	0	0	0	0	DATA _ACK	**RD**	1
DSP_RD1	**91_H**	Coefficient Data								**RD**	1
DSP_RD2	**92_H**	Coefficient Data								**RD**	1
DSP_RD3	**93_H**	Reserved						Coefficient Data		**RD**	1

*) read-back function for test use

Table 6-1 Register Map Reference Table

Reg Name	Access	Address	Reset Value	Comment	Page No.
LP_SEL	WR	$1C_H$	00_H	**Line Port Selection Reg.** line port 0 is selected by default	**6-6**

U-Interface Registers

OPMODE	WR	00_H	02_H	**Opmode Register** LT mode	**6-7**
MFILT	WR	01_H	14_H	**M-Bit Filter Register** – EOC in automode – M4 CRC checked vs. IOM® – M4 TLL checked vs. SM – M56 CRC checked	**6-8**
EOC_CR	WR	02_H	00_H	**EOC Control Register** D-channel arbitration disabled, BSYN inactive	**6-12**
M4RMASK	WR	07_H	00_H	**M4 Read Mask Register** any M4-bit change causes a MON-2 message	**6-13**
M4WMASK	WR	08_H	BC_H	**M4 Write Mask Register** automatic control of ACT, DEA, UOA bit	**6-15**
TEST	WR	$0F_H$	40_H	**TEST Register** propagation delay measurement enabled	**6-17**
LOOP	WR	10_H	08_H	**LOOP Register** all local loops deactivated	**6-19**
FEBE	RD	11_H	00_H	**FEBE Counter Register**	**6-21**
NEBE	RD	12_H	00_H	**NEBE Counter Register**	**6-21**
BERC	RD	$13_H – 14_H$	0000_H	**Bit Error Rate Counter Reg.**	**6-22**
PDU	RD	$15_H – 16_H$	0000_H	**Propagation Delay Counter r**	**6-22**
PHI	RD	$1F_H$	00_H	**Phase Information Register**	**6-23**

DSP Registers

Table 6-1 Register Map Reference Table

Reg Name	Access	Address	Reset Value	Comment	Page No.
DSP_CR1	WR	80_H	00_H	**DSP Control Register 1** all functions enabled	**6-24**
DSP_CR2	WR	81_H	20_H	**DSP Control Register 2** normal operation mode	**6-24**
DSP_ DREQ	WR	82_H	00_H	**DSP Data Request Register**	**6-26**
DSP_ DACK	RD	90_H	00_H	**DSP Data Acknowl. Register**	**6-27**
DSP_RD	RD	91_H–93_H	00_H	**DSP Read Registers**	**6-28**

6.2 Reset of U-Transceiver Functions in State 'Deactivated'

The following U-transceiver registers are reset upon the transition to state 'Deactivated':

Register	Reset to	Affected Bits/ Comment
U-Interface Registers		
TEST		only the bits BER and CCRC are reset
LOOP		only the bits LBBD, LB2 and LB1 are reset
FEBE	00_H	reset upon deactivation
NEBE	00_H	reset upon deactivation
BERC	0000_H	reset upon deactivation
PDU	00_H	reset upon deactivation
PHI	00_H	reset upon deactivation

6.3 Mode Register Evaluation Timing

The point of time when mode settings are detected and executed differs with the mode register type. Three different behaviors can be classified

- evaluation and execution after SW-reset (C/I= RES, RES1)
- evaluation and execution upon transition to state 'Deactivated'
- immediate evaluation and execution

Below the mode registers are listed and grouped according to the different evaluation times as stated above.

Register	Affected Bits	Comment
Registers Evaluated After SW-Reset		
MFILT	complete register	
Registers Evaluated Upon Transition to State 'Deactivated'		
MFILT	complete register	
Immediate Evaluation and Execution		
OPMODE	bit FEBE	

Register	Affected Bits	Comment
EOC_CR	bit BSYN, DARB	
M4RMASK	complete register	
M4WMASK	complete register	
TEST	complete register	
LOOP	complete register	

6.4 Detailed Register Description

6.4.1 LP_SEL - Line Port Selection Register

The **Line Port Selection** register selects the register bank that is associated with the addressed line port. All line port specific register operations - line port specific registers are indicated by a '4' in the last column of the register summary - are performed on the line port that is addressed by the value of LP_SEL.

LP_SEL read/**write** Address: $1C_H$

Reset value: 00_H

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LN2	LN1

LN2,1 Line Port Number

00 = Line port no. 0 is addressed by the following command

01 = Line port no. 1 is addressed by the following command

10 = Line port no. 2 is addressed by the following command

11 = Line port no. 3 is addressed by the following command

U-Interface Registers

6.4.2 OPMODE - Operation Mode Register

The **Op**eration **Mode** register determines the operating mode of the DFE-Q V2.1.

OPMODE read*)/**write** Address: 00_H

Reset value: 02_H

7	6	5	4	3	2	1	0
0	0	FEBE	0	0	0	MODE1 =1	MODE0 =0

FEBE Enable/Disable external write access to FEBE Bit in register M56W

0 = external access to FEBE bit disabled - FEBE bit is set by internal FEBE counter logic

1 = external access to FEBE bit enabled - FEBE bit is controlled by MON-2

MODE1,0 Operation mode setting

10 = LT mode

01 = reserved

11 = reserved

00 = reserved

6.4.3 MFILT - M-Bit Filter Options

The **M-Bit Filter** register defines the validation algorithm received Maintenance channel bits (M1-M6) of the U-interface have to undergo before they are approved and passed on to the system interface.

M-bit changes are reported to the system environment by MON-0 (EOC) or MON-2 (M4-M6) messages via IOM®-2. To lower processor load due to faulty monitor messages three different filter functions are supported, Triple-Last-Look (TLL), CRC check and On Change.

- **Triple-Last-Look (TLL)**
  A change of M-bit data has to be received in three consecutive U-frames until it is approved valid and reported to the system interface.
- **CRC**
  A change of M-bit data is only reported to the system interface if no CRC violation has been detected.
  The forwarding of M-bit changes is delayed by 12ms (= 1x U-superframe) if received M-bits are CRC covered. This way the M-bit data is checked with the actual CRC sum which is received one U-superframe later.
- **On Change**
  Every time the M-bit status has changed a MON-0 or MON-2 message is issued.

Some M4 bits, ACT, DEA and UOA, have two destinations, the state machine and the system interface. Regarding these bits Triple-Last-Look (TLL) is applied by default before the changed status is input to the state machine. Via bit no. 5 of the MFILT register the user can decide whether the M4 bits which are input to the state machine shall be approved by TLL (Bellcore requirement) or by the same verification mode as selected for the issue of a MON-2 message.

The MFILT register setting is evaluated each time the DFE-Q V2.1 enters the “Deactivated” state. For further information on the handling regarding the Maintenance channel please refer to the chapter "Maintenance Channel" on page 3-21.

MFILT read*)/**write** Address: 01_H

Reset value: 14_H

7	6	5	4	3	2	1	0
M56 FILTER		M4 FILTER			EOC FILTER		

M56 FILTER controls the validation mode of the spare bits (M51, M52, M61) **on a per bit base.** Approved M5, M6 bit changes are reported to the system interface by a MON-2 message

X0 = Apply **same filter** to M5 and M6 bit data as programmed for M4 bit data

X1 = **On Change**
if a change of the M5, M6 bit status has occurred a MON-2 message will be issued

M4 Filter 3-bit field which controls the validation mode of the M4 bits **on a per bit base.** Approved M4 bit changes are reported to the system interface by a MON-2 message.

- Bit 3 and 4 determine the filter algorithm that is applied for the triggering of a MON-2 message
- Bit 5 controls whether the forwarding of M4 bits to the internal state machine shall be approved by default by TLL or by the same filtering mode as selected for the forwarding to the system environment

Note: Bellcore TR-NWT-397 (1993) requires to apply TLL to the M4 bits before M4 bit changes are processed by the state machine

x00 = **On Change**
if a change of the M4 bit status has occurred it will be indicated to the system by a MON-2 message

x01 = **TLL coverage** of M4 bit data
a change of M4 bit data is only passed on if it has been received in three consecutive frames

x10 = **CRC coverage** of M4 bit data
a change of M4 bit data is passed on if no CRC violation has been detected

x11 = **CRC and TLL coverage** of M4 bit data
a change in M4 bit data is reported to the system interface if no CRC violation has been detected and if it has been received in three consecutive frames,
the change is reported as soon as 3 complete U-superframes were successfully analysed

0xx = M4 bits **towards state machine** are **covered by TLL**

1xx = M4 bits **towards state machine** are checked by the same validation algorithm as programmed for the reporting to the system interface

EOC FILTER 3-bit field which controls the processing of EOC messages and its verification algorithm

100= EOC **automatic mode**

- 'Return Message Reception Function' is enabled as soon as the LT has transmitted an EOC command. It causes the DFE-Q V2.1 in LT mode to compare the received and verified (by TLL) EOC messages with the last downstream transmitted EOC command. A MON-0 message is issued if they prove to be equal.

  For this particular received EOC message the 'different from previous' rule is NOT applied. This means that a MON-0 message is even issued if the received EOC message is not different to the one previously accepted.

  All other incoming EOC messages besides the echo of the one transmitted downstream will be evaluated by TLL and the 'different from previous' verification.

- if no EOC command has been transmitted downstream a MON-0 message is issued only after the TLL criterion has been met and the message is different from the one previously accepted

001= EOC **transparent mode without any filtering**
- every 6ms an EOC message is passed on by a MON-0 message
- suitable mode for Digital Loop Carrier applications
- no EOC filtering:
  every 6ms an EOC messages is forwarded to the system interface via a MON-0 message
- no acknowledgment
- no execution
- no latching is performed

010= EOC **transparent mode with 'On Change' filtering**
only if **a change** of the received EOC message has been detected it is passed on

011 = EOC **transparent mode with Triple-Last-Look (TLL) filtering**
TLL coverage of EOC messages is enabled

6.4.4 EOC_CR - EOC Control Register

The **EOC C**ont**r**ol Register accommodates control bits for EOC related functions.

EOC_CR read*)/**write** Address: 02_H

Reset value: 00_H

7	6	5	4	3	2	1	0
0	0	0	0	0	0	BSYN	DARB

BSYN Synchronize base stations
BSYN causes the transmission of the EOC message „25H“ as soon as an edge of the RITL/WLL sync signal occurred at pin SYNC. The EOC message will be sent until it is explicitly reset again by the MON-0 command RTN (FF_H) or it is overwritten by any other EOC command. After execution BSYN is reset by the internal logic.

0 = function disabled

1 = triggers the transmission of the sync pattern ’25H’ in the EOC channel with the next edge of a RITL/WLL synchronization signal at pin SYNC,
after execution BSYN is automatically reset

DARB D-channel arbitration

0 = function disabled

1 = triggers the transmission of the pattern ’27H’ or ’25H’ in the EOC channel when the C/I codes AR or AI are applied

6.4.5 M4RMASK - M4 Read Mask Register

Via the **M4 Read Mask** register the user can selectively control which M4 bit changes are to be reported via MON-2 messages.

M4RMASK read*)/**write** Address: 07_H

Reset value: 00_H

7	6	5	4	3	2	1	0
M4 Read Mask Bits							

Bit 7..0

0 = M4 bit change indication by MON-2 message active

1 = M4 bit change indication by MON-2 message masked

Bit 6 **Partial Activation Control External/ Automatic**

– function corresponds to the MON-8 commands PACE, and PACA
– the actual status of the received SAI bit is ignored if external control is enabled - the DFE-Q V2.1 behaves as if SAI= ’1’ is received

0 = Automatic processing of the SAI bit

1 = External Partial Activation Control active

Below the cross reference of the MASK bits to the M4 bits as they are sent from the NT to the LT is given:

7	6	5	4	3	2	1	0
NIB	SAI	M46	CSO	NTM	PS2	PS1	ACT

NIB Network Indication Bit

0 = no function (reserved for network use)

1 = no function (reserved for network use)

SAI S-Activity Indicator

0 = S-interface is deactivated

1 = S-interface is activated

CSO Cold Start Only
- 0 = NT is capable to perform warm starts
- 1 = NT activation with cold start only

NTM NT Test Mode
- 0 = NT busy in test mode
- 1 = inactive

PS2 Power Status Secondary Source
- 0 = secondary power supply failed
- 1 = secondary power supply ok

PS1 Power Status Primary Source
- 0 = primary power supply failed
- 1 = primary power supply ok

ACT Activation Bit
- 0 = layer-2 not established
- 1 = signals layer-2 ready for communication

6.4.6 M4WMASK - M4 Write Mask Register

Access to the **M4 Write Mask** register is controlled by the **M4WMASK** register. By means of the M4WMASK register the user can direct on a per bit base which M4 bits are controlled by the user and which are controlled by the state machine.

M4WMASK read*)/**write** Address: 08_H

Reset value: BC_H

7	6	5	4	3	2	1	0
M4 Write Mask Bits							

Bit 7..0

0 = M4 bit is controlled by state machine

1 = M4 bit is controlled by MON-2 command

Bit 6 **Partial Activation Control External/Automatic**,
function corresponds to the MON-8 commands PACE and PACA

0 = UOA bit is controlled by state machine

1 = UOA bit is controlled by MON-2 command

Below the cross reference of the MASK bits to the M4 bits as transmitted from the LT to the NT is given:

7	6	5	4	3	2	1	0
AIB	UOA	M46	M45	M44	SCO	DEA	ACT

AIB Interruption (according to ANSI)

0 = indicates interruption

1 = inactive

UOA U Activation Only

0 = indicates that only U is activated

1 = inactive

SCO Start-on-Command Only Bit
indicates whether the DLC network will deactivate the loop between calls (defined in Bellcore TR-NWT000397)

0 = ’Start-on-Command-Only’ mode active,
in LULT mode the U-transceiver shall initiate the start-up procedure only upon command from the network (’AR’ primitive)

1 = normal mode,
if the U-transceiver is operated within a DCL configuration as LULT it shall start operation as soon as power is applied

DEA Deactivation Bit

0 = LT informs NT that it will turn off

1 = inactive

ACT Activation Bit

0 = layer 2 not established

1 = signals layer-2 ready for communication

6.4.7 TEST - Test Register

The **Test** register sets the DFE-Q V2.1 in the desired test mode.

TEST read*)/**write** Address: $0F_H$

Reset value: 40_H

7	6	5	4	3	2	1	0
0	MPDU	BER		CCRC	+-1 tones	333Hz	40kHz

MPDU Measure Propagation Delay on U
triggers propagation delay measurement on U

0 = inactive

1 = 14-bit propagation delay value in register PDU is updated every 1.5ms

BER Bit Error Rate Measurement Function

– **prerequisite**: closed loopback #2 on the NT-side
– allows to measure the BER of either the B1-, the B2-, or the B1- and B2- and D-channel in transparent state
– the user data stream is overwritten by a continuous series of zeros

00 = Bit Error Rate (BERC) counter disabled

01 = starts B1-channel BER measurement
Bit Error Rate counter (BERC) is enabled and a continuous series of zeros is sent in channel B1

10 = starts B2-channel BER measurement
Bit Error Rate counter (BERC) is enabled and a continuous series of zeros is sent in channel B2

11 = starts B1-, B2- and D-channel BER measurement
Bit Error Rate counter (BERC) is enabled and a continuous series of zeros is sent in channel B1, B2 and D

CCRC Send Corrupt CRC

0 = inactive

1 = send corrupt (inverted) CRCs

+-1 tones	Send +/-1 pulses instead of +/-3 pulses	
	0 =	no action
	1 =	issues +/-1 pulses instead of +/-3 during 40kHz tone generation or in SSP test mode
333Hz	333Hz Maintenance Tone	
	0 =	no action
	1 =	issues 333Hz maintenance tone
40kHz	40kHz Test Signal	
	0 =	no action
	1 =	issues a 40kHz test signal - suitable for testing of test equipment

6.4.8 LOOP - Loop Back Register

The **Loop** register controls local loopbacks within the DFE-Q V2.1. For the loopback configurations that are available by the LOOP register see section 4.4.1.5 on page 28.

LOOP read*)/**write** Address: 10_H

Reset value: 08_H

7	6	5	4	3	2	1	0
0	DLB	TRANS	U/IOM®	1	LBBD	LB2	LB1

DLB Close Framer/Deframer Loopback
- the loopback is closed at the analog/digital interface
- prerequisite is that LB1, LB2, LBBD and U/IOM® are set to ’0’
- only user data is looped and no maintenance data is not looped back
- the DLB loop operates always in non-transparent mode

0 = Framer/Deframer loopback open

1 = Framer/Deframer loopback closed

TRANS Transparent/ Non-Transparent Loopback
- in transparent mode user data is both passed on and looped back, whereas in non-transparent mode data is not forwarded but substituted by ’1’s (idle code) and just looped back
- if LBBD, LB2, LB1 is closed towards the IOM® interface and bit TRANS is set to ’1’ then the state machine has to be put into state ’Transparent’ first (e.g. by C/I = DT) before data is output on the U-interface
- bit TRANS has no effect on DLB (always non-transparent) and the analog loopback (ARL operates always in transparent mode)

0 = sets transparent loop mode for LBBD, LB2, LB1

1 = sets non-transparent mode for LBBD, LB2, LB1
’1’s are sent on the IOM®-2 interface in the corresponding time-slot

U/IOM® Switch that selects whether looback LB1, LB2 or LBBD is closed towards U or IOM®-2

0 = LB1, LB2, LBBD loops are closed towards IOM®-2

1 = LB1, LB2, LBBD loops are closed towards U

LBBD Close complete loop (B1, B2, D) near the system interface
the direction towards the loop is closed is determined by bit U/IOM®

0 = complete loopback open

1 = complete loopback closed

LB2 Close loop B2 near the system interface
the direction towards the loop is closed is determined by bit U/IOM®

0 = loopback B2 open

1 = loopback B2 closed

LB1 Close loop B1 near the system interface
the direction towards the loop is closed is determined by bit U/IOM®

0 = loopback B1 open

1 = loopback B1 closed

6.4.9 FEBE - Far End Block Error Counter Register

The **F**ar **E**nd **B**lock **E**rror Counter Register contains the FEBE value. If the register is read out it is automatically reset to ’0’.

FEBE **read** Address: 11_H

Reset value: 00_H

7	6	5	4	3	2	1	0
FEBE Counter Value							

6.4.10 NEBE - Near End Block Error Counter Register

The **N**ear **E**nd **B**lock **E**rror Counter Register contains the NEBE value. If the register is read out it is automatically reset to ’0’.

NEBE **read** Address: 12_H

Reset value: 00_H

7	6	5	4	3	2	1	0
NEBE Counter Value							

6.4.11 BERC - Bit Error Rate Counter Register

The **B**it **E**rror **R**ate **C**ounter register contains the number of bit errors that occurred during the period the bit TEST.BER was set active. If the 2nd byte (adr. 14H) of the 16-bit BERC counter is read out the 16-bit value is automatically reset to ’0’.

BERC **read** Address: $13/14_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
Bit Error Rate Counter Value							

7	6	5	4	3	2	1	0
Bit Error Rate Counter Value							

6.4.12 PDU - Propagation Delay on U Register

The **P**ropagation **D**elay on **U** register contains the value that corresponds to the measured propagation delay from FSC-LT to FSC-NT. If the register is read out it is automatically reset to ’0’. The MSB bit reflects the setting of the RANGE bit for compensation of measurement tolerances caused by the range function. Bit 14 indicates the polarity of the two-wire subscriber line.

PDU **read** Address: $15/16_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
RANGE	POL	Propagation Delay on U Counter Value					

7	6	5	4	3	2	1	0
Propagation Delay on U Counter Value							

6.4.13 PHI - Phase Information Register

The **Ph**ase **I**nformation register contains the current phase adjustment value of the addressed line port. It is notified in a 8-bit two's complement format and is required for tolerance minimization of the propagation delay value.

PHI **read** Address: $1F_H$

Reset value: 00_H

7	6	5	4	3	2	1	0
Phase Adjustment Value							

6.4.14 DSP Registers

DSP_CR - DSP Control Registers

Via the **DSP Cont**rol register 1 the operational function of the DSP core can be controlled. With the DSP Control register 2 the coefficient set is determined for the data exchange between the DSP and an external controller.

DSP_CR1 read*)/**write** Address: 80_H

Reset value: 00_H

7	6	5	4	3	2	1	0
0	CH_SEL		DAA	0	0	0	0

CH_SEL Channel Selection
selects the addressed line port - subsequent data transfers are assigned to the selected line port no.

00= selects line port no. 0

01= selects line port no. 1

10= selects line port no. 2

11= selects line port no. 3

DAA Disable all adjust - freeze coefficients
line port selective command: takes only effect for the selected line port as set by CH_SEL

0= inactive

1= disables update of EC, AGC, FFEQ and FBEQ coefficients

DSP_CR2 read*)/**write** Address: 81_H

Reset value: 20_H

7	6	5	4	3	2	1	0
0	0	1	DATA_TYP			DATA_RW	

DATA_TYP DSP Data Access Type

’100’	coefficients set 1
’110’	coefficients set 2
’001’	coefficients set 3
’011’	coefficients set 4

DATA_RW Read DSP Data

00 =	disabled
01 =	read DSP data
10, 11	reserved

DSP_DREQ - DSP Data Request Register

The **DSP** **D**ata **Req**uest register contains the handshake signal ’DATA_REQ’ for communication between the DSP and an external microcontroller. DATA_REQ is controlled by an external controller and signals when the layer-1 controller requests new data.

DSP_DREQ **write** Address: 82_H

Reset value: 00_H

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DATA_REQ

DATA_REQ DSP Data Request

0= External controller busy or inactive

1= indicates that the layer-1 controller has read the data and requests new data

DSP_DACK - DSP Data Acknowledge Register

The **DSP D**ata **Ack**nowledge register contains the handshake signal 'DATA_ACK' for communication between the DSP and an external microcontroller. DATA_ACK is controlled by the DSP and signals whether the DSP is busy or ready for new data access.

DSP_DACK **read** Address: 90_H

Reset value: 00_H

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DATA_ACK

DATA_ACK DSP Data Acknowledge

0= DSP DATA register value has been updated

1= DSP busy

DSP_RD - DSP Read Registers

The **DSP Read** Data registers contain the data that have been requested by an external controller. The data type is determined by the setting of the DSP_CR2 register.

DSP_RD1 **read** Address: 91_H

Reset value: 00_H

7	6	5	4	3	2	1	0
Coefficient Data							

DSP_RD2 **read** Address: 92_H

Reset value: 00_H

7	6	5	4	3	2	1	0
Coefficient Data							

DSP_RD3 **read** Address: 93_H

Reset value: 00_H

7	6	5	4	3	2	1	0
Reserved						Coefficient Data	

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias PEF	T_A	– 40 to 85	°C
Storage temperature	T_{stg}	– 65 to 125	°C
IC supply voltage	V_{DD}	– 0.3 to 6	V
Input/Output voltage on any pin with respect to ground	V_S	– 0.3 to V_{DD} + 0.3 (max. 6)	V
Maximum current on all lines connected to the backplane when the DFE-Q V2.1 is without power supply; at 3.3V external signal level	I_{max}	TBD	mA
ESD robustness[1)]HBM: 1.5 kΩ, 100 pF	$V_{ESD,HBM}$	2000	V

1) According to MIL-Std 883D, method 3015.7 and ESD Ass. Standard EOS/ESD-5.1-1993.

***Note:** Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

7.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Ambient temperature	T_A	– 40	85	°C	
Supply voltage	V_{DD}	3.0	3.6	V	
Ground	V_{SS}	0	0	V	

Note: In the operating range, the functions given in the circuit description are fulfilled.

7.3 DC Characteristics

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input low voltage	V_{IL}	– 0.3	0.8	V	
Input high voltage	V_{IH}	2.0	V_{DD} + 0.3	V	
Output low voltage	V_{OL}		0.45	V	I_{OL} = 7 mA [1] I_{OL} = 2 mA [2]
Output high voltage	V_{OH}	2.4		V	I_{OH} = – 7 mA [1] I_{OH} = – 2 mA [2]
Avg. power supply current	I_{CC} (AV)		TBD	mA	V_{DD} = 3.3 V, T_A = 25 °C: DCL = 4.096 MHz Clock = 15.36 MHz
Input leakage current	I_{IL}	-1	1	µA	V_{DD} = 3.3 V, V_{SS} = 0 V; all other pins are floating; 0 V< V_{IN} < V_{DD}
Output leakage current	I_{OZ}	-1	1	µA	V_{DD} = 3.3 V, V_{SS} = 0 V; 0 V< V_{OUT} < V_{DD}

[1] Apply to: DOUT

[2] Apply to all the I/O and O pins that do not appear in the list in note **1)**

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

7.4 AC Characteristics

Inputs are driven to 2.4 V for a logical ’1’ and to 0.45 V for a logical ’0’. Timing measurements are made at 2.0 V for a logical ’1’ and 0.8 V for a logical ’0’. The AC testing input/output waveforms are shown in **Figure 7-1.**

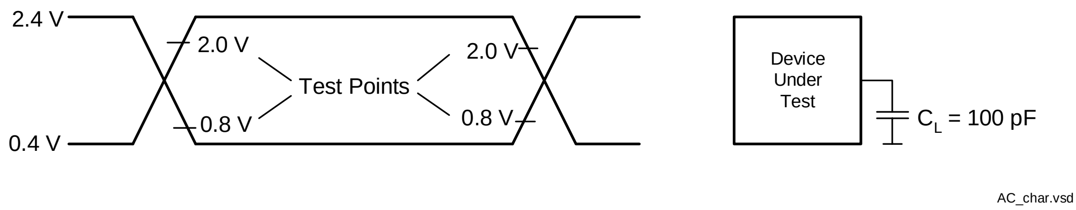


Figure 7-1 Input/Output Waveform for AC Tests

7.4.1 Reset Timing

Parameter	Symbol	Limit Values		Unit	Remark
		min.	max.		
Active Low Period	$t_{\overline{RES}}$	200		ns	**reset is executed 900µs after the low active phase** 15.36MHz master clock has to be applied

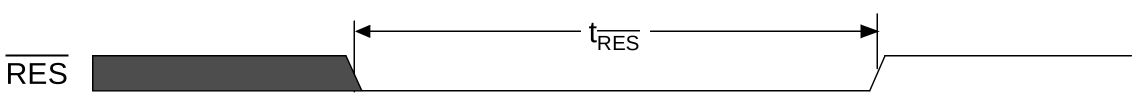


Figure 7-2 Reset Timing

7.4.2 IOM®-2 Interface Timing

The dynamic characteristics of the IOM®-2-interface are given in **Figure 7-3**. In case the period of signals is stated the time reference will be at 1.4 V. In all other cases 0.8 V (low) and 2.0 V (high) thresholds are used as reference.

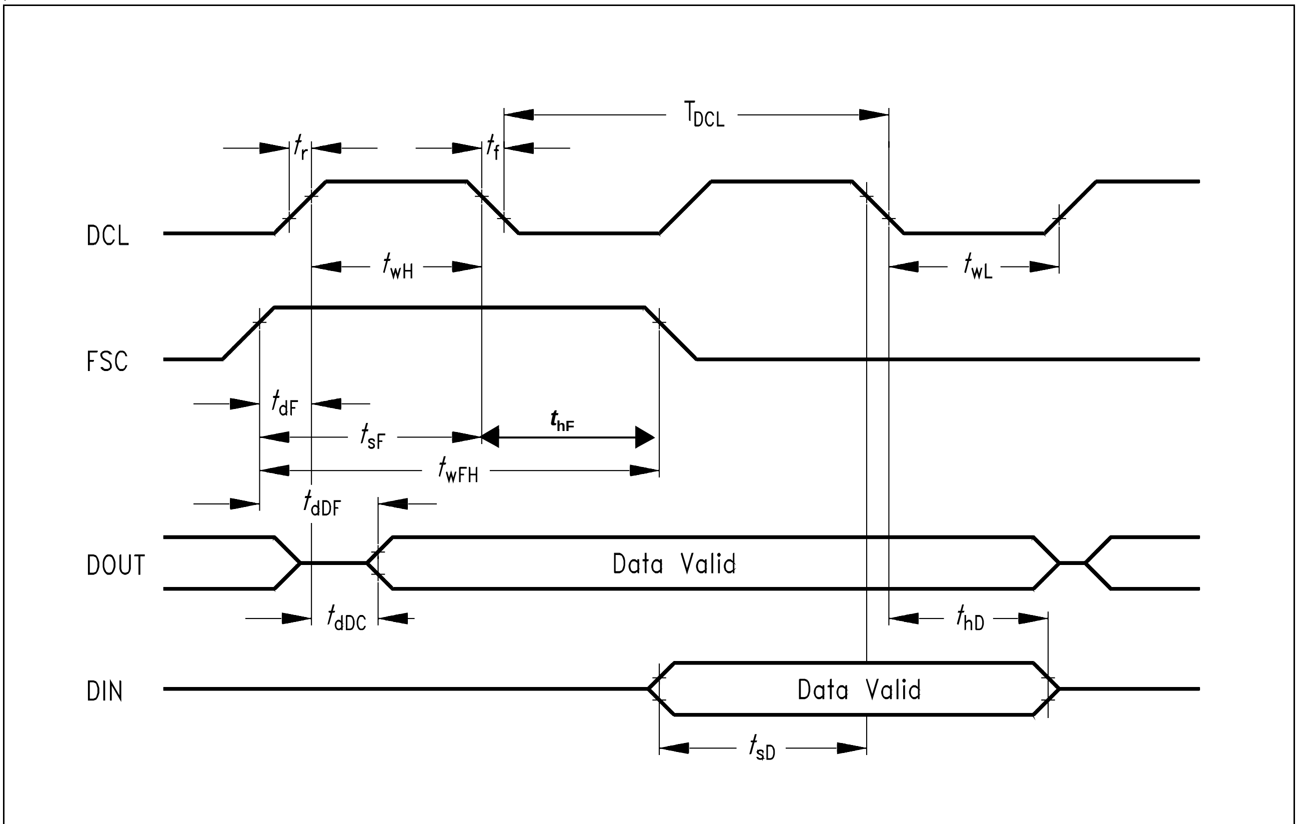


Figure 7-3 IOM®-2 Interface Timing

Table 7-1 IOM®-2 Dynamic Input Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
DCL rise/fall time	t_r, t_f			<60	ns
DCL period	T_{DCL}	122			ns
DCL pulse width, high low	t_{wH} t_{wL}	<53 <53	1/2 xT_{DCL} 1/2 xT_{DCL}		ns ns
FSC rise/fall	t_r, t_f			<60	ns
FSC setup time	t_{sF}	<30			ns
FSC hold time	t_{hF}	$t_{wFH} - t_{sF}$			ns
FSC advance	t_{dF}			$t_{wL} - 30$	ns

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
FSC pulse width, high low	t_{wFH} t_{wFL}	100 $2 \times T_{DCL}$			ns
Superframe FSC pulse width, high low	t_{wFH} t_{wFL}	100 $1 \times T_{DCL}$			ns
DIN setup time	t_{sD}	$<t_{wH} + 20$			ns
DIN hold time	t_{hD}	50			ns

Table 7-2 IOM®-2 Dynamic Output Characteristics

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
DCL Data delay clock [1]	t_{dDC}			<100	ns	C_L = 150 pF
FSC Data delay frame [1]	t_{dDF}			<150	ns	C_L = 150 pF

Notes: [1] The point of time at which the output data will be valid is referred to the rising edges of either FSC (t_{dDF}) or DCL (t_{dDC}). The rising edge of the signal appearing last (normally DCL) shall be the reference.

7.4.3 Interface to the Analog Front End

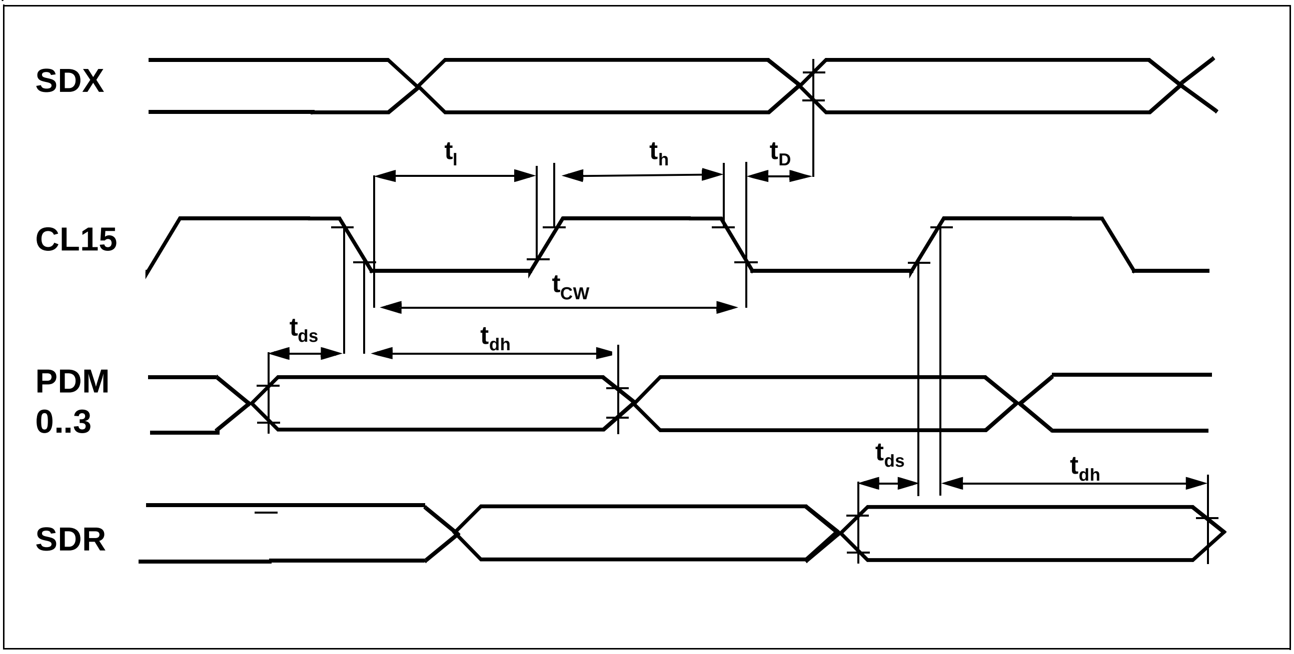


Figure 7-4 Dynamic Input and Output Requirements at the Analog Interface

Table 7-3 Dynamic Input Characteristics

Parameter	Signal	Symbol	Limit Values			Unit
			min.	typ.	max.	
Clock period	CL15	t_{cw}		65		ns
Pulse width high/ low	CL15	t_h t_l	25 25			ns ns
Data setup	SDR PDM0..3	t_{ds}	0 12			ns
Data hold	SDR PDM0..3	t_{dh}	15 8			ns

Table 7-4 Dynamic Output Characteristics

Parameter	Signal	Symbol	Limit Values			Unit
			min.	typ.	max.	
SDX data delay	SDX	t_D			22	ns

7.4.4 Boundary Scan Timing

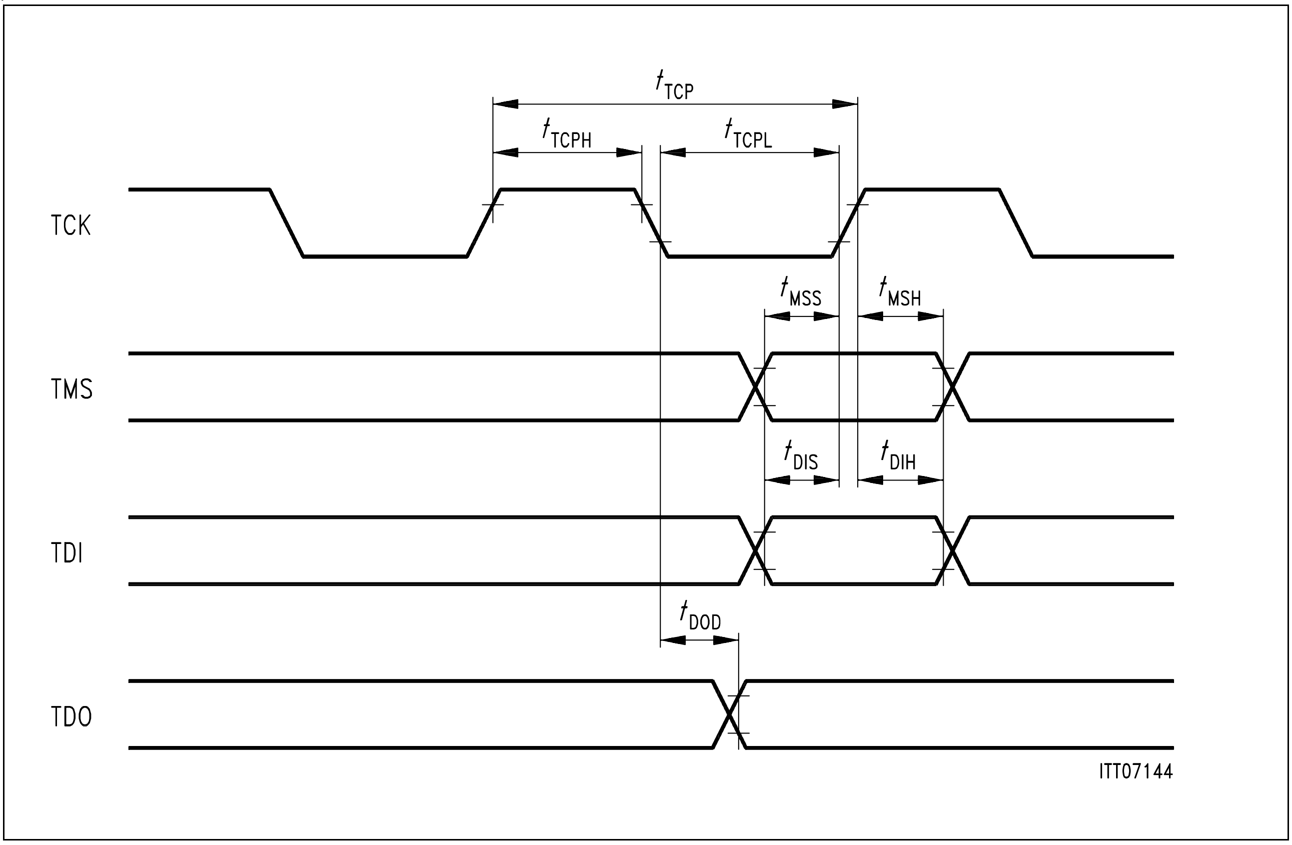


Figure 7-5 Boundary Scan Timing

Table 7-5 Boundary Scan Dynamic Timing Requirements

Parameter	Symbol	Limit Values		Unit
		min.	max.	
test clock period	t_{TCP}	160	-	ns
test clock period low	t_{TCPL}	70	-	ns
test clock period high	t_{TCPH}	70	-	ns
TMS set-up time to TCK	t_{MSS}	30	-	ns
TMS hold time from TCK	t_{MSH}	30	-	ns
TDI set-up time to TCK	t_{DIS}	30	-	ns
TDI hold time from TCK	t_{DIH}	30	-	ns
TDO valid delay from TCK	t_{DOD}	-	60	ns

7.5 Capacitances

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Clock input capacitance	C_{XIN}		TBD	pF	f_C = 1 MHz The pins, which are not under test, are connected to GND
Input capacitance	C_{IN}		7	pF	
Output capacitance	C_{OUT}		10	pF	

7.6 Power Supply

7.6.1 Supply Voltage

V_{DD} to GND = +3.3V ±0.3V

7.6.2 Power Consumption

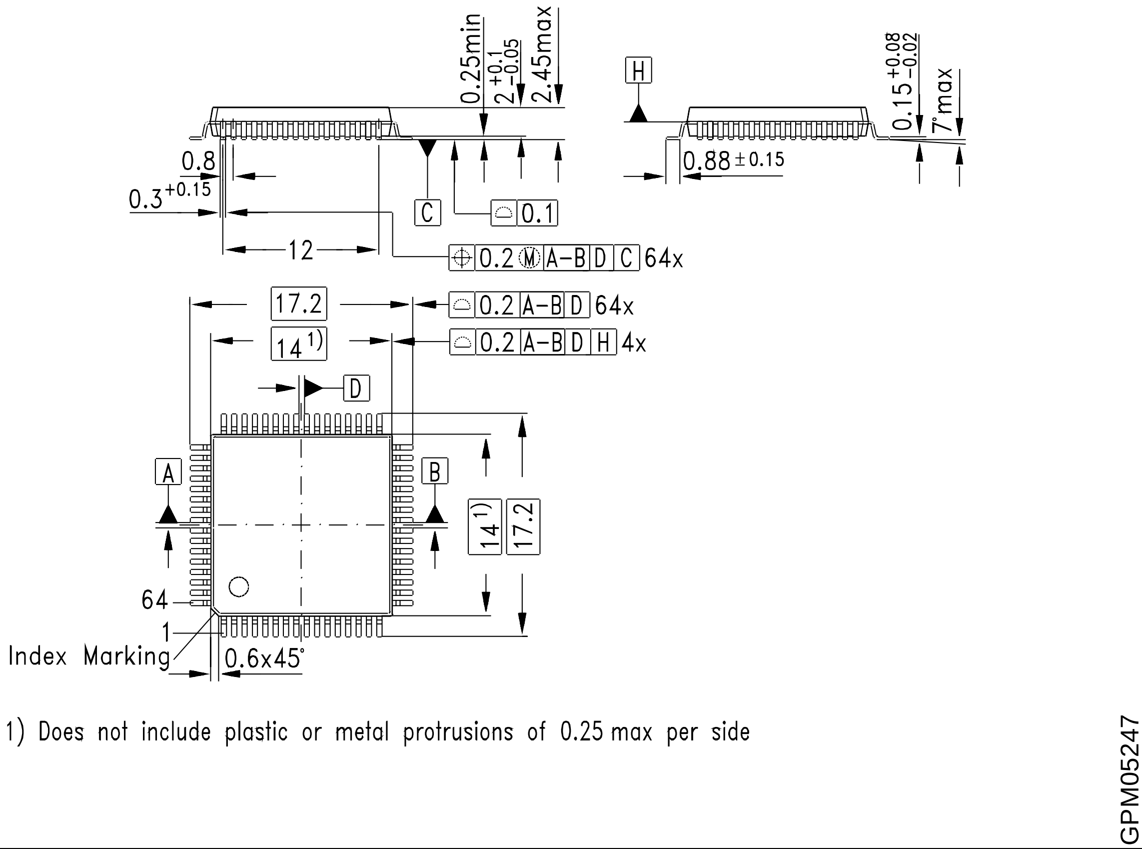
All measurements with random 2B+D data in active states, 3.3V (0°C - 70°C)

Table 7-6 Power Consumption

Mode	Typ. values	Max. values	Unit	Test conditions
Power-up all Channels	<50	<70	mA	3.3 V, open outputs, inputs at V_{DD} /V_{SS}
Power-down	<15	<25	mA	3.3 V, open outputs, inputs at V_{DD} /V_{SS}

8 Package Outlines

P-MQFP-64
(Plastic Metric Quad Flat Package)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our
Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

9 Appendix A: Standards and Specifications

The table below lists the relevant standards concerning transmission performance the DFE-Q V2.1 claims to comply with.

Organization		**Valid for**	**Document**	
ITU	International Telecommunication Union	World-wide	ITU-T G.961	Digital Transmission System on Metallic Line for ISDN Basic Rate Access
ETSI	European Telecommunications Standards Institute	EU	Technical Specification 102 080 V1.3.1 (1988-11), abbrev. TS 102 080 (formerly known as ETR 080)	Transmission and Multiplexing (TM); ISDN basic rate access; Digital transmission systems on metallic local lines
ANSI	American National Standards Institute, Inc.	USA	T1E1 4/92-004 - T1.601-1992	Basic Access Interface for Use on Metallic Loops for Application on the Network Side of the NT (Layer 1 Specification)
Telcordia Technologies Inc. (formerly known as Bellcore)		USA	TR-NWT-000393, Issue 2, December 1992	Generic Requirements for ISDN Basic Access Digital Subscriber Lines
			TR-NWT-000397, Issue 3, December 1993	ISDN Basic Access Transport System Requirements
			TR-NWT-000829, Issue 1, November 1989	OTGR: Generic Operations Interface, Embedded Operations Channel
			SR-NWT-002397, Issue 1, June 1993	Layer 1 Test Plan for ISDN Basic Access Digital Subscriber Line Transceivers
BT	British Telecommunications plc.	GB	Specification RC7355E, Issue E, 03/97	2B1Q Generic Physical Layer Specification

10 Glossary

A/D	Analog to digital
ADC	Analog to digital converter
AGC	Automatic gain control
AIN	Differential U-interface input
ANSI	American National Standardization Institute
AOUT	Differential U-interface output
B1, B2	64-kbit/s voice and data transmission channel
BIN	Differential U-interface input
BOUT	Differential U-interface output
CCRC	Corrupted CRC
C/I	Command/Indicate (channel)
CRC	Cyclic redundancy check
D	16-kbit/s data and control transmission channel
D/A	Digital-to-analog
DAC	Digital-to-analog converter
DCL	Data clock
DD	Data downstream
DT	Data through test mode
DU	Data upstream
EC	Echo canceller
EOC	Embedded operations channel
EOM	End of message
ETSI	European Telephone Standards Institute
FEBE	Far-end block error
FIFO	First-in first-out (memory)
FSC	Frame synchronizing clock
GND	Ground
HDLC	High-level data link control
IEC-Q	ISDN-echo cancellation circuit conforming to 2B1Q-transmission code
IOM®-2	ISDN-oriented modular 2nd generation

INFO	U- and S-interface signal elements as specified by ANSI/ ETSI
ISDN	Integrated services digital network
LBBD	Loop-back of B- and D-channels
LT	Line termination
MON	Monitor channel command
MR	Monitor read bit
MTO	Monitor procedure time-out
MX	Monitor transmit bit
NEBE	Near-end block error
NT	Network termination
PLL	Phase locked loop
PS	Power supply status bit
PSD	Power spectral density
PTT	Post, telephone, and telegraph administration
PU	Power-up
RMS	Root mean square
S/T	Two-wire pair interface
SSP	Send single pulses (test mode)
TE	Terminal equipment
TL	Wake-up tone sent from the LT side
TN	Wake-up tone sent from the NT side
U	Single wire pair interface
2B1Q	Transmission code requiring 80-kHz bandwidth

11 Index