

Features

- Maximum range of the input is 2 V p-p
- Power consumption 650mW
- Analog operating voltage 4.75V to 5.25V
- The converter is operated by one single power supply

General Description

The ADC10P03 is realized as high-speed pipeline architecture. The part operates on one single 5V supply.

Applications

- DST Modems
- High-speed data acquisition
- Video image processing
- Base band cellular processing (GSM)

Product Highlights

- High-speed pipeline architecture
- The ADC10P03 operates on a single 5V supply

ADC10P03

5V, 10-Bit MSPS, Pipeline ADC



AMI 0.6 micron CMOS

Electrical Characteristics

PARAMETER	MIN	TYP	MAX	UNITS
RESOLUTION		10		Bits
DC ACCURACY				
Internal Nonlinearity (INL)		plus or minus 1		LSB
Differential Nonlinearity (DNL)		plus or minus 1		LSB
No Missing Codes				
Offset Error		<0.5		%FSR
Gain Error		<1.0		%FSR
ANALOG INPUT				
Input Range		2		V p-p
Input Capacitance				pF
REFERENCE INPUT				
Reference Top Voltage		3.5		V
Reference Bottom Voltage		1.5		V
Reference Input Resistance				Ohm
Reference Input Current				mA
Reference Top Offset				mV
Reference Bottom Offset				mV
DYNAMIC PERFORMANCE				
Effective Number of Bits (ENOB)				
$f_{IN} = 10$ MHz		>8.5		Bits
$f_{IN} = X.X$ MHz				Bits
$f_{IN} = X.X$ MHz				Bits
Signal-to-Noise and Distortion Ratio (S/N+D)				
$f_{IN} = 10$ MHz		>60		dB
$f_{IN} = 2$ MHz		>72		dB
$f_{IN} = X.X$ MHz				dB
Total Harmonic Distortion (THD)				
$f_{IN} = 10$ MHz		<-60		dB
$f_{IN} = X.X$ MHz				dB
$f_{IN} = X.X$ MHz				dB
Spurious Free Dynamic Range (SFDR)				dB
Full Power Bandwidth				MHz
Differential Phase				Degree
Differential Gain				%
POWER SUPPLIES				
Operating Voltage				
V_{DD}		4.75-5.25		
DV_{DD}		4.5-5.5		
Operating Current				
$I_{AV_{DD}}$				mA
$I_{DV_{DD}}$				mA
Standby Mode				
POWER CONSUMPTION		650		mW
TEMPERATURE RANGE				°C

Digital Specifications

PARAMETER	SYMBOL	DRV _{DD}	MIN	MAX	UNITS
LOGIC INPUT					V
High Level Input Voltage	V _{IH}				V
Low Level Input Voltage	V _{IL}				V
High Level Input Current	I _{IH}				V
Low Level Input Current	I _{IL}				uA
Low Level Input Current (CLK only)	I _{IL}				uA
Input Capacitance	C _{IN}				pF
LOGIC OUTPUTS					
High Level Output Voltage (IOH = X.X uA)	V _{OH}				V
(IOH = X.XuA)					V
Low Level Output Voltage (IOL = X.X mA)	V _{OL}				V
(IOL = X.XmA)					V
Output Capacitance	C _{OUT}				pF
Output Leakage Current	I _{OZ}				uA

Specifications subject to change without notice.

Timing Specifications

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Maximum Conversion Rate ¹		20			MHz
Clock Period	t _c				ns
Clock High	t _{cH}				ns
Clock Low	t _{cL}				ns
Pipeline Delay (Latency)		4			Clk Cycles
Aperture Jitter					ps

NOTE: ¹ The initial circuit will be built using 5 V supplies for all logic and analog sections. Future circuits will allow digital operation at 3.3 V but analog operation will remain at 5 V. ² Conversionrate is operational down to 10 kHz without degradation in specified performance. ³ ENOB @ -0.5 dBFS ⁴ THD @ 0dBFS ⁵ SFDR @ 0dBFS, clk = 20 MHz

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5V, 10-Bit MSPS, Pipeline ADC



AMI 0.6 micron CMOS

Absolute Maximum Ratings

PARAMETERS		
Supply Voltage ($-V_S$)		V
Analog-to-Digital Supply Voltage Differential		V
Analog Input Voltage		V
Digital Input Voltage		V
Reference Input Voltage ($+V_{REF} - V_{REF}$)		V
Differential Reference Voltage		V
Reference Midpoint Current		mA
Digital Output Current		mA
Operating Temperature Range		°C
Storage Temperature Range		°C
Junction Temperature		°C
Lead Soldering Temperature (10 Sec.)		°C

Recommended Operating Conditions

PARAMETERS	INPUT VOLTAGE		
	MIN	NOMINAL	MAX
$-V_S$			
$+V_{REF}$			
$-V_{REF}$			
Analog Input			

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American Microsystems, Inc., 2300 Buckskin Rd., Pocatello, ID 83201, (208) 233-4690, FAX (208) 234-6796
1-800-639-7264, www.amis.com

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