HIGH-VOLTAGE MONOLITHIC IC

ECN2103

ECN2103 is a single chip row driver IC for electroluminescent (EL) display panel.

Functions

- Low-voltage serial to high-voltage parallel converter
- 60 (50) outputs of totem pole type

Features

- Output terminal voltage up to 260V
- Source / Sink current 800mA
- Pin-programmable shift direction

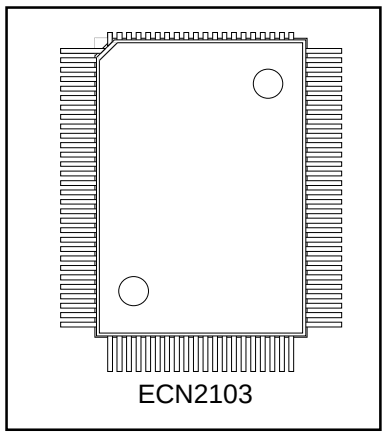
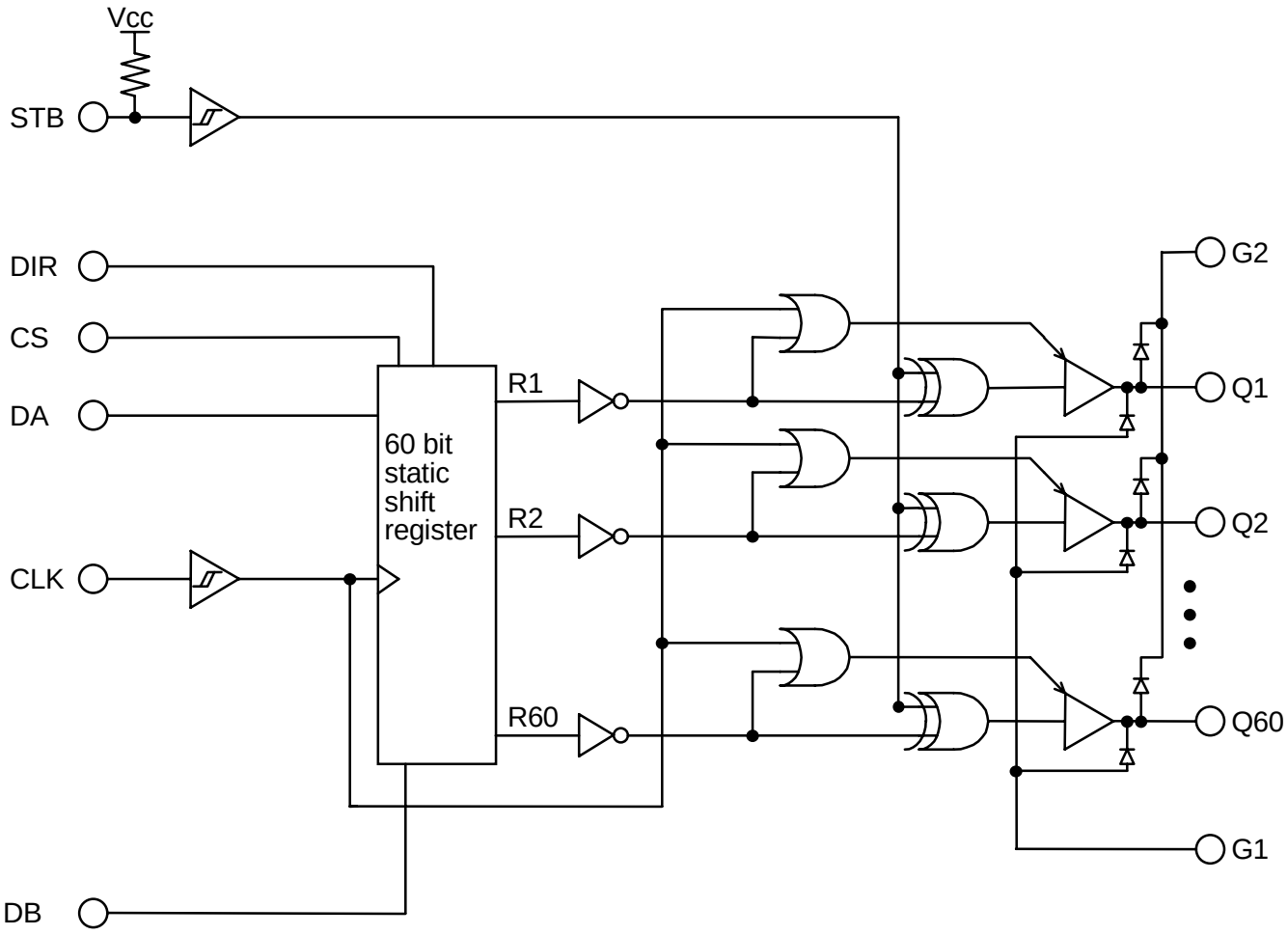


Fig. 1. OUTLINE OF TFP-80 PACKAGE



FUNCTIONAL BLOCK DIAGRAM

ECN2103

1. GENERAL

(1) TYPE ECN2103

(2) APPLICATION Row line driver for Electroluminecent (EL) display panel

(3) STRUCTURE Monolithic IC, processed Dielectric Isolation.

(4) PACKAGE TFP-80 (Fig.1)

2. MAXIMUM ALLOWABLE RATING (Ta=25°C)

No	ITEMS	SYMBOLS	RATINGS	UNITS	CONDITIONS
1	Supply Voltage (logic)	Vcc	-0.5 ~ +7.0	V	to GND terminal
2	Input Voltage (logic)	Vin	-0.5 ~ Vcc+0.5	V	to GND terminal
3	Vs to GND terminal Voltage	V_{SG}	Vcc	V	to GND terminal
4	Output Terminal Voltage	V_Q	±260	V	Between Vs,Vcc,GND, Input and Q output
5	Allowable Power Dissipation	P_T	800	mW	
6	Operating Temperature	Tj	-40 ~ +125	°C	Note 1
7	Storage Temperature	Tstg	-55 ~ +150	°C	

Note1 : Heat resistance between junction to air Rj-a=88°C/W at PCB.

3. RECOMMENDED OPERATING CONDITIONS

No	ITEMS	SYMBOLS	Min.	Typ.	Max.	UNIT	CONDITIONS
1	Supply Voltage (logic)	Vcc	4.5	5.0	6.0	V	
2	Clock Frequency	f_{CLK}	-	-	250	kHz	Vcc = 5V
3	Clock Pulse Width	tw_{CLK}	80	-	-	ns	Vin = 0V / 5V
4	Data Setup Time	t_{su}	80	-	-	ns	
5	Data Hold Time	t_h	80	-	-	ns	
6	Output Terminal Voltage	V_Q	-	±250	-	V	Vcc = 5V
7	Peak Output Source Current	$H_{IOH}1$	-	-	-500	mA	Note 1
	(Source SCR, Sink Diode)	$H_{IOH}2$	-	-	-800	mA	Note 2
8	Peak Output Sink Current	$H_{IOL}1$	-	-	+500	mA	Note 1
	(Sink SCR, Source Diode)	$H_{IOL}2$	-	-	+800	mA	Note 2

Note1 : Conduction period ≤ 5 μs per 1 IC

Note2 : Conduction period ≤ 2 μs per 1 IC

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4. ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta=25°C,VCC=5V,HVCC=250V)

No	ITEMS		SYMBOLS	Min.	Typ.	Max.	UNIT	CONDITIONS	
1	Output Voltage (logic)		V_{OL}	-	-	0.1	V	I_{OL}= 20μA	
			V_{OH}	4.9	-	-	V	I_{OH}=-20μA	
2	Output Current (logic)		I_{OL}	1.0	-	-	mA	V_{OL}= 0.8V	
			I_{OH}	-1.0	-	-	mA	V_{OH}= 4.2V	
3	Input Voltage (logic)		V_{IL}	-	-	1.0	V	DB,DA,DIR,CS input	
			V_{IH}	3.5	-	-	V		
			V_{THL}	-	-	0.4	V	CLK,STB input	
			V_{TLH}	3.5	-	-	V		
4	Input Current (logic)		I_{IH}	-	-	10	μA	Vin=5V all input (per 1 input)	
			I_{IL}	-	-	-10	μA	Vin=0V DB,DA,CLK,DIR,CS (per 1 input)	
				-	-	-100	μA	Vin=0V STB (per 1 input)	
5	Dissipation Current (logic)		Istb	-	-	100	μA	No signal all input 5V, all output Off	
				-	-	25	mA	No signal, 1ch source output On	
				-	-	5	mA	No signal, 1ch sink output On	
6	Output Voltage	(SCRs)	H_{VOL}	-	-	3.0	V	H_{IOL}=1mA	Q out-GND
				-	-	10.0	V	H_{IOL}=300mA	Q out-GND
			H_{VOH}	-	-	4.0	V	H_{IOH}=-1mA	V_S-Q out
				-	-	12.0	V	H_{IOH}=-300mA	V_S-Q out
		(Diodes)	H_{VOL}	-	-	3.0	V	H_{IOL}=1mA	G1- Q out
				-	-	10.0	V	H_{IOL}=300mA	G1- Q out
			H_{VOH}	-	-	4.0	V	H_{IOH}=-1mA	Q out-G2
				-	-	15.0	V	H_{IOH}=-300mA	Q out-G2
7	Output SCR dv/dt capability		dv/dt1	200	-	-	V/μs	Vs-Q out, +dv/dt apply (fig.7)	
			dv/dt2	200	-	-	V/μs	Q out-GND, -dv/dt apply (fig.8)	
8	Output device Off Period		t_{p+}	-	-	15	μs	Source side charge (fig.9)	
			t_{p-}	-	-	15	μs	Source side discharge	
	(Don't use under this period)		t_{n+}	-	-	15	μs	Sink side charge (fig.9)	
			t_{n-}	-	-	15	μs	Sink side discharge	

5. SWITCHING CHARACTERISTICS (Unless otherwise specified, Ta= 25°C, Vcc= 5V)

No	ITEMS	SYMBOLS	Min.	Typ.	Max.	UNIT	CONDITIONS
1	Output Delay Time (logic)	t_{PLH}	-	-	300	ns	CL=15pF
		t_{PHL}	-	-	300	ns	(shown fig.6)
2	Output Delay Time	t_{QLH}	-	-	3	μs	RLQ=1kΩ
		t_{QHL}	-	-	3	μs	CLQ=2000pF (shown fig.6)

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6. FUNCTION TABLE

	CONTROL INPUT					SHIF REGISTER	OUTPUT	
	CLK	D	DIR	CS	STB	Rn	SO(Note 1)	Q
SHIFT OPERATION	↑	*	*	*	*	shift	—	—
	no↑	*	*	*	*	keep		
	*	*	H	*	*	R1→R60	R60	
	*	*	L	*	*	R60→R1	R1 or R11	
	*	*	*	H	*	11-60ch(Note 4)	—	
	*	*	*	L	*	1-60ch		
OUTPUT OPERATION	L	*	*	*	H	H	—	H (Note 2)
						L		OFF
				(Note 4)	L	H		L (Note 3)
						L		OFF
	H	*	*	*	*	*		ALL OFF

Note ((D:DB , SO:DA) or (D:DA , SO:DB))

(Note 1) 60th data is pushed out as output at the state of down edge↓ of clock signal.

(Note 2) When shift register is "H", source SCR of Q output is driven to ON.

(Note 3) When shift register is "H", sink SCR of Q output is driven to ON.

(Note 4) When CS input is "L" , shift registers R1 - R60 are usable. When CS input is "H", R1-R10 are invalid, and passed.

When DIR input is "H", inputted data is transported to R1 (or R11). When DIR input is "L", inputted data is transported to R60.

When power is ON, shift registers R1-R60 are not confirmed. CS input is "H", the data "L" is transported to R1 (or R11).

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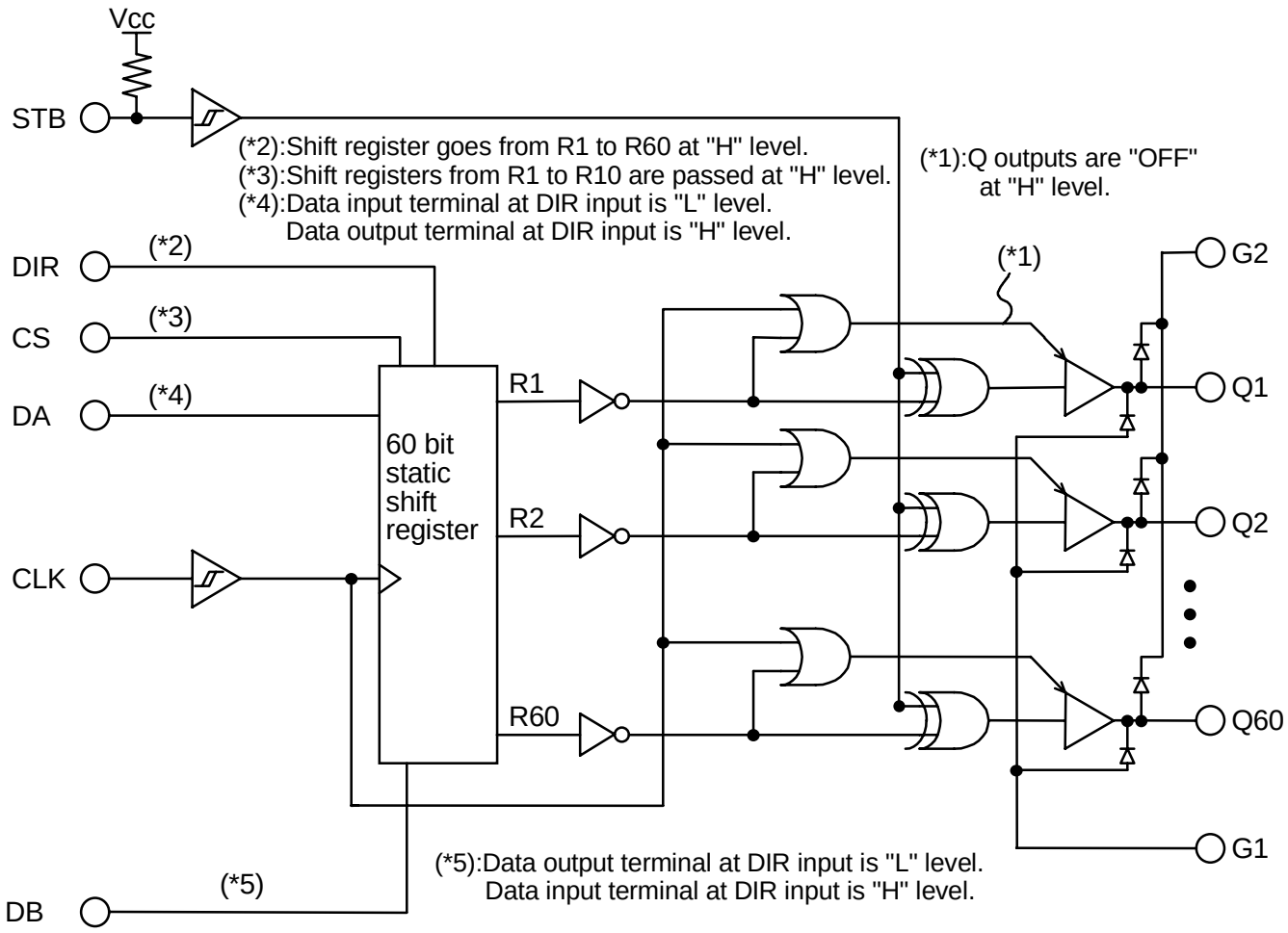

Fig. 2. FUNCTIONAL BLOCK DIAGRAM

7. INPUT/OUTPUT CIRCUIT

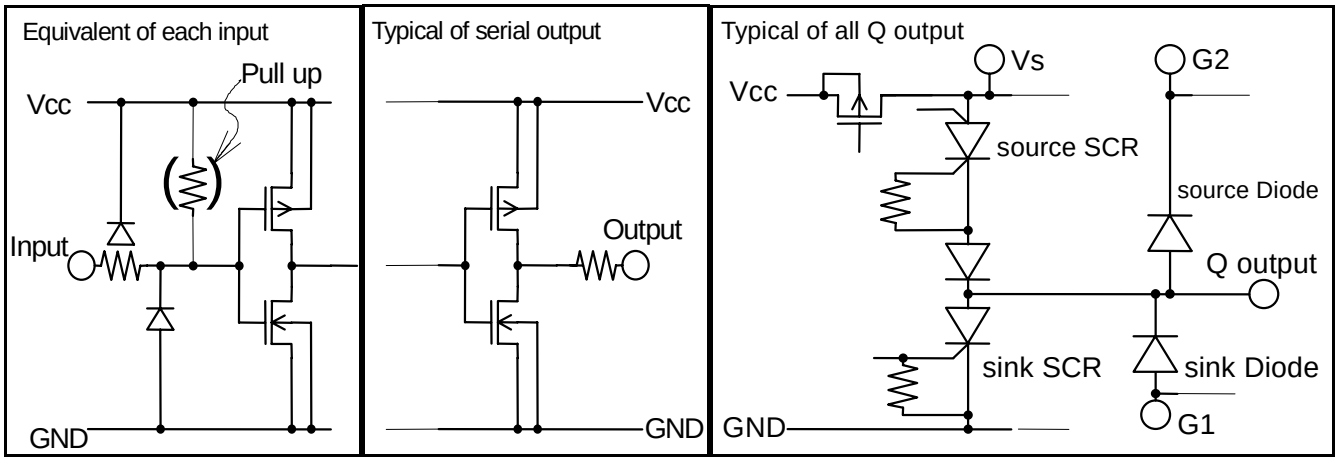

Fig. 3. Input/Output Circuit

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8. EXAMPLE OF OPERATING TIMING CHART

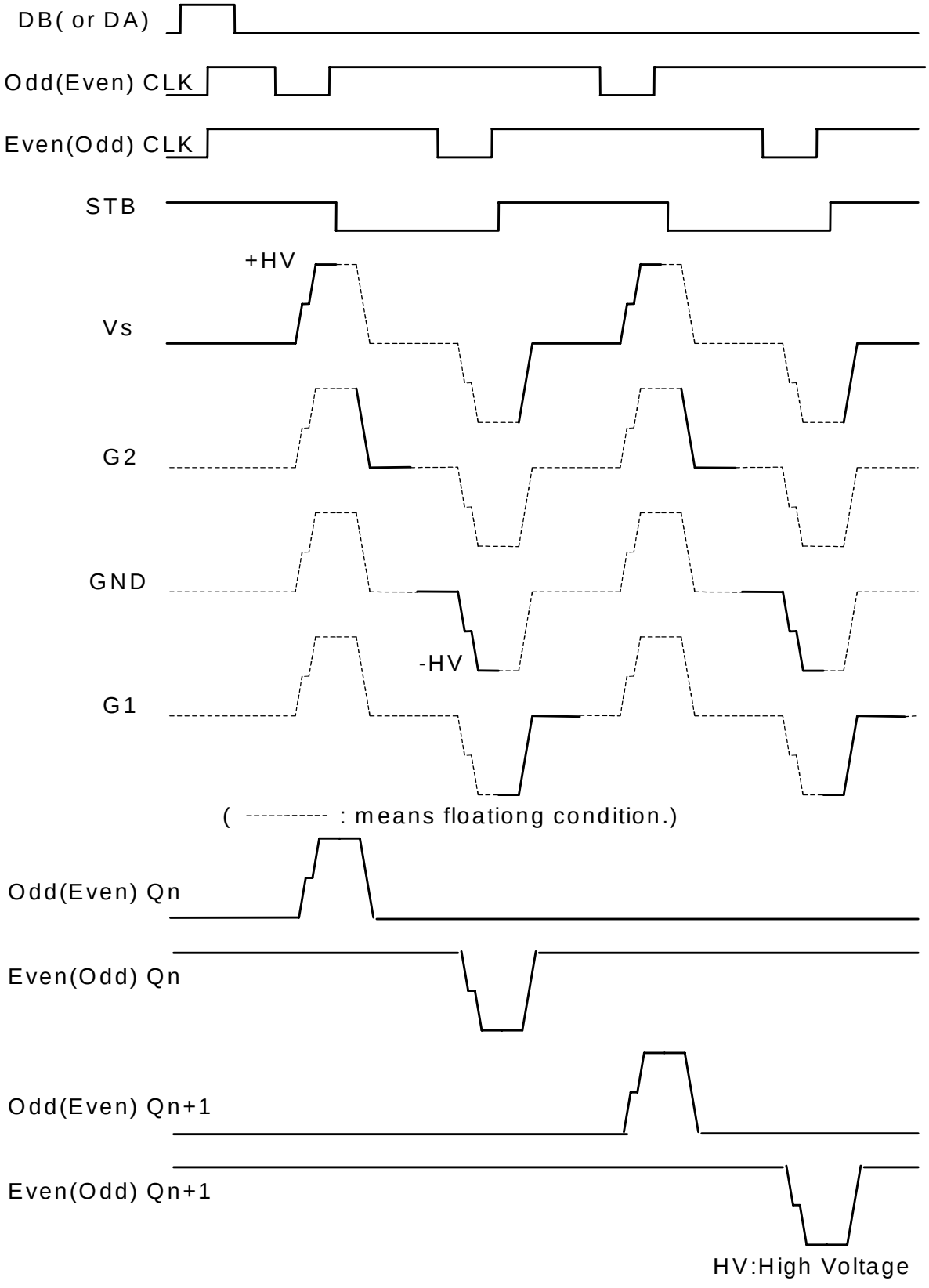

Fig. 4. Example of Operating Timing Chart

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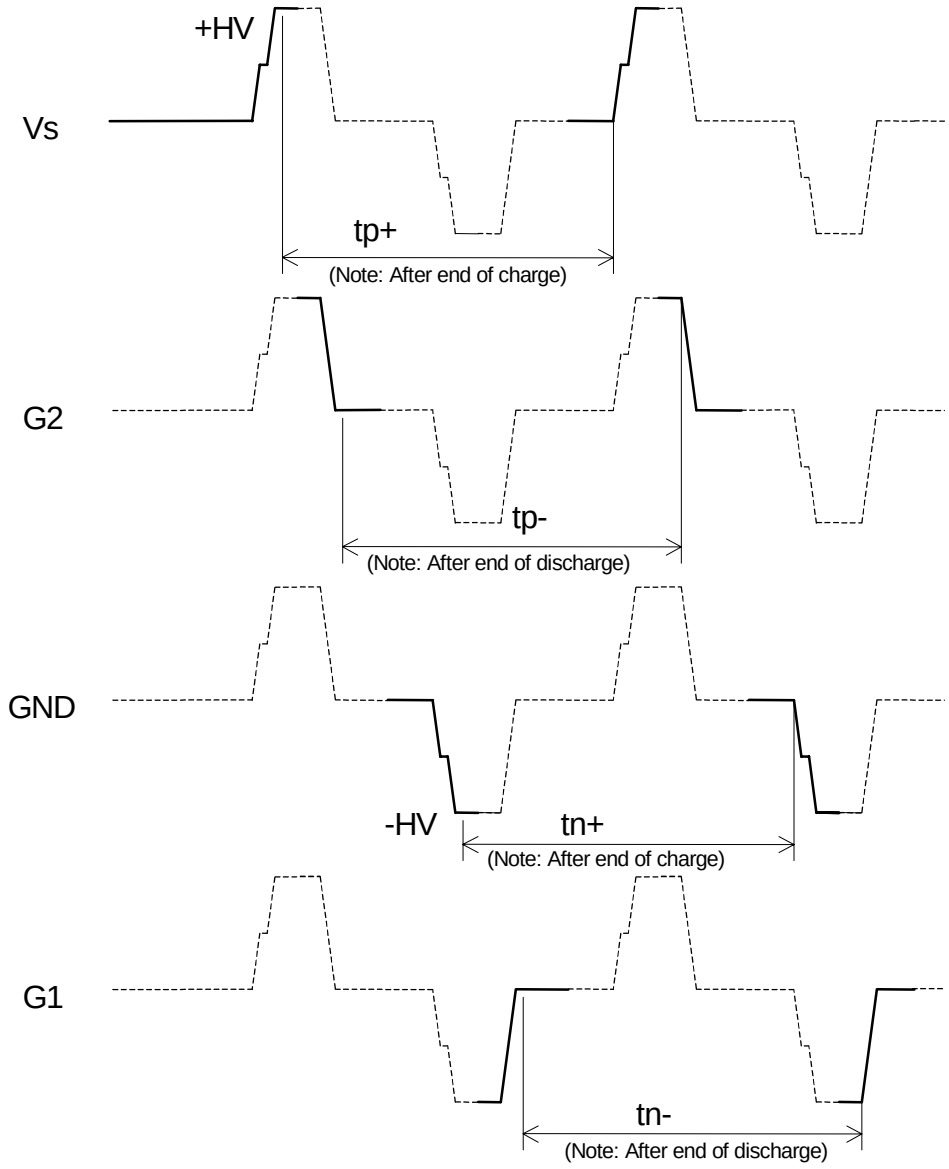

Fig. 5. Timing of off period of output devices.

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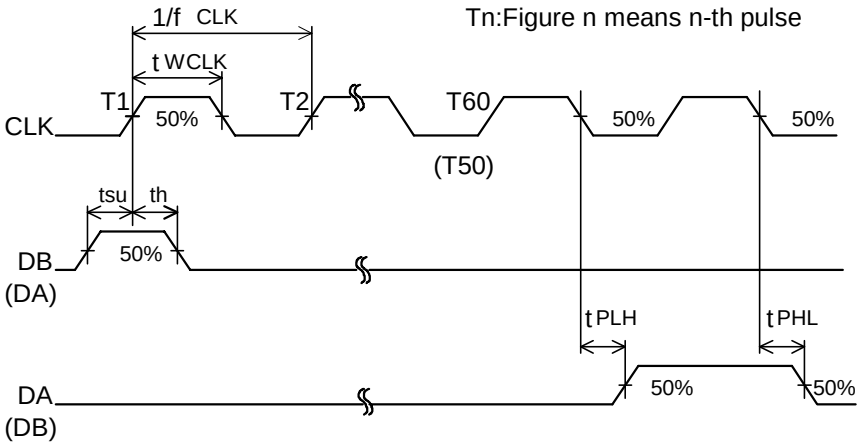
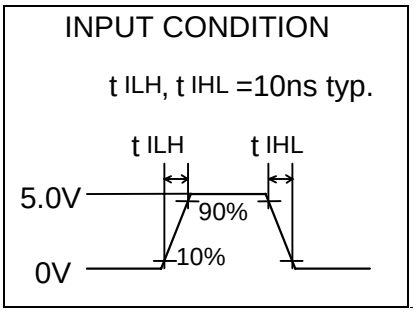
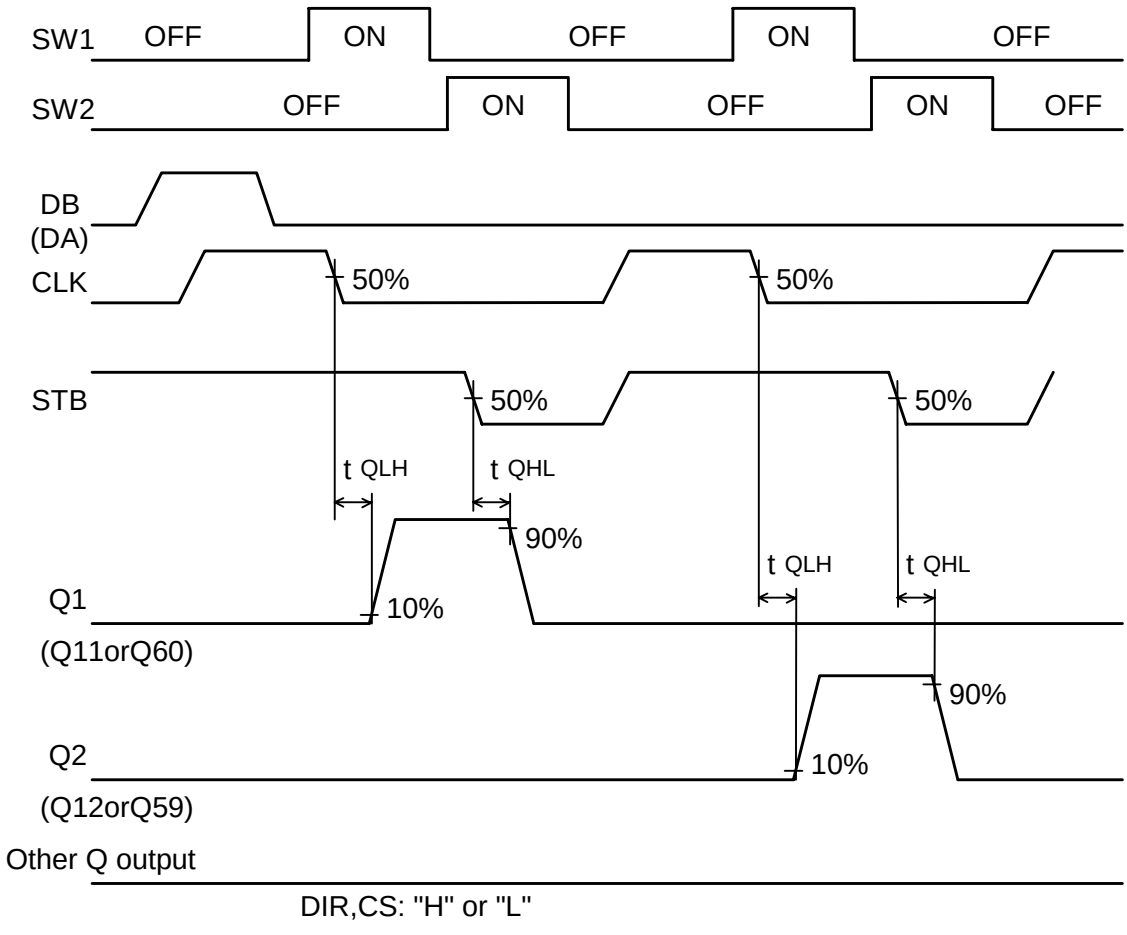
9. MEASUREMENT AND MEASUREMENT CIRCUIT





(a) Shift Function (SW1→OFF, SW2,3→ON)



(b) Output Function (SW3→OFF)

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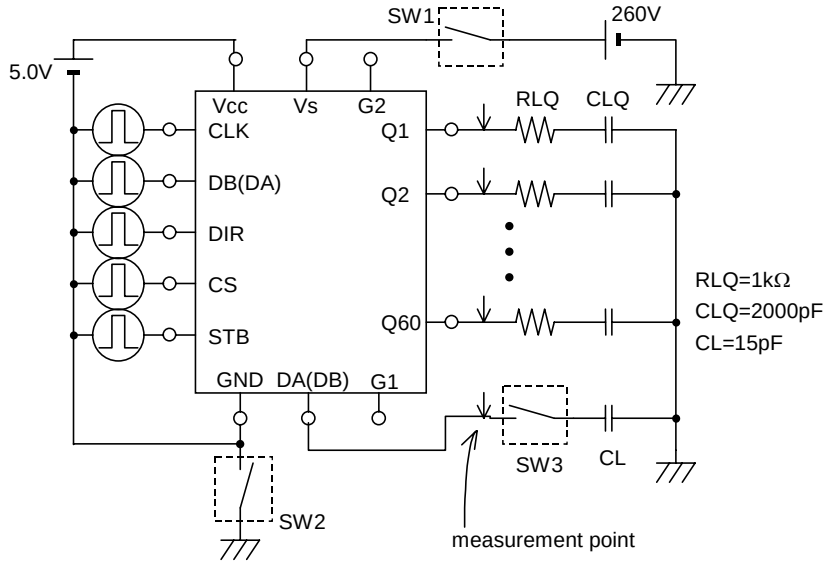

Fig. 6. Switching Characteristics Measurement Circuit

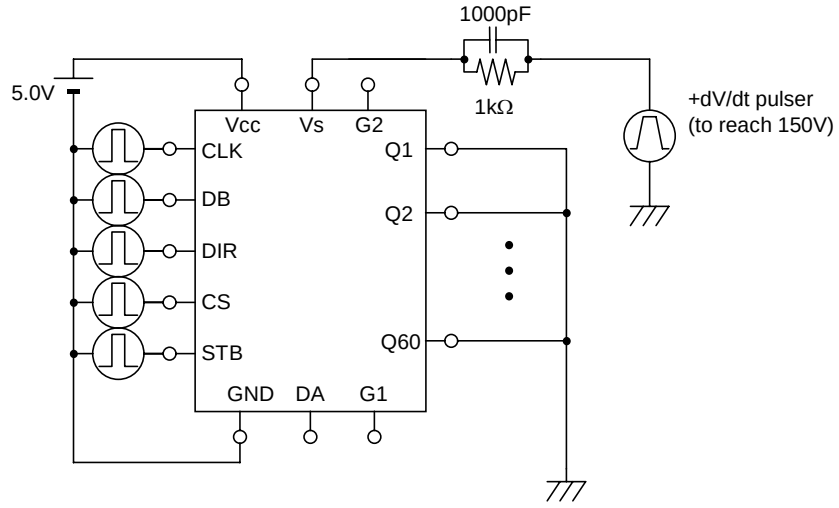

Fig. 7. Output SCR dV/dt capability (dV/dt1) Measurement Circuit

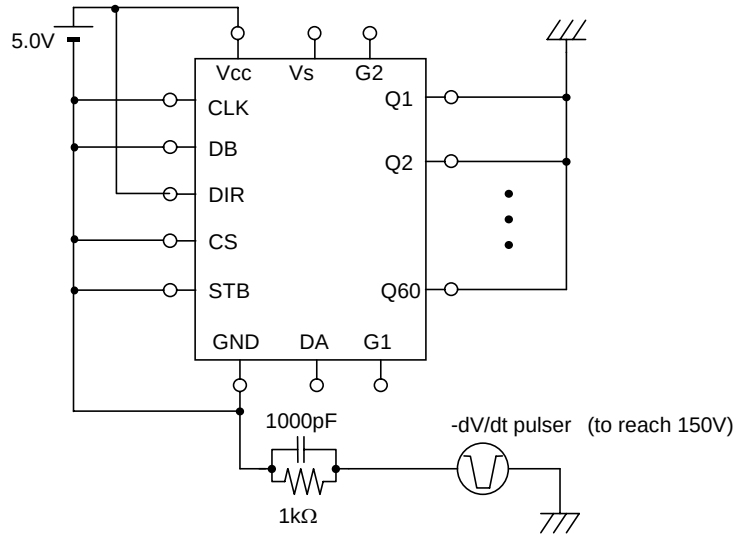

Fig. 8. Output SCR dV/dt capability (dV/dt2) Measurement Circuit

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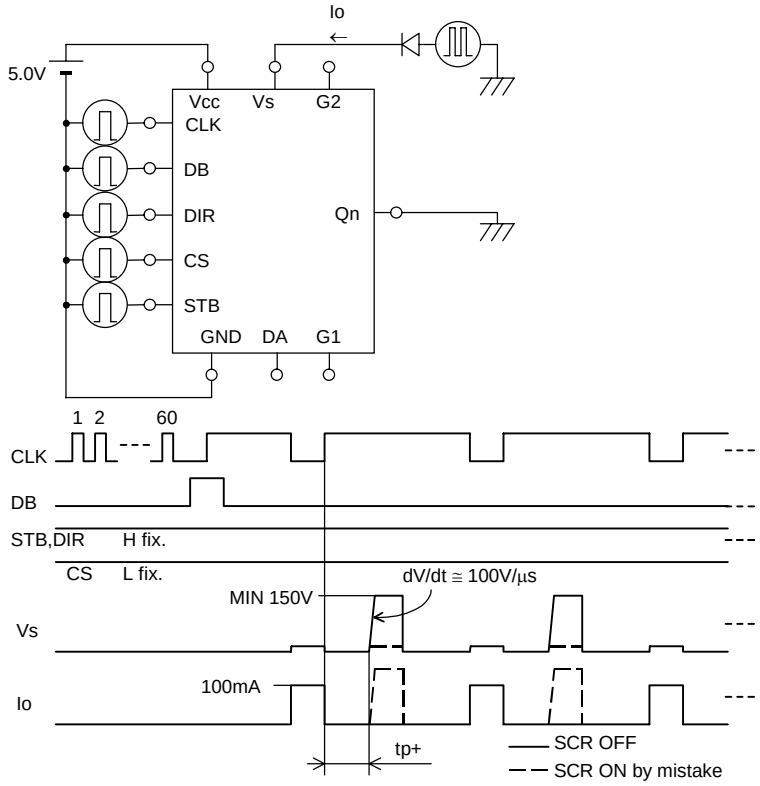
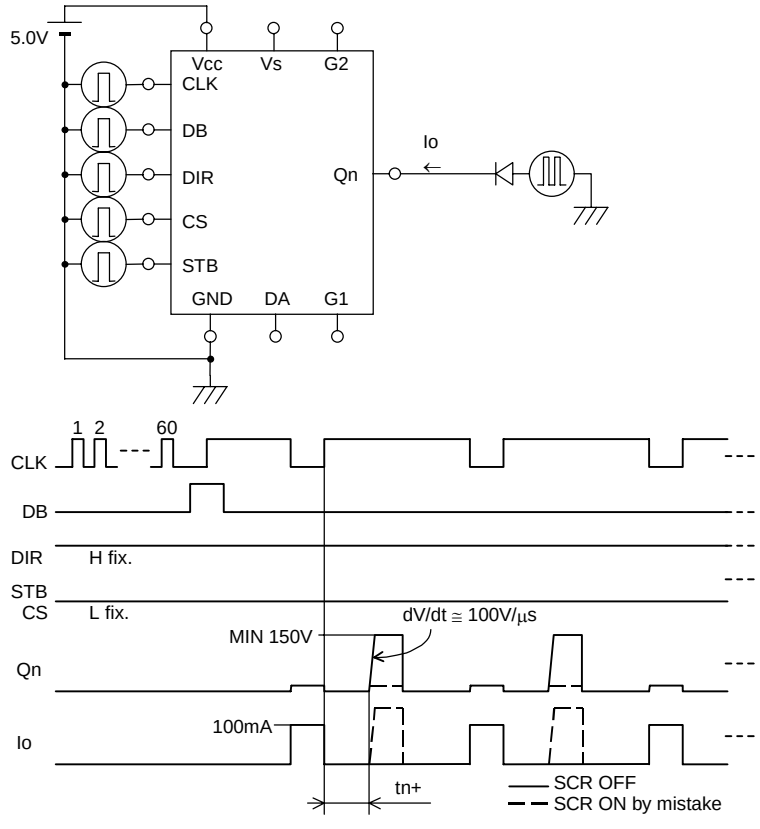


(a) Source SCR



(b) Sink SCR

Fig. 9. Output SCR Off Period (tp+,tn+) Measurement

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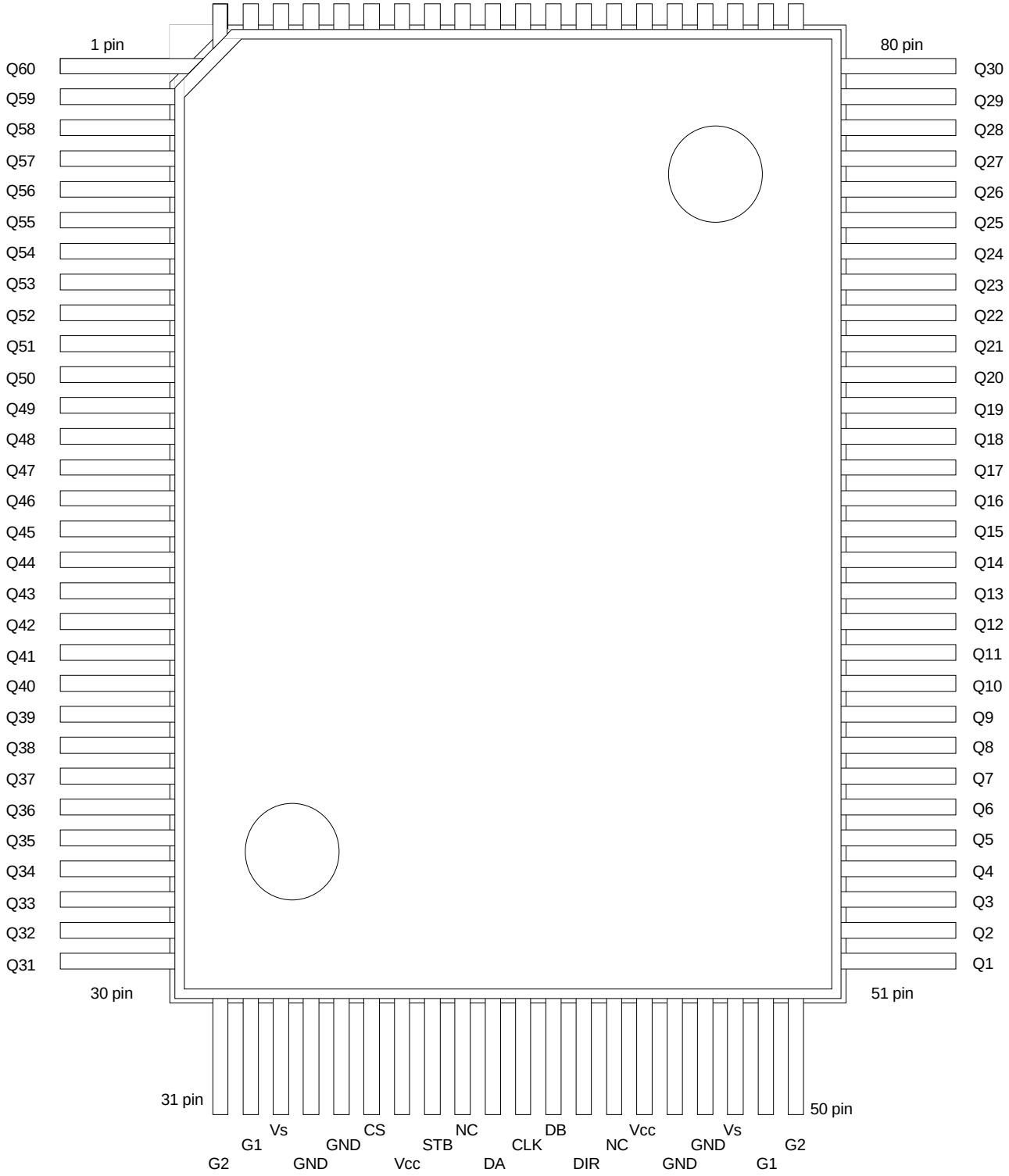
10. PIN LOCATION



Terminal interval : 0.65mm.

This Figure doesn't show package outline dimensions.

Fig. 10. Pin Location (Top view) for ECN2103

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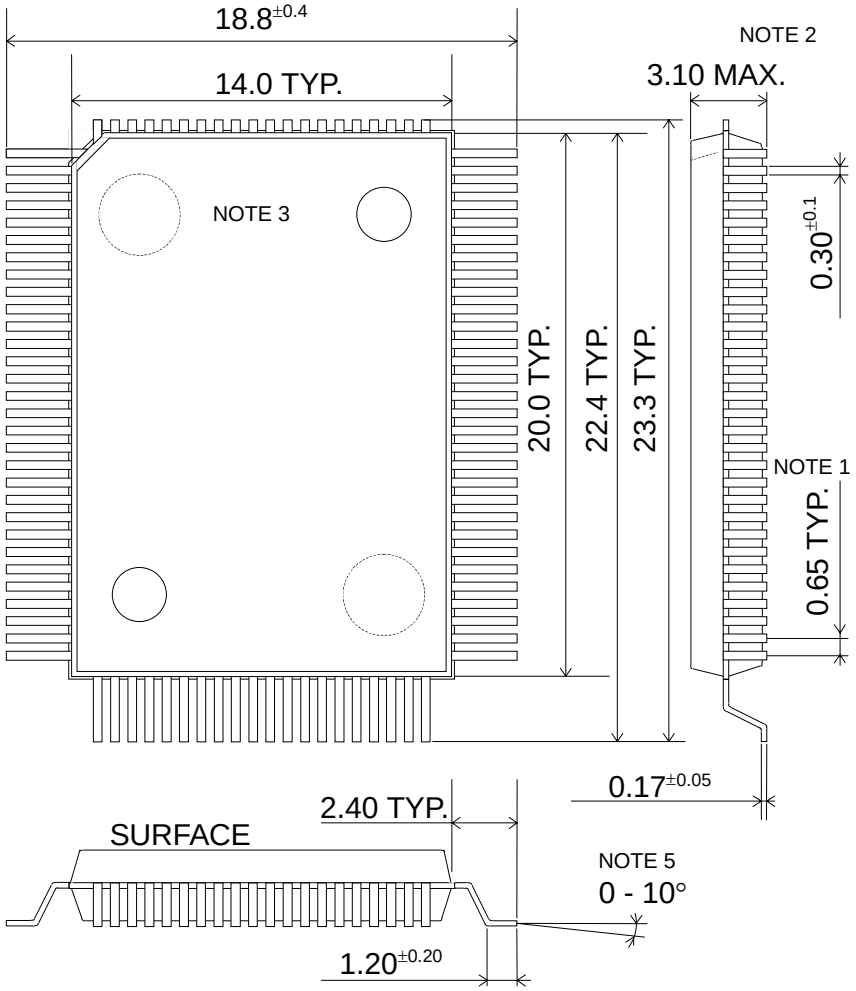
11. PACKAGE OUTLINE (Unit : mm)



Notes.

1. THIS DIMENSION IS MEASURED AT ROOT OF LEAD. SPACING AT TIP OF LEAD IS MIN 0.1.
2. THIS DIMENSION INCLUDES A WARPAGE OF PACKAGE.
3. MARKING IS ON THE SURFACE OF PACKAGE, INCLUDING HITACHI MARK, TYPE NAME, LOT NUMBER, AND JAPAN MARK.
4. LEADS ARE SOLDER PLATED.
5. THIS IS THE BENDING ANGLE WITH HORIZONTAL PLANE.

Fig. 11. Package outline

HITACHI POWER SEMICONDUCTORS

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