



## TRI-STATE® 7-Segment to BCD Decoder

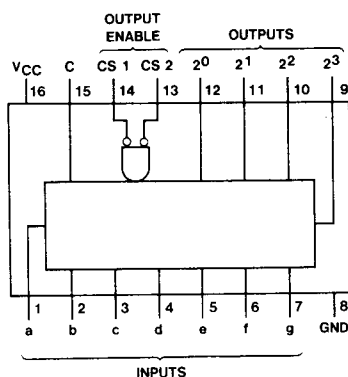
### General Description

These circuits are low power converters which accept 7-segment data on the inputs, and provide binary-coded decimal (BCD) data on the outputs. An input control line is also provided, in the event that the 7-segment input data is presented in inverted form. The BCD outputs are normally of the standard totem-pole TTL type, however they may also be converted to high-impedance (TRI-STATE) types by applying a high logic level to either of the two output enable pins.

### Features

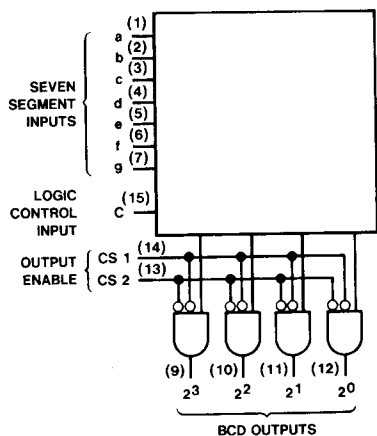
- TRI-STATE outputs
- Typical power dissipation 75 mW
- Typical propagation delay 70 ns

### Connection Diagram



76L25(J,W); 86L25 (N)

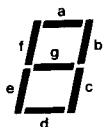
### Logic Diagram



### Truth Table

Digit	a	b	c	d	e	f	g	CTL	CS 1	CS 2	2 <sup>3</sup>	2 <sup>2</sup>	2 <sup>1</sup>	2 <sup>0</sup>
0	H	H	H	H	H	H	L	H	L	L	L	L	L	L
1	L	H	H	L	L	L	L	H	L	L	L	L	L	L
2	L	H	L	H	H	L	H	H	L	L	L	L	H	L
3	H	H	H	H	L	L	H	H	L	L	L	L	L	H
4	L	H	H	L	L	H	H	H	L	L	L	H	L	L
5	H	L	H	H	L	H	H	H	L	L	L	L	H	L
6	L	L	H	H	H	H	H	H	L	L	L	L	H	H
7	H	L	H	H	H	H	H	H	L	L	L	L	H	H
8	H	H	H	L	L	L	L	H	L	L	L	L	H	L
9	H	H	H	L	L	H	H	H	L	L	L	L	H	L
9	H	H	H	L	L	H	H	H	L	L	L	L	H	L
BLANK	L	L	L	L	L	L	L	H	L	L	L	L	H	H
L	L	L	L	H	H	H	L	H	L	L	L	H	H	L
E	H	L	L	H	H	H	H	H	L	L	L	H	H	L
R	H	H	H	L	H	H	H	H	L	L	L	H	L	H
P	H	H	L	L	H	H	H	H	L	L	L	H	L	H
-	L	L	L	L	L	L	L	H	L	L	L	H	H	L
0	L	L	L	L	L	L	L	H	L	L	L	L	L	L
1	H	L	L	H	H	H	H	L	L	L	L	L	L	H
2	L	L	H	L	L	H	L	L	L	L	L	L	L	H
3	L	L	L	L	H	H	L	L	L	L	L	L	L	H
4	H	L	L	H	H	L	L	L	L	L	L	L	H	L
5	L	L	L	L	H	L	L	L	L	L	L	L	H	L
6	H	H	L	L	L	L	L	L	L	L	L	L	H	H
7	L	H	L	L	L	L	L	L	L	L	L	L	H	H
8	L	L	L	L	H	H	H	H	L	L	L	L	L	H
9	L	L	L	L	L	L	L	L	L	L	L	L	H	L
9	L	L	L	L	H	H	L	L	L	L	L	L	H	L
9	L	L	L	L	H	L	L	L	L	L	L	L	H	L
BLANK	H	H	H	H	H	H	H	L	L	L	L	H	H	H
L	H	H	H	L	L	L	L	L	L	L	L	H	H	L
E	L	H	H	L	L	L	L	L	L	L	L	H	H	L
R	L	L	L	L	L	L	L	L	L	L	L	L	H	L
P	L	L	H	H	L	L	L	L	L	L	L	H	L	H
-	H	H	H	H	H	H	L	L	L	L	L	H	H	L
X	X	X	X	X	X	X	X	X	H	X	Z	Z	Z	Z
X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z
All Other Input Combinations	L	L	L	L	L	L	L	L	L	L	H	H	H	H

### Segment Identification



H = High Level (Steady State)  
 L = Low Level (Steady State)  
 Z = High Impedance  
 X = Don't Care



## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

Parameter	Conditions	DM76			DM86			Units		
		L25			L25					
		Min	Typ (1)	Max	Min	Typ (1)	Max			
V <sub>IH</sub>	High Level Input Voltage	2			2			V		
V <sub>IL</sub>	Low Level Input Voltage			0.7			0.7	V		
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = -12 mA							V	
I <sub>OH</sub>	High Level Output Current			-1.0			-1.0	mA		
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, V <sub>IH</sub> = 2 V V <sub>IL</sub> = 0.7 V, I <sub>OH</sub> = -1.0 mA			2.4		2.4		V	
I <sub>OL</sub>	Low Level Output Current			2.0			3.6	mA		
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, V <sub>IH</sub> = 2 V V <sub>IL</sub> = 0.7 V, I <sub>OL</sub> = Max			0.3		0.4	V		
I <sub>O(OFF)</sub>	Off State (High Impedance State) Output Current	V <sub>CC</sub> = Max, V <sub>IH</sub> = 2 V V <sub>IL</sub> = 0.7 V		V <sub>O</sub> = 0.3 V	-40		-40	μA		
				V <sub>O</sub> = 2.4 V	40		40			
I <sub>I</sub>	Input Current at Maximum Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 5.5 V				100		100	μA	
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 2.4 V				10		10	μA	
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 0.3 V				-180		-180	μA	
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (2)			-6	-30	-6	-30	mA	
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 0 V				15	20	15	20	mA

Note 1: All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

Note 2: Not more than one output should be shorted at a time.

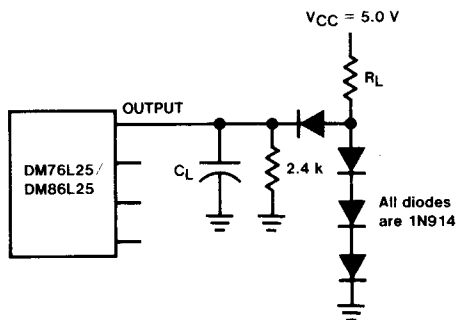
## Switching Characteristics

V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

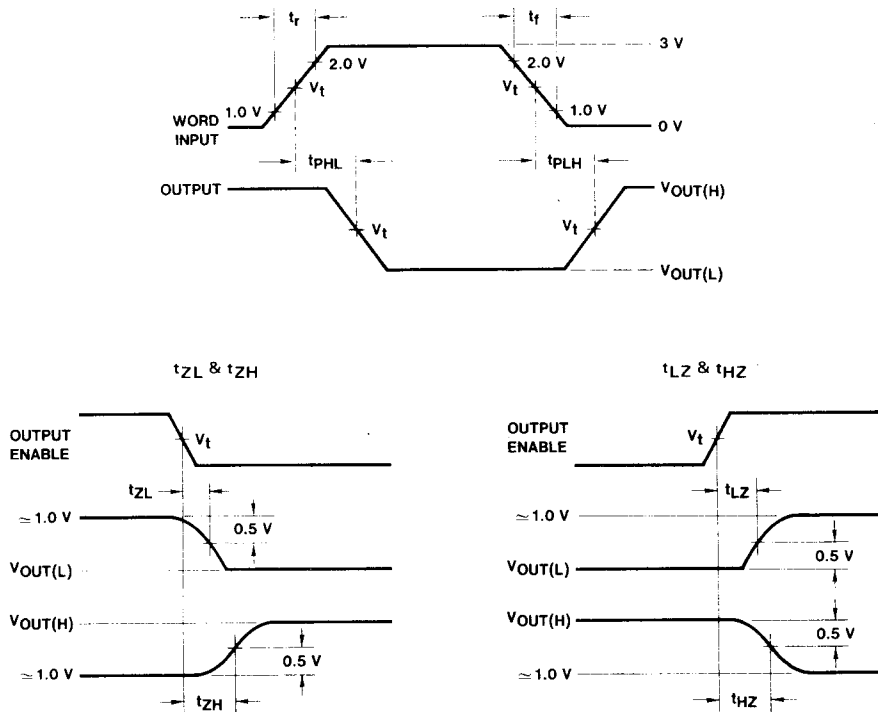
Parameter	From (Input)	To (Output)	Conditions	DM76/86			Units
				L25			
				Min	Typ	Max	
t <sub>PLH</sub>	Propogation Delay Time, Low-to-High Level Output	Data	Output		86	130	ns
t <sub>PHL</sub>	Propogation Delay Time, High-to-Low Level Output	Data	Output		55	85	ns
t <sub>ZH</sub>	Output Enable Time to High Level			C <sub>L</sub> = 50 pF R <sub>L</sub> = 4 kΩ	34	51	ns
t <sub>ZL</sub>	Output Enable Time to Low Level				47	70	ns
t <sub>HZ</sub>	Output Disable Time from High Level			C <sub>L</sub> = 5 pF R <sub>L</sub> = 4 kΩ	15	23	ns
t <sub>LZ</sub>	Output Disable Time from Low Level				57	86	ns



### AC Test Circuit



### Switching Time Waveforms



Note: The pulse generator has the following characteristics:  $V = 3.0\text{ V}$ ,  $t_r = 15\text{ ns}$ ,  $t_f = 5.0\text{ ns}$ ,  $F = 500\text{ kHz}$ , duty cycle = 50%,  $Z_{OUT} = 50\Omega$ ,  $V_t = 1.3\text{ V}$  @  $25^\circ\text{C}$ .