

Product Preview
Numerically Controlled Oscillator

Motorola's gallium arsenide (GaAs) 120NCO is a high-speed integrated circuit developed to support the special requirements of very high performance Direct Digital Synthesizer (DDS) circuits. The device provides for 84 signal lines and two different power supplies. Signals are carried on 50 Ω controlled impedance transmission lines between the package leads and the cavity bond pads. Excellent signal isolation is provided by multiple ground pins among the signal pins.

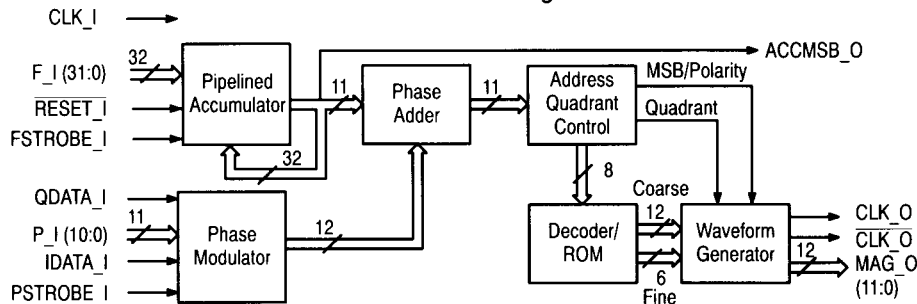
Internal ground and power planes and decoupling capacitors minimize switching noise on the power supplies.

The 120NCO is a key element in equipment such as ground-based transmitters and receivers, special test equipment, and any system which requires precise frequency resolution.

For additional information on Direct Digital Synthesis, see data sheet 120DDSEVK/D.

- 32-Bit Frequency Resolution
- 12-Bit Parallel Sine Output
- 11-Bit Phase Modulation Ports
- Direct PSK and DPSK Modulation Ports
- Clock Speed guaranteed to 300 MHz
- Spectral Purity: (worst case spur)
 - 66 dBc 12-Bits
 - 59 dBc 10-Bits
 - 46 dBc 8-Bits

GaAs NCO Block Diagram



FOR MORE INFORMATION CONTACT
MPO MARKETING (602) 897-3850

120NCO



AVAILABLE AS

- 1) JAN: N/A
- 2) SMD: N/A
- 3) 883: N/A
- 4) Commercial: Planned

**X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CLCC: U**

XX = Speed in ns (XX)

PIN NAMES

VCC	+ 5.0 V Power Supply
VEE	- 5.2 V Power Supply
VSS	Ground
CLK_I	Main Clock Input
F_I (31:0)	Frequency Word Input
P_I (10:0)	Phase Word Input
IDATA_I	I Data Modulation Input
QDATA_I	Q Data Modulation Input
FSTROBE_I	Frequency Strobe
PSTROBE_I	Phase Strobe
RESET_I	Reset
MAG_O (11:0)	Amplitude Word Output
CLK_O	Clock Output
CLK_O	Inverted Clock Output
TEST_ACC7_O	Accumulator Bit 7 Output
TEST_ACC15_O	Accumulator Bit 15 Output
ACCMSB_O	Accumulator MSB Output

PIN ASSIGNMENTS							
Function	CLCC	Function	CLCC	Function	CLCC	Function	CLCC
VEE	1	VCC	34	VEE	67	VCC	100
N.C.	2	F_I11	35	ACCMSB_O	68	CLK_O	101
N.C.	3	F_I12	36	PSTROBE_I	69	CLK_O	102
GND	4	GND	37	GND	70	GND	103
N.C.	5	F_I13	38	QDATA_I	71	MAG_O11	104
N.C.	6	F_I14	39	IDATA_I	72	MAG_O10	105
GND	7	GND	40	GND	73	GND	106
N.C.	8	F_I15	41	P_I0	74	N.C.	107
N.C.	9	F_I16	42	P_I1	75	MAG_O9	108
GND	10	GND	43	GND	76	GND	109
TEST_ACC7_0	11	F_I17	44	P_I2	77	MAG_O8	110
TEST_ACC15_0	12	F_I18	45	P_I3	78	N.C.	111
GND	13	GND	46	GND	79	GND	112
RESET_I	14	F_I19	47	P_I4	80	MAG_O7	113
F_I0	15	F_I20	48	P_I5	81	MAG_O6	114
GND	16	GND	49	GND	82	GND	115
F_I1	17	F_I21	50	P_I6	83	N.C.	116
F_I2	18	GND	51	GND	84	GND	117
GND	19	F_I22	52	P_I7	85	MAG_O5	118
F_I3	20	F_I23	53	P_I8	86	MAG_O4	119
F_I4	21	GND	54	GND	87	GND	120
GND	22	F_I24	55	P_I9	88	N.C.	121
F_I5	23	F_I25	56	P_I10	89	MAG_O3	122
F_I6	24	GND	57	GND	90	GND	123
GND	25	F_I26	58	N.C.	91	MAG_O2	124
F_I7	26	F_I27	59	CLK_I	92	N.C.	125
F_I8	27	GND	60	GND	93	GND	126
GND	28	F_I28	61	N.C.	94	MAG_O1	127
F_I9	29	F_I29	62	VREF	95	MAG_O0	128
GND	30	GND	63	GND	96	GND	129
F_I10	31	F_I30	64	N.C.	97	N.C.	130
FSTROBE_I	32	F_I31	65	N.C.	98	N.C.	131
VCC	33	VEE	66	VCC	99	VEE	132

ABSOLUTE MAXIMUM RATINGS (See Note)				
Rating	Symbol	Min	Max	Unit
Power Supply Voltage (Positive)	V _{CC}	0	7.0	V
Power Supply Voltage (Negative)	V _{EE}	-7.0	0	V
Output Voltage (ECL)	V _{OUT-max}	V _{EE} - 0.5	0.5	V
Output Current (ECL)	I _{OUT-max}	—	40	mA
Input Voltage (ECL)	V _{IN-max}	V _{EE} - 0.5	0.5	V
Input Current (ECL)	I _{IN-max}	-1.0	1.0	mA
Input Current (CMOS/TTL)	I _{IN-max}	-1.0	1.0	mA
Input Voltage (CMOS/TTL)	V _{IN-max}	-0.5	V _{CC} + 0.5	V
Operating Temperature Range (Channel)	T _A	-55	+150	°C
Storage Temperature Range	T _{stg}	-65	+175	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

DC POWER CHARACTERISTICS					
Parameter	Symbol	Min	Typ	Max	Unit
Positive Supply Voltage	V _{CC}	-4.5	—	+5.5	V
Negative Supply Voltage	V _{EE}	-5.5	—	-4.5	V
Positive Supply Current	I _{CC}	—	48	—	mA
Negative Supply Current	I _{EE}	—	600	—	mA

ECL I/O CHARACTERISTICS					
Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V _{IH}	-1100	—	-700	mV
Input Low Voltage	V _{IL}	V _{tt}	—	-1500	mV
Input High Current	I _{IH}	—	—	+10	μA
Input Low Current	I _{IL}	—	—	-10	μA
Output High Voltage (See note 1)	V _{OH}	-1000	—	-500	mV
Output Low Voltage (See note 1)	V _{OL}	V _{tt}	—	-1600	mV
Output Current High (See note 2)	I _{OH}	20	23	30	mA
Output Current Low (See note 2)	I _{OL}	0	5	8	mA
Internal ECL Reference	V _{Ref}	—	-1300	—	mV

Notes:

1. R_{Load} = 50 Ω to V_{tt} = -2.0 V.
2. Not tested, consistent with V_{OH} and V_{OL} tests.

CMOS I/O CHARACTERISTICS					
Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V _{IH}	3.5	—	V _{CC}	V
Input Low Voltage	V _{IL}	0	—	1.5	V
Input High Current	I _{IH}	—	—	+100	μA
Input Low Current	I _{IL}	-100	—	—	μA

Note:

The maximum CMOS input frequency shall be no greater than 50 MHz.

NCO TIMING PARAMETERS					
Characteristic	Symbol	Min	Typ	Max	Unit
PSTROBE_I or FSTROBE_I to data setup	t_{su}	—	500	—	ps
PSTROBE_I or FSTROBE_I to data hold	t_{hold}	—	250	—	ps
RESET_I to pulse width	t_{re}	—	2.50	—	ns
RESET_I to Clock setup	t_{sr}	—	300	—	ps
Clock to Output delay (Load = 15 pF)	t_{cd}	—	300	—	ps
Clock High ($F_{clk} = 300$ MHz max)	t_{c-High}	1.33	—	—	ns
Clock Low ($F_{clk} = 300$ MHz max)	t_{c-Low}	1.33	—	—	ns
Output Clock to Output Magnitude	t_{OUT}	—	250	—	ps

Clock Speed Requirements — The NCO shall operate within specifications under any clock speed from 10 MHz to 300 MHz.

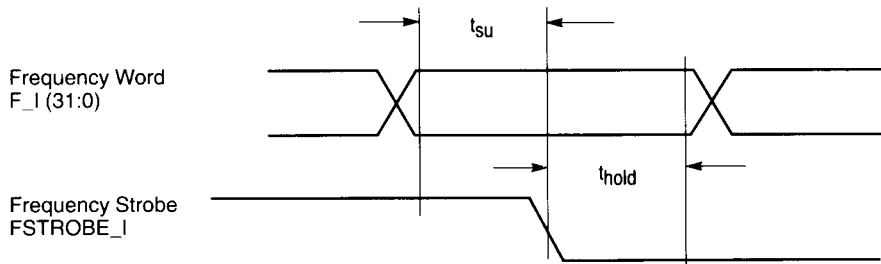
Clock Characteristics — The NCO clock shall be sinusoidal with a peak to peak voltage swing of 800 ± 140 mV. The duty cycle of the clock shall be $60\% \pm 10\%$.

Temperature Range — The NCO shall properly operate within specifications over -55°C to $+125^{\circ}\text{C}$.

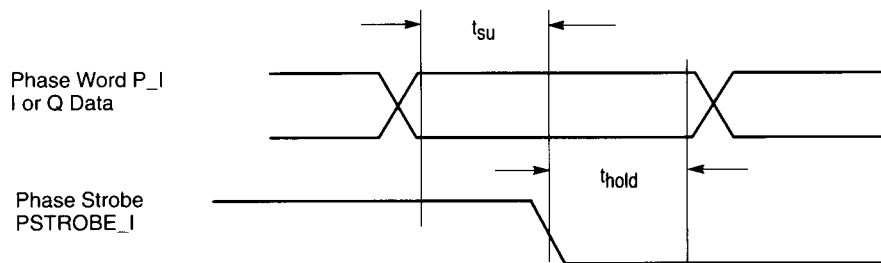
Strobe to Frequency Change — The time delay from frequency strobe to a change in output frequency shall be no greater than 12 clock cycles.

Strobe to Phase Change — The time delay from phase strobe to a change in output phase shall be no greater than 8 clock cycles.

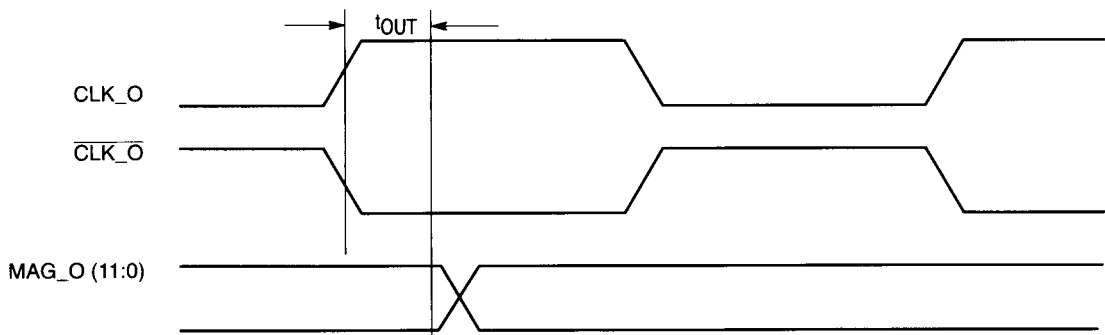
NCO INPUT FREQUENCY WORD TIMING DIAGRAM



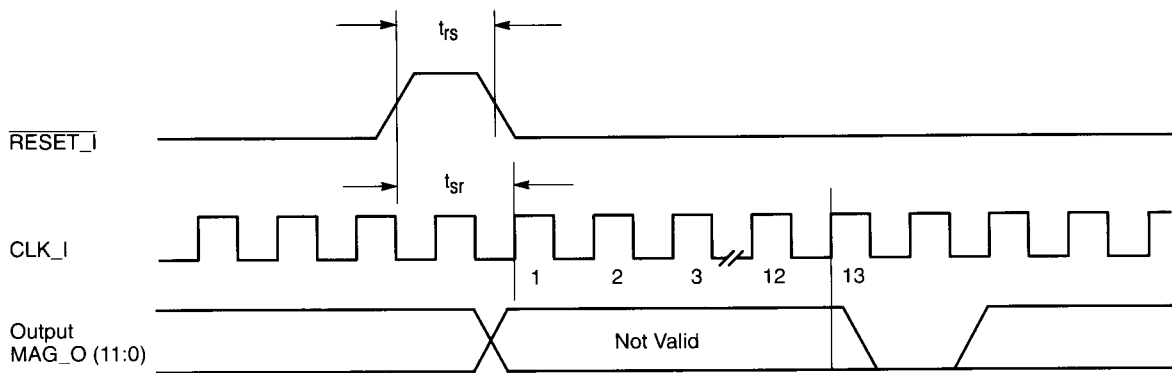
NCO INPUT WORD TIMING DIAGRAM



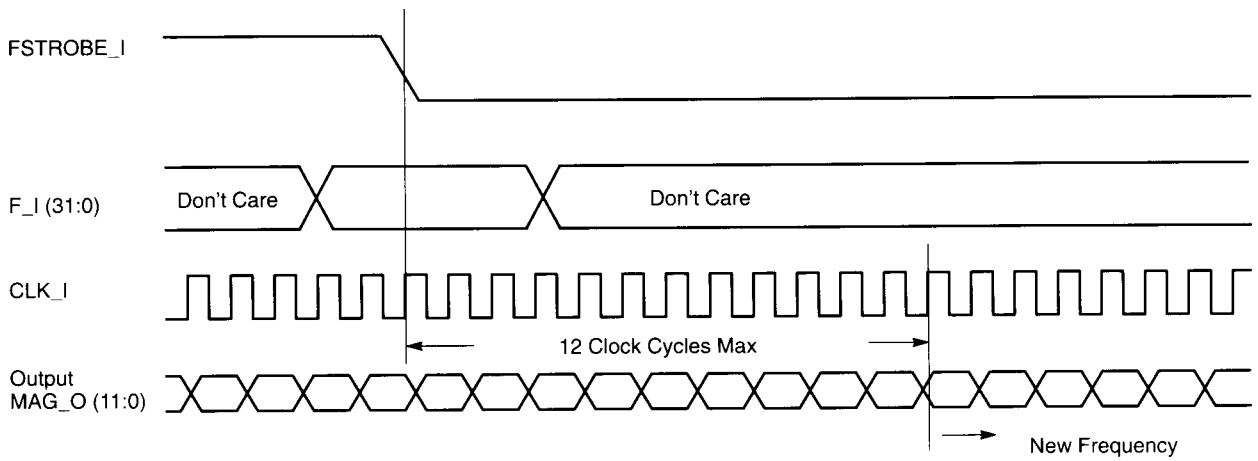
OUTPUT MAGNITUDE TIMING



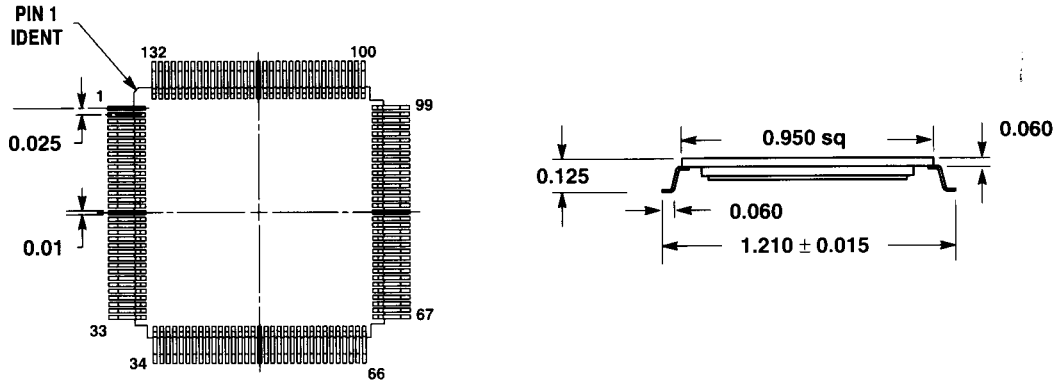
NCO RESET TIMING DIAGRAM



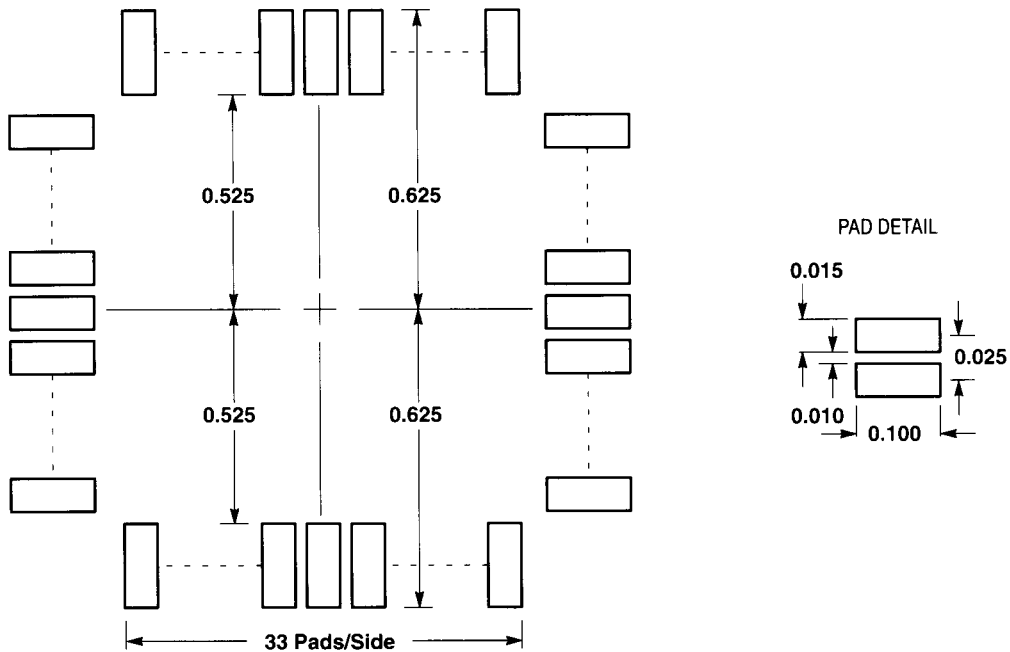
NCO OUTPUT AMPLITUDE WORD TIMING DIAGRAM



PACKAGE OUTLINE



MOUNTING FOOTPRINT



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