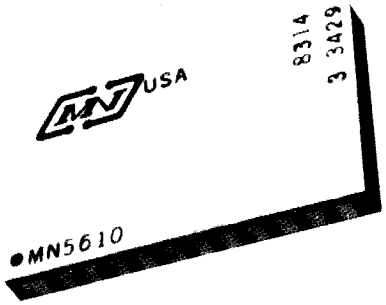


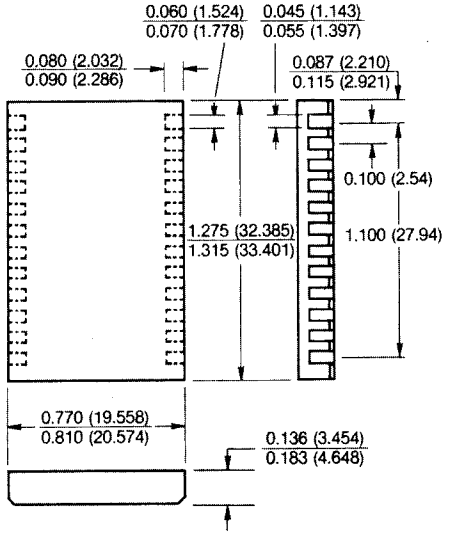
MN5610 Series

LEADLESS PACKAGE
HIGH-SPEED 12-BIT
A/D CONVERTERS

FEATURES

- **24 Pin Hermetically Sealed Leadless Package**
- **Fast 13μsec Conversion Time**
- **± ½LSB Linearity Over Temperature**
- **No Missing Codes Over Temperature**
- **Low Power 915mW Maximum**
- **Adjustment Free No Gain or Offset Adjust Pots Required**
- **Full Mil Operation −55°C to +125°C Available Fully Screened and Processed to MIL-STD-883, Method 5008.**

24 PIN LEADLESS PACKAGE



Dimensions in inches (millimeters)

DESCRIPTION

MN5610 Series devices are high-speed (13μsec), 12-bit, successive approximation type A/D converters that meet all performance specifications when operated with a 1MHz clock. Offering both parallel and serial data outputs, MN5610 Series devices are packaged in hermetically sealed, 1.3″ × 0.8″, low-profile, ceramic leadless packages with 24 pads on 100 mil centers. 12-bit linearity (± ½LSB maximum error) and "no missing codes" are guaranteed over each device's entire specified temperature range (including −55°C to +125°C), and 100% screening to MIL-STD-883, Method 5008 is optional.

These A/D converters are available with either of four input voltage ranges (0 to +10V, 0 to −10V, ±5V, ±10V). For each range, the user has the option of specifying a model complete with internal reference or, for improved overall accuracy, a model that uses an external reference.

MN5610 A/D's are designed to operate without external gain and offset adjusting potentiometers. Their high initial accuracies and highly stable performance over temperature are the result of active laser trimming of thin-film resistor networks. Zero Error, for example, is guaranteed to be better than ±0.025% FSR at +25°C and better than ±0.05% FSR over the entire operating temperature range (including −55°C to +125°C). All units are fully specified and 100% tested for linearity and accuracy at their operating temperature extremes as well as at room temperature.

Being TTL compatible and operating from ±15V and +5V supplies, the MN5610 Series is similar in function and fabrication to Micro Networks MN5210 Series A/D's. The MN5210 Series is the industry's most widely accepted 12 bit A/D for military/aerospace applications having been designed into more than 50 military/aerospace programs. The MN5610 was specifically designed for military/aerospace, industrial and OEM applications in which high-speed A/D conversion and low power consumption are required and surface-mounted-device packaging is necessary or mandated.

Micro Networks
A DIVISION OF UNITRODE CORPORATION
324 Clark Street, Worcester, MA 01606 • Tel: (617) 852-5400

MN5610 SERIES LEADLESS PACKAGE A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
Standard Product	0°C to +70°C
"E", "E/B" Models	−25°C to +85°C
"H", "H/B" Models	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (+V_{CC}, Pin 15)	−0.5 to +18 Volts
−15V Supply (−V_{CC}, Pin 13)	+0.5 to −18 Volts
+5V Supply (+V_{dd}, Pin 2)	−0.5 to +7 Volts
Analog Input (Pin 14)	±25 Volts
Digital Inputs (Pins 1, 24)	−0.5 to +5.5 Volts
Digital Outputs	+V_{dd}
Ref. Input (MN5613, 14, 15, 17)	0 to −15 Volts

ORDERING INFORMATION

PART NUMBER — MN561XH/B

Model Selection (0°C to +70°C)

Add "E" for fully specified −25°C to +85°C operation or "H" for fully specified −55°C to +125°C operation.

Add "/B" for 100% Screening According to Method 5008 of MIL-STD-883

EXAMPLE:

0°C to +70°C (±10V Input, Ext. Ref.) — MN5615

−55°C to +125°C Operation — MN5615H

−55°C to +125°C Operation and 100% Screening MIL-STD-883 — MN5615H/B

SPECIFICATIONS (T_A = 25°C, Supply Voltages ±15V and +5V, for Ext. Ref. Models V_{Ref} = −10.000V, unless otherwise specified)

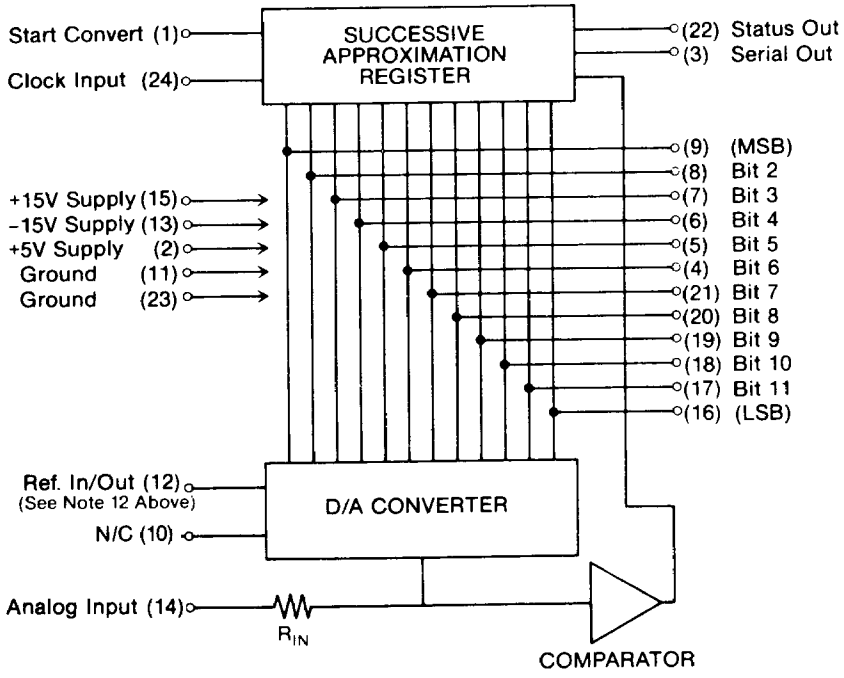
ANALOG INPUTS					
Input Range (Input Impedance) (Note 1): 0 to −10V (6.7kΩ) −5V to +5V (6.7kΩ) −10V to +10V (13.4kΩ) 0 to +10V (6.7kΩ)	(Internal Ref.) ✓MN5610 ✓MN5611 ✓MN5612 ✓MN5616		(External Ref.) ✓MN5613 ✓MN5614 ✓MN5615 ✓MN5617		
TRANSFER CHARACTERISTICS (Note 2)	TYP.	MAX.	TYP.	MAX.	
Linearity Error (Note 3): +25°C 0°C to +70°C −55°C to +125°C ("H" Models)	±¼ ±¼	±½ ±½ ±½	±¼ ±¼	±½ ±½ ±½	LSB LSB LSB
Differential Linearity Error	±½		±½		LSB
No Missing Codes	Guaranteed Over Temperature				
Full Scale Absolute Accuracy Error (Notes 4, 5): +25°C 0°C to +70°C −55°C to +125°C ("H" Models)	±0.025 ±0.2	±0.05 ±0.4 ±0.4	±0.025 ±0.05	±0.05 ±0.1 ±0.1	%FSR %FSR %FSR
Zero Error (Notes 4, 5): +25°C 0°C to +70°C −55°C to +125°C ("H" Models)	±0.01 ±0.025	±0.025 ±0.05 ±0.05	±0.01 ±0.025	±0.025 ±0.05 ±0.05	%FSR %FSR %FSR
Gain Error (Note 5) Gain Drift	±0.025 ±10		±0.025 ±3		% ppm/°C
Conversion Time (Note 6)		13		13	μsec
POWER SUPPLIES					
Power Supply Range: ±15V Supplies +5V Supply		±3 ±5		±3 ±5	% %
Power Supply Rejection (Note 7): +15V Supply −15V Supply	±0.005 ±0.01	±0.02 ±0.05	±0.005 ±0.005	±0.02 ±0.02	%FSR/%Vs %FSR/%Vs
Current Drain: +15V Supply −15V Supply +5V Supply −10V Reference (MN5613, 14, 15, 17)	23 −15 25	28 −19 42	23 −5 25 −1.5	28 −6.3 42 −2	mA mA mA mA
Power Consumption	695	915	567	744	mW
DIGITAL INPUTS, ALL UNITS	MIN.	TYP.	MAX.		
Logic Levels: Logic "1" Logic "0"	2.0		0.7		Volts Volts
Clock Input (Note 8): Pulse Width High Pulse Width Low Loading High (V_{in} = 2.4V) Loading Low (V_{in} = 0.3V) Frequency (Note 6)	125 175	 2 −0.25	 20 −0.4 1		nsec nsec μA mA MHz
Start Convert Input: Loading High (V_{in} = 2.4V) Loading Low (V_{in} = 0.3V) Setup Time Start Low to Clock (Note 9)	 25	4 −0.25	40 −0.4		μA mA nsec

DIGITAL OUTPUTS (ALL UNITS)	MIN.	TYP.	MAX	UNITS
Logic Coding (Note 10): Unipolar Ranges Bipolar Ranges		Complementary Straight Binary Complementary Offset Binary		
Logic Levels: Logic "1" Logic "0"	2.4	3.6 0.15	 0.3	Volts Volts
Output Drive Capability, All Outputs (Note 11): Logic "1" Logic "0"	8 2			TTL Loads TTL Loads
REFERENCE INPUT/OUTPUT (Note 12)				
Internal Reference: Voltage Accuracy Tempco of Drift Max. External Current		−6.3 ±2 ±5	 100	Volts % ppm/°C μA
External Reference: Voltage Loading		−10.000	 −2	Volts mA

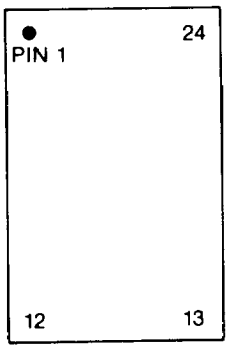
SPECIFICATION NOTES

1. Consult factory for other available input voltage ranges.
2. Specifications listed for "H" models also apply for "E" models.
3. Micro Networks tests and guarantees maximum linearity error at room temperature and at both the high and low extremes of the specified operating range. 1LSB for a 12 bit converter corresponds to 0.024%FSR. See Note 4.
4. FSR stands for Full Scale Range and is equal to the peak to peak voltage of the selected input range. For the ± 10V input range, FSR is 20 volts, and 1LSB is equal to 4.88mV. For the 0 to + 10V, 0 to − 10V, and ± 5V ranges, FSR is 10 volts, and 1LSB is equal to 2.44mV.
5. See MN5210 Series data sheet for an explanation of how Micro tests and specifies Full Scale Absolute Accuracy, Gain, and Zero Errors.
6. Conversion Time is defined as the width of the converter's Status (E.O.C.) pulse (see Timing Diagram). Micro Networks guarantees MN5610 Series converters will meet all specs with clock frequencies up to 1MHz.
7. Micro Networks tests and guarantees Power Supply Rejection over the ± 15V ± 3% range.
8. The clock may be asymmetrical with minimum positive or negative pulse widths. See Note 6.
9. In order to reset the converter, Start Convert must be brought low at least 25nsec prior to a low to high clock transition. See Timing Diagram.
10. Serial and parallel output data have the same coding. Serial data is in Non-Return to Zero (NRZ) format. See Output Coding and Timing Diagram.
11. One TTL load is defined as sinking 40μA with a logic "1" applied and sourcing 1.6mA with a logic "0" applied.
12. MN5610, MN5611, MN5612 and MN5616 have an internal − 6.3V reference. MN5613, MN5614, MN5615 and MN5617 require an external − 10.000V reference.

BLOCK DIAGRAM



PIN DESIGNATIONS



Pin 1	Start Convert	Pin 24	Clock Input
Pin 2	+5V Supply	Pin 23	Ground
Pin 3	Serial Output	Pin 22	Status (E.O.C.)
Pin 4	Bit 6	Pin 21	Bit 7
Pin 5	Bit 5	Pin 20	Bit 8
Pin 6	Bit 4	Pin 19	Bit 9
Pin 7	Bit 3	Pin 18	Bit 10
Pin 8	Bit 2	Pin 17	Bit 11
Pin 9	Bit 1 (MSB)	Pin 16	Bit 12 (LSB)
Pin 10	N/C	Pin 15	+15V Supply
Pin 11	Ground	Pin 14	Analog Input
Pin 12	Ref. Out (-6.3V) Ref. In (-10.0V)	Pin 13	-15V Supply

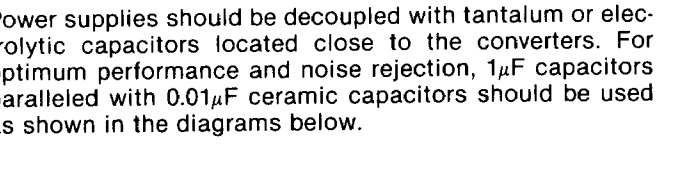
APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION—The Successive Approximation Register (SAR) is a set of flip flops (and control logic) whose outputs act as both the direct (parallel) data outputs of the Analog to Digital Converter (A/D) and the digital drive for the A/D's internal Digital to Analog Converter (D/A). See Block Diagram. Holding the A/D's Start Convert (pin 1) low during a clock low to high transition resets the SAR. In this state, the output of the MSB flip flop is set to logic "0", the outputs of the other bit flip flops are set to logic "1", and the Status output (pin 22) is set to logic "1" (see Timing Diagram). The Start Convert must now be brought high again for the conversion to continue. If the Start is not brought high, the converter will remain in the reset state.

The D/A internal to the A/D continuously converts the A/D's digital output back to an analog signal. The comparator output ("1" or "0") informs the SAR whether the present digital output (0111 1111 1111 in the reset state) is "greater than" or "less than" the analog input. Depending upon which is greater, on the first rising clock edge after the Start has returned high, the SAR will set the MSB to its final state ("1"or "0") and bring bit 2 down to a "0". The digital output is now X011 1111 1111. The D/A converts this to an analog value, and the comparator determines whether this value is greater or less than the analog input. On the next rising clock edge, the SAR reads the comparator feedback, sets bit 2 to its final value, and brings bit 3 down to a logic "0". The digital output is now XX01 1111 1111. This successive approximation procedure continues until all the output bits are set. The rising clock edge that sets the LSB (bit 12) also drops the Status Output to a "0" signaling that the conversion is complete. Output data is now valid and will remain so until another conversion is started. The clock does not have to be turned off.

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies from MN5610 Series converters. The units' two Ground pins (pins 11 and 23) are not connected to each other internally. They should be tied together as close to the package as possible and connected to system analog ground, preferably through a large ground plane underneath the package. If the grounds cannot be tied together and must be run separately, a non polarized 0.01μF bypass capacitor should be connected between pins 11 and 23 as close to the unit as possible and wide conductor runs employed.

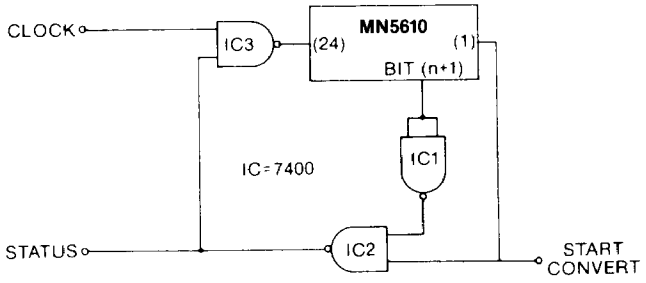
Power supplies should be decoupled with tantalum or electrolytic capacitors located close to the converters. For optimum performance and noise rejection, 1μF capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the diagrams below.



POWER SUPPLY DECOUPLING

CONTINUOUS CONVERTING—MN5610 Series A/D converters can be made to continuously convert by tying the Status output (pin 22) to the Start Convert input (pin 1). In this configuration, Status (Start Convert) will go low at the end of a conversion (see Timing Diagram) and the next rising clock edge will reset the converter bringing Status (Start Convert) high again. The MSB will be set on the next rising clock edge. The result is that the Status will go low for approximately one clock period following each conversion. Please read the section describing the Status output. See below for continuous conversions while short cycling.

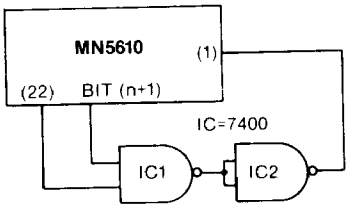
SHORT CYCLING—For applications requiring less than 12 bits resolution, MN5610 Series A/D's can be truncated or short cycled to the desired number of bits with a proportionate decrease in conversion time. The following circuit may be used to truncate at n bits.



SHORT CYCLING SINGLE CONVERSIONS

Assuming a conversion is already in progress, bit (n + 1) will go low as bit n is being set (see Timing Diagram). Since the Start Convert signal is high at this time, Status (the output of IC2) will go low gating off the clock at IC3 ending the conversion. To begin a new conversion, Start Convert is brought low driving Status high and gating on the clock. The first rising clock edge the converter sees with Start Convert low will reset the converter bringing bit (n + 1) high again. Now Status will remain high as Start Convert is brought back high allowing the conversion to continue. Therefore, in this configuration, Status and Start Convert function normally, i.e., the same as Status and Start Convert for a converter not being short cycled.

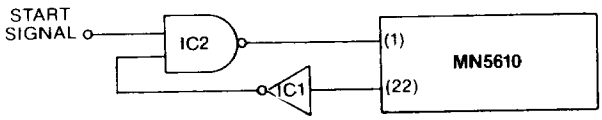
SHORT CYCLING AND CONTINUOUS CONVERTING—A previous section described how continuous converting for 12 bits could be accomplished by simply tying the Status output back to the Start Convert input. To continuously convert at n bits, one simply has to tie the bit (n + 1) output back to the Start convert input. The bit (n + 1) output acts like a Status when one short cycles at n bits. It goes high when the converter is reset, remains a "1" during the conversion, and drops to a "0" as bit n is being set. Since it is possible for the converter to come on in any state at power-on, a lock-up condition may occur if bit (n + 1) comes on as a "1" and the conversion process comes on at bit (n + 2). This situation can be avoided by making the Start Convert input the AND function of bit (n + 1) and the Status output.

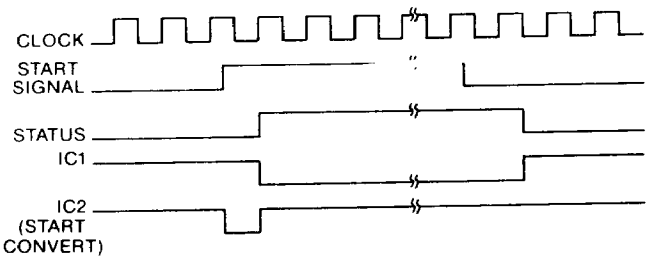


SHORT CYCLING CONTINUOUS CONVERTING

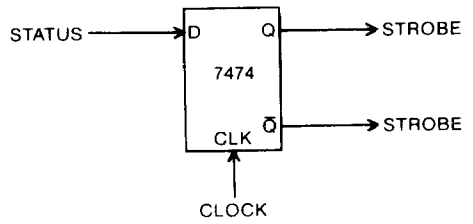
If one is already using the circuit described in the section labeled Short Cycling, one can short cycle and continuously convert by making the Start Convert input the AND function of Status (IC2) and Status (pin 7) outputs.

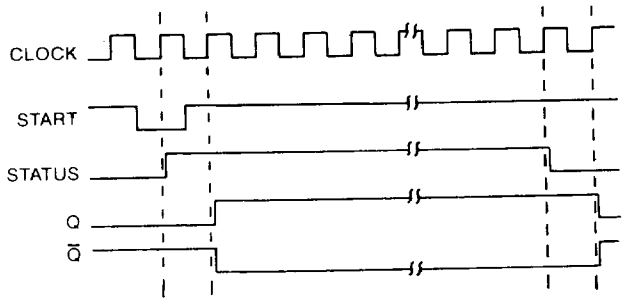
TRIGGERING WITH A POSITIVE EDGE—If it is inconvenient to generate a negative going Start Convert Pulse of the proper width, MN5610 Series A/D's can be made to start converting on a positive going edge by employing the circuit shown below. Assuming the previous conversion is done and the Start Signal is low, the Status output will be low, the output of IC1 will be high, and the output of IC2 will be high. A rising edge as a Start Signal will drive the output of IC2 low. The converter will reset on the next rising clock edge. Resetting brings the Status high; IC1 goes low; the Start Signal is still high so the output of IC2 goes high allowing the conversion to continue immediately. The Start Signal has only to be brought back down before the conversion is completed.





STATUS OUTPUT—The Status or End of Conversion (E.O.C.) output will be set to a logic "1" when the converter is reset; will remain high during conversion; and will drop to a logic "0" when conversion is complete. Due to propagation delays, the least signifigant bit (LSB) of a given conversion may not be valid until a maximum of 30nsec after Status has returned low. Therefore, an adequate delay must be provided if Status is to be used to strobe latches to hold output data. Simple gate delays can be employed or the Status can be made the input of a D flip flop whose clock input is the same as the converter clock (see sketch). In this situation, the Q output will change one clock period after Status changes.



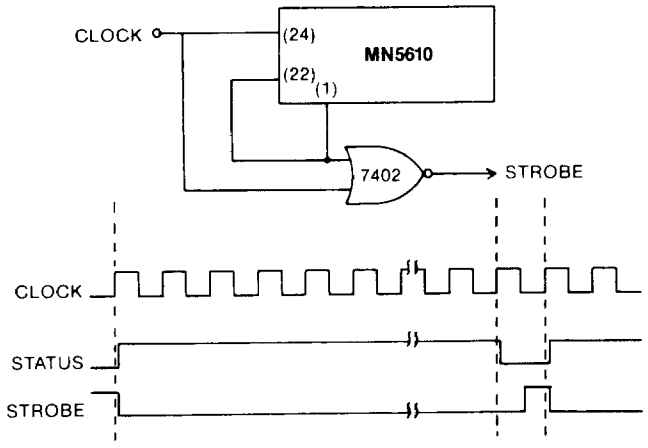


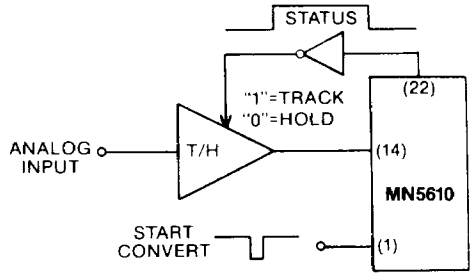
If continuously converting the Status (E.O.C.) output can be NORed with the converter clock, as shown at the top of the next page, to produce a positive strobe pulse ½ period wide, ½ period after the Status output has gone low. The rising edge of this pulse can be used to latch data after each conversion.

DIGITAL OUTPUT CODING

ANALOG INPUT				DIGITAL OUTPUT
MN5610, 5613	MN5611, 5614	MN5612, 5615	MN5616, 5617	MSB LSB
0.0000V	+5.0000V	+10.0000V	+10.0000V	0000 0000 0000
- 0.0024V	+4.9976V	+ 9.9951V	+ 9.9976V	0000 0000 0000*
- 4.9976V	+0.0024V	+ 0.0049V	+ 5.0024V	0111 1111 1110*
- 5.0000V	0.0000V	0.0000V	+ 5.0000V	**0000 0000 0000***
- 5.0024V	-0.0024V	- 0.0049V	+ 4.9976V	1000 0000 0000*
- 9.9976V	-4.9976V	- 9.9951V	+ 0.0024V	1111 1111 1110*
-10.0000V	- 5.0000V	-10.0000V	0.0000V	1111 1111 1111

* Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated. See the section on Absolute Accuracy Error for an explanation of Output Transition Voltages.
EXAMPLE For an MN5612/15 (+10V analog input range) the transition from digital output 0000 0000 0000 to 0000 0000 0001 (or vice versa) will ideally occur at an input voltage of +9.9951 volts. Subsequently, any input voltage more positive than +9.9951 volts will give a digital output of all "0's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input of zero volts, and the 1111 1111 1111 to 1111 1111 1110 transition should occur at -9.9951 volts. An input more negative than -9.9951 volts will give all "1's".

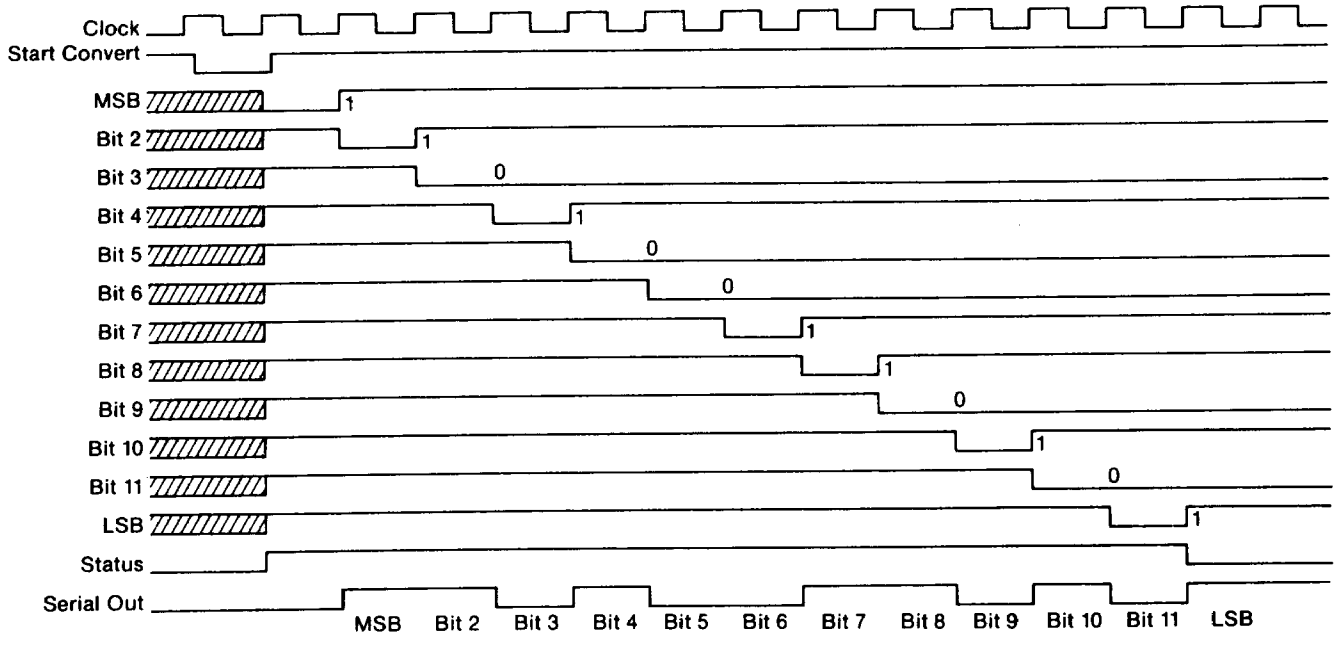




USING A TRACK AND HOLD AMP WITH MN5610 SERIES A/D's—The error that results when trying to convert moving analog signals with a successive approximation A/D can be as great as the amount the analog signal changes during a single A/D conversion time. If this error is unacceptable, a Track and Hold (T/H) or Sample and Hold (S/H) amplifier can be placed between the analog signal source and the A/D converter. A careful error analysis will be necessary to determine if the T/H is actually reducing and not increasing overall error. T/H parameters such as aperture uncertainty, gain accuracy, pedestal error and droop rate will have to be contended with (see the tutorial section of the Micro Networks' Application Manual and Product Guide for a complete discussion of T/H parameters).

Normally, the T/H can be controlled directly by the A/D's Status output. Typical connections are shown above for Micro Networks MN343 (10μsec acquisition time to $\pm$0.01%) and MN346 (2μsec acquisition time to $\pm$0.01%) Track and Hold Amplifiers. The Status output changes from a "0" to a "1" when the converter is reset. This drives the T/H from the track to the hold mode. At the end of conversion, Status returns to a "0" restoring the T/H to the track mode.

TIMING DIAGRAM



TIMING DIAGRAM NOTES

1. Operation shown is for the digital word 1101 0011 0101 which corresponds to 1.7432V on the 0 to + 10V input range (MN5616). See Output Coding.
2. Conversion Time is defined as the width of the Status (E.O.C.) pulse.
3. The converter is reset (MSB = "0", all other bits = "1", Status = "1") by holding the Start Convert low during a low to high clock transition. The Start Convert must be low for a minimum of 25nsec prior to the clock transition. Holding the Start low will hold the converter in the reset state. Actual conversion will begin on the next rising clock edge after the Start has returned high.
4. The delay between the resetting clock edge and Status actually rising to a "1" is 120nsec maximum.
5. The Start Convert may be brought low at any time during a conversion to reset and begin converting again.
6. Both serial and parallel data bits become valid on the same rising clock edges. Serial data is valid on subsequent falling clock edges, and these edges can used to clock serial data into receiving registers.
7. Output data will be valid 30nsec (maximum) after the Status (E.O.C.) output has returned low. Parallel output data will remain valid and the Status output low until another conversion is initiated.
8. For continuous conversion, connect the Status output (pin 22) to the Start Convert input (Pin 1). See section on Continuous Conversion.
9. When the converter is initially "powered up", it may come on at any point in the conversion cycle.