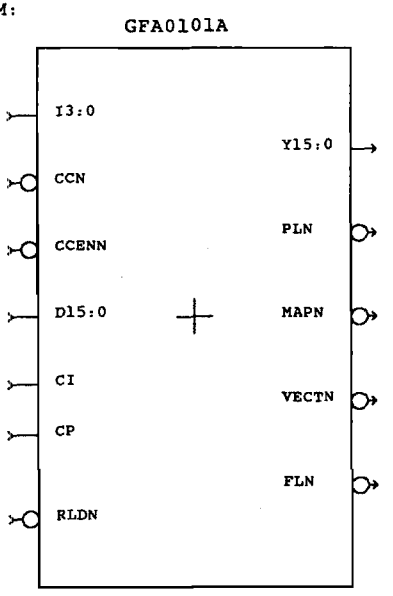
GFA0101A MICROPROGRAM CONTROLLER

GENERAL DESCRIPTION:

THE GFA0101A IS A 5-DEEP STACK, 16-BIT WIDE ADDRESS SEQUENCER WHICH CONTROLS THE SEQUENCE OF EXECUTION OF THE MICRO-INSTRUCTIONS. IT IS DESIGNED TO BE FULLY COMPATIBLE WITH THE AM2910 EXCEPT WHEN ILLEGAL OPERATIONS ARE PERFORMED ON THE STACK (E.G., TRYING TO POP AN EMPTY STACK OR PUSH ONTO A FULL STACK). THE GFA0101A IS ALSO 16 BITS WIDE AND THE Y OUTPUTS ARE SLIGHTLY DIFFERENT; I.E., THEY ARE NOT TRISTATE OUTPUTS. FOR A DETAILED FUNCTIONAL DESCRIPTION, SEE THE AMD 2900 DATA BOOK.

PIN DIAGRAM:



- GATES USED = 1137
- AREA USED = 1235 GATE LOCATIONS
- 5-WORD DEEP STACK
- 16-BIT WIDE ADDRESS
- LL7000 SERIES COMPATIBLE
- LSA2000 SERIES COMPATIBLE

INPUT LOADING: (LOADING IN TRANSISTOR PAIRS):

I3 = 2	CCENN = 1	D11 = 5	D6 = 5	D1 = 5
I2 = 2	D15 = 5	D10 = 5	D5 = 5	D0 = 5
I1 = 2	D14 = 5	D9 = 5	D4 = 5	CI = 7
I0 = 2	D13 = 5	D8 = 5	D3 = 5	CP = 75
CCN = 1	D12 = 5	D7 = 5	D2 = 5	RLDN = 1

OUTPUT DRIVE: (DRIVE IN (#P,#N)):

Y15 = (2,2)	Y11 = (2,2)	Y7 = (2,2)	Y3 = (2,2)	PLN = (1,0.5)
Y14 = (2,2)	Y10 = (2,2)	Y6 = (2,2)	Y2 = (2,2)	MAPN = (1,0.25)
Y13 = (2,2)	Y9 = (2,2)	Y5 = (2,2)	Y1 = (2,2)	VECTN = (1,0.25)
Y12 = (2,2)	Y8 = (2,2)	Y4 = (2,2)	Y0 = (2,2)	FLN = (2,1)

NDL SYNTAX:

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Z(I3,I2,I1,I0,CCN,CCENN,D15,D14,D13,D12,D11,D10,D9,D8,D7,D6,D5,D4,D3,D2,D1,D0,
  CI,CP,RLDN)

=GFA0101A (Y15,Y14,Y13,Y12,Y11,Y10,Y9,Y8,Y7,Y6,Y5,Y4,Y3,Y2,Y1,Y0,PLN,MAPN,VECTN,
  FLN)$
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PIN DESCRIPTION:

INPUTS:

I3:0	INPUT INSTRUCTIONS TO SELECT ONE OF SIXTEEN INSTRUCTIONS FOR THE GFA0101A
CCN	CONDITION CODE; USED AS TEST CRITERION
CCENN	CONDITION CODE ENABLE
D15:0	DIRECT INPUT TO REGISTER/COUNTER AND MULTIPLEXER
CI	CARRY-IN
CP	CLOCK PULSE
RLDN	REGISTER LOAD

OUTPUTS:

Y15:0	ADDRESS TO MICROPROGRAM MEMORY
PLN	PIPELINE ADDRESS ENABLE
MAPN	MAP ADDRESS ENABLE
VECTN	VECTOR ADDRESS ENABLE
FLN	FULL WARNING OUTPUT; INDICATES THAT FIVE ITEMS ARE ON THE STACK

AC CHARACTERISTICS*

CYCLE TIME AND CLOCK CHARACTERISTICS:

TIME	5K TYP.(N)	7K TYP.(N)
MINIMUM CLOCK LOW TIME	30	18
MINIMUM CLOCK HIGH TIME	27	15
MINIMUM CYCLE TIME I = 14	44	24.5
MINIMUM CYCLE TIME ALL OTHER I	67	39.6

MAXIMUM COMBINATIONAL PROPAGATION DELAY:

OUTPUT / INPUT	5K TYPICAL (N)					7K TYPICAL (N)				
	Y	PLN	MAPN	VECTN	FLN	Y	PLN	MAPN	VECTN	FLN
D15:0	11	——	——	——	——	5.3	——	——	——	——
I3:0	38	13	12	10	——	23.9	8.3	7.2	6.5	——
CCN	39	——	——	——	——	23.2	——	——	——	——
CCENN	39	——	——	——	——	24	——	——	——	——
CLK/ * I=8,9,15	43	——	——	——	20	26.4	——	——	——	12.1
CLK/ ALL OTHER I	36	——	——	——	20	20.1	——	——	——	12.1

SET-UP AND HOLD TIMES:

FROM INPUT	5K TYPICAL (N)		7K TYPICAL (N)	
	SET-UP TIME	HOLD TIME	SET-UP TIME	HOLD TIME
D15:0 TO R	11	2	5.3	1
D(I) TO PC	33	0	19.5	0
I3:0	60	0	37.1	0
CCN	60	0	36.3	0
CCENN	62	0	37.2	0
CI	18	0	10.4	0
RLDN	21	0	11.9	0

* THESE INSTRUCTIONS ARE CONDITIONAL ON THE COUNTER. USE THIS DELAY ONLY IF THE PREVIOUS INSTRUCTION COULD AFFECT THE COUNTER.