

PIN-PROGRAMMABLE PRECISION CLOCK MULTIPLIER

Description

The Si5365 is a low jitter, precision clock multiplier for high-speed communication systems, including SONET OC-48/OC-192, Ethernet, and Fibre Channel, in which the application requires clock multiplication without jitter attenuation. The Si5365 accepts four clock inputs ranging from 19.44 to 707 MHz and generates five frequency-multiplied clock outputs ranging from 19.44 to 1050 MHz. The input clock frequency and clock multiplication ratio are selectable from a table of popular SONET, Ethernet, and Fibre Channel rates. The Si5365 is based on Silicon Laboratories' 3rd-generation DSPLL[®] technology, which provides any-rate frequency synthesis in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. Operating from a single 1.8 or 2.5 V supply, the Si5365 is ideal for providing clock multiplication in high performance timing applications.

Applications

- SONET/SDH OC-48/OC-192 line cards
- GbE/10GbE, 1/2/4/8/10GFC line cards
- ITU G.709 line cards
- Test and measurement

Features

- Selectable output frequencies ranging from 19.44 to 1050 MHz
- Low jitter clock outputs w/jitter generation as low as 0.6 ps rms (50 kHz–80 MHz)
- Integrated loop filter with selectable loop bandwidth (30 kHz to 1.3 MHz)
- Four clock inputs w/manual or automatically controlled hitless switching
- Five clock outputs with selectable signal format (LVPECL, LVDS, CML, CMOS)
- Support for ITU G.709 FEC ratios (255/238, 255/237, 255/236)
- LOS alarm outputs
- Digitally-controlled output phase adjust
- Pin-programmable settings
- On-chip voltage regulator for 1.8 or 2.5 V $\pm 10\%$ operation
- Small size: 14 x 14 mm 100-pin TQFP
- Pb-free, RoHS compliant

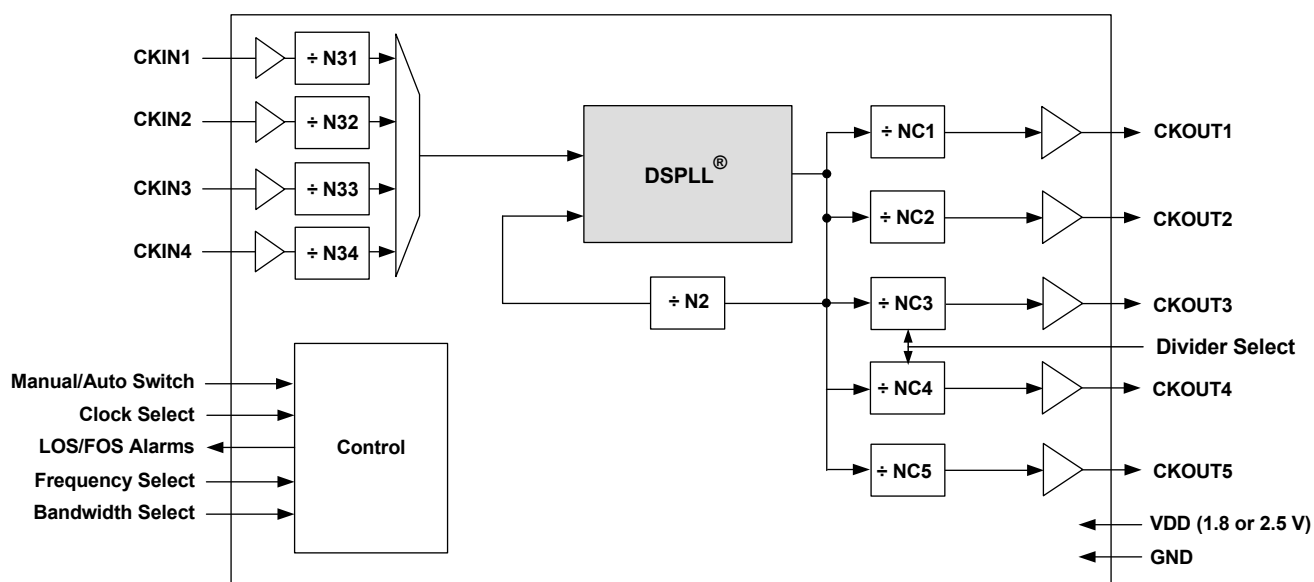


Table 1. Performance Specifications(V_{DD} = 1.8 or 2.5 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature Range	T _A		–40	25	85	°C
Supply Voltage	V _{DD}		2.25	2.5	2.75	V
			1.62	1.8	1.98	V
Supply Current	I _{DD}	f _{OUT} = 622.08 MHz All CKOUTs enabled LVPECL format output	—	394	435	mA
		Only CKOUT1 enabled	—	253	284	mA
		f _{OUT} = 19.44 MHz All CKOUTs enabled CMOS format output	—	278	321	mA
		Only CKOUT1 enabled	—	229	261	mA
		Tristate/Sleep Mode	—	TBD	TBD	mA
Input Clock Frequency (CKIN1, CKIN2, CKIN3, CKIN4)	CK _F	Input frequency and clock multiplication ratio pin- selectable from table of val- ues using FRQSEL and FRQTBL settings. Consult Silicon Laboratories configu- ration software DSPLLsim or Any-Rate Precision Clock Family Reference Manual at www.silabs.com/timing for table selections.	19.44	—	707.35	MHz
Output Clock Frequency (CKOUT1, CKOUT2, CKOUT3, CKOUT4, CKOUT5)	CK _{OF}		19.44	—	1049.76	MHz
Input Clocks (CKIN1, CKIN2, CKIN3, CKIN4)						
Differential Voltage Swing	CKN _{DPP}		0.25	—	1.9	V _{PP}
Common Mode Voltage	CKN _{VCM}	1.8 V ±10%	0.9	—	1.4	V
		2.5 V ±10%	1.0	—	1.7	V
Rise/Fall Time	CKN _{TRF}	20–80%	—	—	11	ns
Duty Cycle	CKN _{DC}	Whichever is less	40	—	60	%
			50	—	—	ns
Output Clocks (CKOUT1, CKOUT2, CKOUT3, CKOUT4, CKOUT5)						
Common Mode	V _{OCM}	LVPECL 100 Ω load line-to-line	V _{DD} – 1.42	—	V _{DD} – 1.25	V
Differential Output Swing	V _{OD}		1.1	—	1.9	V
Single Ended Output Swing	V _{SE}		0.5	—	0.93	V
Rise/Fall Time	CKO _{TRF}	20–80%	—	230	350	ps
Note: For a more comprehensive listing of device specifications, please consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual. This document can be downloaded from www.silabs.com/timing .						

Table 1. Performance Specifications (Continued)(V_{DD} = 1.8 or 2.5 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Duty Cycle	CKO _{DC}		45	—	55	%
PLL Performance						
Jitter Generation	J _{GEN}	f _{OUT} = 622.08 MHz, LVPECL output format 50 kHz–80 MHz	—	0.6	TBD	ps rms
		12 kHz–20 MHz	—	0.6	TBD	ps rms
Jitter Transfer	J _{PK}		—	0.05	0.1	dB
Phase Noise	CKO _{PN}	f _{OUT} = 622.08 MHz 100 Hz offset	—	TBD	TBD	dBc/Hz
		1 kHz offset	—	TBD	TBD	dBc/Hz
		10 kHz offset	—	TBD	TBD	dBc/Hz
		100 kHz offset	—	TBD	TBD	dBc/Hz
		1 MHz offset	—	TBD	TBD	dBc/Hz
Subharmonic Noise	SP _{SUBH}	Phase Noise @ 100 kHz Offset	—	TBD	TBD	dBc
Spurious Noise	SP _{SPUR}	Max spur @ n x F3 (n ≥ 1, n x F3 < 100 MHz)	—	TBD	TBD	dBc
Package						
Thermal Resistance Junction to Ambient	θ _{JA}	Still Air	—	40	—	°C/W
Note: For a more comprehensive listing of device specifications, please consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual. This document can be downloaded from www.silabs.com/timing .						

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	−0.5 to 2.75	V
LVC MOS Input Voltage	V _{DIG}	−0.3 to (V _{DD} + 0.3)	V
Operating Junction Temperature	T _{JCT}	−55 to 150	°C
Storage Temperature Range	T _{STG}	−55 to 150	°C
ESD HBM Tolerance (100 pF, 1.5 kΩ)		2	kV
ESD MM Tolerance		200	V
Latch-Up Tolerance		JESD78 Compliant	
Note: Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.			

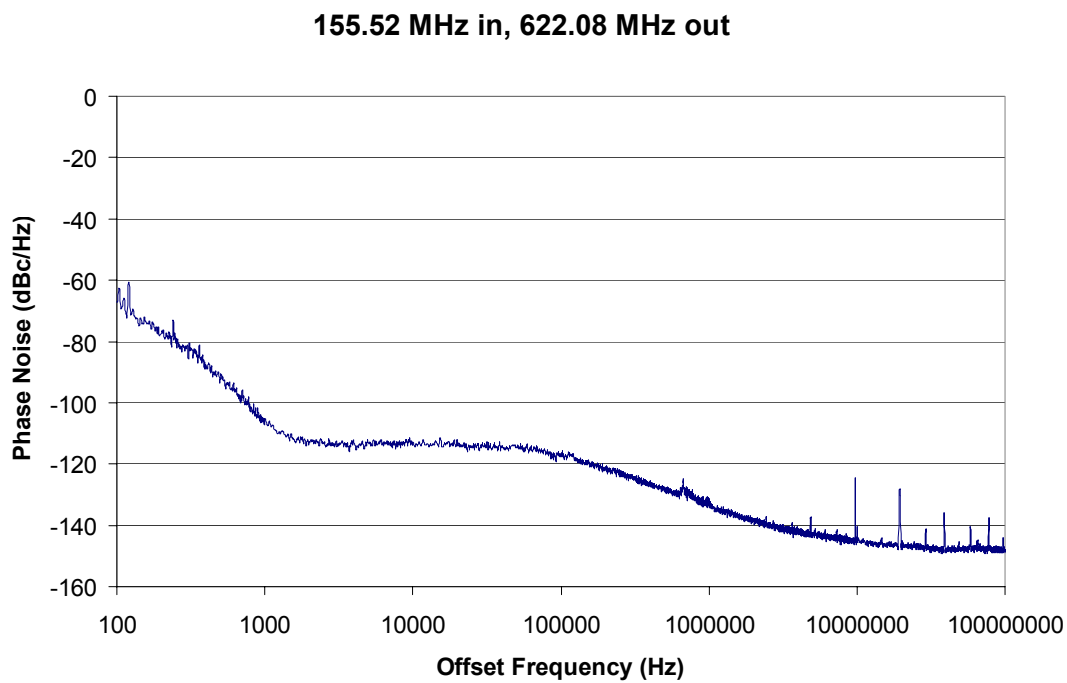
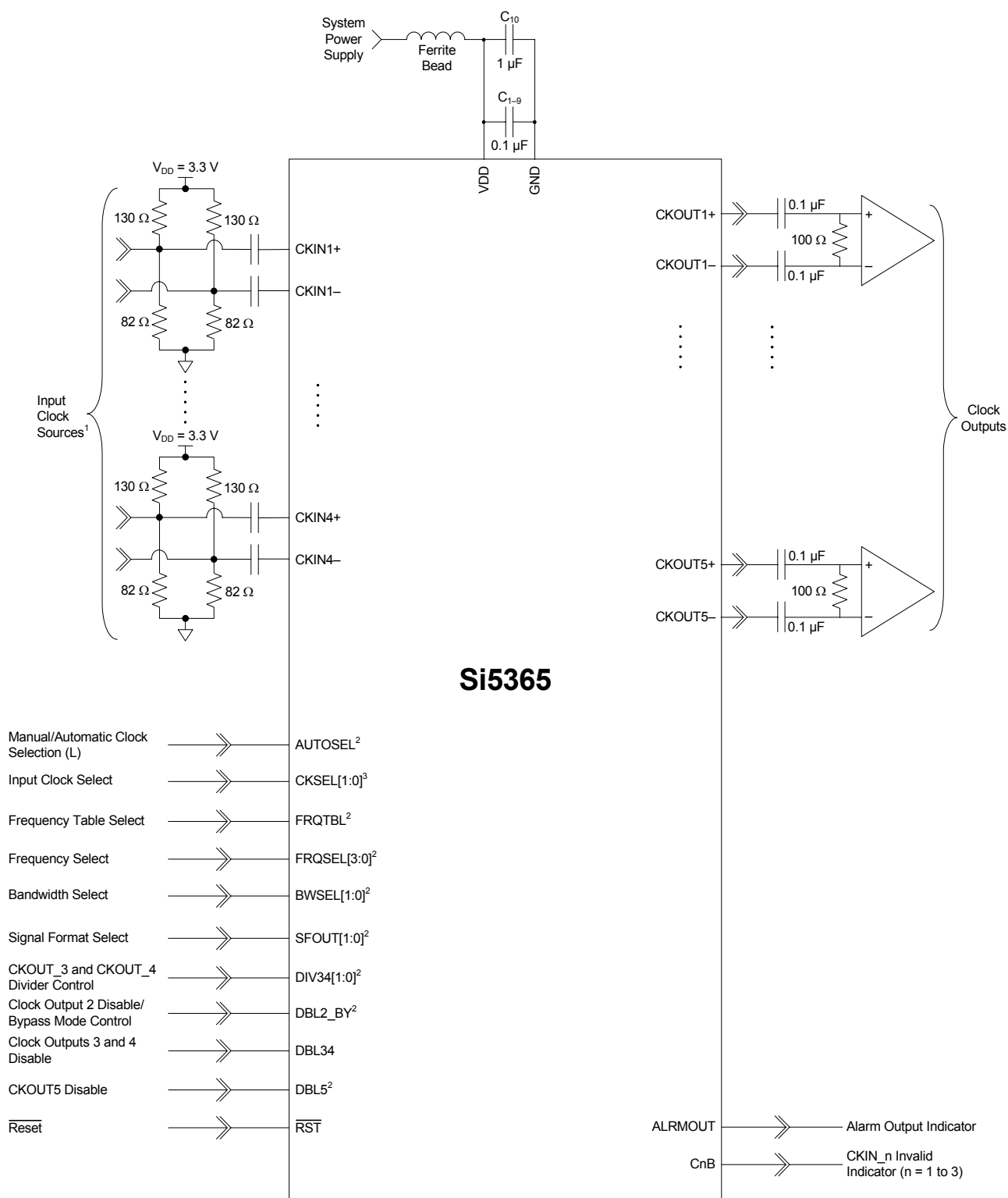


Figure 1. Typical Phase Noise Plot



Notes: 1. Assumes differential LVPECL termination (3.3 V) on clock inputs.
 2. Denotes tri-level input pins with states designated as L (ground), M ($V_{DD}/2$), and H (V_{DD}).
 3. Assumes manual input clock selection.

Figure 2. Si5365 Typical Application Circuit

1. Functional Description

The Si5365 is a low jitter, precision clock multiplier for high-speed communication systems, including SONET OC-48/OC-192, Ethernet, and Fibre Channel, in which the application requires clock multiplication without jitter attenuation. The Si5365 accepts four clock inputs ranging from 19.44 to 707 MHz and generates five frequency-multiplied clock outputs ranging from 19.44 to 1050 MHz. By default the four clock inputs are at the same frequency and the five clock outputs are at the same frequency. Two of the output clocks can be divided down further to generate an integer sub-multiple frequency. The input clock frequency and clock multiplication ratio are selectable from a table of popular SONET, Ethernet, and Fibre Channel rates. In addition to providing clock multiplication in SONET and datacom applications, the Si5365 supports SONET-to-datacom frequency translations. Silicon Laboratories offers a PC-based software utility, *DSPLLsim*, that can be used to look up valid Si5365 frequency translations. This utility can be downloaded from www.silabs.com/timing. This information is also available in the Any-Rate Precision Clock Family Reference Manual, also available from www.silabs.com/timing.

The Si5365 is based on Silicon Laboratories' 3rd-generation DSPLL[®] technology, which provides any-rate frequency synthesis in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The Si5365 PLL loop bandwidth is digitally programmable via the BWSEL[1:0] pins and supports a range from 30 kHz to 1.3 MHz. The *DSPLLsim* software utility can be used to calculate valid loop bandwidth settings for a given input clock frequency/clock multiplication ratio.

The Si5365 monitors all input clocks for loss-of-signal and provides a LOS alarm when it detects a missing clock.

In the case when the input clocks enter alarm conditions, the PLL will freeze the DCO output frequency near its last value to maintain operation with an internal state close to the last valid operating state.

The Si5365 has five differential clock outputs. The signal format of the clock outputs is programmable to support LVPECL, LVDS, CML, or CMOS loads. If not required, unused clock outputs can be powered down to minimize power consumption. The phase difference between the selected input clock and the output clocks is adjustable in 200 ps increments for system skew control. For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device is powered by a single 1.8 or 2.5 V supply.

1.1. Further Documentation

Consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual (FRM) for more detailed information about the Si5365. The FRM can be downloaded from www.silabs.com/timing.

Silicon Laboratories has developed a PC-based software utility called *DSPLLsim* to simplify device configuration, including frequency planning and loop bandwidth selection. This utility can be downloaded from www.silabs.com/timing.

2. Pin Descriptions: Si5365

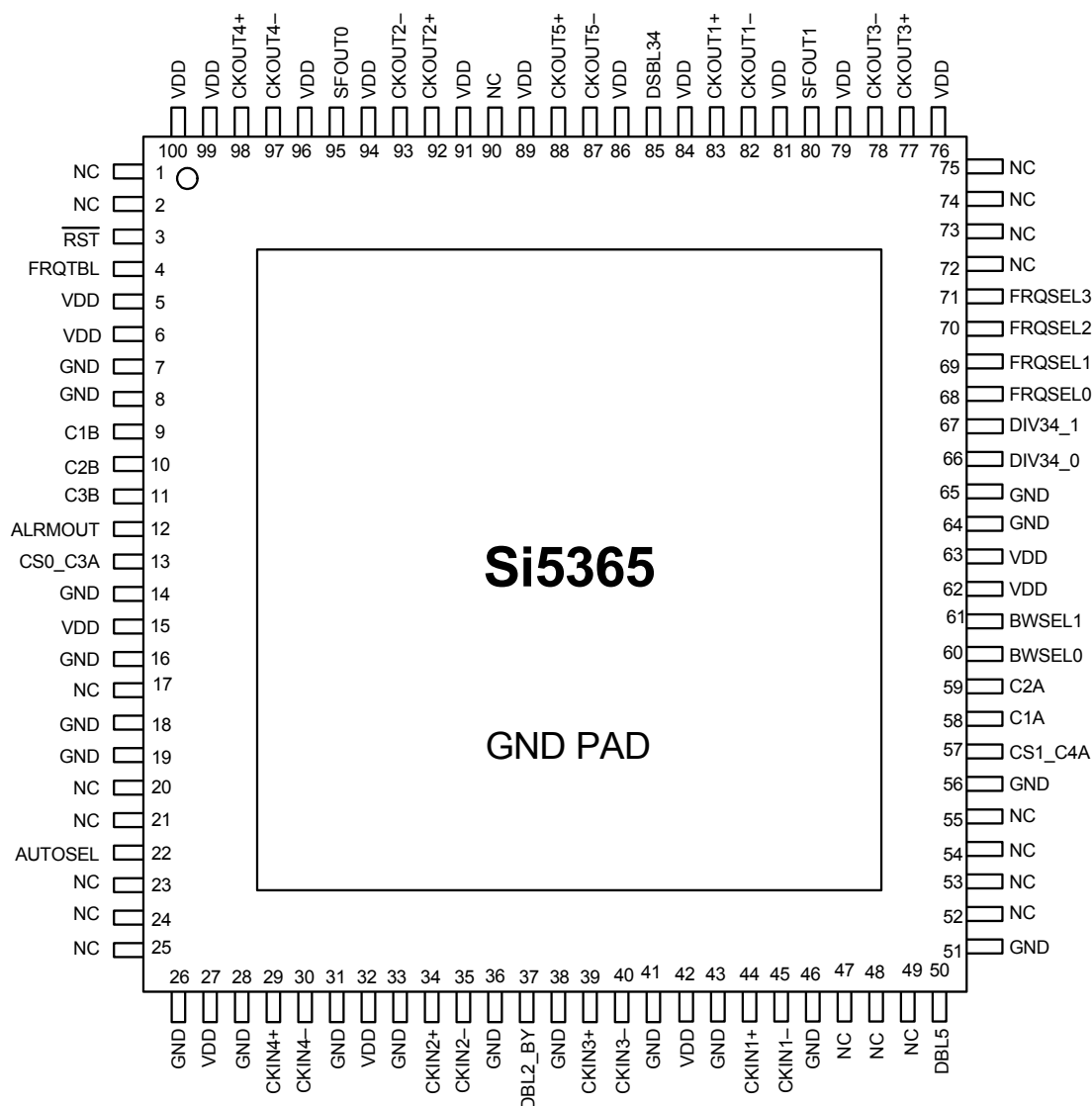


Table 3. Si5365 Pin Descriptions

Pin #	Pin Name	I/O	Signal Level	Description
1, 2, 17, 20, 21, 23, 24, 25, 47, 48, 49, 52, 53, 54, 55, 72, 73, 74, 75, 90	NC			No Connect. These pins must be left unconnected for normal operation.

Table 3. Si5365 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description																				
3	RST	I	LVC MOS	External Reset. Active low input that performs external hardware reset of device. Resets all internal logic to a known state and forces the device registers to their default value. Clock outputs are tristated during reset. After rising edge of RST signal, the device will perform an internal self-calibration. This pin has a weak pull-up.																				
4	FRQTBL	I	3-Level	Frequency Table Select. This pin selects SONET/SDH, datacom, or SONET/SDH to datacom frequency translation table. L = SONET/SDH. M = Datacom. H = SONET/SDH to Datacom. This pin has a weak pull-down.																				
5, 6, 15, 27, 32, 42, 62, 63, 76, 79, 81, 84, 86, 89, 91, 94, 96, 99, 100	V _{DD}	V _{DD}	Supply	V_{DD}. The device operates from a 1.8 or 2.5 V supply. Bypass capacitors should be associated with the following V _{DD} pins: <table><tr><td>Pins</td><td>Bypass Cap</td></tr><tr><td>5, 6</td><td>0.1 μF</td></tr><tr><td>15</td><td>0.1 μF</td></tr><tr><td>27</td><td>0.1 μF</td></tr><tr><td>62, 63</td><td>0.1 μF</td></tr><tr><td>76, 79</td><td>1.0 μF</td></tr><tr><td>81, 84</td><td>0.1 μF</td></tr><tr><td>86, 89</td><td>0.1 μF</td></tr><tr><td>91, 94</td><td>0.1 μF</td></tr><tr><td>96, 99, 100</td><td>0.1 μF</td></tr></table>	Pins	Bypass Cap	5, 6	0.1 μF	15	0.1 μF	27	0.1 μF	62, 63	0.1 μF	76, 79	1.0 μF	81, 84	0.1 μF	86, 89	0.1 μF	91, 94	0.1 μF	96, 99, 100	0.1 μF
Pins	Bypass Cap																							
5, 6	0.1 μF																							
15	0.1 μF																							
27	0.1 μF																							
62, 63	0.1 μF																							
76, 79	1.0 μF																							
81, 84	0.1 μF																							
86, 89	0.1 μF																							
91, 94	0.1 μF																							
96, 99, 100	0.1 μF																							
7, 8, 14, 16, 18, 19, 26, 28, 31, 33, 36, 38, 41, 43, 46, 51, 56, 64, 65	GND	GND	Supply	Ground. These pins must be connected to system ground. Minimize the ground path impedance for optimal performance.																				
9	C1B	O	LVC MOS	CKIN1 Invalid Indicator. This pin is an active high alarm output associated with CKIN1. Once triggered, the alarm will remain high until CKIN1 is validated. 0 = No alarm on CKIN1. 1 = Alarm on CKIN1.																				
10	C2B	O	LVC MOS	CKIN2 Invalid Indicator. This pin is an active high alarm output associated with CKIN2. Once triggered, the alarm will remain high until CKIN2 is validated. 0 = No alarm on CKIN2. 1 = Alarm on CKIN2.																				
11	C3B	O	LVC MOS	CKIN3 Invalid Indicator. This pin is an active high alarm output associated with CKIN3. 0 = No alarm on CKIN3. 1 = Alarm on CKIN3.																				

Table 3. Si5365 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description										
12	ALRMOUT	O	LVC MOS	Alarm Output Indicator. This pin is an active high alarm output associated with CKIN4 or the frame sync alignment alarm. 0 = ALRMOUT not active. 1 = ALRMOUT active.										
13 57	CS0_C3A CS1_C4A	I/O	LVC MOS	Input Clock Select/CKINn Active Clock Indicator. If manual clock selection mode is chosen (AUTOSEL = 1), the CS[1:0] pins function as the manual input clock selector control. <table border="1"><thead><tr><th>CS[1:0]</th><th>Active Input Clock</th></tr></thead><tbody><tr><td>00</td><td>CKIN1</td></tr><tr><td>01</td><td>CKIN2</td></tr><tr><td>10</td><td>CKIN3</td></tr><tr><td>11</td><td>CKIN4</td></tr></tbody></table> These inputs are internally deglitched to prevent inadvertent clock switching during changes in the CSn input state. If automatic clock detection is chosen (AUTOSEL = M or H), these pins function as the CKINn active clock indicator output. 0 = CKINn is not the active input clock. 1 = CKINn is currently the active input clock to the PLL. This pin has a weak pull-down.	CS[1:0]	Active Input Clock	00	CKIN1	01	CKIN2	10	CKIN3	11	CKIN4
CS[1:0]	Active Input Clock													
00	CKIN1													
01	CKIN2													
10	CKIN3													
11	CKIN4													
22	AUTOSEL	I	3-Level	Manual/Automatic Clock Selection. Three level input that selects the method of input clock selection to be used. L = Manual. M = Automatic non-revertive. H = Automatic revertive.										
29 30	CKIN4+ CKIN4–	I	MULTI	Clock Input 4. Differential clock input. This input can also be driven with a single-ended signal.										
34 35	CKIN2+ CKIN2–	I	MULTI	Clock Input 2. Differential input clock. This input can also be driven with a single-ended signal.										
37	DBL2_BY	I	3-Level	CKOUT2 Disable/PLL Bypass Mode Control. Controls enable of CKOUT2 divider/output buffer path and PLL bypass mode. L = CKOUT2 Enabled. M = CKOUT2 Disabled. H = BYPASS Mode with CKOUT2 enabled.										
39 40	CKIN3+ CKIN3–	I	MULTI	Clock Input 3. Differential clock input. This input can also be driven with a single-ended signal.										
44 45	CKIN1+ CKIN1–	I	MULTI	Clock Input 1. Differential clock input. This input can also be driven with a single-ended signal.										

Table 3. Si5365 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
50	DBL5	I	3-Level	CKOUT5 Disable. This pin performs the following functions: L = Normal operation. Output path is active and signal format is determined by SFOUT inputs. M = CMOS signal format. Overrides SFOUT signal format to allow CKOUT5 to operate in CMOS format while the clock outputs operate in a differential output format. H = Powerdown. Entire CKOUT5 divider and output buffer path is powered down. CKOUT5 output will be in tristate mode during powerdown.
58	C1A	O	LVC MOS	CKIN1 Active Clock Indicator. This pin serves as the CKIN1 active clock indicator. 0 = CKIN1 is not the active input clock. 1 = CKIN1 is currently the active input clock to the PLL.
59	C2A	O	LVC MOS	CKIN2 Active Clock Indicator. This pin serves as the CKIN2 active clock indicator. 0 = CKIN2 is not the active input clock. 1 = CKIN2 is currently the active input clock to the PLL.
60 61	BWSEL0 BWSEL1	I	3-Level	Bandwidth Select. These pins are three level inputs that select the DSPLL closed loop bandwidth according to the Any-Rate Precision Clock Family Reference Manual.
66 67	DIV34_0 DIV34_1	I	3-Level	CKOUT3 and CKOUT4 Divider Control. These pins control the division of CKOUT3 and CKOUT4 relative to the CKOUT2 output frequency. Detailed operations and timing characteristics for these pins may be found in the Any-Rate Precision Clock Family Reference Manual.
68 69 70 71	FRQSEL0 FRQSEL1 FRQSEL2 FRQSEL3	I	3-Level	Multiplier Select. These pins are three level inputs that select the input clock and clock multiplication setting according to the Any-Rate Precision Clock Family Reference Manual, depending on the FRQTBL setting.
77 78	CKOUT3+ CKOUT3–	O	MULTI	Clock Output 3. Differential output clock with a frequency specified by FRQSEL and FRQTBL settings. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.

Table 3. Si5365 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description																				
80 95	SFOUT1 SFOUT0	I	3-Level	Signal Format Select. Three level inputs that select the output signal format (common mode voltage and differential swing) for all of the clock outputs and CKOUT5. <table><tr><th>SFOUT[1:0]</th><th>Signal Format</th></tr><tr><td>HH</td><td>Reserved</td></tr><tr><td>HM</td><td>Reserved</td></tr><tr><td>HL</td><td>CML</td></tr><tr><td>MH</td><td>LVPECL</td></tr><tr><td>MM</td><td>Reserved</td></tr><tr><td>ML</td><td>LVDS</td></tr><tr><td>LH</td><td>CMOS</td></tr><tr><td>LM</td><td>Tristate/Sleep</td></tr><tr><td>LL</td><td>Reserved</td></tr></table>	SFOUT[1:0]	Signal Format	HH	Reserved	HM	Reserved	HL	CML	MH	LVPECL	MM	Reserved	ML	LVDS	LH	CMOS	LM	Tristate/Sleep	LL	Reserved
SFOUT[1:0]	Signal Format																							
HH	Reserved																							
HM	Reserved																							
HL	CML																							
MH	LVPECL																							
MM	Reserved																							
ML	LVDS																							
LH	CMOS																							
LM	Tristate/Sleep																							
LL	Reserved																							
82 83	CKOUT1– CKOUT1+	O	MULTI	Clock Output 1. Differential output clock with a frequency specified by FRQSEL and FRQTBL. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.																				
85	DBL34	I	LVC MOS	Output 3 and 4 Disable. Active high input. When active, entire CKOUT3 and CKOUT4 divider and output buffer path is powered down. CKOUT3 and CKOUT4 outputs will be in tristate mode during powerdown. This pin has a weak pull-down.																				
87 88	CKOUT5– CKOUT5+	O	MULTI	Clock Output 5. Fifth high-speed clock output with a frequency specified by FRQSEL and FRQTBL. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.																				
92 93	CKOUT2+ CKOUT2–	O	MULTI	Clock Output 2. Differential output clock with a frequency specified by FRQSEL and FRQTBL. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.																				
97 98	CKOUT4– CKOUT4+	O	MULTI	Clock Output 4. Differential output clock with a frequency specified by FRQSEL and FRQTBL settings. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.																				
GND PAD	GND PAD	GND	Supply	Ground Pad. The ground pad must provide a low thermal and electrical impedance to a ground plane.																				

3. Ordering Guide

Ordering Part Number	Package	Temperature Range
Si5365-B-GQ	100-Pin 14 x 14 mm TQFP	–40 to 85 °C

4. Package Outline: 100-Pin TQFP

Figure 3 illustrates the package details for the Si5365. Table 4 lists the values for the dimensions shown in the illustration.

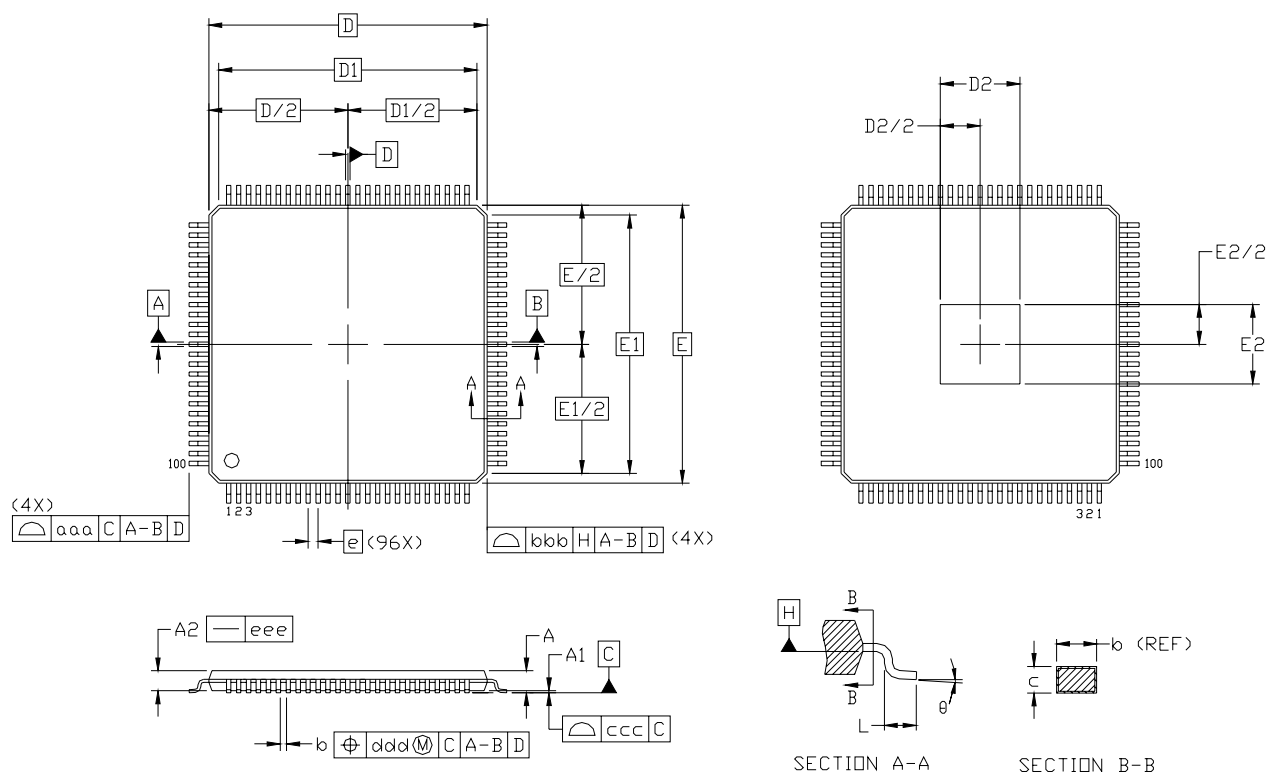


Figure 3. 100-Pin Thin Quad Flat Package (TQFP)

Table 4. 100-Pin Package Diagram Dimensions

Dimension	Min	Nom	Max	Dimension	Min	Nom	Max
A	—	—	1.20	E	16.00 BSC.		
A1	0.05	—	0.15	E1	14.00 BSC.		
A2	0.95	1.00	1.05	E2	3.85	4.00	4.15
b	0.17	0.22	0.27	L	0.45	0.60	0.75
c	0.09	—	0.20	aaa	—	—	0.20
D	16.00 BSC.			bbb	—	—	0.20
D1	14.00 BSC.			ccc	—	—	0.08
D2	3.85	4.00	4.15	ddd	—	—	0.08
e	0.50 BSC.			Θ	0°	3.5°	7°

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant AED-HD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

5. Recommended PCB Layout

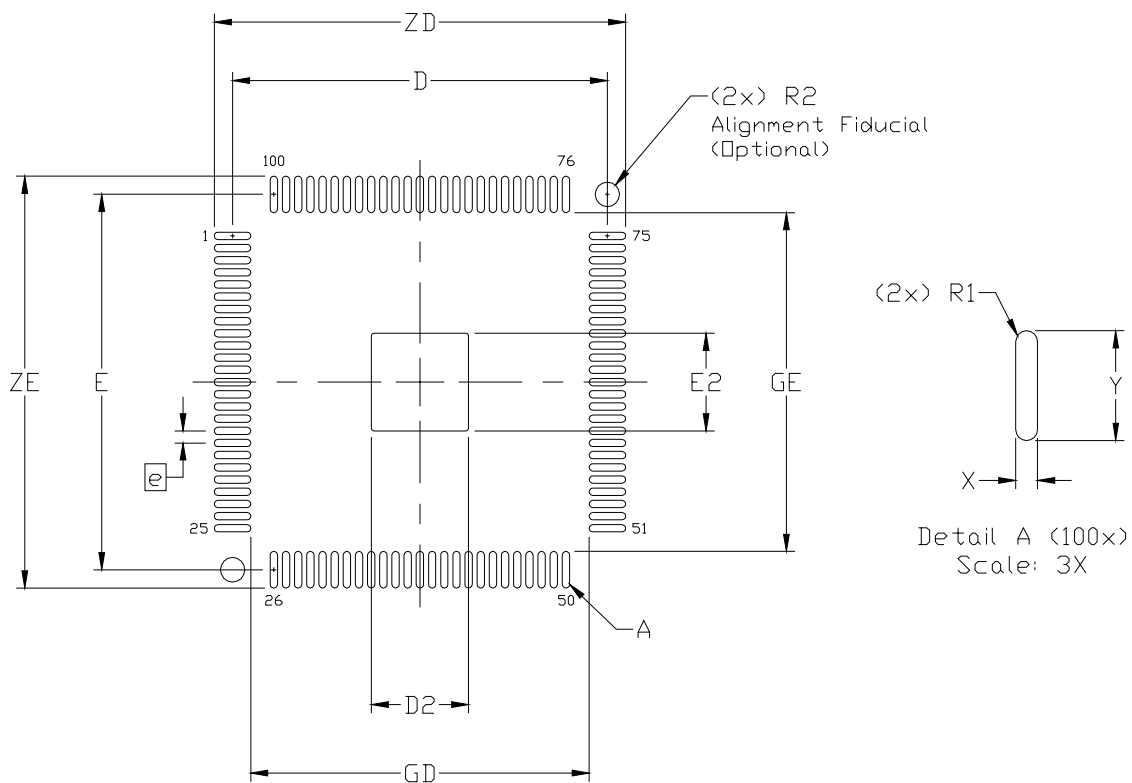


Figure 4. PCB Land Pattern Diagram

Table 5. PCB Land Pattern Dimensions

Dimension	MIN	MAX
e	0.50 BSC.	
E	15.40 REF.	
D	15.40 REF.	
E2	3.90	4.10
D2	3.90	4.10
GE	13.90	—
GD	13.90	—
X	—	0.30
Y	1.50 REF.	
ZE	—	16.90
ZD	—	16.90
R1	0.15 REF	
R2	—	1.00

Notes (General):

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Notes (Solder Mask Design):

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μ m minimum, all the way around the pad.

Notes (Stencil Design):

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 4 x 4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

Notes (Card Assembly):

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

DOCUMENT CHANGE LIST

Revision 0.32 to Revision 0.33

- Condensed format.

Revision 0.33 to Revision 0.34

- Removed references to latency control, INC, and DEC pins.
- Updated Table 1, "Performance Specifications," on page 2.
- Changed LVTTTL to LVCMOS in Table 2, "Absolute Maximum Ratings," on page 3.
- Added Figure 1, "Typical Phase Noise Plot," on page 4.
- Updated Figure 2, "Si5365 Typical Application Circuit".
- Updated "2. Pin Descriptions: Si5365".
- Updated "3. Ordering Guide" on page 12.
- Added "5. Recommended PCB Layout".

NOTES:

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