

**1M x 32 5.0V IC DRAM Card**
**Features**

- Industry Standard 88Pin IC DRAM Card
- Performance:

|           |                              |       |
|-----------|------------------------------|-------|
|           |                              | -70   |
| $t_{RAC}$ | $\overline{RAS}$ Access Time | 70ns  |
| $t_{CAC}$ | $\overline{CAS}$ Access Time | 29ns  |
| $t_{AA}$  | Access Time From Address     | 46ns  |
| $t_{RC}$  | Cycle Time                   | 130ns |
| $t_{PC}$  | Fast Page Mode Cycle Time    | 45ns  |

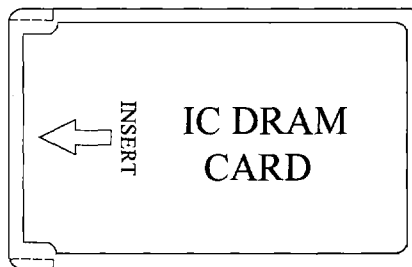
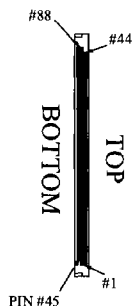
- Industry Standard DRAM functions & timings
- High Performance CMOS process

- Single 5.0,  $\pm$  0.25V Power Supply
- All inputs buffered except  $\overline{RAS}$  and DATA inputs
- Multiple  $\overline{RAS}$  inputs for x16 or x32 selectability
- 10/10 Addressing (Row/Column)
- Optional Fast Page Mode access cycle
- Refresh Modes:  $\overline{RAS}$ -Only,  $\overline{CAS}$  before  $\overline{RAS}$  and BBU (Battery Backup)
- 1024 refresh cycles distributed across 128ms
- Polarized Connector

**Description**

The IBM11J1320BL is a 4MB industry standard 88-pin IC DRAM card. It is organized as a 1M x 32 high speed memory array. It is built using 8 1Mx4 devices and is compatible to the JEDEC/PCM-CIA/JEIDA 88-pin standard. Improved system performance is provided by the on-card buffering of selected input signals. The specified timings include all buffer, net and skew delays, which allow the system designer to work with a simpler interface. The DQ and  $\overline{RAS}$  signals are not buffered, which preserves the access specification of 70ns. Multiple  $\overline{RAS}$  inputs are used to conserve power by allowing individual bank selection. In the x32 configuration

the memory is a single bank, having four unique bytes. The x16 configuration may be utilized as two banks each having two unique bytes. Only one bank is activated by each  $\overline{RAS}$ , leaving the other bank in standby mode, thus saving power. All IBM IC DRAM cards are packaged in a rugged metal case for maximum device protection in portable applications. The related 1M x 36 versions of these IC DRAM cards is IBM11J1360BLA.

**Card Outline**




**1M x 32 5.0V IC DRAM Card**

**Pin Description**

|                                       |                       |
|---------------------------------------|-----------------------|
| $\overline{RAS0}$ , $\overline{RAS2}$ | Row Address Strobe    |
| $\overline{CAS0}$ - $\overline{CAS3}$ | Column Address Strobe |
| $\overline{WE}$                       | Read/write Input      |
| A0 - A9                               | Address Inputs        |
| DQ0-7, 9-16, 18-25, 27-34             | Data Input/output     |
| V <sub>CC</sub>                       | Power (+5V)           |
| V <sub>SS</sub>                       | Ground                |
| NC                                    | No Connect            |
| PD1 - PD8                             | Presence Detects      |

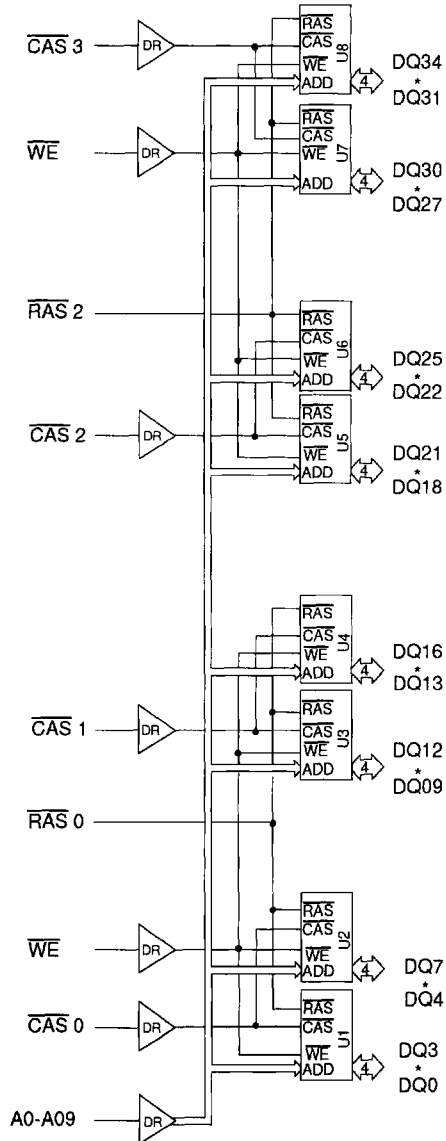
**Pinout**

| Pin# | Name              | Pin# | Name              | Pin# | Name              | Pin# | Name              |
|------|-------------------|------|-------------------|------|-------------------|------|-------------------|
| 1    | V <sub>SS</sub>   | 23   | $\overline{CAS0}$ | 45   | V <sub>SS</sub>   | 67   | V <sub>SS</sub>   |
| 2    | DQ1               | 24   | $\overline{CAS1}$ | 46   | DQ18              | 68   | $\overline{CAS3}$ |
| 3    | DQ1               | 25   | NC                | 47   | DQ19              | 69   | NC                |
| 4    | DQ2               | 26   | $\overline{RAS2}$ | 48   | DQ20              | 70   | $\overline{WE}$   |
| 5    | DQ3               | 27   | V <sub>CC</sub>   | 49   | DQ21              | 71   | PD1               |
| 6    | DQ4               | 28   | PD2               | 50   | DQ22              | 72   | PD3               |
| 7    | DQ5               | 29   | PD4               | 51   | DQ23              | 73   | V <sub>SS</sub>   |
| 8    | DQ6               | 30   | PD6               | 52   | DQ24              | 74   | PD5               |
| 9    | V <sub>CC</sub>   | 31   | NC                | 53   | DQ25              | 75   | PD7               |
| 10   | DQ7               | 32   | NC                | 54   | NC                | 76   | PD8               |
| 11   | NC                | 33   | NC                | 55   | NC                | 77   | NC                |
| 12   | NC                | 34   | DQ9               | 56   | V <sub>SS</sub>   | 78   | NC                |
| 13   | A0                | 35   | NC                | 57   | A1                | 79   | NC                |
| 14   | A2                | 36   | DQ10              | 58   | A3                | 80   | DQ27              |
| 15   | V <sub>CC</sub>   | 37   | V <sub>CC</sub>   | 59   | A5                | 81   | DQ28              |
| 16   | A4                | 38   | DQ11              | 60   | A7                | 82   | DQ29              |
| 17   | NC                | 39   | DQ12              | 61   | A9                | 83   | DQ30              |
| 18   | A6                | 40   | DQ13              | 62   | NC                | 84   | DQ31              |
| 19   | A8                | 41   | DQ14              | 63   | V <sub>SS</sub>   | 85   | DQ32              |
| 20   | NC                | 42   | DQ15              | 64   | NC                | 86   | DQ33              |
| 21   | NC                | 43   | DQ16              | 65   | NC                | 87   | DQ34              |
| 22   | $\overline{RAS0}$ | 44   | V <sub>SS</sub>   | 66   | $\overline{CAS2}$ | 88   | V <sub>SS</sub>   |

1. DQ numbering is compatible with parity (x36) version)

**Ordering Information**

| Part Number      | Organization | Speed | Notes  |
|------------------|--------------|-------|--|
| IBM11J1320BLA-70 | 1M x 32      | 70ns  | For 80ns applications use this 70ns Part Number. Be aware if the application makes use of PD's, PD6 & PD7 are different from the 70ns version. |

**Block Diagram**


**1M x 32 5.0V IC DRAM Card**
**Truth Table**

| Function   | $\overline{\text{RAS}}$ | $\overline{\text{CAS}}$ | $\overline{\text{WE}}$ | Row Address | Column Address | All DQ bits    |
|--|-------------------------|-------------------------|------------------------|-------------|----------------|----------------|
| Standby  | H                       | X                       | X                      | X           | X              | High Impedance |
| Read   | L                       | L                       | H                      | Row         | Col            | Valid Data Out |
| Early-Write  | L                       | L                       | L                      | Row         | Col            | Valid Data In  |
| Fast Page Mode - Read:<br>1st Cycle                              | L                       | H→L                     | H                      | Row         | Col            | Valid Data Out |
| Subsequent Cycles  | L                       | H→L                     | H                      | N/A         | Col            | Valid Data Out |
| Fast Page Mode - Write:<br>1st Cycle                             | L                       | H→L                     | L                      | Row         | Col            | Valid Data In  |
| Subsequent Cycles  | L                       | H→L                     | L                      | N/A         | Col            | Valid Data In  |
| $\overline{\text{RAS}}$ -Only Refresh                            | L                       | H                       | X                      | Row         | N/A            | High Impedance |
| $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh | H→L                     | L                       | H                      | X           | X              | High Impedance |

**Presence Detect**

| Pin                                   | -70             |
|---------------------------------------|-----------------|
| PD1 (PD1 - PD4: Addressing/Dram Type) | V <sub>ss</sub> |
| PD2                                   | NC              |
| PD3                                   | V <sub>ss</sub> |
| PD4                                   | V <sub>ss</sub> |
| PD5 ( Number of Banks/Organization)   | NC              |
| PD6 ( Speed)                          | V <sub>ss</sub> |
| PD7                                   | NC              |
| PD8 (Refresh Type)                    | NC              |
| 1. NC= OPEN, V <sub>ss</sub> = GND    |                 |

### Absolute Maximum Ratings

| Symbol    | Parameter                                | Rating                 | Units | Notes |
|-----------|--|------------------------|-------|-------|
| $V_{CC}$  | Power Supply Voltage                     | -1.0 to +6.0           | V     | 1     |
| $V_{IN}$  | Input Voltage ( $\overline{RAS}$ & DATA) | -1.0 to +6.0           | V     | 1     |
|           | Input Voltage (Redriven Signals)         | -0.5 to $V_{CC} + 0.5$ | V     | 1     |
| $V_{OUT}$ | Output Voltage                           | -1.0 to +6.0           | V     | 1     |
| $T_{OPR}$ | Operating Temperature                    | 0 to +55               | °C    | 1     |
| $T_{STG}$ | Storage Temperature                      | -40 to +85             | °C    | 1     |
| $P_D$     | Power Dissipation                        | 4.2                    | W     | 1, 2  |
| $I_{OUT}$ | Short Circuit Output Current             | 50                     | mA    | 1     |

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

### Recommended DC Operating Conditions ( $T_A = 0$ to $55^\circ\text{C}$ )

| Symbol   | Parameter                                     | Min  | Typ | Max          | Units | Notes |
|----------|---|------|-----|--------------|-------|-------|
| $V_{CC}$ | Supply Voltage                                | 4.75 | 5.0 | 5.25         | V     | 1     |
| $V_{IH}$ | Input High Voltage ( $\overline{RAS}$ & DATA) | 2.4  | —   | $V_{CC}+0.5$ | V     | 1     |
|          | Input High Voltage (Redriven Signals)         | 2.0  | —   | $V_{CC}$     | V     | 1     |
| $V_{IL}$ | Input Low Voltage ( $\overline{RAS}$ & DATA)  | -0.5 | —   | 0.8          | V     | 1     |
|          | Input Low Voltage (Redriven Signals)          | 0.0  | —   | 0.8          | V     | 1     |

1. All voltages referenced to  $V_{SS}$ .

### Capacitance ( $T_A = 0$ to $+55^\circ\text{C}$ , $V_{CC} = 5.0 \pm 0.25\text{V}$ )

| Symbol    | Parameter                              | Max | Units | Notes |
|-----------|--|-----|-------|-------|
| $C_{I1}$  | Input Capacitance (A0-A9)              | 15  | pF    |       |
| $C_{I2}$  | Input Capacitance ( $\overline{RAS}$ ) | 43  | pF    |       |
| $C_{I3}$  | Input Capacitance ( $\overline{CAS}$ ) | 15  | pF    |       |
| $C_{I4}$  | Input Capacitance ( $\overline{WE}$ )  | 20  | pF    |       |
| $C_{I/O}$ | Output Capacitance (DQ0-DQ34)          | 25  | pF    |       |

## 1M x 32 5.0V IC DRAM Card

DC Electrical Characteristics ( $T_A = 0$  to  $+55^\circ\text{C}$ ,  $V_{CC} = 5.0 \pm 0.25\text{V}$ )

| Symbol    | Parameter   | Min   | Max | Units | Notes         |         |
|-----------|---|---|-----|-------|---------------|---------|
| $I_{CC1}$ | Operating Current<br>Average Power Supply Operating Current<br>( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , Address Cycling: $t_{RC} = t_{RC \text{ min}}$ )   | -70   | —   | 800   | mA            |         |
| $I_{CC2}$ | Standby Current (TTL)<br>Power Supply Standby Current<br>( $\overline{\text{RAS}} = \overline{\text{CAS}} \geq V_{IH}$ )  | —   | —   | 16    | mA            | 1, 3    |
| $I_{CC3}$ | $\overline{\text{RAS}}$ Only Refresh Current<br>Average Power Supply Current, $\overline{\text{RAS}}$ Only Mode<br>( $\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} \geq V_{IH}$ ; $t_{RC} = t_{RC \text{ min}}$ )   | -70   | —   | 800   | mA            |         |
| $I_{CC4}$ | Fast Page Mode Current<br>Average Power Supply Current, Fast Page Mode<br>( $\overline{\text{RAS}} = V_{IL}$ , $\overline{\text{CAS}}$ , Address Cycling: $t_{PC} = t_{PC \text{ min}}$ )   | -70   | —   | 800   | mA            | 1, 2, 3 |
| $I_{CC5}$ | Standby Current (CMOS)<br>Power Supply Standby Current<br>( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{CC} - 0.2\text{V}$ )  | —   | —   | 1.6   | mA            |         |
| $I_{CC6}$ | $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Current<br>Average Power Supply Current, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Mode<br>( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , Cycling: $t_{RC} = t_{RC \text{ min}}$ ) | -70   | —   | 800   | mA            |         |
| $I_{CC7}$ | Battery Backup Refresh Current<br>Average Power Supply Current during Battery Backup refresh<br>( $\overline{\text{CAS}} \leq V_{IL}$ , $\overline{\text{WE}} \geq V_{IH}$ , $t_{RAS} \leq 1\mu\text{Sec}$ , $t_{RC} = 125\mu\text{Sec}$ )                            |   |     | 2.4   | mA            | 1, 2    |
| $I_{IL}$  | Input Leakage Current<br>Input Leakage Current, any input<br>( $0.0 \leq V_{IN} \leq (V_{CC} < 6.0\text{V})$ )<br>All Other Pins Not Under Test = 0V  | $\overline{\text{RAS}}$                           | -40 | +40   | $\mu\text{A}$ |         |
|           |   | $\overline{\text{CAS}}$ , $\overline{\text{ADD}}$ | -10 | +10   |               |         |
|           |   | $\overline{\text{WE}}$                            | -20 | +20   |               |         |
| $I_{OL}$  | Output Leakage Current<br>( $D_{OUT}$ is disabled, $0.0 \leq V_{OUT} \leq V_{CC}$ )   | -10   | +10 |       | $\mu\text{A}$ |         |
| $V_{OH}$  | Output High Level<br>Output "H" Level Voltage ( $I_{OUT} = -2\text{mA}$ @ 2.4V)   | 2.4   | —   |       | V             |         |
| $V_{OL}$  | Output Low Level<br>Output "L" Level Voltage ( $I_{OUT} = +2\text{mA}$ @ 0.4V)  | —   | 0.4 |       | V             | 4       |

1.  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$  and  $I_{CC6}$  depend on cycle rate.  
2.  $I_{CC1}$ ,  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.  
3. Address can be changed once or less while  $\overline{\text{RAS}} = V_{IL}$ . In the case of  $I_{CC4}$ , it can be changed once or less when  $\overline{\text{CAS}} = V_{IH}$   
4. Refresh current is specified for the X32 configuration using One Bank

**AC Characteristics** ( $T_A = 0$  to  $+55^\circ\text{C}$ ,  $V_{CC} = 5.0 \pm 0.25\text{V}$ )

- $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- An initial pause of  $100\mu\text{s}$  is required after power-up followed by 8  $\overline{\text{RAS}}$  only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycles instead of 8  $\overline{\text{RAS}}$  only refresh cycles is required.
- The specified timings include buffer, loading and skew delays: 2ns minimum, 10ns ( $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$ ) or 11ns (Address) maximum delay, no pulse shrinkage. The data and  $\overline{\text{RAS}}$  signals are not buffered, which preserves the DRAMs access specifications of 70ns
- AC measurements assume  $t_T = 5\text{ns}$ .

**Read, Write, and Refresh Cycles** (Common Parameters)

| Symbol    | Parameter   | -70 |     | Units | Notes |
|-----------|---|-----|-----|-------|-------|
|           |   | Min | Max |       |       |
| $t_{RC}$  | Random Read or Write Cycle Time                                   | 130 | —   | ns    |       |
| $t_{RP}$  | $\overline{\text{RAS}}$ Precharge Time                            | 50  | —   | ns    |       |
| $t_{CP}$  | $\overline{\text{CAS}}$ Precharge Time                            | 10  | —   | ns    |       |
| $t_{RAS}$ | $\overline{\text{RAS}}$ Pulse Width                               | 70  | 10K | ns    |       |
| $t_{CAS}$ | $\overline{\text{CAS}}$ Pulse Width                               | 21  | —   | ns    | 2     |
| $t_{ASR}$ | Row Address Setup Time  | 11  | —   | ns    |       |
| $t_{RAH}$ | Row Address Hold Time   | 10  | —   | ns    |       |
| $t_{ASC}$ | Column Address Setup Time   | 3   | —   | ns    |       |
| $t_{CAH}$ | Column Address Hold Time  | 17  | —   | ns    |       |
| $t_{RCD}$ | $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time     | 20  | 42  | ns    | 2     |
| $t_{RAD}$ | $\overline{\text{RAS}}$ to Column Address Delay Time              | 15  | 24  | ns    | 3     |
| $t_{RSH}$ | $\overline{\text{RAS}}$ Hold Time                                 | 29  | —   | ns    |       |
| $t_{CSH}$ | $\overline{\text{CAS}}$ Hold Time                                 | 70  | —   | ns    |       |
| $t_{CRP}$ | $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time | 20  | —   | ns    |       |
| $t_{DZC}$ | $\overline{\text{CAS}}$ Delay Time from $D_{IN}$                  | 0   | —   | ns    |       |
| $t_{AR}$  | Column Address Hold Time Referenced to $\overline{\text{RAS}}$    | —   | —   | ns    | 4     |
| $t_T$     | Transition Time (Rise and Fall)                                   | 3   | 50  | ns    |       |

- The minimum  $t_{CAS}$  requires  $t_{CSH}$  to be met for both writes and reads. Also, because of the buffer, the minimum  $t_{CAS}$  for a read cycle must be extended to guarantee the data out window ( $t_{OH}$ ) in the application. For example, a  $t_{CAS}$  of 19ns plus a minimum  $t_{OH}$  of 2ns would result in turning data out of the card at 21ns (7ns before max  $t_{CAC}$  of 28ns).
- Operation within the  $t_{RCD}$  (max) limit ensures that  $t_{RAC}$  (max) can be met.  $t_{RCD}$  (max) is specified as a reference point only: if  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (max) limit, then access time is controlled by  $t_{CAC}$ .
- Operation within the  $t_{RAD}$  (max) limit ensures that  $t_{RAC}$  (max) can be met.  $t_{RAD}$  (max) is specified as a reference point only: if  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (max) limit, then access time is controlled by  $t_{AA}$ .
- This timing parameter is not applicable to this product, but may apply to a related product in this family.

**1M x 32 5.0V IC DRAM Card**
**Write Cycle**

| Symbol    | Parameter  | -70 |     | Units | Notes |
|-----------|--|-----|-----|-------|-------|
|           |  | Min | Max |       |       |
| $t_{WCS}$ | Write Command Set Up Time                              | 2   | —   | ns    |       |
| $t_{WCH}$ | Write Command Hold Time                                | 15  | —   | ns    |       |
| $t_{WP}$  | Write Command Pulse Width                              | 16  | —   | ns    |       |
| $t_{RWL}$ | Write Command to $\overline{RAS}$ Lead Time            | —   | —   | ns    | 1     |
| $t_{CWL}$ | Write Command to $\overline{CAS}$ Lead Time            | —   | —   | ns    | 1     |
| $t_{WCR}$ | Write Command Hold Time Referenced to $\overline{RAS}$ | —   | —   | ns    | 1     |
| $t_{DHR}$ | Data Hold Time Referenced to $\overline{RAS}$          | —   | —   | ns    | 1     |
| $t_{DS}$  | $D_{IN}$ Setup Time                                    | 0   | —   | ns    |       |
| $t_{DH}$  | $D_{IN}$ Hold Time                                     | 25  | —   | ns    |       |

1. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.

**Read Cycle**

| Symbol    | Parameter                                    | -70 |     | Units | Notes |
|-----------|--|-----|-----|-------|-------|
|           |  | Min | Max |       |       |
| $t_{RAC}$ | Access Time from $\overline{RAS}$            | —   | 70  | ns    | 1, 2  |
| $t_{CAC}$ | Access Time from $\overline{CAS}$            | —   | 29  | ns    | 1, 2  |
| $t_{AA}$  | Access Time from Address                     | —   | 46  | ns    | 1, 2  |
| $t_{RCS}$ | Read Command Setup Time                      | 2   | —   | ns    |       |
| $t_{RCH}$ | Read Command Hold Time to $\overline{CAS}$   | 0   | —   | ns    | 3     |
| $t_{RRH}$ | Read Command Hold Time to $\overline{RAS}$   | 0   | —   | ns    | 3     |
| $t_{RAL}$ | Column Address to $\overline{RAS}$ Lead Time | 46  | —   | ns    |       |
| $t_{CAL}$ | Column Address to $\overline{CAS}$ Lead Time | —   | —   | ns    | 4     |
| $t_{CLZ}$ | $\overline{CAS}$ to Output in Low-Z          | 2   | —   | ns    |       |
| $t_{OH}$  | Output Data Hold Time                        | 2   | —   | ns    |       |
| $t_{CDD}$ | $\overline{CAS}$ to $D_{IN}$ Delay Time      | 29  | —   | ns    |       |
| $t_{OFF}$ | Output Buffer Turn-off Delay                 | 2   | 29  | ns    | 5     |

1. Access time is determined by the later of  $t_{RAC}$ ,  $t_{CAC}$ ,  $t_{AA}$  or  $t_{CPA}$ .  
2. Measured with two TTL loads and 100pF.  
3. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.  
4. This timing parameter is not applicable to this product, but may be applicable to a related product in this family.  
5.  $t_{OFF}$  (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.



### Fast Page Mode Cycle

| Symbol     | Parameter  | -70 |     | Units | Notes |
|------------|--|-----|-----|-------|-------|
|            |  | Min | Max |       |       |
| $t_{PC}$   | Fast Page Mode Cycle Time                                  | 45  | —   | ns    |       |
| $t_{RASP}$ | Fast Page Mode $\overline{RAS}$ Pulse Width                | 70  | 10K | ns    |       |
| $t_{CPRH}$ | $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge | 49  | —   | ns    |       |
| $t_{CPA}$  | Access Time from $\overline{CAS}$ Precharge                | —   | 49  | ns    | 1, 2  |

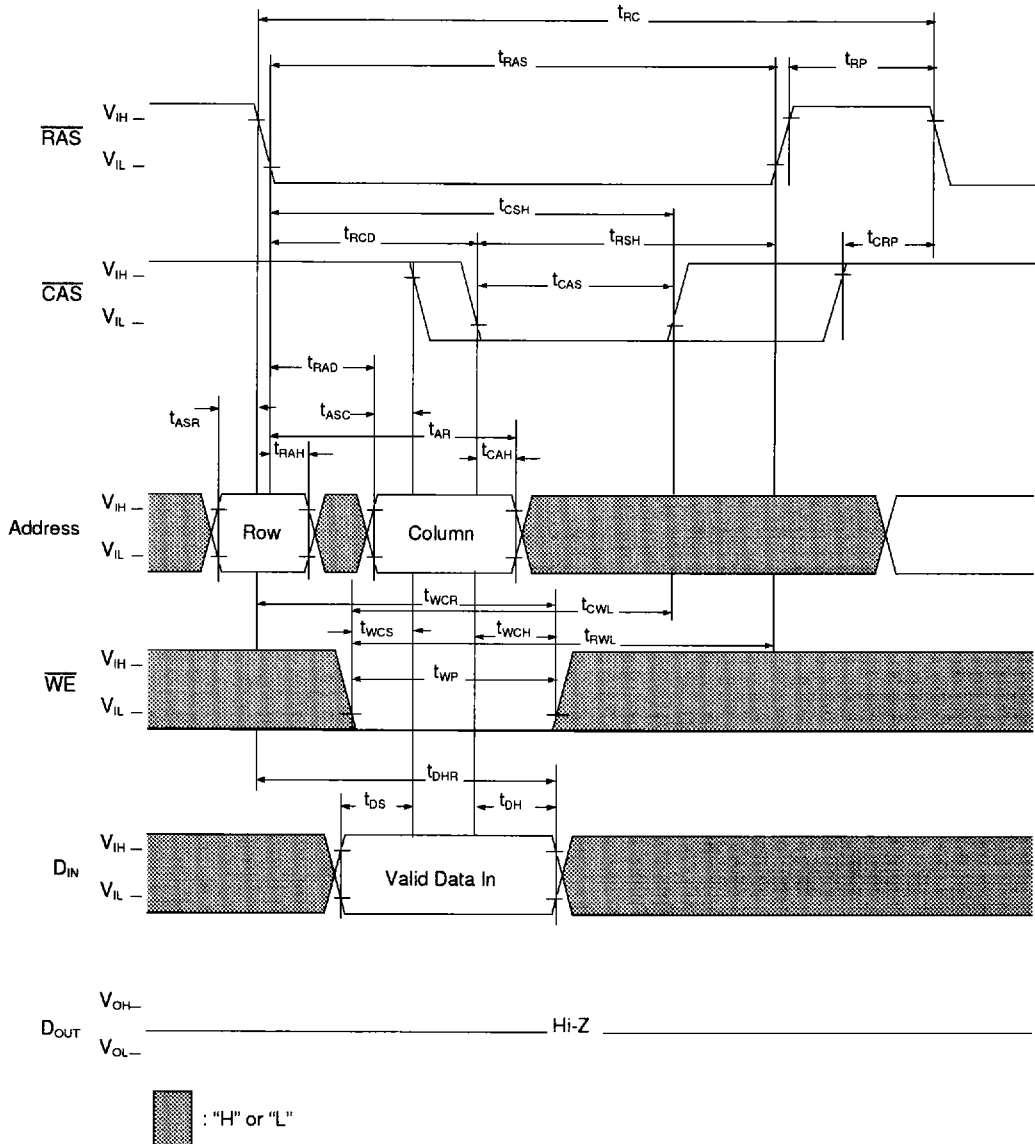
1. Access time is determined by the latter of  $t_{RAC}$ ,  $t_{CAC}$ ,  $t_{CPA}$ ,  $t_{AA}$ .  
2. Access time assumes a load of 100pf.

### Refresh Cycle

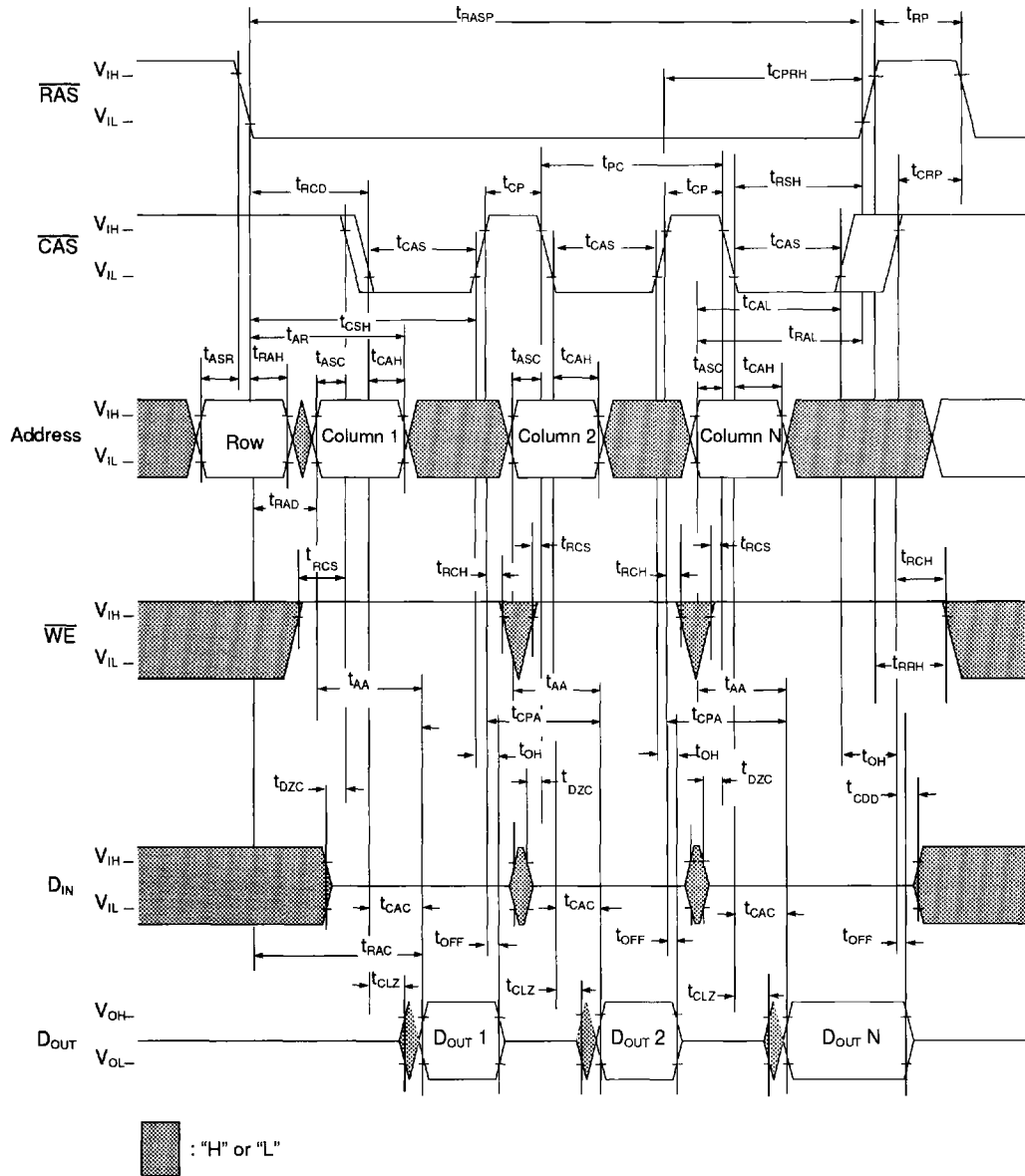
| Symbol    | Parameter  | -70 |     | Units | Notes |
|-----------|--|-----|-----|-------|-------|
|           |  | Min | Max |       |       |
| $t_{CHR}$ | $\overline{CAS}$ Hold Time<br>( $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)  | 13  | —   | ns    |       |
| $t_{CSR}$ | $\overline{CAS}$ Setup Time<br>( $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle) | 20  | —   | ns    |       |
| $t_{WRP}$ | $\overline{WE}$ Setup Time<br>( $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)  | 20  | —   | ns    |       |
| $t_{WRH}$ | $\overline{WE}$ Hold Time<br>( $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)   | 10  | —   | ns    |       |
| $t_{RPC}$ | $\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time                                 | 8   | —   | ns    |       |
| $t_{REF}$ | Refresh Period   | —   | 128 | ms    | 1     |

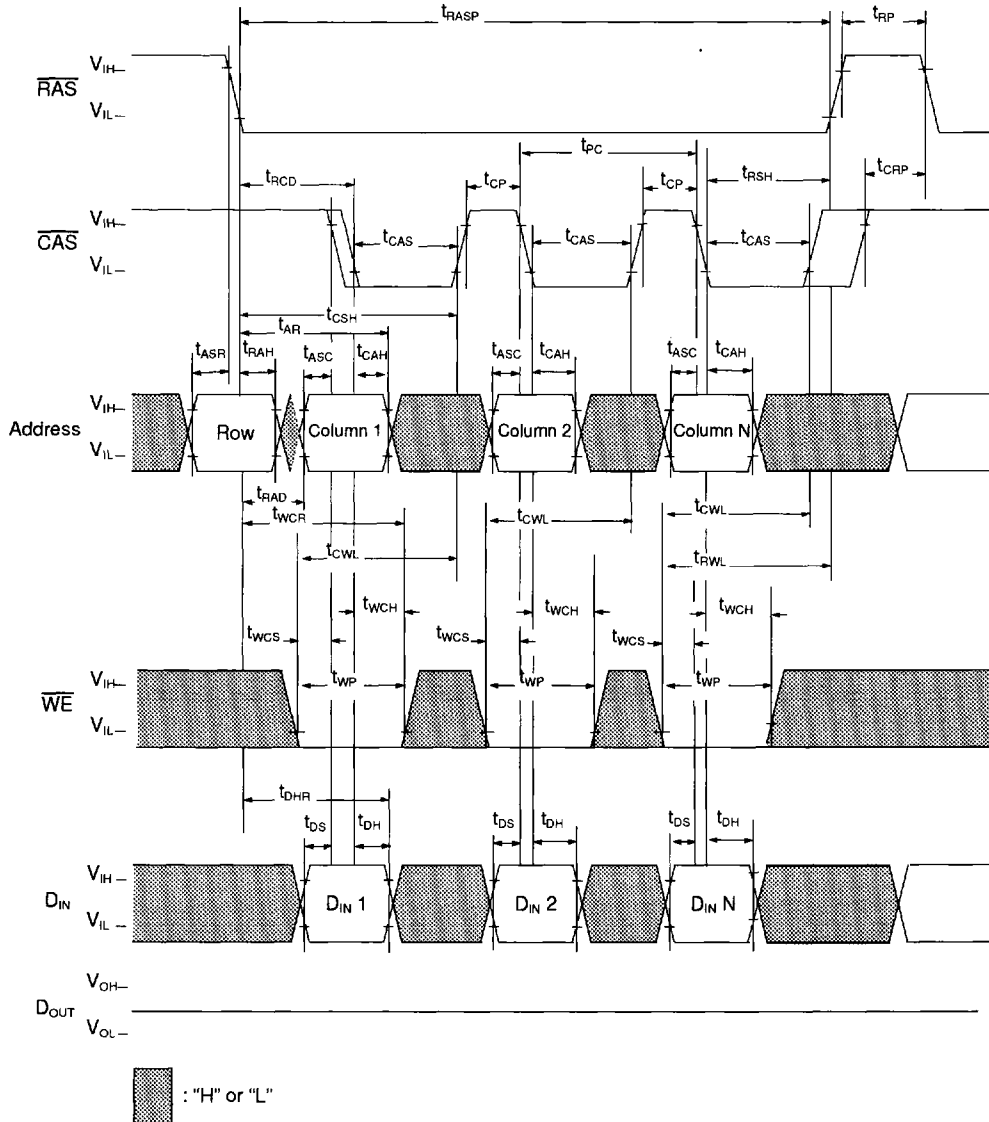
1. 1024 refreshes are required every 128ms.



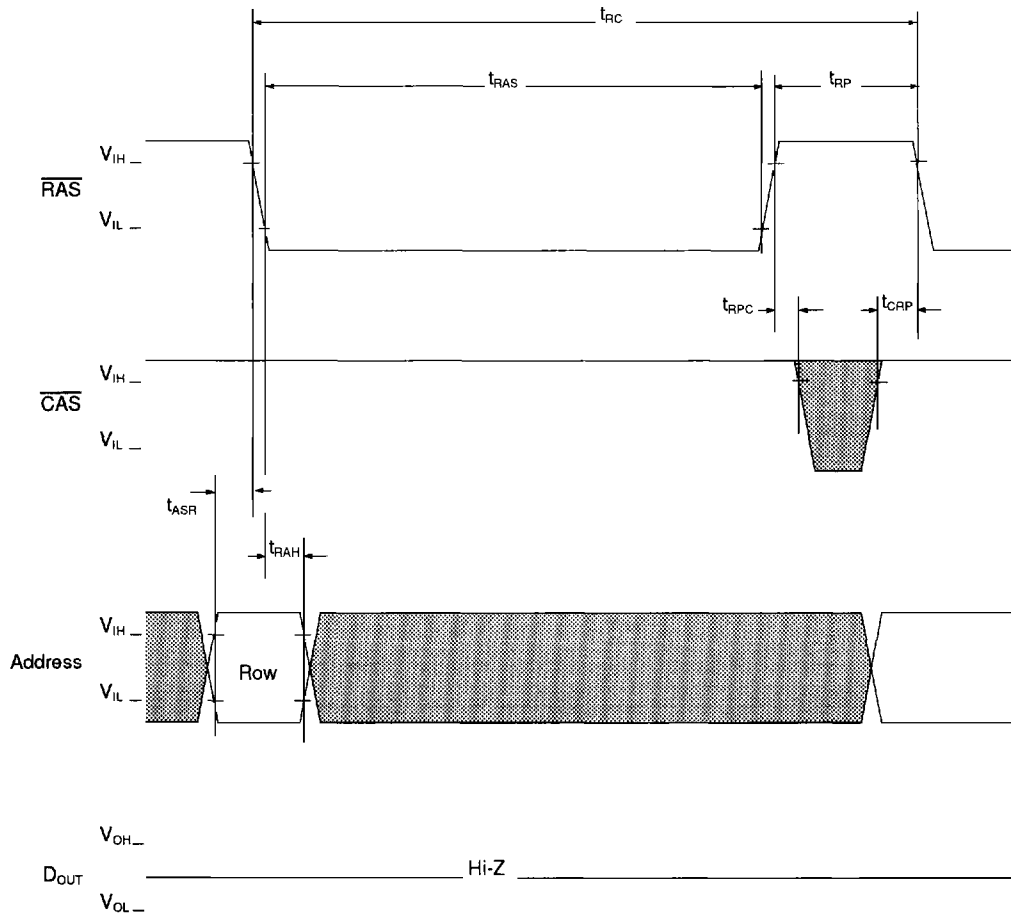
**Write Cycle (Early Write)**


### Fast Page Mode Read Cycle



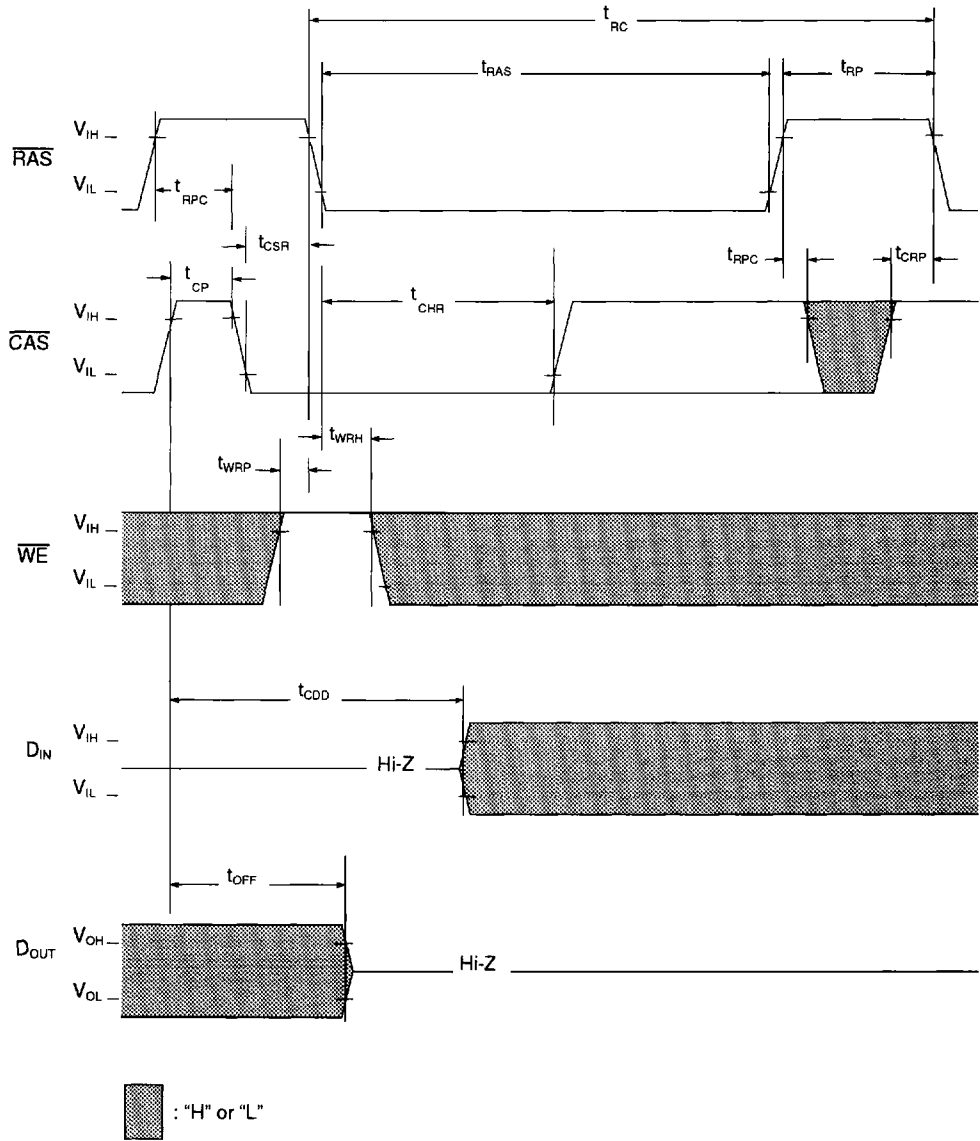
**Fast Page Mode Write Cycle**


**RAS Only Refresh Cycle**



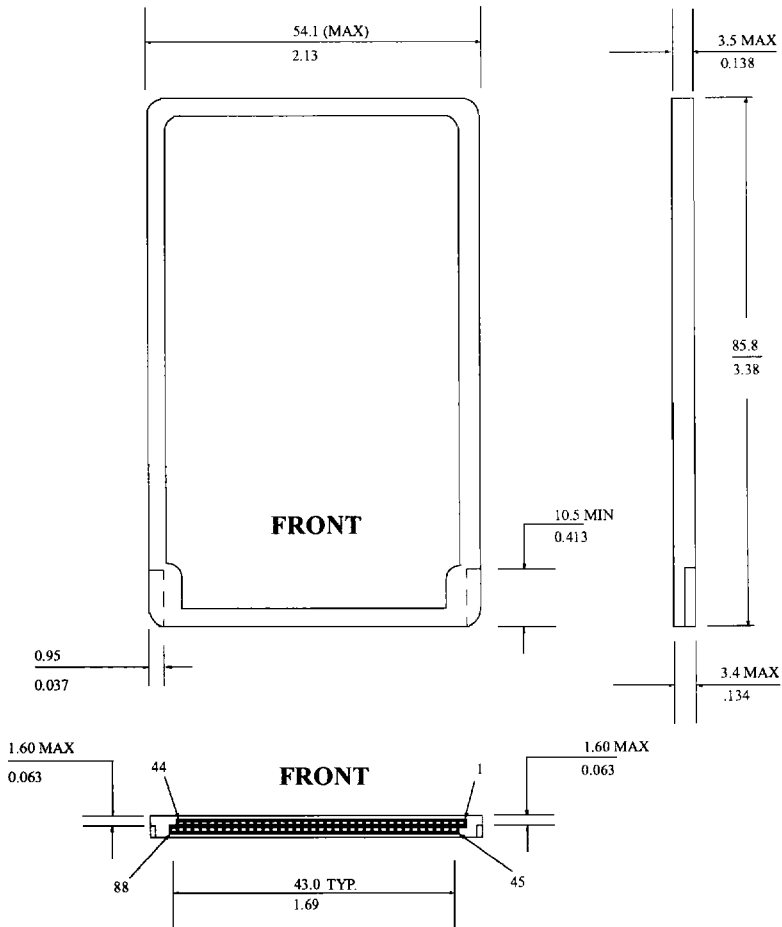
: "H" or "L"

Note:  $\overline{\text{WE}}$ ,  $\text{D}_{\text{IN}}$  are "H" or "L"

**CAS Before RAS Refresh Cycle**


Note: Addresses are "H" or "L"

### Layout Drawing



**NOTE:** All dimensions are typical unless otherwise stated.  $\frac{\text{MILLIMETERS}}{\text{INCHES}}$