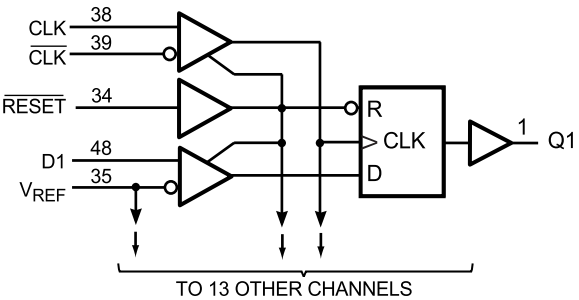
PI74SSTV16857D

14-Bit Registered Buffer

Product Features

- PI74 SSTV16857D is designed for low-voltage operation, $V_{DD} = V_{DDQ} = 2.3V$ to 2.7V
- Supports SSTL_2 Class I and II specifications
- SSTL_2 Input and Output Levels
- Data inputs have clamp diodes to V_{DD}
- Designed for DDR Memory
- Flow-Through Architecture
- Package available:
  - 48-pin 240 mil wide plastic TSSOP (A)
  - 48-pin 173 mil wide plastic TVSOP (K)

Logic Block Diagram



Product Pin Description

Pin Name	Description
$\overline{RESET}$	Reset (Active Low)
CLK	Clock Input
$\overline{CLK}$	Clock Input
D	Data Input
Q	Data Output
GND	Ground
V_{DD}	Core Supply Voltage
V_{DDQ}	Output Supply Voltage
V_{REF}	Input Reference Voltage

Truth Table(1)

Inputs				Outputs
$\overline{RESET}$	CLK	$\overline{CLK}$	D	Q
L	X	X	X	L
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q_0(2)

Notes:

1. H = High Signal Level
   L = Low Signal Level
   ↑ = Transition LOW-to-HIGH
   ↓ = Transition HIGH-to-LOW
   X = Irrelevant
2. Output level before the indicated steady state input conditions were established.

Product Description

Pericom Semiconductor's PI74SSTV16857 series of logic circuits are produced using the Company's advanced 0.35 micron CMOS technology, achieving industry leading speed.

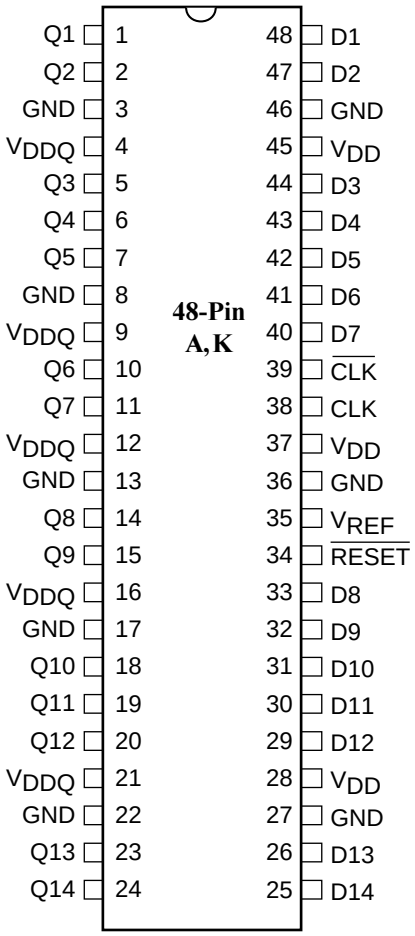
The 14-bit PI74SSTV16857D universal bus driver is designed for 2.3V to 2.7V V_{DD} operation and SSTL_2 I/O Levels except for the $\overline{Reset}$ input which is LVCMOS.

Data flow from D to Q is controlled by the differential clock , CLK, $\overline{CLK}$ and $\overline{Reset}$. Data is triggered on the positive edge of CLK. $\overline{CLK}$ must be used to maintain noise margins.

$\overline{Reset}$ must be supported with LVCMOS levels as V_{REF} may not be stable during power-up. $\overline{Reset}$ is asynchronous and is intended for power-up only and when low assures that all of the registers reset to the Low State, Q outputs are low, and all input receivers, data and clock, are switched off.

Pericom's PI74SSTV16857D is characterized for operation from 0° to 70°C.

Product Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Item	Symbol/Conditions	Ratings	Units
Storage temperature	T_{stg}	–65 to 150	°C
Supply voltage	V_{DD} or V_{DDQ}	–0.5 to 3.6	V
Input voltage[1]	V_I	–0.5 to V_{DD} +0.5	
Output voltage[1,2]	V_O	–0.5 to V_{DDQ} +0.5	
Input clamp current	I_{IK}, V_I<0	–50	mA
Output clamp current	I_{OK}, V_O<0	±50	
Continuous output current	I_O, V_O = 0 to V_{DDQ}	±50	
V_{DD}, V_{DDQ} or GND current/pin	I_{DD}, I_{DDQ} or I_{GND}	±100	
Package Thermal Impedance[3]	θJ_A	70	°C/W

Notes:

1. The input and output negative voltage ratings may be excluded if the input and output clamp ratings are observed.
2. This current will flow only when the output is in the high state level $V_O > V_{DDQ}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Parameters	Description		Min.	Nom.	Max.	Units
V_{DD}	Supply Voltage		2.3	2.5	2.7	V
V_{DDQ}	I/O Supply Voltage		2.3	2.5	2.7	
V_{REF}	Reference Voltage V_{REF} = 0.5X V_{DDQ}		1.15	1.25	1.35	
V_{TT}	Termination Voltage		V_{REF} –0.04	V_{REF}	V_{REF} +0.04	
V_{IH}	DC Input High Voltage	Data Inputs	V_{REF} +0.15		V_{DDQ} +0.3	
V_{IL}	DC Input Low Voltage		–0.3		V_{REF} –0.15	
V_{IH}	Input High Voltage	$\overline{\text{Reset}}$	1.7		V_{DDQ} +0.3	
V_{IL}	Input Low Voltage		–0.3		0.8	
V_{IN}	Input Voltage Level	CLK,$\overline{\text{CLK}}$	–0.3			
V_{ID}	Input Differential Voltage		0.36		V_{DDQ} +0.6	
V_{IX}	Cross Point Voltage of Differential Clock Pair		(V_{DDQ}/2) –0.2		(V_{DDQ}/2) +0.2	
I_{OH}	High-Level Output Current		–20			mA
I_{OL}	Low-Level Output Current		20			
T_A	Operating Free-Air Temperature		0		70	°C

DC Electrical Characteristics (Over the Operating Range (T_A = 0°C to +70°C, V_{DD} = 2.5V ±200mV, V_{DDQ} = 2.5V ±200mV)

Parameters		Test Conditions		V_{DD}	Min.	Typ.(4)	Max.	Units
V_{IK}		I_I = –18mA		2.3V			–1.2	V
V_{OH}		I_{OH} = –100µA		2.3V-2.7V	V_{DD} –0.2			
		I_{OH} = –16mA		2.3V	1.95			
V_{OL}		I_{OL} = 100µA		2.3V-2.7V			0.2	
		I_{OH} =16mA		2.3V			0.35	
I_I	All Inputs	$V_I = V_{DD}$ or GND		2.7V			5	µA
I_{DD}	Standby (Static)	$\overline{Reset}$ = GND	I_O = 0	2.7V			100	µA
	Operating (Static)	$V_I = V_{IH}$ ($\overline{AC}$) or V_{IL} (AC), $\overline{Reset} = V_{DD}$					TBD	mA
I_{DDD}	Dynamic operating - clock only	$\overline{RESET} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CK and $\overline{CK}$ switching 50% duty cycle .					TBD	µA/ clock MHz
	Dynamic Operating - per each data input	$\overline{RESET} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CK and $\overline{CK}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle					TBD	µA/ clock MHz/ data
C_i	Data Inputs	$V_I = V_{REF}$ ±350mV		2.5V	2.5		4.5	pF
	CK and $\overline{CK}$	V_{ICR} =1.25V, $V_{I(PP)}$ = 360mV			2.5		3.5	

Notes:
4. Typical values are at V_{DD} = Nominal V_{DD}, T_A = +25°C.

Timing Requirements over recommended operating free-air temperature range (unless otherwise noted).

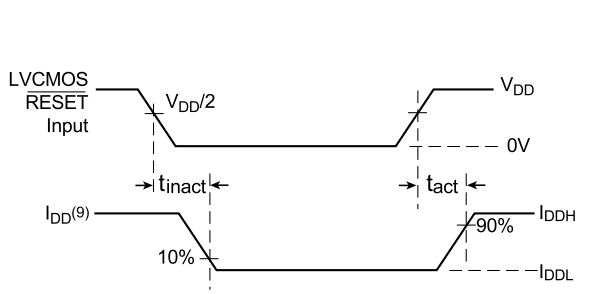
			V_{DD} = 2.5V ±0.2V		Units
			Min.	Max.	
f_{clock}	Clock frequency			170	MHz
t_{PD}	Clock to output time		TBD	TBD	ns
t_{RST}	Reset to output time			5	
t_{SL}	Output slew rate		1	4	V/ns
t_{su}	Setup time, fast slew rate(5,7)	Data before CK↑, $\overline{CK}$↓	0.75		ns
	Setup time, slow slew rate(6,7)		0.9		
t_h	Hold time, fast slew rate(5,7)	Data after CK↑, $\overline{CK}$↓	0.75		
	Hold time, slow slew rate(6,7)		0.9		

Notes: 5. For data signal input slew rate ≥1V/ns.
6. For data signal input slew rate ≥0.5V/ns and <1V/ns.
7. CLK, $\overline{CLK}$ signals input slew rates are ≥1V/ns.

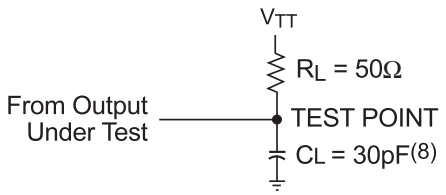
Switching characteristics over recommended operating free-air temperature range
(Unless otherwise noted. See test circuits and switching waveforms).

Parameter	From (Input)	To (Output)	V_{DD} = 2.5V ±0.2V			Units
			Min.	Typ.	Max.	
f_{max}			170			MHz
t_{pd}	CLK, $\overline{CLK}$	Q	1.1		2.8	ns
t_{phl}	$\overline{RESET}$	Q			5.0	

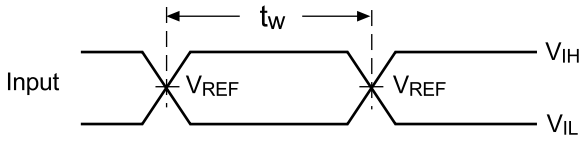
Test Circuit and Switching Waveforms



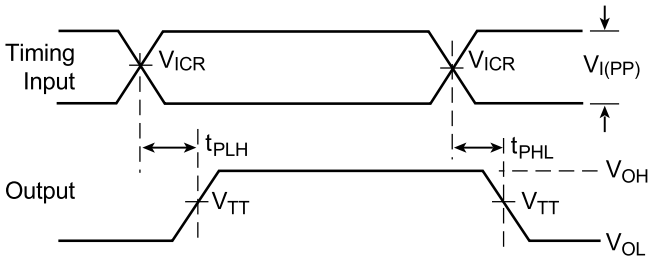
Voltage and Current Waveforms
Input Active and Inactive Times



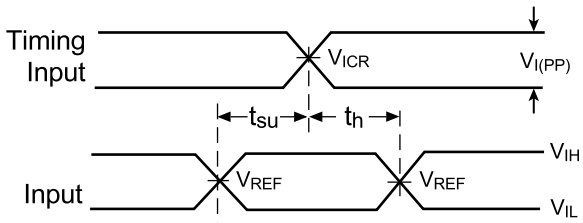
Load Circuit



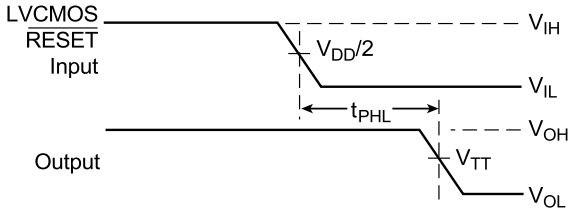
Voltage Waveforms - Pulse Duration



Voltage Waveforms - Propagation Delay Times



Voltage Waveforms - Setup and Hold Times



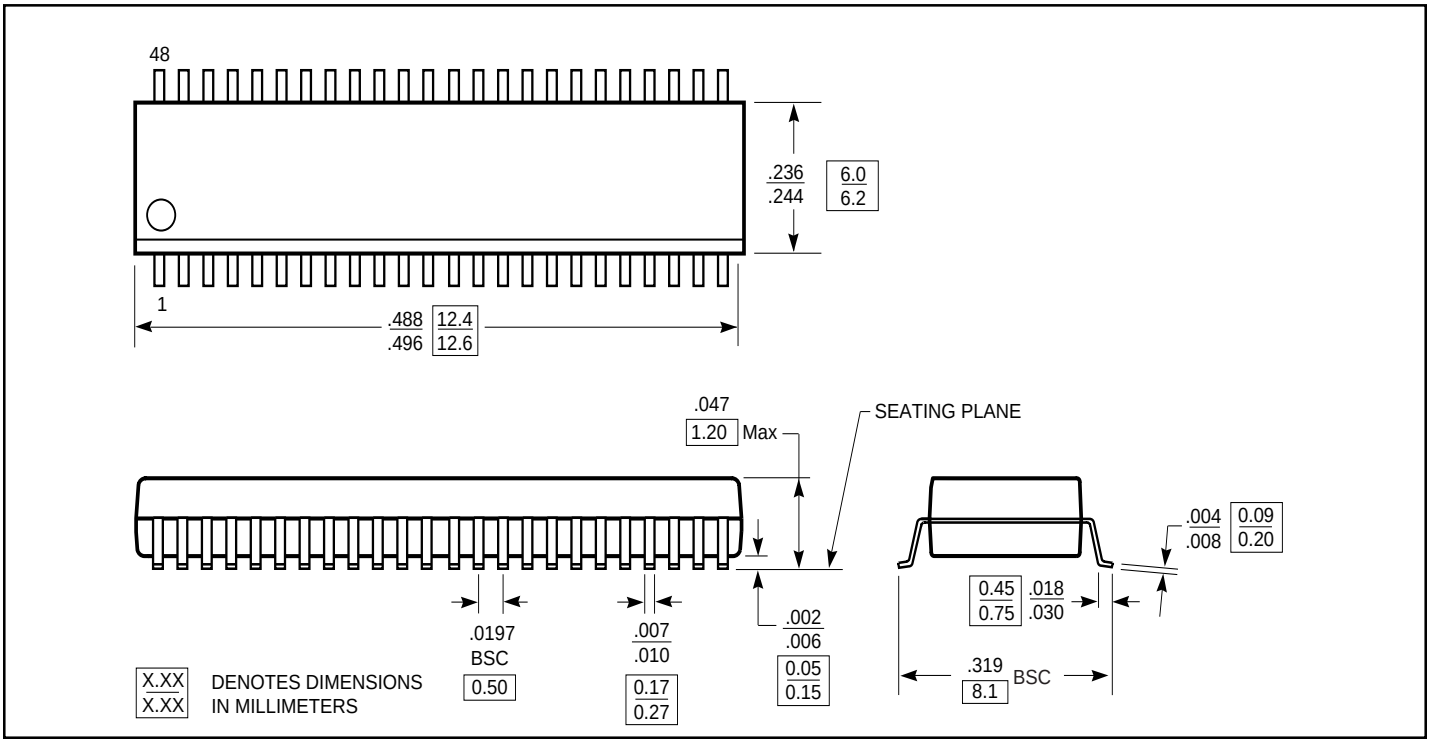
Voltage Waveforms - Propagation Delay Times

Parameter Measurement Information (V_{DD} = 2.5V ±0.2V)

Notes:

8. C_L includes probe and jig capacitance.
9. I_{DD} tested with clock and data inputs held at V_{DD} or GND, and I_O = 0mA.
10. All input pulses are supplied by generators having the following characteristics: PRR ≤10 MHz, Z_O = 50Ω. Input slew rate = 1V/ns ±20% (unless otherwise specified).
11. The outputs are measured one at a time with one transition per measurement.
12. $V_{TT} = V_{REF} = V_{DDQ}/2$
13. $V_{IH} = V_{REF}$ + 350mV (ac voltage levels) for SSTL inputs. $V_{IH} = V_{DD}$ for LVCMOS input.
14. $V_{IL} = V_{REF}$ + 350mV (ac voltage levels) for SSTL inputs. V_{IL} = GND for LVCMOS input.
15. t_{PLH} and t_{PHL} are the same as t_{pd}.

48-Pin TSSOP Package (A)



48-Pin TSSOP Package (K)