

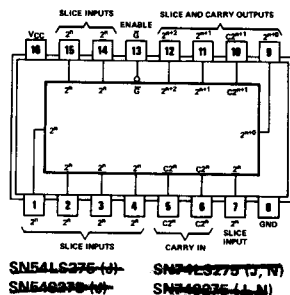
54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEW)

7-BIT SLICE WALLACE TREES

275 3-STATE OUTPUTS

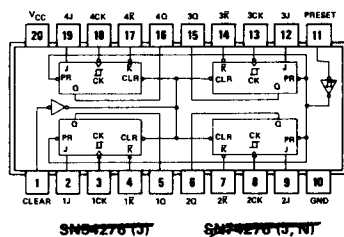
See page 7-391



QUAD J-K FLIP-FLOPS

276 SEPARATE CLOCKS
EDGE-TRIGGERING
COMMON DIRECT CLEAR AND PRESET

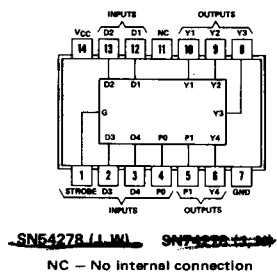
See page 7-401



4-BIT CASCADEABLE PRIORITY REGISTERS

278 LATCHED DATA INPUTS
PRIORITY OUTPUT GATING

See page 7-403



QUAD S-R LATCHES

279 DIODE-CLAMPED INPUTS
TOTEM-POLE OUTPUTS

FUNCTION TABLE

INPUTS		OUTPUT
\bar{S} [†]	\bar{R}	Q
H	H	Q ₀
L	H	H
H	L	L
L	L	H*

H = high level

L = low level

Q₀ = the level of Q before the indicated input conditions were established.

* This output level is pseudo stable; that is, it may not persist when the \bar{S} and \bar{R} inputs return to their inactive (high) level.

[†] For latches with double \bar{S} inputs:

H = both \bar{S} inputs high

L = one or both \bar{S} inputs low

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