8T24
TRIPLE LINE RECEIVER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 8T24 Triple Line Receiver is designed specifically to meet the IBM System/360 I/O Interface Specification (File No. S360-19). The logic and strobe inputs are fully TTL or DTL compatible. The R inputs are designed to withstand a positive dc input of +7 V with power on (V+ = 5 V) and +6 V with power off, V+ = 0 V) and a negative dc input of 0.15 V with power on or off. This protection allows normal bus operation even if one or more receivers have been powered down.

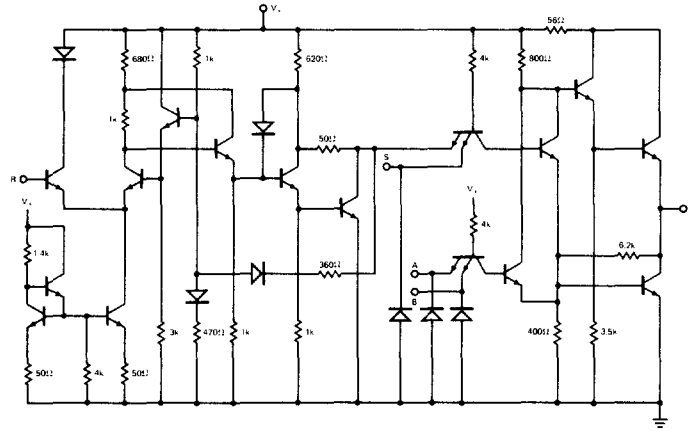
- **MEETS IBM SYSTEM/360 I/O INTERFACE SPECIFICATION**
- **BUILT-IN INPUT THRESHOLD HYSTERESIS**
- **HIGH SPEED**
- **INDEPENDENT CHANNEL STROBING**
- **FANOUT OF 10 TTL LOADS**
- **SINGLE +5V SUPPLY OPERATION**

ABSOLUTE MAXIMUM RATINGS

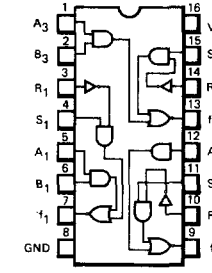
Input Voltage (Note 1)	+5.5V
Output Voltage (Note 1)	+7.0V
Supply Voltage (Note 1)	+7.0V
Storage Temperature Range	
Molded DIP (N8T24B)	−55°C to +125°C
Hermetic DIP (N8T24E)	−65°C to +150°C
Operating Temperature Range	0°C to +75°C
Lead Temperatures	
Hermetic DIP (soldering, 60 seconds)	300°C
Molded DIP (soldering, 10 seconds)	260°C
Internal Power Dissipation (Note 2)	730mW

NOTES:
1. Voltages are with respect to the ground pin (pin 8).
2. Rating applies to ambient temperatures up to 70°C. Above 70°C derate linearly at 8.3mW/°C.

EQUIVALENT CIRCUIT (EACH RECEIVER)



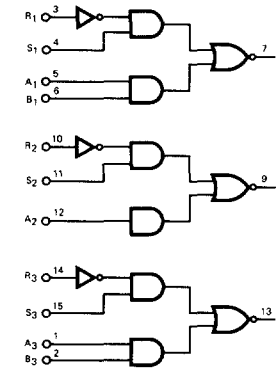
CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6B, 9B



ORDER INFORMATION

TYPE	PART NO.
N8T24	N8T24E
N8T24	N8T24B

LOGIC DIAGRAM



PIN 8 = GND
PIN 16 = V_+

ELECTRICAL CHARACTERISTICS (V_+ = 5.0 V ±5%, T_A = 0°C to +75°C)

PARAMETER		TEST CONDITIONS					NOTES	LIMITS			UNITS
		R	S	A	B	OUTPUTS		MIN.	TYP.	MAX.	
Output HIGH Voltage		1.70V	4.5V	0V	0V	–800μA	8	2.6	3.4		V
		0V	0.7V	0V	0V	–800μA	8	2.6	3.4		V
Output LOW Voltage		0.70V	1.7V	0V	0V	16mA	9		0.2	0.4	V
		0V	0V	1.7V	1.7V	16mA	9		0.2	0.4	V
Input LOW Current	S_n	0V	0.4V					–0.1		–1.6	mA
	A_n	0V		0.4V				–0.1		–1.6	mA
	B_n				0.4V			–0.1		–1.6	mA
Input HIGH Current	R_n	3.11V								0.17	mA
	R_n	7.0V								5.0	mA
	R_n	6.0V					10			5.0	mA
	S_n	3.11V	4.5V							40	μA
	A_n			4.5V	0V					40	μA
	B_n			0V	4.5V					40	μA

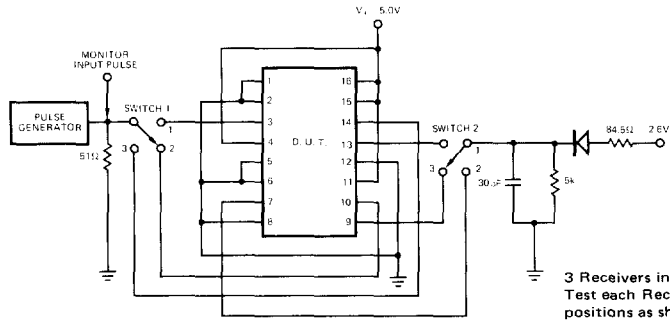
ELECTRICAL CHARACTERISTICS (V_+ = 5.0 V, T_A = 25°C)

PARAMETER		TEST CONDITIONS					NOTES	LIMITS			UNITS
		R	S	A	B	OUTPUTS		MIN.	TYP.	MAX.	
Turn-on Propagation Delay t_{PHH}		V_{IN}	5.0V	0V	0V		14		20	30	ns
Turn-off Propagation Delay t_{PLL}		V_{IN}	5.0V	0V	0V		14		20	30	ns
Hysteresis		V_{IN}	4.5V	0V	0V		12,13	0.2	0.4		V
Power/Consumption							15		315	380	mW
Supply Current							15		60	72	mA
Input Latch Voltage	S_n	3.11V	10mA	0V	0V		11	5.5			V
	A_n	0V	0V	10mA	0V		11	5.5			V
	B_n	0V	0V	0V	10mA		11	5.5			V
Output Short Circuit Current		3.11V	0V	0V	0V			–50		–100	mA
Input Clamp Diode Voltage	S_n		–12mA							–1.5	V
	A_n			–12mA						–1.5	V
	B_n				–12mA					–1.5	V

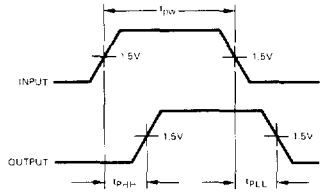
NOTES:

3. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
4. All measurements are taken with ground pin tied to zero volts.
5. Positive current is defined as into the terminal referenced.
6. Positive logic definition: "UP" Level = "HIGH", "DOWN" Level = "LOW".
7. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
8. Output source current is applied through a resistor to ground.
9. Output sink Current is supplied through a resistor to V_+.
10. V_+ = 0.00V
11. This test guarantees operation free of Input latch up over the specified operating supply voltage range.
12. Hysteresis is defined as the voltage difference between the R input level at which the output begins to go from "HIGH" to "LOW" state and the level at which the output begins to go from HIGH to LOW.
13. See Hysteresis test circuit.
14. Refer to AC test circuits.
15. V_+ = 5.25V.

AC TEST CIRCUIT AND WAVEFORMS



3 Receivers in the package. Test each Receiver using switch positions as shown in Table 1.



Input Pulse:
Amplitude = 2.6V
Pulse width = 200ns
(50% Duty Cycle)
$t_r = t_f = 5$ns (10% to 90%)

TABLE 1

Receiver no.	Position	
	Switch 1	Switch 2
Receiver 1	1	1
Receiver 2	2	2
Receiver 3	3	3

HYSTERESIS TEST CIRCUIT

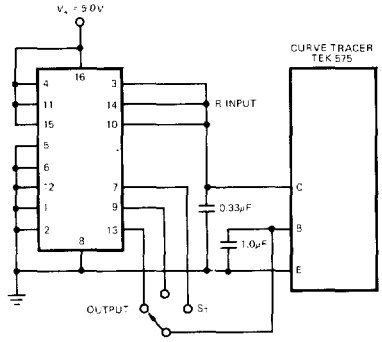
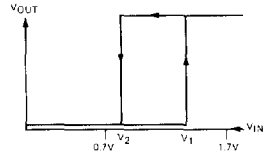


Fig. 1



Verify in each of three (3) positions of S_1 (Fig. 1) that the following occurs per Fig. 2.

1. V_1x and V_2 must be between 0.7V minimum and 1.7V maximum.
2. Hysteresis = $V_1 - V_2$

Fig. 2

TYPICAL APPLICATION