HARRIS

HS-3447

ADVANCE INFORMATION

Cypher 1™ CMOS Data Encryption Device

Features

- Endorsed by National Security Agency for Protecting Unclassified National Security Related Information (UNSR)
- Per DOD Drawing ON304455
- Alternative to WD 2001/2002 and MC6859 NMOS Devices
- Uses single 5V Power Supply
- Operating Range -55°C to +125°C
- Lower Power Operation 250mW at 10MHz
- Maximum Transfer Rate:
  - 20MHz at 7 Volts
  - 10MHz at 5 Volts
  - 20MHz at 5 Volts (-55°C to +85°C)
- Encrypts/Decrypts via Serial Data Stream
- Available to Class B and Class S Equivalent Screening
- Inputs TTL Compatible
- Key Variable Stored On-Chip is Not Externally Accessible
- Available in Special Configurations

Applications

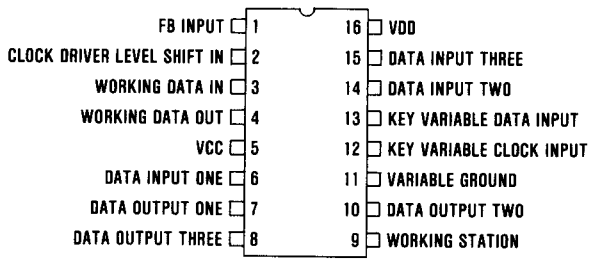
- Commercial Communications Systems
- Satellite Communications Systems
- Mainframe Communications
- Packet Switching Transmission
- Remote and Host Computer Communications
- Brokerage Transactions
- Disk or Mag Tape Data Storage
- Electronic Funds Transfers
- Banking/Business Accounting
- Spread Spectrum and Frequency Hopping Applications

Description

The HS-3447 Data Encryption/Decryption device is designed to encrypt and decrypt a serial data stream using a National Security Agency algorithm. The device encrypts a plain text message using a specified variable to produce a cipher text data out. When reversed the cipher text data is decrypted to produce the original plain text data. Integration of this device into an equipment/system does not in itself guarantee endorsement of the equipment/system by the NSA under the Commercial COMSEC Endorsement Program (CCEP).

Pinout

TOP VIEW



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I. C. handling procedures should be followed.

Cypher I™ is a trademark of Harris Corporation

Absolute Maximum Ratings

Voltage, Pin 16 (VDD), with respect to Pin 9 (VSS W) and Pin 11 (VSS V) ..... +12.0V
Voltage, any pin, with respect to Pin 16 VDD ..... +0.5V
Voltage, any pin except Pins 13 (VAR IN), 12 (VAR CLK) and 11 (VSS V) with respect to Pin 9 (VSS W) ..... −0.5V
Voltage, Pins 13 (VAR IN) and 12 (VAR CLK) with respect to Pin 11, variable ground ..... −0.5V

Storage Temperature ..... −65°C to +150°C
Case Operating Temperature ..... −55°C to +125°C
Maximum source or sink current, all outputs 30mA
Maximum source or sink current, all inputs 10mA
V_{CC} voltage should never exceed V_{DD} Including power up/down

The maximum values listed in this paragraph represent limiting values above which devices may be damaged or parameter values permanently altered. The voltage values above are not intended to be used as operational parameters.

OPERATING RANGE

Operating Voltage:
V_{DD} 4.6V to 7.8V
V_{CC} 4.6V to 5.4V
Operating Case Temperature ..... −55°C to +125°C

Working Register

		VCC = VDD = 4.6 to 5.4V Tc = −55 to +125°C		VCC = 4.6 to 5.4V VDD = 6.9 to 7.8V Tc = −55 to +125°C		VCC = VDD = 5.7 to 6.0V Tc = −55 to +125°C	
SYMBOL	**DEFINITION**	**MIN.**	**MAX.**	**MIN.**	**MAX.**	**MIN.**	**MAX.**
INPUTS (DATA)							
ts	Input Set-up Time (pins 6, 1, 15 & 14)	15ns	—	10ns	—	10ns	—
	(pin 3)	45ns		35ns		10ns	
th	Input Hold Time (pins 6, 1, 15 & 14)	15ns	—	15ns	—	15ns	—
	(pin 3)	0		0		0	
tr, tf	Input Rise/Fall Time	—	35ns	—	20ns	—	25ns
VIH	"1" Input Voltage Level	VDD − 0.4V	VDD + 0.4V	VDD − 0.4V	VDD + 0.4V	VDD − 0.4V	VDD + 0.4V
VIL	"0" Input Voltage Level	GND − 0.4V	GND + 0.4V	GND − 0.4V	GND + 0.4V	GND − 0.4V	GND + 0.4V
OUTPUTS							
tr, tf*	Output Rise/Fall Time	—	35ns	—	20ns	—	30ns
tpd*	Output Propagation Delay	6ns	65ns	6ns	45ns	6ns	55ns
VOH	"1" Output Voltage Level	VDD − 0.2V	VDD + 0.2V	VDD − 0.2V	VDD + 0.2V	VDD − 0.2V	VDD + 0.2V
VOL	"0" Output Voltage Level	GND − 0.2V	GND + 0.2V	GND − 0.2V	GND + 0.2V	GND − 0.2V	GND + 0.2V
CLOCK & DATA PATH							
f = 1/T	Clock Repetition Rate (pin 2)	0	11MHz	0	20MHz	0	11MHz
pw	Pulse Width	36ns	500ns or T − 36ns**	20ns	500ns or T − 20ns†	36ns	500ns or T − 36ns**
tri, tfi	Input Rise/Fall Time (pins 3 & 2)	—	20ns	—	10ns	—	20ns
tr, tf	Output Rise/Fall Time (pin 4)	—	20ns	—	10ns	—	20ns
VIH	Input "1" Level Tc = −55°C	VCC − 1.8	VCC + 0.4V	VCC − 1.8	VCC + 0.4V	VCC − 1.8	VCC + 0.4V
pin 3 & 2	Input "1" Level Tc = +125°C	VCC − 1.6	VCC + 0.4V	VCC − 1.6	VCC + 0.4V	VCC − 1.6	VCC + 1.4V
	Input "1" Level (CMOS input)	—	—	VDD − 0.4	VDD + 0.4V	—	—
VIL	Input "0" Level	GND − 0.4V	GND + 0.4V	GND − 0.4V	GND + 0.4V	GND − 0.4V	GND + 0.4V
tpd	Output Propagation Delay (pin 3 to 4)	4ns	30ns	4ns	25ns	4ns	30ns
f = 1/T	WDI Repetition Rate (pin 3)	0	11MHz	0	11MHz	0	11MHz

* Pins 7, 10, and 8 loaded with 35pf, pin 4 loaded w/15pf.
** At frequencies which have a period less than 536ns, T-36ns is the maximum pulse width.
†At frequencies which have a period less than 520ns, T-20ns is the maximum pulse width.

Variable Register

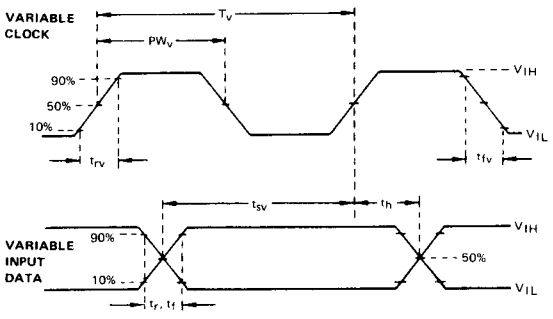


Figure 1 – Variable Register Inputs

Variable Register Inputs

		VCC = 4.6 to 7.8V Tc = −55 to +125°C	
SYMBOL	**DEFINITION**	**MIN.**	**MAX.**
tsv	Variable Set-up Time	50ns	—
tr, tf	Variable Input Rise/Fall Time	—	1us
VIH	"1" Voltage Level	VDD − 0.4V	VDD + 0.4V
VIL	"0" Voltage Level	GND − 0 4V	GND + 0.4V
f = 1/Tv	Variable Clock Repetition Rate	1 KHz	5 MHz
trv, tfv	Variable Clock Rise/Fall Time	—	2us
PWv	Variable Clock Pulse Width	80ns	Tv − 80ns
th	Variable Input Hold Time	50ns	—
	Variable Hold Voltage	1.5V	—

Timing Waveforms

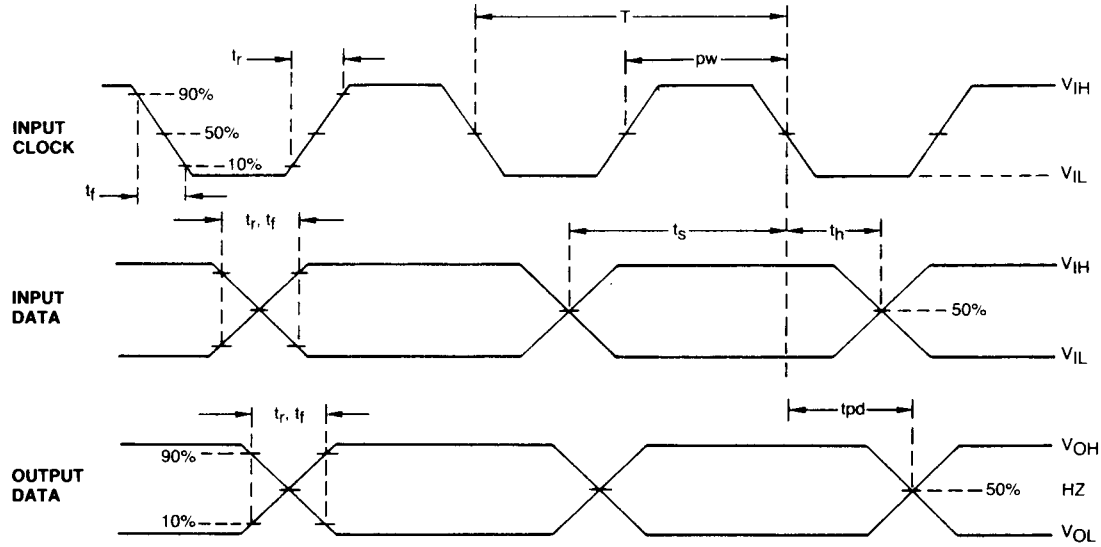


Figure 2–Working Register Input/Output Signals

Power Dissipation

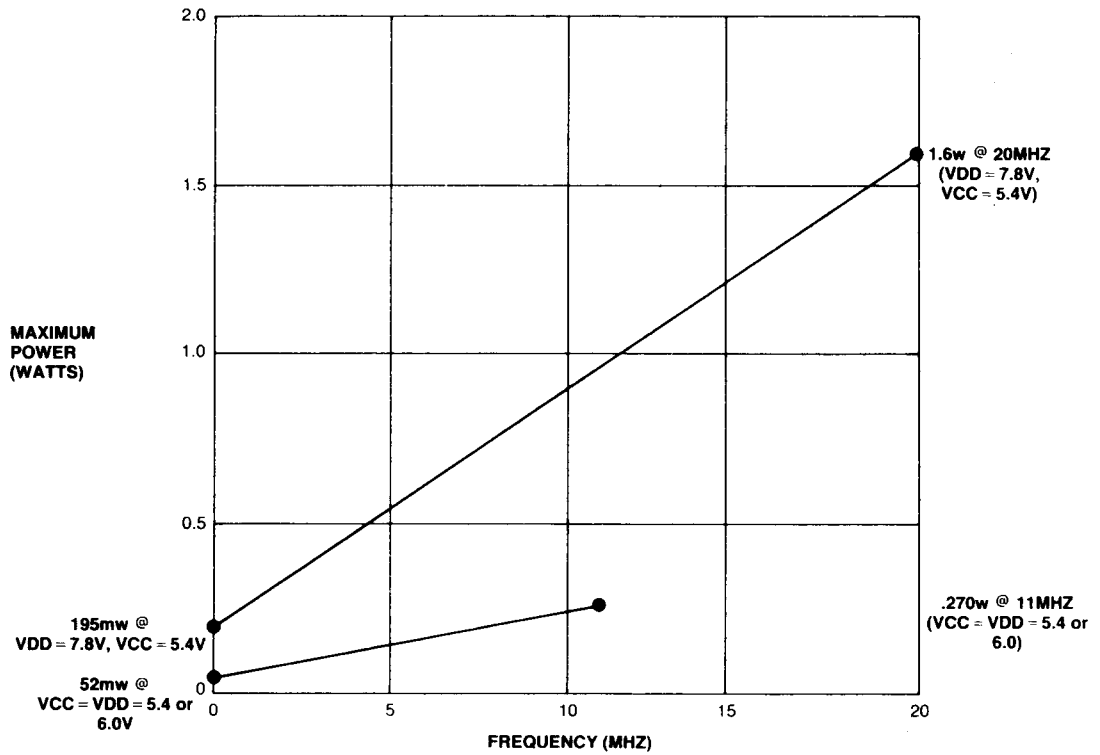


Figure 3–Maximum Power Consumption