

74AC/ACT11374

Octal D-Type Flip-Flop; Positive-Edge Trigger; 3-State

Product Specification

ACL Products

FEATURES

- 3-State output buffers
- Common 3-State Output Enable
- Independent register and 3-State buffer operation
- Output capability: ± 24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50 Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11374 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11374 device is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Clock (CP) and Output Enable (\overline{OE}) control gates. The register is fully edge-triggered. Once the set-up requirements are met, when the Clock Pulse (CP) rises the state of each D input is transferred to the corresponding flip-flop's Q output.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS $T_A = 25^\circ\text{C}; \text{GND} = 0\text{V};$ $V_{CC} = 5.0\text{V}$	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay CP to Q_n	$C_L = 50\text{pF}$	6.0	8.5	ns
C_{PD}	Power dissipation capacitance per flip-flop ¹	$f = 1\text{MHz};$ $C_L = 50\text{pF}$	Enabled 75	107	pF
			Disabled 66	96	
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	4.0	4.0	pF
C_{OUT}	Output capacitance	$V_I = 0\text{V}$ or V_{CC} ; Disabled	10	10	pF
I_{LATCH}	Latch-up current	Per Jeduc JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	$C_L = 50\text{pF}; V_{CC} = 5.5\text{V}$	110	70	MHz

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_I + \sum (C_L \times V_{CC}^2 \times f_O) \text{ where:}$$

f_I = input frequency in MHz, C_L = output load capacitance in pF,

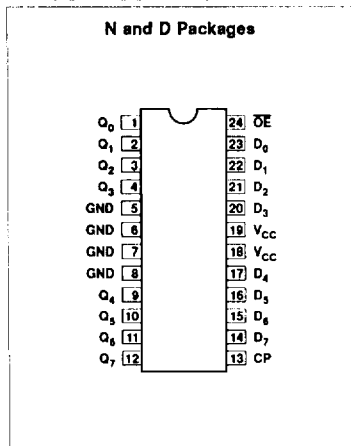
f_O = output frequency in MHz, V_{CC} = supply voltage in V,

$\sum (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

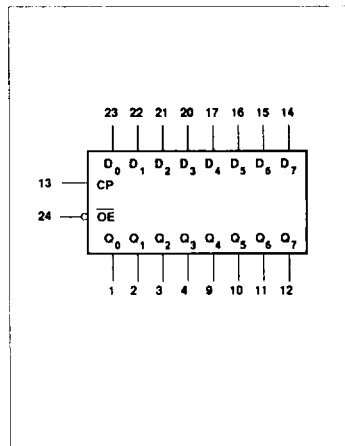
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11374N 74ACT11374N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11374D 74ACT11374D

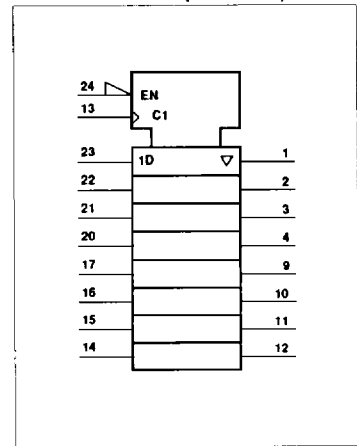
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable (\overline{OE}) controls all eight 3-State buffers independent of the clock operation.

When \overline{OE} is Low, the stored data appears at the outputs. When \overline{OE} is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	\overline{OE}	Output enable
23, 22, 21, 20, 17, 16, 15, 14	$D_0 - D_7$	Data inputs
1, 2, 3, 4, 9, 10, 11, 12	$Q_0 - Q_7$	Data outputs
13	CP	Clock input
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	\overline{OE}	CP	D_n		Q_n
Load and read register	L	\uparrow	l	L	L
	L	\uparrow	h	H	H
Disable outputs	H	X	X	X	Z

H = High voltage level steady state

h = High voltage level one set-up time prior to the Low-to-High clock transition

L = Low voltage level steady state

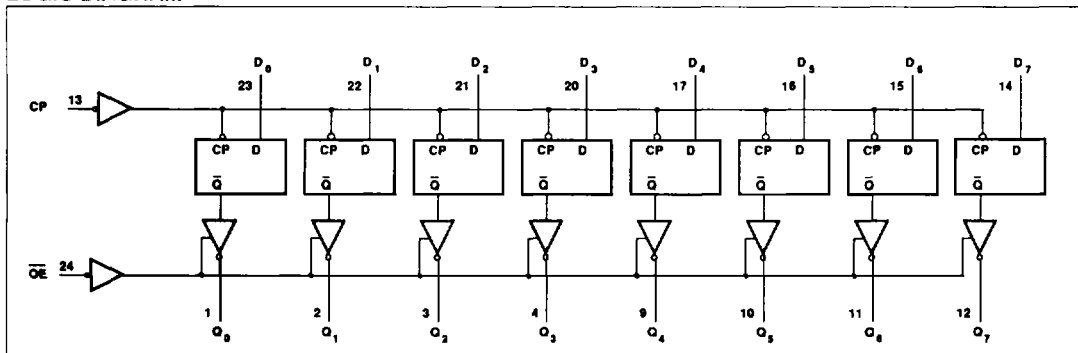
l = Low voltage level one set-up time prior to the Low-to-High clock transition

X = Don't care

Z = High-impedance "OFF" state

\uparrow = Low-to-High transition

LOGIC DIAGRAM



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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11374			74ACT11374			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0 ¹	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta V/\Delta V$	Input transition rise or fall rate	Data	0	10	0		10	ns/V
		Output enable	0	5	0		10	
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

- No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK} or V_I	DC input diode current ²	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to $V_{CC} + 0.5$	V
I_{OK} or V_O	DC output diode current ²	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to $V_{CC} + 0.5$	V
I_O	DC output source or sink current per output pin	$V_O = 0$ to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C: derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C: derate linearly by 6mW/K	400	mW

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	V _{CC} V	74AC11374				74ACT11374				UNIT	
				T _A = +25°C		T _A = -40°C (to +85°C)		T _A = +25°C		T _A = -40°C (to +85°C)			
				Min	Max	Min	Max	Min	Max	Min	Max		
V _{IH}	High-level input voltage		3.0	2.10		2.10						V	
			4.5	3.15		3.15		2.0		2.0			
			5.5	3.85		3.85		2.0		2.0			
V _{IL}	Low-level input voltage		3.0		0.90		0.90					V	
			4.5		1.35		1.35		0.8		0.8		
			5.5		1.65		1.65		0.8		0.8		
V _{OH}	High-level output voltage	V _I = V _{IL} or V _{IH}	I _{OH} = -50μA	3.0	2.9		2.9					V	
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I _{OH} = -4mA	3.0	2.58		2.48						
				4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
V _{OL}	Low-level output voltage	V _I = V _{IL} or V _{IH}	I _{OL} = 50μA	3.0		0.1		0.1				V	
				4.5		0.1		0.1		0.1			0.1
				5.5		0.1		0.1		0.1			0.1
			I _{OL} = 12mA	3.0		0.36		0.44					
				4.5		0.36		0.44		0.36			0.44
				5.5		0.36		0.44		0.36			0.44
I _{OL} = 75mA ¹	3.0				1.65				1.65				
	5.5				1.65				1.65				
I _I	Input leakage current	V _I = V _{CC} or GND	5.5		±0.1		±1.0		±0.1		±1.0	μA	
I _{OZ}	3-State output off-state current	V _I = V _I or V _{IH} ; V _O = V _{CC} or GND	5.5		±0.5		±5.0		±0.5		±5.0	μA	
I _{CC}	Quiescent supply current	V _I = V _{CC} or GND, I _O = 0	5.5		8.0		80		8.0		80	μA	
ΔI _{CC}	Supply current, TTL inputs High ²	One input at 3.4V, other inputs at V _{CC} or GND	5.5						0.9		1.0	mA	

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

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AC ELECTRICAL CHARACTERISTICS AT 3.3V \pm 0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11374					UNIT
			T _A = +25°C			T _A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f _{MAX}	Maximum clock frequency	1	75	90		75		MHz
t _{PLH} t _{PHL}	Propagation delay CP to Q _n	1	1.5 1.5	9.5 9.0	12.5 12.6	1.5 1.5	14.2 14.0	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	2	1.5 1.5	8.0 8.0	10.9 11.1	1.5 1.5	12.3 12.3	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	2	1.5 1.5	10.0 8.0	12.1 10.7	1.5 1.5	12.5 11.6	ns
t _W	Clock pulse width High or Low	1	6.5			6.5		ns
t _S	Setup time D _n to CP	3	2.5			2.5		ns
t _H	Hold time D _n to CP	3	4.5			4.5		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V \pm 0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11374					UNIT
			T _A = +25°C			T _A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f _{MAX}	Maximum clock frequency	1	95	110		95		MHz
t _{PLH} t _{PHL}	Propagation delay CP to Q _n	1	1.5 1.5	6.5 5.5	9.0 9.1	1.5 1.5	10.2 10.1	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	2	1.5 1.5	5.5 5.5	8.0 8.4	1.5 1.5	9.1 9.4	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	2	1.5 1.5	9.0 6.0	11.0 8.6	1.5 1.5	11.2 9.2	ns
t _W	Clock pulse width High or Low	1	5.0			5.0		ns
t _S	Setup time D _n to CP	3	2.5			2.5		ns
t _H	Hold time D _n to CP	3	3.5			3.5		ns

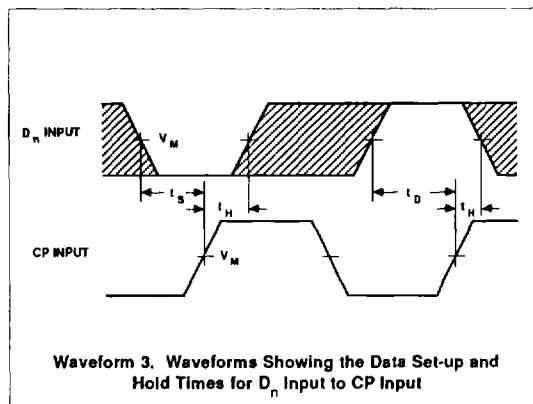
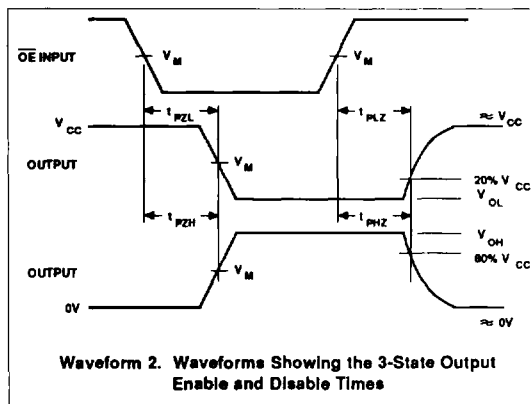
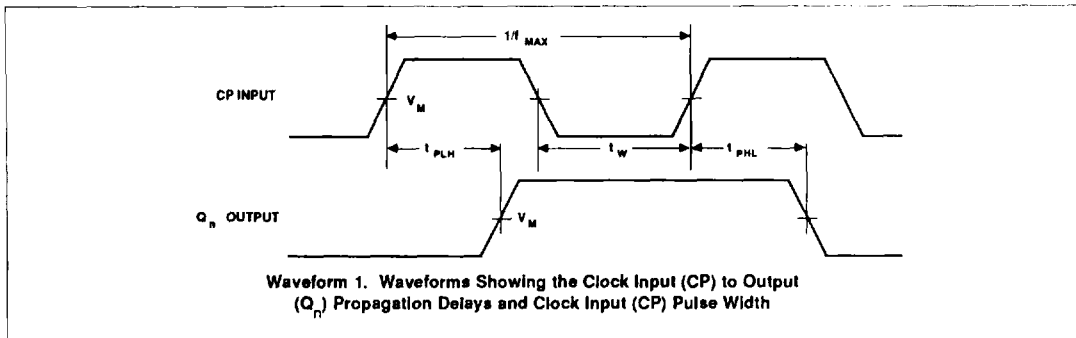
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AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11374					UNIT
			T _A = +25°C			T _A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t _{MAX}	Maximum clock frequency	1	55	70		55		MHz
t _{PLH} t _{PHL}	Propagation delay CP to Q _n	1	1.5 1.5	8.5 8.5	10.7 11.3	1.5 1.5	12.4 13.0	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	2	1.5 1.5	7.5 7.5	11.0 11.0	1.5 1.5	12.3 12.3	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	2	1.5 1.5	11.0 8.0	12.7 10.0	1.5 1.5	13.2 10.8	ns
t _W	Clock pulse width High or Low	1	9.0			9.0		ns
t _S	Setup time D _n to CP	3	3.0			3.0		ns
t _H	Hold time D _n to CP	3	5.5			5.5		ns

AC WAVEFORMS



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WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	$V_{IN} = \text{GND to } V_{CC}$ $V_M = 50\% V_{CC}$	$V_{OUT} = V_{OL} \text{ to } V_{OH}$ $V_M = 50\% V_{CC}$
ACT	$V_{IN} = \text{GND to } 3.0V$ $V_M = 1.5V$	

TEST CIRCUIT

