

FEATURES

Microcontroller Interface

- Supports high-speed microcontroller interfaces (e.g., 16 MHz 80188, 12 MHz 68HC11, 30 MHz HPC460X3)
- Supports direct microcontroller access to the SCSI Bus, buffer memory, and external switches
- Supports separate host and disk interrupt structures for flexible interrupt or polled firmware design

SCSI Interface

- Supports SCSI-2 Initiator and Target modes
- Supports asynchronous DMA/PIO transfers up to 3 Mbytes/second
- Supports synchronous DMA/PIO transfers up to 5 Mbytes/second
- Supports up to 15-byte synchronous transfer offsets and 12 programmable transfer periods
- Controls synchronous transfer overrun/underrun
- Transfers SCSI information to/from the microcontroller through a 16-byte FIFO under Automatic Programmed I/O (PIO)
- Controls arbitration, selection, and reselection in hardware
- Detects selected and reselected conditions automatically

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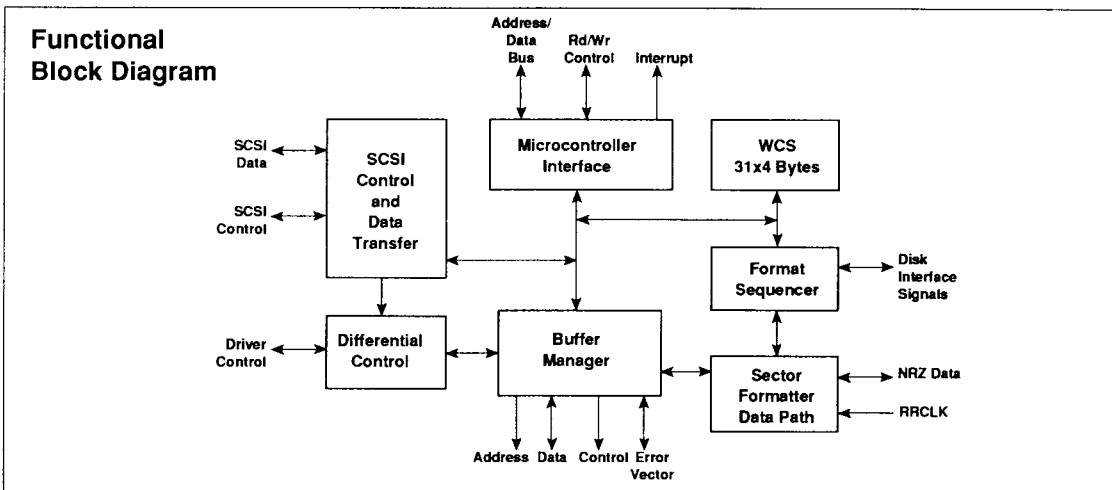
**SCSI Optical
Disk Controller**

OVERVIEW

The CL-SM331 is a VLSI component designed to work with the CL-SM330 ECC/ENDEC to provide the majority of the hardware necessary to build a Small Computer System Interface (SCSI) Optical disk controller. The CL-SM331 design combines: a high-speed local microcontroller port, extensive hardware support for the SCSI interface, a two-channel Buffer Manager, and an advanced Sector Formatter. With the addition of only a few discrete components for the device-level interface, the CL-SM331 and the CL-SM330 along with a local microcontroller, system ROM and RAM, and an optional data separator completes an optical disk controller subsystem with high performance at a low overall cost.

A local microcontroller provides the CL-SM331 with initial operating parameters that include disk sector format, the type and size of buffer memory, and SCSI Host Control. During data transfer

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FEATURES (cont.)

- Integrates 48 mA SCSI Bus drivers in the interface
- Provides control for the external differential driver option

Sector Formatter

- Supports up to 24 MHz NRZ data rates
- Programmable Format Sequencer Writable Control Store (WCS-31 x 4 bytes)
- Offers advanced branch commands that automate retry algorithms

Buffer Manager

- Dual channel circular buffer control with priority resolution
- Direct buffer addressing up to 256K bytes of SRAM and 4 Mbytes of DRAM

- Permits concurrent buffer memory throughput up to 10 Mbytes/second in DRAM page mode and 12 Mbytes/second for SRAM
- Odd parity data verification between the SCSI Bus and the Sector Formatter
- Automatically accepts and processes ECC correction vectors from companion optical ENDEC/ECC (CL-SM330) Integrated Circuit

Technology

- 100-pin Quad Flat Pack (QFP) package
- Pinout organized for optimum board layout efficiency
- Advanced, low-power double metal CMOS technology

OVERVIEW (cont.)

operations, the CL-SM331 requires only minimal intervention from the local microcontroller. The microcontroller to CL-SM331 communication path is a multiplexed address and data bus similar to that provided by the Intel® 80188 and the Motorola® 68HC11 class of controllers. There is a configuration signal available to allow for either family of data control signal methods. The CL-SM331 has centralized status registers with interrupt capability. These features allow firmware designers flexibility in writing polled loops or interrupt handlers that provide real-time process control critical in embedded controller drive applications.

The SCSI Host Interface is designed for compliance with the proposed SCSI-2 specification. This ensures long-term compatibility for both the hardware and the firmware developed around the CL-SM331. The SCSI Interface logic includes integrated high current (48 mA) drivers for the single-ended option as well as signals for control of the external logic necessary to implement the differential transceiver option. Both the asynchronous and synchronous transfer protocols are supported in either Initiator or Target mode. Routine bus control operations such as arbitration, selection, and reselection are

automatically sequenced in hardware. This method of implementing the SCSI Interface makes the SCSI protocol firmware extremely flexible and very efficient.

The Sector Formatter provides the disk data and control functions. The Sector Formatter is capable of handling NRZ data rates up to 24 Mbits/second. The Sector Formatter is subdivided into a Format Sequencer and the Sector Formatter Data path. The Format Sequencer uses a 31-word-by-4-byte Writable Control Store (WCS) to hold a user-written program. This program contains the control information for the disk track and sector format. The Sector Formatter Data path consists of the NRZ data handling circuitry that includes the serializer/deserializer (SERDES), the SERDES parity logic, and the data signals to the Buffer Manager Interface.

The Buffer Manager controls the flow of data between the host and disk interfaces. These interfaces store and retrieve data from the buffer memory using interleaved access cycles. The actual buffer memory may be implemented with static or dynamic RAM devices. The CL-SM331 Buffer Manager is programmable to provide all of the necessary address and control signals for RAM devices of varying

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OVERVIEW (cont.)

access times. Up to 256K bytes of SRAM can be directly addressed by the CL-SM331. As much as 4 Mbytes of DRAM is directly supported by the CL-SM331 with specific control for 64K, 256K, 1Mbit and 4 Mbit devices. In DRAM mode, refresh is generated automatically through a third channel to

the buffer memory in addition to the concurrent disk and host accesses. The CL-SM331 Buffer Manager will accept hardware ECC correction vectors from the CL-SM330 optical ENDEC/ECC Integrated Circuit and automatically correct errors in the buffer RAM within one sector time.

ADVANTAGES

Unique Features:

- *Programmable wait states for microcontroller*
- *Pin-configurable microcontroller data control interface*
- *Separate disk and host microcontroller interrupts*
- *15-byte offset in synchronous mode*
- *16-byte FIFO for automatic PIO transfers*
- *External differential SCSI Bus support*
- *Two Buffer Manager DMA channels*
- *Direct 256K SRAM and 4 Mbytes DRAM addressing*
- *Odd-through-parity buffer verification*
- *64K buffer segmentation logic*
- *Programmable read synchronization time-out*
- *Full hardware support for processing ECC correction vectors supplied by companion CL-SM330*

Benefits:

- *Allows the fastest microcontrollers to operate without degrading bus performance*
- *Allows for direct connect to Intel-or Motorola-style microcontrollers*
- *Supports faster, more direct interrupt processing by microcontroller*
- *Greater flexibility for synchronous data transfer negotiations*
- *Decreases command and information transfer overhead*
- *Allows connection to any SCSI system with longer cable lengths*
- *Enables read-look-ahead for high performance*
- *Increases buffer size alternatives to support caching*
- *Improves data integrity between host and disk data transfers*
- *Allows protected data segments in buffer*
- *Provides real-time processing of synchronization windows*
- *Automatic error correction within one sector time without microcontroller intervention*

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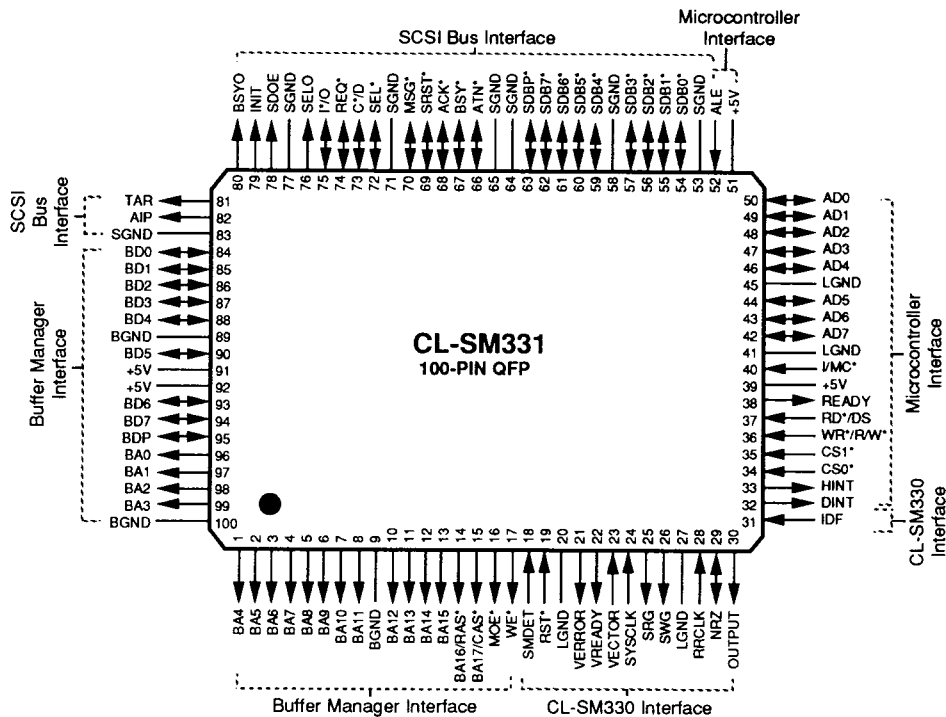
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1. PIN INFORMATION

The CL-SM331 is available in a 100-pin Quad Flat Pack (QFP) package. The diagram below shows the pinout of this package. All unused inputs must be tied to the inactive state to VCC or GND, respectively.

1.1 Pin Diagram for the 100-Pin Quad Flat Pack (QFP) Package



2. PIN ASSIGNMENTS

The following conventions are used in the pin assignment tables. An asterisk (*) denotes a negative true signal. An (I) indicates an input pin. An (O) indicates an output pin. An input/output pin is indicated by (I/O). A (Z) indicates a tri-state output. Open drain output pins are indicated by (OD). All unused inputs must be tied to the inactive state to VCC or GND, respectively.

2.1 Microcontroller Interface Pins

SYMBOL	QFP PIN NUMBER	TYPE	DESCRIPTION
DINT	32	O,OD,Z	DISK INTERRUPT: This signal is a disk interrupt line to the microcontroller, and is programmable for either a push-pull or open-drain output circuit. This signal powers up in the high-impedance state.
CS0*	34	I	CHIP SELECT 0, 1: Either chip select signal 0 or 1 must be asserted low for the microcontroller accesses to the CL-SM331 registers and to the Writable Control Store (WCS). Unused chip select pin must be tied to high.
CS1*	35	I	
WR*/R/W*	36	I	<p>WRITE STROBE/READ/WRITE: When the Intel Bus Control Interface is selected (the I/MC* Signal (Pin 40) is asserted high), this signal acts as the WR* Signal. When the Write Strobe Signal is asserted low and the CS* Signal (Pin 34 or 35) is asserted low, the data on the A/D lines will be written to the specified register.</p> <p>When the Motorola Bus Control Interface is selected (the I/MC* Signal (Pin 40) is deasserted low), this signal acts as the R/W* Signal. A high on this input along with the RD*/DS Signal (Pin 37) asserted and the CS* Signal (Pin 34 or 35) asserted low indicates a read operation. A low on this input along with the RD*/DS Signal (Pin 37) asserted and the CS* Signal (Pin 34 or 35) asserted low indicates a write operation.</p>

2.1 Microcontroller Interface Pins (cont.)

SYMBOL	QFP PIN NUMBER	TYPE	DESCRIPTION
RD*/DS	37	I	<p>READ STROBE/DATA STROBE: When the Intel Bus Control Interface is selected (the I/MC* Signal (Pin 40) is asserted high), this signal acts as the RD* Signal. When the Read Strobe Signal is asserted low and the CS* Signal (Pin 34 or 35) is asserted high, the data from the specified register will be driven onto the A/D lines.</p> <p>When the Motorola Bus Control Interface is selected (the I/MC* Signal (Pin 40) is deasserted low), this signal acts as the DS Signal. A high on the R/W* Signal along with this signal asserted and the CS* Signal (Pin 34 or 35) asserted high indicates a read operation. A low on the R/W* Signal along with this signal asserted and the CS* Signal (Pin 34 or 35) asserted high indicates a write operation.</p>
READY	38	OD	<p>READY: This is the microcontroller ready line. When this is deasserted low, the microcontroller shall insert wait states to allow time for the CL-SM331 to respond to the access.</p>
I/MC*	40	I	<p>INTEL/MOTOROLA: This signal selects the microcontroller interface to be used. When this signal is asserted high, it selects the Intel Bus Control Interface. When this signal is deasserted low, it selects the Motorola Bus Control Interface. This input signal may be legally 'floated' with the default selection of the Intel Bus Control Interface.</p>
HINT	33	O, OD, Z	<p>HOST INTERRUPT: This signal is a Host Interrupt line to the microcontroller. It is programmable for either a push-pull or open-drain output circuit. This signal powers up in the high-impedance state.</p>
AD0:7	42-44, 46-50	IO	<p>LOCAL MICROCONTROLLER ADDRESS/ DATA BUS: These are tri-state Address/Data lines that interface with a multiplexed Microcontroller Address/Data Bus.</p>
ALE	52	I	<p>ADDRESS LATCH ENABLE: The trailing edge of this control signal latches the address on the A/D lines.</p>
RST*	19	I	<p>RESET: An asserted low input generates a component reset that stops all operations within the chip and deasserts all output signals. All input/output signals, the SCSI Interface Output signals and the HINT Signal (Pin 33) and the DINT Signal (Pin 32) are set to the high-impedance state. Refer to the section on register initialization (Section 5.3).</p>

2.2 SCSI Bus Interface Pins

SYMBOL	QFP PIN NUMBER	TYPE	DESCRIPTION
SDB0*:7*	54-57, 59-62	I/O, OD	SCSI DATA BUS: These eight signals comprise the SCSI Data Bus for information transfer.
SDBP*	63	I/O, OD	SCSI DATA BUS PARITY: This signal transfers odd parity of the SCSI Data Bus.
ATN*	66	I/O, OD	SCSI ATTENTION: This signal indicates the Attention condition on the SCSI Bus.
BSY*	67	I/O, OD	SCSI BUSY: This signal when asserted low indicates that the SCSI Bus is being used.
ACK*	68	I/O	SCSI ACKNOWLEDGE: When this signal is asserted low, it indicates that the SCSI Initiator has acknowledged the data transfer.
SRST*	69	I/O, OD	SCSI RESET: This signal when asserted low indicates that the Reset Condition is on the SCSI Bus.
MSG*	70	I/O, OD	SCSI MESSAGE: When this signal is asserted low, it indicates that the SCSI Message Phase is active on the SCSI Bus.
SEL*	72	I/O, OD	SCSI SELECT: This signal is used by a SCSI Initiator to select a SCSI Target or by a SCSI Target to reselect a SCSI Initiator.
C*/D	73	I/O, OD	SCSI COMMAND/DATA: This signal indicates whether Control (when asserted low), or Data (when deasserted high) information is on the SCSI Data Bus signals.
REQ*	74	I/O	SCSI REQUEST: This signal when asserted low indicates that a request for a data transfer is active on the SCSI Bus.
I*/O	75	I/O, OD	SCSI INPUT/OUTPUT: This signal controls the direction of data transfer on the SCSI Data Bus signals with respect to a SCSI Initiator. When this signal is asserted low, it indicates information input to the SCSI Initiator. When this signal is deasserted high, it indicates output from the SCSI Initiator. This signal is also used to distinguish between the SCSI Selection and the SCSI Reselection phases.

2.3 SCSI Bus Control Pins

SYMBOL	QFP PIN NUMBER	TYPE	DESCRIPTION
SDOE	78	○	SCSI DATA BUS OUTPUT ENABLE: This signal is asserted high when the SCSI Data Bus is to be driven by the CL-SM331.
INIT	79	○	INITIATOR: When this signal is asserted, it indicates that the CL-SM331 is an Initiator device active on the SCSI Bus.
TAR	81	○	TARGET: When this signal is asserted, it indicates that the CL-SM331 is a Target device active on the SCSI Bus.
AIP	82	○	ARBITRATION IN PROGRESS: When this signal is asserted, it indicates that the CL-SM331 is in the SCSI Arbitration Phase.
BSYO	80	○	BUSY OUT: This is the SCSI Busy Output Signal. When this signal is asserted, it indicates that the CL-SM331 is driving the SCSI Busy Signal (Pin 67).
SELO	76	○	SELECT OUT: This is the SCSI Select output Signal. When it is asserted, it indicates that the CL-SM331 is driving the SCSI Select Signal (Pin 72).

2.4 Buffer Manager Interface Pins

SYMBOL	QFP PIN NUMBER	TYPE	DESCRIPTION
BA17/CAS*	15	O	BUFFER MEMORY ADDRESS 17/COLUMN ADDRESS STROBE: This signal is used for addressing the buffer memory in SRAM Mode or as the column address strobe in DRAM Mode.
BA16/RAS*	14	O	BUFFER MEMORY ADDRESS 16/ROW ADDRESS STROBE: This signal is used for addressing the buffer memory in SRAM Mode or as the row address strobe in DRAM Mode.
MOE*	16	O	MEMORY OUTPUT ENABLE: In SRAM Mode this signal is asserted low when every buffer memory access is active. It is recommended that this signal be connected to the SRAM Output enable for high-speed operation. In DRAM Mode this signal is asserted low only for buffer memory read operations.
WE*	17	O	WRITE ENABLE: This signal is asserted low when a buffer memory write operation is active in both SRAM and DRAM Modes.
SYSClk	24	I	SYSTEM CLOCK: This is the clock input that is used to generate buffer memory access cycles, to control automatic SCSI timing operations, and to clock ECC Correction Vector processes.
BD0:7	84-88, 90,93-94	IO	BUFFER MEMORY DATA BUS: These eight signals are Bits 0-7 of the eight-bit parallel data lines to/ from the buffer memory.
BDP	95	IO	BUFFER MEMORY DATA PARITY: This signal transfers odd parity of the Buffer Memory Data Bus to/from the buffer memory.
BA0:15	96-99 1-8, 10-13	O	BUFFER MEMORY ADDRESS LINES: These are signals 0-15 for addressing the buffer memory.
VECTOR	23	I	ECC CORRECTION VECTOR: This signal accepts ECC correction vector packets from the companion CL-SM330.
VERROR	21	O	ECC CORRECTION VECTOR ERROR: This signal is asserted if either the ECC Correction Vector packet was received with a protocol error or if the correction process was not successful.
VREADY	22	O	ECC CORRECTION VECTOR READY: This signal is asserted if the ECC Correction Circuit is ready to accept an ECC Correction Vector packet.

2.5 Sector Formatter Interface Pins

SYMBOL	QFP PIN NUMBER	TYPE	DESCRIPTION
SMDET	18	I	SECTOR MARK DETECTED: This is the input for the sector pulse received from the disk drive.
IDF	31	I	FORMAT SEQUENCER INPUT: This input signal is available to synchronize the Format Sequencer to an external event.
SRG	25	O	SYSTEM READ GATE: This signal is asserted when a disk read operation is in progress, and the NRZ Data is input to the CL-SM331.
SWG	26	O	SYSTEM WRITE GATE: This signal is used to enable the writing of NRZ Data out to the storage device during a write operation.
RRCLK	28	I	READ REFERENCE CLOCK: This signal input clocks the NRZ Data.
NRZ	29	IO	NON RETURN TO ZERO: This signal is the read data input from the disk drive when the Read Gate Signal (Pin 43) is asserted; it is the write data output to the disk drive when the Write Gate Signal (Pin 44) is asserted.
OUTPUT	30	O	FORMAT SEQUENCER OUTPUT: This output signal is available to synchronize the external hardware to the Format Sequencer. This signal is controlled by Bit 2 of the Control Field of the Writable Control Store (WCS).

2.6 Power and Ground Pins

SYMBOL	QFP PIN NUMBER	TYPE	DESCRIPTION
BGND [†]	9, 89, 100	N/A	BUFFER GROUND PINS.
LGND [†]	20, 27, 41, 45	N/A	LOGIC GROUND PINS.
+5V	39, 51, 91-92	N/A	POWER SUPPLY (+5V).
SGND [†]	53, 58, 64-65, 71 77, 83	N/A	HIGH CURRENT SCSI GROUND PINS.

NOTE: The superscript † indicates that SGND, BGND, and LGND are connected to three separate ground rings internally.

3. REGISTER TABLES

3.1 SCSI Interface Registers

ADDRESS	TYPE	DESCRIPTION/FUNCTION
40H/60H	RW	Direct SCSI Access Port
41H/61H	R	Selection/Reselection ID Input
41H/61H	W	Selection/Reselection ID Output
42H/62H	RW	SCSI Phase Control
43H/63H	RW	SCSI Synchronous Control
44H/64H	RW	SCSI Mode Control
45H/65H	RW	SCSI Operation Control
46H/66H	RW	SCSI Status Register 1
47H/67H	RW	SCSI Interrupt Enable Register 1
48H	RW	SCSI Status Register 2
49H	RW	SCSI Interrupt Enable Register 2
4AH	RW	Microcontroller SCSI FIFO Access Port

3.2 Buffer Manager Registers

ADDRESS	TYPE	DESCRIPTION/FUNCTION
50H	RW	Scheduled Buffer Data
51H	RW	Buffer Status/Control Register
52H	RW	Buffer Transfer Control
53H	RW	Buffer Mode Control
54H	RW	Buffer Manager Timing Control
55H	RW	DRAM Refresh Period
56H	RW	Buffer Size
57H-59H	RW	Disk Address Pointer
5AH-5CH	RW	Host Address Pointer
5DH-5FH	RW	Stop Address Pointer
71H-73H	R	Vector Process Address Pointer
74H	R	Vector Process Error Pattern

3.3 Sector Formatter Registers

ADDRESS	TYPE	DESCRIPTION/FUNCTION
4EH	RW	Sector Size
4FH	RW	Sector Formatter Mode Control
70H	RW	Synchronization Byte-Count Limit
75H-76H		Reserved
77H	RW	Sector Formatter Operation Control
78H	R	Next Format Sequencer Address
78H	W	Branch Address
79H	R	Format Sequencer Status Register 1
79H	W	Format Sequencer Start Address
7AH	R	Format Sequencer Status Register 2
7BH-7CH		Reserved
7DH	RW	Sector Formatter Interrupt
7EH	RW	Sector Formatter Interrupt Enable
7FH	R	Sector Formatter Stack
7FH	W	Reserved

3.4 Writable Control Store (WCS) Fields

ADDRESS	TYPE	DESCRIPTION/FUNCTION
80H-9EH	RW	Next Address Field
A0H-BEH	RW	Control Field
C0H-DEH	RW	Count Field
E0H-FEH	RW	Data/Branch Field

3.5 Sequencer Registers

ADDRESS	TYPE	DESCRIPTION/FUNCTION
9FH	RW	Current Sequencer Word — Next Address Field
BFH	RW	Current Sequencer Word — Control Field
DFH	RW	Current Sequencer Word — Count Field
FFH	RW	Current Sequencer Word — Data/Branch Field

3.6 Register and Bit Table

ADDRESS	TYPE	DESCRIPTION/FUNCTION
40H/60H	RW	Direct SCSI Access Port
41H/61H	R	Selection/Reselection ID Input
41H/61H	W	Selection/Reselection ID Output
42H/62H	RW	SCSI Phase Control Bit 7: SCSI Acknowledge Bit 6: SCSI Attention Bit 5: SCSI Select Bit 4: SCSI Busy Bit 3: SCSI Request Bit 2: SCSI Message Bit 1: SCSI Input/Output* Bit 0: SCSI Control/Data*
43H/63H	RW	SCSI Synchronous Control Bits 7-4: Synchronous Transfer Rate Bits 3-0: Offset Count
44H/64H	RW	SCSI Mode Control Bits 7-5: SCSI Logic Clock Prescaler Bit 4: SCSI Logic Clock Disable Bit 3: SCSI Parity Enable Bits 2-0: SCSI ID Bits
45H/65H	RW	SCSI Operation Control Bit 7: SCSI Reset Out Bit 6: SCSI Active Pull-up Select Bit 5: Enable Initiator Bit 4: Enable Target Bit 3: Microcontroller Direct SCSI Output Enable Bit 2: SCSI Automatic Selection/Reselection Mode Bit 1: SCSI Automatic Selection/Reselection Enable Bit 0: Arbitration/Selection Start
46H/66H	RW	SCSI Status Register 1 Bit 7: SCSI Rst In Bit 6: SCSI Parity Error Bit 5: SCSI Bus Parity Error Detected Bit 4: SCSI/Buffer Parity Error Detected Bit 3: SCSI Bus Free Detected Bit 2: SCSI Offset Overrun/Underrun Detected Bit 1: SCSI Attention Detected Bit 0: SCSI Reset Detected

3.6 Register and Bit Table (cont.)

ADDRESS	TYPE	DESCRIPTION/FUNCTION
47H/67H	RW	SCSI Interrupt Enable Register Bits 7-6: Reserved Bit 5: SCSI Bus Parity Error Enable Bit 4: SCSI/Buffer Parity Error Enable Bit 3: SCSI Bus Free Detected Enable Bit 2: Offset Overrun/Underrun Enable Bit 1: Attention Detected Enable Bit 0: SCSI Reset Detected Enable
48H	RW	SCSI Status Register 2 Bit 7: Req-On Bit 6: SCSI Phase Mismatch Bit 5: Transfer Halted Bit 4: Transfer Done Bit 3: Automatic Selecting/Reselecting Done Bit 2: Arbitration Won Bit 1: Device Reselected Bit 0: Device Selected
49H	RW	SCSI Interrupt Enable Register 2 Bit 7: Req-On Enable Bit 6: SCSI Phase Mismatch Enable Bit 5: Transfer Halted Bit 4: Transfer Done Enable Bit 3: Automatic Selecting/Reselecting Enable Bit 2: Arbitration Won Enable Bit 1: Device Reselected Enable Bit 0: Device Selected Enable
4AH	RW	Microcontroller SCSI FIFO Access Port
4BH-4DH		Reserved
4EH	RW	Sector Size
4FH	RW	Sector Formatter Mode Control Bit 7: Reserved Bit 6: Local Int* Mode Enable Bit 5: Interrupt Polarity Bit 4: SCSI Interface Register Decode Select Bit 3: Local Int* Pin Pull-up Disable Bit 2: Local Dint Enable Bit 1: Local Hint Enable Bit 0: Sector Formatter Reset
50H	RW	Scheduled Buffer Data

3.6 Register and Bit Table (cont.)

ADDRESS	TYPE	DESCRIPTION/FUNCTION
51H	RW	Buffer Status/Control Register Bit 7: Reserved Bit 6: DRAM Burst Enable Bit 5: SCSI Data Set Up Select Bit 4: Clear FIFO Bits 3-0: Synchronous Data Transfer Offset (Read Only)
52H	RW	Buffer Transfer Control Bits 7-4: PIO Transfer Count Bit 3: SCSI R/W* Transfer Direction Bit 2: PIO Start Bit 1: DMA Start Bit 0: Enable Buffer Segmentation
53H	RW	Buffer Mode Control Bits 7-6: Wait States Bit 5: Host/Buffer Reset Bit 4: MOE Disable Bit 3: Buffer Memory Parity Enable Bits 2-1: DRAM Type Bit 0: DRAM/SRAM*
54H	RW	Buffer Manager Timing Control Bits 7-6: CAS* High Time Bits 5-4: CAS* Low Time Bits 3-2: RAS* High Time Bits 1-0: RAS* Low Time/SRAM Cycle Time
55H	RW	DRAM Refresh Period
56H	RW	Buffer Size
57H-59H	RW	Disk Address Pointer
5AH-5CH	RW	Host Address Pointer
5DH-5FH	RW	Stop Address Pointer
70H	RW	Synchronization Byte-Count Limit
71H-73H	R	Vector Process Address Pointer
74H	R	Vector Process Error Pattern
75H-76H		Reserved

3.6 Register and Bit Table (cont.)

ADDRESS	TYPE	DESCRIPTION/FUNCTION
77H	RW	Sector Formatter Operation Control Bits 7-6: Reserved Bit 5: Edge Detect Sensitivity Selection Bit 4: Inhibit Data Field Carry Bit 3: Buffer/Disk R/W* Transfer Direction Bit 2: Suppress Transfer Bit 1: Data/Branch Field Mode Enable Bit 0: Reserved
78H	R	Next Format Sequencer Address Bits 7-5: Reserved Bits 4-0: Next Active Format Sequencer Address
78H	W	Branch Address Bits 7-5: Reserved Bits 4-0: Branch Address
79H	R	Format Sequencer Status Register 1 Bit 7: Byte Ready Bit 6: Format Sequencer Output Bit 5: Format Sequencer Input Bit 4: Synchronization Detect Status Bit 3: Branch Active Bit 2: Data Transfer Bit 1: AM Active Bit 0: Format Sequencer Active
79H	W	Format Sequencer Start Address Bits 7-5: Reserved Bits 4-0: Start Address
7AH	R	Format Sequencer Status Register 2 Bit 7: Reserved Bit 6: Disk/Buffer Parity Error Bit 5: Reserved Bit 4: Synchronization Time-Out Error Bit 3: Data Field CRC Error Bit 2: Compare Less Than Bit 1: Compare Greater Than Bit 0: Compare Equal
7BH-7CH		Reserved

3.6 Register and Bit Table (cont.)

ADDRESS	TYPE	DESCRIPTION/FUNCTION
7DH	RW	Sector Formatter Interrupt Bit 7: Vector Parity Error Detected Bit 6: Sequencer Output Detected Bit 5: Data Transfer Detected Bit 4: Branch Active Detected Bit 3: Sequencer Stopped Detected Bit 2: Input Detected Bit 1: Vector Transmission Error Detected Bit 0: SMDDET Detected
7EH	RW	Sector Formatter Interrupt Enable Bit 7: Vector Parity Error Detected Enable Bit 6: Sequencer Output Detected Enable Bit 5: Data Transfer Detected Enable Bit 4: Branch Active Detected Enable Bit 3: Sequencer Stopped Detected Enable Bit 2: Input Detected Enable Bit 1: Vector Transmission Error Detected Enable Bit 0: SMDDET Detected Enable
7FH	R	Sector Formatter Stack
7FH	W	Reserved
80H-9EH	RW	WCS Next Address Field Bits 7-5: Branch Command Bits 4-0: Next Address
9FH	RW	Current Sequencer Word — Next Address Field
A0H-BEH	RW	WCS Control Field Bit 7: Alternate Branch Command Select Bits 6-5: Control Field Bit 4: Stack Enable Bit 3: Invalid NRZ Control Bit 2: Output Bit 1: Compare Enable Bit 0: Data Transfer
BFH	RW	Current Sequencer Word — Control Field
C0H-DEH	RW	WCS Count Field Bit 7: Count/Process AM Bit 6: Count/Process CRC/Start Synchronization Timer Bits 5-0: Count
DFH	RW	Current Sequencer Word — Count Field
E0H-FEH	RW	WCS Data/Branch Field
FFH	RW	Current Sequencer Word — Data/Branch Field

4. FUNCTIONAL DESCRIPTION

Within high-performance, intelligent, disk drive controller subsystems the CL-SM331 is the VLSI component that enables the local microcontroller to off load all of the disk controller real-time tasks. Consequently, the microcontroller can execute commands at a higher level by parsing the command into lower level, high-speed tasks. These lower level, high-speed tasks are in turn completely managed by the CL-SM331.

As the block diagram on the cover page indicates, the components can be divided into the following four functional blocks:

- **Microcontroller,**
- **SCSI Host,**
- **Buffer Manager, and**
- **Sector Formatter.**

Each of these functional logic blocks has an associated interface that is specifically designed to manage the operation of the external devices and buses. In order to provide this support each interface uses information that is programmed by the local microcontroller in advance of the required operations.

4.1 Microcontroller Interface

A number of features have been included in the Microcontroller Interface to enable the CL-SM331 to operate with a variety of high-speed microcontrollers. For example, the CL-SM331 has a configuration signal called the I/MC* Signal (Pin 40) that allows for either the Intel or the Motorola method of data control to be used. Through the CL-SM331 Microcontroller Interface all of its registers are read or written, and the Writable Control Store (WCS) is programmed for the required operations of any sector and track format.

4.1.1 Microcontroller Interface to the CL-SM331

The microcontroller to CL-SM331 communication path is a multiplexed, 8-bit address and Data Bus similar to that provided by the Intel 80188 and the Motorola 68HC11 class of controllers. The CL-SM331 can use either the Intel or the Motorola method of data control. If the I/MC* Configuration Signal (Pin 40) is connected to power, or is left unconnected then the component uses the Intel method of data control. When the Intel Interface is selected, the WR*/R/W* Signal (Pin 36) acts as a write strobe. In the case of a write operation, this write strobe provides the timing and control for the data transfers. Similarly in the case of a read operation, the RD*/DS Signal (Pin 37) acts as a read strobe to provide the timing and the control for the data transfers.

If the I/MC* Signal (Pin 40) is connected to ground then the Motorola Interface is assumed. This configuration converts the WR*/R/W* Signal (Pin 36) into a control signal that is used *only* to determine the direction of the data transfer. When the input to this signal is high, a read operation is in progress; when it is low, a write operation is in progress. Data timing is derived with respect to the RD*/DS Signal (Pin 37). In the case of a read operation, the rising (leading) edge of the RD*/DS Signal (Pin 37) indicates when the CL-SM331 can start driving the Data Bus. In the case of a write operation, the falling (trailing) edge is used by the CL-SM331 to latch the data from the Microcontroller Address/Data Bus.

The CL-SM331 can also generate wait states to the local microcontroller through its READY signal (Pin 38). This permits microcontrollers with a wait state input to operate the disk controller system bus without any loss of performance if the microcontroller can normally perform read or write accesses faster than the CL-SM331 permits. The component powers up with the maximum number of wait states inserted into every microcontroller access. The microcontroller can then program either no wait states or the actual number of wait states required by the system microcontroller.

4.1.2 Microcontroller-to-Buffer Manager Interface

Microcontroller access to the contents of the RAM Data Buffer and the Buffer Memory Data Bus are made accessible through the CL-SM331 Microcontroller Interface. The local microcontroller can read or write the contents of the RAM Data Buffer by means of a scheduled Buffer Memory access using the CL-SM331 Port 50H (the Scheduled Buffer Data Register). The memory cycle access is considered scheduled because it is granted based on a rotating priority by the Buffer Manager regardless of whether it is a read or write memory request. The Disk Address Pointer (Registers 57H-59H) is used as the pointer into the Buffer Memory for all of the microcontroller accesses. Consequently, all disk operations must be terminated before the local microcontroller attempts any access to the RAM Data Buffer.

In order to write a byte to the Buffer Memory, the microcontroller loads the CL-SM331 Port 50H (the Scheduled Buffer Data Register) with the data to be written to the Buffer Memory. This generates a transfer request to the Buffer Manager which will grant a prioritized Buffer Memory access cycle. When the byte has been successfully written, the Byte Ready Bit (Register 79H, Bit 7) will be set. Reading a byte from the Buffer Memory is initiated by having the microcontroller read Port 50H (the Scheduled Buffer Data Register). This first byte is discarded because it is a dummy read. When the status for byte ready becomes valid (the Byte Ready Bit (Register 79H, Bit 7) is set), then the first valid byte which is the byte pointed to by the Disk Address Pointer (Registers 57H-59H) has been read into Port 50H (the Scheduled Buffer Data Register). When that byte is read, the read strobe causes an automatic request for another Buffer Memory access cycle. This request causes the byte located at the next address pointed to by the Disk Address Pointer (Registers 57H-59H) to be fetched. Note that the Disk Address Pointer (Registers 57H-59H) is automatically increment after each access.

Switches or jumpers for user configurable options can be implemented on the Buffer Memory Data Bus. The logical value of these switches is read in much the same way as a

byte of data is read from the Buffer Memory. However, the Memory Output Enable Signal (MOE* - Pin 16) should be disabled for both SRAM and DRAM Modes, and the BA16/RAS* (Pin 14) and the BA17/CAS* (Pin 15) signals should be disabled in DRAM Mode to prevent the Buffer Memory from driving the bus. The MOE* Signal (Pin 16), the BA16/RAS* Signal (Pin 14), and the BA17/CAS* Signal (Pin 15) can be disabled by setting the MOE Disable Bit (Register 53H, Bit 4).

4.1.3 Microcontroller-to-SCSI Interface

There are two methods that the local microcontroller can use to access the SCSI Data Bus: (1) transfers that are controlled completely by the firmware, or (2) Programmed I/O (PIO) transfers that use the CL-SM331 FIFO.

In the first method, a single byte at a time is transferred and the transfer is handled completely by the firmware. Using firmware control to handshake and read or write each byte to the SCSI Data Bus is appropriate for particular SCSI Bus phases such as the Message In Phase or the Message Out Phase. This transfer method allows the microcontroller to monitor the SCSI Attention Signal (ATN* - Pin 68) on a byte-by-byte basis (monitoring of the SCSI Attention Signal is a requirement of the SCSI-2 protocol during message transfers when a device is operating in Target Mode).

For firmware controlled accesses, the information bytes are either read or written through the Direct SCSI Access Port (Register 40H/60H). The SCSI Request Signal (REQ* - Pin 74) and the SCSI Acknowledge Signal (ACK* - Pin 68) are controlled and monitored in the SCSI Phase Control Register (42H/62H). The SCSI Phase is set in advance of the transfer in the SCSI Phase Control Register (42H/62H).

In the second method, the CL-SM331 16-byte FIFO is used for automatic Programmed I/O (PIO) transfers. This permits automatic handshaking of the SCSI Request Signal (REQ* - Pin 74) and the SCSI Acknowledge Signal (ACK* - Pin 68) which allows up to 15 bytes of information to be transferred without any

microcontroller intervention. This method of transfer is useful for example in the SCSI Command Phase in order to bring in the first six bytes of a command. In fact, because most SCSI commands are six bytes long, this transfer method will bring in all of the command. Programmed I/O (PIO) transfers can be asynchronous or synchronous. For example, asynchronous transfers would be used to transfer a command; whereas, synchronous transfers (if the negotiation is still valid) would be used to transfer the data requested by an Initiator.

The microcontroller always accesses the CL-SM331 FIFO for reads or writes through the Microcontroller SCSI FIFO Access Port (Register 4AH). The Programmed I/O (PIO) transfer count, control, and direction are all managed in the Buffer Transfer Control Register (52H).

4.1.4 The CL-SM331 Local Microcontroller Interface

Interrupts and status to the local microcontroller are consistently implemented from all four of the CL-SM331 functional blocks. The SCSI Host and the Buffer Manager interrupts are located in the SCSI Status Registers (46H/66H and 48H). The Sector Formatter interrupts are located in the Sector Formatter Interrupt Register (7DH).

The SCSI Host and the Buffer Manager interrupts have their own dedicated interrupt signal output to the microcontroller via the CL-SM331 HINT Signal (Pin 33). The Sector Formatter interrupts also have their own dedicated interrupt signal output to the microcontroller via the CL-SM331 DINT Signal (Pin 32). This permits the microcontroller to localize the source of the interrupt or the pending status much quicker than if all of the interrupts were connected to the same interrupt output. If the local microcontroller permits only one interrupt signal then these interrupt sources collectively can be configured to drive only one interrupt output signal by setting the Local Int[†] Mode Enable Bit (Register 4FH, Bit 6).

In addition each SCSI Host and Buffer Manager Status Bit can be masked individually via the SCSI Interrupt Enable Registers (47H/67H and

49H). Each Sector Formatter Status Bit can also be masked individually via the Sector Formatter Interrupt Enable Register (7EH). Because of this masking capability the bit can be prevented from generating an interrupt yet it still can provide status information to the microcontroller that is operating in polled mode. The interrupt output signals can be configured for open-drain operation in a multiplexed interrupt system by setting the Local Int Pin Pull-Up Disable Bit (Register 4FH, Bit 3). Interrupts can be disabled completely by resetting the interrupt enables. Interrupts are enabled by setting the Local HINT Enable Bit and the Local DINT Enable Bit (Bits 1 and 2, respectively, of the Sector Formatter Mode Control Register (4FH)). Interrupts are disabled by resetting Bits 1 and 2 of Register 4FH.

4.2 SCSI Functional Description

The second functional logic block of the CL-SM331 is the CL-SM331 Small Computer System Interface (SCSI). The control, timing, interface, and data transfer sections of this interface adhere to the requirements of the SCSI-2 proposed specification as well as to the ANSI X3.131-1986 SCSI specification. It is assumed that the reader is familiar with these requirements; otherwise, it is assumed that the ANSI document will be used in conjunction with Section 4.2.

The SCSI Interface is the means of communication between a host computer system and one or more peripheral devices. A SCSI device assumes one of two roles in any SCSI Bus communication. The Initiator is defined as the SCSI device that generates a process, or more specifically the nexus. The Target is the recipient of the Initiator request and must execute some operation in response to an Initiator request.

The SCSI Bus is an intermediate physical construct between the host system and the attached peripheral device(s). The host system uses an interface circuit to gain access to the SCSI Bus. Previously, the peripheral device usually required external interface circuitry to connect to the SCSI Bus. In the case of the CL-SM331, however, all of the required interface,

timing, control, and data paths are included in one integrated circuit.

The majority of the activity on the SCSI Bus is with the host system computer acting as an Initiator that issues commands to a Target device such as a disk controller. It is through a well-defined protocol that the Initiator can request data reads or writes and other more sophisticated operations of the Target. It is permissible for a Target to assume the role of an Initiator and vice versa.

4.2.1 Overview of the CL-SM331 SCSI Capabilities

Implementation of the SCSI Bus Phases can be cumbersome. Consequently, many of these often-repeated processes are designed into the CL-SM331 control logic. Such routine SCSI Bus control operations as arbitration, selection and reselection are automatically sequenced in the CL-SM331 hardware; this results in more automated handling and ease of use.

Program a SCSI ID for the device into Bits 2-0 of the SCSI Mode Control Register (44H/64H). The CL-SM331 can be programmed to assume either the role of an Initiator or a Target. For firmware-controlled operations the selection of a Target or Initiator is controlled by setting either the Enable Target Bit or the Enable Initiator Bit (Bits 4 and 5, respectively, in Register 45H/65H). Otherwise, the Target or Initiator role is derived from the programmed automatic operation (e.g., the selection, reselection, selection detected, or reselection detected process).

The SCSI Bus signals can be programmed as open drain or active pull-up by setting the SCSI Active Pull-Up Select Bit (Register 45H/65H, Bit 6) to the proper value.

4.2.2 Microcontroller-to-SCSI Bus Connection

The local microcontroller is allowed access to the SCSI Data Bus through two distinct CL-SM331 address ports — (1) Port 40H/60H (the Direct SCSI Access Port Register), and (2) Port 4AH (the Microcontroller SCSI FIFO Access Port

Register). The accesses can be handled singly under direct firmware control or by an automatic Programmed I/O (PIO) circuit in the event of multiple bytes. In the latter case, the data is stored or received in the CL-SM331 16-byte FIFO.

The local microcontroller is provided access to the SCSI Bus through addressing Port 40H/60H (the Direct SCSI Access Port Register). The microcontroller can either read or write data directly to the SCSI Bus through this port. The 16-byte FIFO is given a separate port address so that the hardware can automatically distinguish the type of microcontroller to SCSI Bus access. The FIFO must be addressed by writing or reading Port 4AH (the Microcontroller SCSI FIFO Access Port Register). The FIFO can be used for stacking messages, sense data, or any other concurrent information transfer that would not constitute a DMA Data transfer. The direction of the information transfer is controlled by the SCSI R/W* Transfer Direction Bit (Register 52H, Bit 3). This applies to both DMA transfers (refer to the section on the SCSI Data transfers, Section 4.2.5) as well as automatic Programmed I/O (PIO) transfers through the FIFO.

For the Programmed I/O (PIO) Mode of operation the REQ*/ACK* handshake is handled automatically by an internal CL-SM331 state machine. In the case of reading information from the bus, the expected or minimum number of bytes to be read should be loaded into the PIO Transfer Count Field (Register 52H, Bits 7-4). In the case of writing bytes to the SCSI Bus, the exact number of bytes to be written is always known so that the number of bytes for the Programmed I/O (PIO) transfer should be loaded into the PIO Transfer Count Field (Register 52H, Bits 7-4).

Before commencing with any new operation that will use the FIFO, the FIFO must be cleared by setting the Clear FIFO Bit (Bit 4) and then resetting this bit of the Buffer Status/Control Register (51H). The sequence is then started by setting the PIO Start Bit (Bit 2) of the Buffer Transfer Control Register (52H). The byte count in the FIFO can be obtained by reading the count in Bits 7-4 of Register 52H. The PIO Start

Bit (Register 52H, Bit 2) is automatically reset when the FIFO count has reached zero.

Programmed I/O (PIO) transfers can be either asynchronous or synchronous. If the information being transferred is data and a previous synchronous negotiation is still in effect then the Programmed I/O (PIO) transfer should be configured for synchronous transfers (refer to the section on SCSI Data transfers, Section 4.2.5).

4.2.3 SCSI Phase Control

The majority of the SCSI Phase control and detection can be handled under the hardware control of the CL-SM331 if the CL-SM331 is programmed accordingly. The SCSI Arbitration Phase is automatically started by setting the Arbitration/Selection Start Bit (Register 45H/65H, Bit 0). After waiting the appropriate Bus Free delay, the CL-SM331 ID Bit driven onto the SCSI Bus during the SCSI Arbitration Phase is derived from the encoded Bits 2-0 of the SCSI Mode Control Register (44H/64H). Arbitration has been won when the Arbitration/Selection Start Bit (Register 45H/65H, Bit 0) resets itself or the Arbitration Won Bit (Register 48H, Bit 2) is set. If arbitration was lost, the CL-SM331 continues to arbitrate for control of the SCSI Bus until arbitration has been won, or until the Arbitration/Selection Start Bit (Register 45H/65H, Bit 0) is reset by the local microcontroller.

Whether the SCSI Selection Phase or the SCSI Reselection Phase is the pending phase (one or the other is the only possible phase after the SCSI Arbitration Phase) both the CL-SM331 ID and the desired Target or Initiator ID Bit must be set by writing to the Selection/Reselection ID Output Register (41H/61H).

The SCSI Selection or Reselection phases are allowed to start automatically after a successful SCSI Arbitration Phase by setting the SCSI Automatic Selection/Reselection Enable Bit (Register 45H/65H, Bit 1). For the SCSI Selection Phase the SCSI Automatic Selection/Reselection Mode Bit (Register 45H/65H, Bit 2) must be set. To go to the SCSI Reselection Phase the SCSI Automatic

Selection/Reselection Mode Bit (Register 45H/65H, Bit 2) must be reset.

If the device is an Initiator, then the SCSI Selection Phase is the appropriate SCSI Bus Phase to follow arbitration. The SCSI Attention Bit (Bit 6) of the SCSI Phase Control Register (42H/62H) should be set such that the SCSI Attention Signal (Pin 66) is automatically asserted low during the SCSI Selection Phase. This should be done before setting the SCSI Automatic Selection/Reselection Enable Bit (Register 45H/65H, Bit 1). Having set the SCSI Automatic Selection/Reselection Enable Bit (Bit 1) of the SCSI Operation Control Register (45H/65H), the CL-SM331 will then proceed to the SCSI Selection Phase.

If the device is a Target, then the SCSI Reselection Phase is the next phase to follow arbitration. The SCSI Input/Output* Bit (Bit 1) of the SCSI Phase Control Register (42H/62H) should be set such that the SCSI Input/Output Signal (Pin 75) is automatically asserted low during the SCSI Reselection Phase. This should be done before setting the SCSI Automatic Selection/Reselection Enable Bit (Register 45H/65H, Bit 1). Having set the SCSI Automatic Selection/Reselection Enable Bit (Bit 1) of the SCSI Operation Control Register (45H/65H), the CL-SM331 will then proceed to the SCSI Reselection Phase.

The CL-SM331 will also perform the converse of these functions automatically if the SCSI Automatic Selection/Reselection Enable Bit (Register 45H/65H, Bit 1) is set. That is, if the CL-SM331 is being selected by an Initiator, it will detect that it is being selected and will set the Device Selected Bit (Bit 0) in the SCSI Status Register 2 (48H). In addition, the CL-SM331 will respond to the selection by: (1) setting the Enable Target Bit (Bit 4) of the SCSI Operation Control Register (45H/65H), (2) asserting low the SCSI Busy Signal (Pin 67), (3) setting the SCSI Busy Bit (Bit 4) of the SCSI Phase Control Register (42H/62H), and (4) latching the contents of the SCSI Data Bus into the Selection/Reselection ID Input Register (41H/61H).

If a valid reselection by a Target is observed on the bus, the CL-SM331 will set the Device Reselected Bit (Bit 1) of the SCSI Status Register 2 (48H). The CL-SM331 will also do the following: (1) set the Enable Initiator Bit (Register 45H/65H, Bit 5), (2) assert the SCSI Busy Signal (Pin 67) low and set the SCSI Busy Bit (Bit 4) of the SCSI Phase Control Register (42H/62H) until the SCSI Select Signal (Pin 72) is asserted low, and (3) latch the contents of the SCSI Data Bus into the Selection/ Reselection ID Input Register (41H/61H).

If the control of the SCSI Selection or Reselection Phase is performed through firmware operations then the SCSI control signals are qualified with one of two bits — the Enable Target Bit or the Enable Initiator Bit (Bits 4 and 5, respectively, of Register 45H/65H).

The Enable Target Bit (Register 45H/65H, Bit 4) is set to allow the CL-SM331 to drive the following Target signals: the SCSI Message Signal (Pin 70), the SCSI Command /Data Signal (Pin 73), the SCSI Input/Output Signal (Pin 75), and the SCSI Request Signal (Pin 74). These signals can be individually controlled or monitored in the SCSI Phase Control Register (42H/62H).

The Enable Initiator Bit (Register 45H/65H, Bit 5) is set to allow the CL-SM331 to drive the following Initiator signals: the SCSI Attention Signal (Pin 66) and the SCSI Acknowledge Signal (Pin 68). These two signals can be controlled or monitored through the SCSI Phase Control Register (42H/62H).

The SCSI Busy Signal (Pin 67) and the SCSI Select Signal (Pin 72) that are controlled by Bits 4 and 5 of Register 42H/62H are not gated by either the Enable Target Bit or the Enable Initiator Bit (Bits 4 and 5, respectively, of Register 45H/65H). The SCSI Select Signal (Pin 72) can be driven to allow for a firmware-controlled SCSI Selection Phase in Initiator Mode or a SCSI Reselection Phase in Target Mode. This also permits the SCSI Busy Signal (Pin 69) to be asserted low by the firmware in response to being selected or reselected yet still allows the CL-SM331 to assert this signal for automatic arbitration.

Because the SCSI Data Bus must be driven with the Initiator and Target ID values during the SCSI Selection and Reselection phases the Microcontroller Direct SCSI Output Enable Bit (Register 45H/65H, Bit 3) must be set before setting the Enable Target Bit or the Enable Initiator Bit (Bits 4 and 5, respectively, of Register 45H/65H). This allows the SCSI Data Bus to be driven provided that the Enable Initiator Bit or the Enable Target Bit is set during the selection or reselection process.

The RST* Signal (Pin 19) has a more global effect on the function of the SCSI Bus and can be asserted low at anytime by setting the SCSI Reset Out Bit (Bit 7) of the SCSI Operation Control Register (45H/65H).

4.2.4 SCSI Information Transfer Phases

All SCSI Bus phases other than the Arbitration, Selection, and Reselection phases are collectively defined as Information Transfer phases. The Information Transfer Phase is always set by the Target device during communication with an Initiator. The phase is defined by the encoded values of the following SCSI signals: the SCSI Command/Data Signal (Pin 73), the SCSI Input/Output Signal (Pin 75), and the SCSI Message Signal (Pin 70). The Information Transfer Phase is set through firmware by the local microcontroller for the particular Target. The Enable Target Bit (Register 45H/65H, Bit 4) must be set either in firmware or through an automatic selection or selection detected process before these signals are actively driven by the CL-SM331. Note that the corresponding bits in the SCSI Phase Control Register (42H/62H) for the SCSI Command/Data Signal (Pin 73), the SCSI Input/Output Signal (Pin 75), and the SCSI Message Signal (Pin 70) are the logical complement of the levels on the bus because the SCSI Bus is an active low bus.

Bit 0 of the SCSI Phase Control Register (42H/62H) is the SCSI Control/Data* Bit. When this bit is set, it indicates that the information being transferred on the SCSI Data Bus signals is either command, status, or message byte(s). Resetting this bit to a logical zero indicates that the information being transferred is data byte(s).

Bit 1 of the SCSI Phase Control Register (42H/62H) is the SCSI Input/Output* Bit. This bit indicates the direction of information transfer with respect to the Initiator. When this bit is set to a logical one, the information will be transferred in to the Initiator. Resetting this bit to a logical zero indicates that the information will be transferred out from the Initiator to the Target.

Bit 2 of the SCSI Phase Control Register (42H/62H) is the SCSI Message Bit. When this bit is set, it indicates that the information transfer is specifically a SCSI message. When this bit is reset, then the information could be data, a command, or status. A SCSI message could be either a Message In to the Initiator or a Message Out to the Target.

The following table lists the permissible Information Transfer phases for the encoded states of Bits 2-0 of the SCSI Phase Control Register (42H/62H).

Information Transfer Phase Control Bits

Register 42H/62H			
Bit 2	Bit 0	Bit 1	Information
MSG	C/D*	I/O*	Transfer Phase
0	0	0	Data Out Phase
0	0	1	Data In Phase
0	1	0	Command Out Phase
0	1	1	Status In Phase
1	0	0	Undefined
1	0	1	Undefined
1	1	0	Message Out Phase
1	1	1	Message In Phase

As a Target, the CL-SM331 can go to a SCSI Message In phase at any time by setting the three bit values as shown in the table above. As an Initiator, however, the CL-SM331 has no control over these three bits. As an Initiator to request a SCSI Message Out Phase, the local microcontroller should set the SCSI Attention Bit (Bit 6) of the SCSI Phase Control Register (42H/62H). The Target device should respond by setting the phase to a SCSI Message Out Phase at the earliest possible time.

These three Information Transfer Phase Control bits can also be used by the Initiator to read their value if required. They will provide status to the Initiator if the Target changes one or more of their values to an Information Transfer Phase that the Initiator is not expecting.

In the execution of most SCSI nexus, the Initiator can predict the next phase of operation. For example from the SCSI Command Phase, depending on the command, the Target will typically enter a SCSI Status Phase or Data Phase. The Initiator can predict this from the command sent. When in Initiator Mode, the CL-SM331 provides a status signal or an interrupt if the Target device drives to a SCSI Bus Phase that the Initiator does not expect (e.g., the Message In Phase). A transfer will not occur to prevent erroneous information transfer.

Bits 2-0 of Register 42H/62H should be set by the Initiator Microcontroller to the predicted state. That is, the expected Information Transfer Phase should be encoded using the SCSI Message Bit, the SCSI Input/Output* Bit, and the SCSI Control/Data* Bit (Bits 2-0, respectively, of Register 42H/62H). On each falling (leading) edge of the SCSI Request Signal (Pin 74), the CL-SM331 compares the Target-Driven Phase against the predicted state programmed in the CL-SM331. If any one of the three signals differ from the bits pre-programmed by the Initiator then the SCSI Phase Mismatch Bit (Bit 6) of the SCSI Status Register 2 (48H) will be set.

These bits can be read at anytime by either an Initiator or a Target. The values read always reflect the logical complement of the value on the CL-SM331 SCSI Bus Pin.

4.2.5 SCSI Data Transfers

SCSI Data is transferred either during a SCSI Data In or Data Out Phase. This is done either by an Initiator or a Target with the Target device controlling the data transfer. The major features in the CL-SM331 to improve data integrity, ease of implementation, and performance include the following: odd parity generation and detection, a 16-byte FIFO, an automatic DMA Transfer Mode, and both asynchronous and synchronous data transfers with the option of either a single-ended or differential bus connection.

SCSI parity checking is enabled by setting the SCSI Parity Enable Bit (Register 44H/64H, Bit 3). Parity generation is not affected by the value of the SCSI Parity Enable Bit (Register 44H/64H, Bit 3). If a parity error is detected during a data transfer then the SCSI Bus Parity Error Detected Bit (Bit 5) of the SCSI Status Register 1 (46H/66H) is set. A parity error can only be detected on the SCSI Bus when data is being read from the other device whether it is a Target or Initiator.

In addition to SCSI Bus parity, there is a parity circuit between the internal CL-SM331 SCSI Bus and the RAM Data Buffer Port. This parity detection circuitry is enabled if the Buffer Memory Parity Enable Bit (Bit 3) of the Buffer Mode Control Register (53H) is set. This

ensures the integrity of the data being read from the RAM Data Buffer to the CL-SM331 SCSI Interface logic. If a parity error is detected, it is latched in the SCSI/Buffer Parity Error Detected Bit (Bit 4) of the SCSI Status Register 1 (46H/66H).

Internal to the CL-SM331 and transparent to the user is a 16 byte bidirectional FIFO used in data reads or writes with the RAM Data Buffer. This FIFO acts as a buffer between the host (SCSI) transfer rate and the rate at which data is written to or read from the Buffer Memory. The FIFO is useful for preventing overruns or underruns as its status is used to control the assertion low of the SCSI Request Signal (Pin 74) as a Target or the assertion low of the SCSI Acknowledge Signal (Pin 68) as an Initiator.

The transfer of data is under the control of an automatic state sequencer which allows for the ability of a high-speed, DMA transfer to or from the RAM Data Buffer. DMA Data transfers are enabled by setting the DMA Start Bit (Bit 1) in the Buffer Transfer Control Register (52H). This bit is reset at the completion of a DMA transfer. A DMA transfer that is in progress can be cleanly terminated by resetting the DMA Start Bit (Register 52H, Bit 1).

The CL-SM331 is capable of asynchronous data transfers up to 3 Mbytes/second, and synchronous data transfers up to 5 Mbytes/second. Synchronous transfers are established through a defined message protocol. The two parameters that must be agreed upon between the Initiator and Target are an offset count and a synchronous transfer period. It is incumbent on the local microcontroller to arrive at compatible parameters with the other SCSI device. The parameters can then be programmed into the SCSI Synchronous Control Register (43H/63H). The offset count can be loaded with values from 1-15 bytes by setting the appropriate values into Bits 3-0 of Register 43H/63H. An offset of zero sets data transfers to the asynchronous mode of operation. The synchronous transfer period is a function of the input SYSCLK frequency and can assume 12 different periods depending on the values programmed in Bits 7-4 of Register 43H/63H.

4.2.6 Differential SCSI

Six additional pins are provided with the CL-SM331 for the control of the external logic that is necessary to implement the Differential Mode of bus operation. The Differential Mode is always enabled such that the six control pins always drive the correct control and timing. If Differential Mode is designed then the pins are connected controlling the external logic; otherwise, the outputs are left unconnected. There are no internal control bits in the CL-SM331 to differentiate between the Single-ended and the Differential Mode of operation.

4.3 Buffer Manager Interface

The third functional logic block of the CL-SM331 is the Buffer Manager Interface. This block controls the flow of data between the external RAM Data Buffer and the CL-SM331 SCSI Interface, the Sector Formatter Data path, and the Microcontroller Buffer Memory access ports. The Buffer Manager Interface provides the external RAM addressing, timing, and control signals necessary for the CL-SM331 to interface with the RAM Data Buffer. The Buffer Manager Interface also provides an additional data bit signal called the Buffer Memory Data Parity Signal (BDP - Pin 95) for odd parity generation and checking.

The Buffer Manager logic can control either a Static RAM (SRAM) Buffer or Dynamic RAM (DRAM) Buffer. The CL-SM331 powers up in the SRAM Mode. If DRAM Operation is desired then the DRAM/SRAM* Bit (Register 53H, Bit 0) should be set. The topics that are common to these two modes of operation are discussed in Sections 4.3.1 - 4.3.2. The two modes of operation, however, are sufficiently different that most of the logic is described in two different sections depending on the configuration. For details on the SRAM Buffer Interface Operation refer to Section 4.3.3. For details on the DRAM Buffer Interface Operation refer to Section 4.3.4. For details on hardware ECC Vector Processing, refer to Section 4.3.5.

4.3.1 RAM Data Buffer Segmentation

For optimum data flow control it is often desirable to divide the Buffer Memory into smaller 'protected' segments. The Buffer Manager provides the option to configure the RAM Data Buffer into 64K bytes data segments on 64K bytes address boundaries. The data segment is designated by the two or four most significant RAM address bits.

This Buffer Segmentation Mode is enabled by setting the Enable Buffer Segmentation Bit (Register 52H, Bit 0). In this mode after a Buffer Memory transfer is completed, only the address pointer lower and middle bytes are incremented. Consequently, the lower and middle bytes of the address pointers would roll over to 0000H without any change to the address pointer upper two bits which designate the segment.

4.3.2 RAM Data Buffer Parity

The CL-SM331 supports data parity on the external RAM Data Buffer. The Buffer Manager interface can be configured to generate the odd parity of the 8-bit data being written to the RAM Buffer. This parity check bit is written along with the 8-bit data to a 9-bit wide RAM Data Buffer. The Buffer Memory Data Parity Signal (Pin 95) is connected to the additional RAM device(s).

If the data is sourced from the Sector Formatter Data path, then the odd parity is generated at the serializer/deserializer (SERDES) and is passed through to the Buffer Memory Data Parity Signal (Pin 95). If the data is sourced from the SCSI Host Interface then the parity generation is dependent on the value of the SCSI Parity Enable Bit (Bit 3) of the SCSI Buffer Control Register (44H/64H). If this bit is set then the value of the parity received from the SCSI Data Bus is passed through to the Buffer Memory Data Parity Signal (Pin 95). If this bit is reset then the odd parity value of the data received from the SCSI Data Bus is generated inside the CL-SM331, and then is written out on the Buffer Memory Data Parity Signal (Pin 95).

When data is being read from the RAM Data Buffer, the odd parity value can be tested or ignored. If the Buffer Memory Parity Enable Bit

(Bit 3) of the Buffer Mode Control Register (53H) is set, then the bit value received from the Buffer Memory Data Parity Signal (Pin 95) is tested. It is tested to see if it is the odd parity value of the eight bits on the Buffer Memory Data Bus signals (BD0-7). The data being read from the RAM Data Buffer is either for the SCSI Host Interface or the SERDES of the Sector Formatter Data path. In both cases there is a bit available to report a parity error if one is detected by the CL-SM331 parity checking circuitry.

If the Sector Formatter is reading the RAM Data Buffer and a parity error is detected on the Buffer Memory Data Parity Signal (Pin 95), then the Disk/Buffer Parity Error Bit (Bit 6) of the Format Sequencer Status Register 2 (7AH) is set. If the SCSI Host Interface is reading from the RAM Data Buffer and a parity error is detected, then the SCSI/Buffer Parity Error Detected Bit (Bit 4) of the SCSI Status Register 1 (46H/66H) is set. The subsequent actions are firmware dependent; this enables different responses to the RAM Data Buffer parity errors to be constructed in the program.

If the Buffer Memory Parity Enable Bit (Bit 3) of the Buffer Mode Control Register (53H) is reset then the two status bits — the Disk/Buffer Parity Error Bit (Register 7AH, Bit 6), and the SCSI/Buffer Parity Error Detected Bit (Register 46H/66H, Bit 4) are always reset.

4.3.3 SRAM Buffer Interface Operation

In order to ensure the proper operation of the Buffer Manager in SRAM Mode, the DRAM/SRAM* Bit (Bit 0) of the Buffer Mode Control Register (53H) and the DRAM Burst Enable Bit (Bit 6) of the Buffer Status/Control Register (51H) must be reset.

4.3.3.1 SRAM Addressing Operation

When in the SRAM Mode of operation, the Buffer Manager Interface can address up to 256K bytes of memory. This requires 18 address lines that correspond to the Buffer Manager Address signals BA0-17 (Pins 96-99, 1-8, and 10-15). The Buffer Memory Address is never placed in a high-impedance state; it is

always driven by one of two sources — the Disk Address Pointer (Registers 57H-59H) or the Host Address Pointer (Registers 5AH-5CH). These pointers have various initialization conditions and their starting values can be changed via direct firmware control.

The Disk Address Pointer (Registers 57H-59H) is dedicated for disk and microcontroller transfers. The two high-order bits of the Disk Address Pointer (Registers 57H-59H) are in Bits 1-0 of Register 59H. The middle-order eight bits are in Register 58H, and the low-order eight bits are in Register 57H. Any access to the RAM Data Buffer by the Sector Formatter selects the value in Registers 57H-59H, the Disk Address Pointer, to be driven out on the Buffer Memory Address Bus.

When the local microcontroller accesses the Buffer Memory, the Disk Address Pointer (Registers 57H-59H) is also used. Consequently, in order to prepare for a local microcontroller access to the Buffer Memory all disk transfers to or from the CL-SM331 must be terminated before the Disk Address Pointer (Registers 57H-59H) is loaded.

The Host Address Pointer (Registers 5AH-5CH) is reserved for transfers between the SCSI Bus and the RAM Data Buffer. The Host Address Pointer two high-order bits are in Bits 1-0 of Register 5CH. The middle-order eight bits are in Register 5BH, and the low-order eight bits are in Register 5AH. Any access to the RAM Data Buffer by the SCSI Interface logic selects the value in Registers 5AH-5CH, the Host Address Pointer, and has the CL-SM331 drive this value onto the Buffer Memory Address Bus.

The Host Address Pointer (Registers 5AH-5CH) is compared with the Stop Address Pointer (Registers 5DH-5FH) in order to contain the data transfers to a particular block boundary value. To translate the value of the Host Address Pointer (Registers 5AH-5CH) into a repeatable block size, the Buffer Size Register (56H) is used to mask the upper address bits of the Host Address Pointer (Registers 5AH-5CH) and the Stop Address Pointer (Registers 5DH-5FH). Consequently, only the lower significant bits that are module a block size are used for the comparison. When the comparison of the Host

Address Pointer (Registers 5AH-5CH) and the Stop Address Pointer (Register 5DH-5FH), masked by the Buffer Size Register (56H), is equal, then the host transfer is terminated.

Both the Disk Address Pointer (Registers 57H-59H) and the Host Address Pointer (Registers 5AH-5CH) are automatically incremented by a count of one after the completion of each access to the RAM Data Buffer.

If Buffer Manager segmentation is disabled (refer to the section on Buffer Manager segmentation, Section 4.3.1), then all 18 buffer Memory Address lines (BA0-17) are subject to being incremented after each RAM Data Buffer access. If the system static Buffer Memory is less than 256K bytes, then do not use the remaining most significant Buffer Memory Address lines as memory chip selects. This limitation is imposed because the incrementing of the high-order address lines will deselect the memory chip(s). The firmware may avoid this problem by managing the address pointers (the Disk Address Pointer (Registers 57H-59H) and the Host Address Pointer (Registers 5AH-5CH)) on the proper address block boundaries.

4.3.3.2 SRAM Read/Write Access Control

The Buffer Manager accesses the Buffer Memory Data Bus to read or to write the contents of the RAM Data Buffer, or to read the static state of the Data Bus (refer to Section 4.1.2 for more details). The direction of the access must be specified in order to generate the correct control signals. The SCSI Host, the Sector Formatter, and the local microcontroller all use unique methods to specify the direction of the access.

In the case of SCSI Host transfers, the read/write control is set by the SCSI R/W* Transfer Direction Bit (Bit 3) of the Buffer Transfer Control Register (52H). When this bit is set, the data read from the RAM Data Buffer is transferred through the CL-SM331 chip to the SCSI Host Interface. If this bit is reset then the data is transferred from the SCSI Host Interface through the CL-SM331 chip and written to the RAM Data Buffer.

In the case of Sector Formatter transfers, the transfer direction is controlled by the Buffer/Disk R/W* Transfer Direction Bit (Bit 3) of the Sector Formatter Operation Control Register (77H). When this bit is set, the data read from the RAM Data Buffer is transferred to the Sector Formatter. In order to write to the RAM Data Buffer from the Sector Formatter this bit must be reset.

In the case of microcontroller transfers, the microcontroller control strobe is used in order to determine the transfer direction. A read of the CL-SM331 Port 50H (the Scheduled Buffer Data Register) results in a read of the RAM Data Buffer. A write to Port 50H (the Scheduled Buffer Data Register) causes a write to the RAM Data Buffer.

Given the direction of data transfer from the above controls, all read operations are the same regardless of the requesting source and similarly, all write operations are the same. Both the read and write operation commence when the correct address pointer (the Disk Address Pointer (Registers 57H-59H), or the Host Address Pointer (Registers 5AH-5CH)) is driven onto the Buffer Memory Address Bus.

In the case of a read to the RAM Data Buffer, the Memory Output Enable Signal (MOE* - Pin 16) is asserted low after the address is driven onto the Address Bus. This signal should be connected to the SRAM Output enable(s) to ensure the highest throughput. Data must be provided from the SRAM shortly before the rising (trailing) edge of the Memory Output Enable Signal (MOE* - Pin 16). The duration of the Memory Output Enable Signal (MOE* - Pin 16) is a programmable parameter (refer to the section on SRAM Signal timing, Section 4.3.3.3). The Write Enable Signal (WE* - Pin 17) remains deasserted high throughout the entire SRAM access.

In the case of a write to the RAM Data Buffer, the Memory Output Enable Signal (MOE* - Pin 16) and the Write Enable Signal (WE* - Pin 17) are concurrently asserted low after the address is driven onto the Address Bus. In order to ensure the highest throughput the Memory Output Enable Signal (MOE* - Pin 16) should be connected to the SRAM Output enable(s) and

the Write Enable Signal (WE* - Pin 17) should be connected to the SRAM write enable or read/write control pin. Data is driven from the CL-SM331 to the RAM Data Buffer shortly after the address is driven. The Memory Output Enable Signal (MOE* - Pin 16) and the Write Enable Signal (WE* - Pin 17) are deasserted high at the same time near the end of the cycle. The duration of the Memory Output Enable Signal (MOE* - Pin 16) and the Write Enable Signal (WE* - Pin 17) are a programmable parameter (refer to the following section on SRAM Signal timing, Section 4.3.3.3).

4.3.3.3 SRAM Signal Timing

For both a read and a write access to the RAM Data Buffer the correct address pointer (the Disk Address Pointer (Registers 57H-59H), and the Host Address Pointer (Registers 5AH-5CH)) is driven with respect to the rising edge of the SYSCLK Signal Input (Pin 24). For both read and write accesses the Memory Output Enable Signal (MOE* - Pin 16) is asserted low one-half SYSCLK after the address is driven. In the case of a write access, the Write Enable Signal (WE* - Pin 17) also starts being driven off of the falling edge of the SYSCLK Signal (Pin 24) one-half clock after the address is driven.

The Memory Output Enable Signal (MOE* - Pin 16) and the Write Enable Signal (WE* - Pin 17) in the case of a write are both deasserted high one-half SYSCLK before the end of the SRAM access. This implies that the total SRAM access time controls the pulse width of these signals. The complete SRAM access time is programmed in terms of SYSCLK Input Signal (Pin 24) periods. By programming a value into Bits 1-0, RAS* Low Time/SRAM Cycle Time, of the Buffer Manager Timing Control Register (54H) an access time of 2T to 5T (where T is the SYSCLK Signal (Pin 41) period) can be obtained.

The values of 2t, 3t, 4t, or 5t refer to the time from the rising edge of SYSCLK, that drives the address valid, to the rising edge of SYSCLK following the release of the Memory Output Enable Signal (MOE* - Pin 16) and the Write Enable Signal (WE* - Pin 17) one-half clock earlier. This yields a Memory Output Enable and Write Enable pulse width of approximately

one period less than the value programmed. The address is held one-half clock after the release of the Memory Output Enable (MOE* - Pin 16) and the Write Enable (WE* - Pin 17) signals.

In the case of a read access to the RAM Data Buffer, data is clocked into the CL-SM331 on the same falling edge of SYSCLK that causes the release of the Memory Output Enable Signal (MOE* - Pin 16). In the case of a write, data is held by the CL-SM331 until the same rising edge of SYSCLK, which removes the address. The Write Enable Signal (WE* - Pin 17) is released one-half clock earlier to write the data to the RAM Data Buffer.

The Buffer Memory Data Parity Signal (Pin 95) has the same timing output and input requirements as all of the Buffer Memory Data Bus signals (BD0-7).

In SRAM Mode, the theoretical maximum Buffer Manager throughput is 12 Mbytes/second. The actual throughput is a function of the NRZ clock frequency from the disk drive, the SRAM speed used or required, the desired host throughput, and the input SYSCLK Signal (Pin 24) frequency. In general, the actual SRAM throughput available can be derived from the SRAM access time programmed in Bits 1-0 of Register 54H. The total Buffer Manager throughput that is available can be obtained by multiplying the SYSCLK period times the number of cycles programmed; the throughput is the inverse of this value.

4.3.4 DRAM Buffer Interface Operation

When the CL-SM331 is operating in DRAM Mode, the Buffer Manager Interface can address up to 4 MByte of memory. Before programming the CL-SM331 for DRAM Operation, the refresh period, the DRAM device organization, and the DRAM timing parameters must be programmed. The CL-SM331 is configured for DRAM Operation by setting the DRAM/SRAM* Bit (Bit 0) of the Buffer Mode Control Register (53H).

4.3.4.1 DRAM Parameter Programming

The refresh period is programmed in the DRAM Refresh Period Register (55H). This is an eight-bit value that is appended to a ninth (least significant value) bit which is always preset to one. This refresh period multiplied by the SYSCLK Input period sets the time interval between automatic Refresh operations.

The CL-SM331 supports a read Address Strobe (RAS) – only refresh scheme. This scheme is supported with an on-board, nine-bit refresh counter. This counter is referred to as the Refresh Address Counter and holds the Buffer Memory row address that is to be refreshed. It is incremented after a memory refresh cycle. This counter is initialized to zero when the RST* Signal (Pin 19) is asserted low.

The Buffer Manager Timing Control Register (54H) contains the following four fields – CAS* High Time (Bits 7-6), CAS* Low Time (Bits 5-4), RAS* High Time (Bits 3-2), and RAS* Low Time (Bits 1-0). These four fields must be programmed with the specific timing characteristics of the DRAM devices used. Each of these four fields is allocated two bits. This enables each of the four DRAM timing characteristics to be programmed with one of four values. The values are integral multiples of the SYSCLK Input Signal (Pin 41) period.

The parameters that need to be programmed into these four fields are as follows: (1) the BA17/ CAS* Signal (Pin 15) high time for a DRAM Page Mode access, (2) the BA17/CAS* Signal (Pin 15) low time for a DRAM Page Mode Access, (3) the BA16/RAS* Signal (Pin 14) high or precharge time, and (4) the BA16/RAS* Signal (Pin 14) low time during a normal DRAM access. Refer to the section on the BA16/RAS* and BA17/CAS* Signal timing, Section 4.3.4.4, for more details on these parameters.

To ensure that the Buffer Manager drives the row and column address bits on the correct signal lines without any multiplexing or other external logic being required, the device organization should be programmed into the DRAM Type Field (Register 53H, Bits 2-1). The following four DRAM types are supported 64K bits, 256K bits by 1 bit or 4 bits, 1 Mbit and 4 Mbit devices.

4.3.4.2 DRAM Addressing Operation

The CL-SM331 supports 64K bytes, 256K bytes, 1 Mbytes, and 4 Mbytes DRAMs, and provides up to 4 Mbytes of address space. The following table shows how the bits from the address pointer (either the Disk Address Pointer Registers 57H-59H, or the Host Address Pointer Registers 5AH-5CH) map into the Buffer Memory Address lines BA0-10 (Pins 96-99, 1-7) for each DRAM size during row and column address time:

MEMORY SIZE		BUFFER ADDRESS LINES										
		10	9	8	7	6	5	4	3	2	1	0
64K DRAM	ROW ADDRESS	18	17	16	15	14	13	12	11	10	9	8
	COLUMN ADDRESS	10	9	8	7	6	5	4	3	2	1	0
256K DRAM	ROW ADDRESS	19	18	17	16	15	14	13	12	11	10	9
	COLUMN ADDRESS	10	9	8	7	6	5	4	3	2	1	0
1 M DRAM	ROW ADDRESS	20	19	18	17	16	15	14	13	12	11	10
	COLUMN ADDRESS	10	9	8	7	6	5	4	3	2	1	0
4 M DRAM	ROW ADDRESS	21	20	19	18	17	16	15	14	13	12	11
	COLUMN ADDRESS	10	9	8	7	6	5	4	3	2	1	0

During a refresh operation the 11-bit Refresh Address Counter is driven on the Buffer Memory Address lines BA0-10 (Pins 96-99, 1-7). Unlike SRAM Mode, for DRAM Operation the most significant bits of the Buffer Memory Address are constant for 64K bit, 256K bit and 1 Mbit devices. These upper bits are managed by the firmware and force an inherent buffer segmentation equal to the RAM device size. In the case of a 4 Mbit device, all of the Buffer Memory Address bits (Bits 21-0) can be incremented.

The concept of the Buffer Size Register (56H) masking the comparison of the high-order bits between the Host Address Pointer (Registers 5AH-5CH), and the Stop Address Pointer (Registers 5DH-5FH) is the same as described for the SRAM Mode of operation (refer to Section 4.3.3.1). The value in the Buffer Size Register (56H) determines the number of high-order address bits to mask in the comparison between the Host Address Pointer (Registers 5AH-5CH) and the Stop Address Pointer (Registers 5DH-5FH). The result of this comparison is used by the Buffer Manager to decide when to terminate the current Buffer Memory transfer. Bits are masked starting from the most significant row address bits until the request segment size is reached.

4.3.4.3 DRAM Page and Burst Mode Operation

The Buffer Manager always accesses the DRAM in Page Mode. This mode allows multiple byte accesses for each assertion of the BA16/RAS* Signal (Pin 14). To operate DRAM in Page Mode the Buffer Manager first asserts the BA16/RAS* Signal (Pin 14) followed by multiple CAS* cycles to strobe each new byte. This is the reason the CAS* timing programmed into Register 54H is the Page Mode CAS* timing rather than the single access timing. As mentioned previously, Refresh operations are Read Address Strobe (RAS) – only and are not considered Page Mode accesses.

When in DRAM Mode, the SCSI Host requests and the Sector Formatter requests for a Buffer Memory access are all Page Mode accesses in one of two forms. Setting the DRAM Burst Enable Bit (Bit 6) of the Buffer Status/Control Register (51H) forces the Buffer Manager into a memory access when four bytes are ready for transfer. This mode of operation assures the most efficient use of the DRAM devices because it uses them in their fastest access mode.

If the Host Interface has a byte ready for transfer to the RAM Data Buffer the Buffer Manager will not grant memory access cycles for the data in the host FIFO until there are at least four bytes ready for transfer. The same applies to the Sector Formatter Interface to the Buffer Manager. The Sector Formatter has an internal FIFO used to stack data that is to be read from or written to the RAM Data Buffer. The length of the data burst may be less than four bytes when the Buffer Manager is transferring the last or remaining data bytes of the requested transfer. Because DRAMs require a new RAS* cycle at each page break of the column address the Buffer Manager must stop a burst transfer on a page boundary and this could also result in a data burst of less than four bytes.

If the DRAM Burst Enable Bit (Register 51H, Bit 6) is reset then the Buffer Manager operates in a demand mode. In this mode, the Buffer Manager transfers up to four bytes to or from an interface. That is, if the SCSI Host Interface has only one byte in the internal FIFO or one byte available then that byte is transferred to or from the RAM

Data Buffer. In the interim due to requests from the Sector Formatter and/or a Refresh Operation, three bytes have been either filled or emptied from the host FIFO. The request is then recognized and granted. After the request is granted, three bytes are transferred to or from the RAM Data Buffer. Requests are granted in a rotating priority with the request for a Refresh Operation always taking precedence. Consequently, the Sector Formatter FIFO can give or receive up to four bytes and then the Host Interface FIFO will have a request granted for up to four bytes.

The Microcontroller Interface into the RAM Data Buffer has no FIFO available; consequently, only single byte requests can be transferred.

4.3.4.4 BA16/RAS* and BA17/CAS* Signal Timing

The Buffer Manager DRAM controller timing is specified in the Buffer Manager Timing Control Register (54H) as discussed in the section on DRAM parameter programming, Section 4.3.4.1. Register 54H four timing parameters yield the following BA16/RAS* Signal (Pin 14) and BA17/CAS* Signal (Pin 15) timing:

CAS* HIGH TIME — (Register 54H, Bits 7-6). This field specifies the CAS* precharge time in DRAM Page Mode access.

CAS* LOW TIME — (Register 54H, Bits 5-4). This field specifies the BA17/CAS* Signal (Pin 15) low time in a Page Mode access. In a DRAM Page Mode access, the BA17/CAS* Signal (Pin 15) low time for the very first access of the burst access is the BA16/RAS* Signal (Pin 14) low time minus one SYSCLK cycle, as in the normal access. For the subsequent accesses, however, it is specified by the BA17/CAS* Signal (Pin 15) low time -Bits 5-4 of Register 54H.

RAS* HIGH TIME — (Register 54H, Bits 3-2). This field specifies the minimum number of SYSCLK cycles that the BA16/RAS* Signal (Pin 14) is deasserted for RAS precharge.

RAS* LOW TIME — (Register 54H, Bits 1-0). This field specifies the number of SYSCLK cycles that the BA16/RAS* Signal (Pin 14) is

asserted in a normal DRAM access cycle. The BA16/RAS* Signal (Pin 14) is asserted in phase 2 (the second half) of the first SYSCLK cycle starting the access; the BA17/CAS* Signal (Pin 15) is asserted one SYSCLK cycle later. The BA16/RAS* Signal (Pin 14) and the BA17/CAS* Signal (Pin 15) are deasserted simultaneously in a normal cycle.

For read accesses of the DRAM Data Buffer, the Memory Output Enable Signal (MOE* - Pin 16) is asserted low with the first assertion of the BA17/CAS* Signal (Pin 15) regardless of

whether it is a single or multiple byte access. The Memory Output Enable Signal (MOE* - Pin 16) is deasserted high along with the last BA17/CAS* Signal (Pin 15). For DRAM write accesses to the RAM Data Buffer, the Write Enable Signal (WE* - Pin 17) is asserted low with the assertion of the BA16/RAS* Signal (Pin 14) and is deasserted high with the deassertion of the BA16/RAS* Signal (Pin 14). During a Refresh Operation neither the Memory Output Enable Signal (MOE* - Pin 16) nor the Write Enable Signal (WE* - Pin 17) is asserted low.

4.3.5 Hardware ECC Correction Vector Operation

Hardware ECC correction vectors from ECC/ENDEC IC (CL-SM330) are sent to CL-SM331 through VECTOR Signal (Pin 23), clocked by the SYSCLK Signal (Pin 24). The serial data enters CL-SM331 as a packet of 42 bits.

The Error Correction Vector Packet format is as follows:

- First 4 bits contain the Synchronization pattern 'D'H(1101B).
- The next 22 bits contain the address for Buffer Memory access (the MSB arrives first).
- After the address is the 8-bit error pattern at the packet address (the MSB arrives first).
- The last 8 bits contain the redundancy bits.

bit 0	bit 3	bit 4	bit 25	bit 26	bit 33	bit 34	bit 41
[S3 S2 ... S0]		[BA21 BA20 ... BA0]		[EP7 EP6 ... EP0]		[RED7 RED6 ... RED0]	
Synchronization Character		Buffer Memory Address		Error Pattern		Redundancy Bits	

Error Correction Vector Packet processing occurs independently of other operations in the CL-SM331. Upon the detection of Synchronization byte at VECTOR Signal (Pin 23), the VREADY Signal (Pin 22) is negated to stop CL-SM330 from starting any more packets. If the 8-bit error detection circuit verifies the data, a Read/Modify/Write access sequence of the Buffer Memory will be automatically scheduled. In this sequence, data will be read from Buffer Memory and then XORed with the 8-bit error pattern. The XORed result will be written back to Buffer Memory to complete this sequence. After verifying the redundancy bits of the Error Correction Vector Packet, the VREADY Signal (Pin 22) is asserted again to allow additional packets to be transferred.

The VERROR Signal (Pin 21) is asserted to notify CL-SM330 either the Error Detection circuit found a transmission error or the Buffer Memory parity logic detected a parity error (if Buffer Memory Parity Enable Bit, Register 53H, Bit 3 is set) on the Buffer Read during the vector processing sequence.

The following is the 8-bit polynomial for the Error Correction Vector Packet:

$$(x^8+x^7+x^2+1).$$

4.4 Sector Formatter and Format Sequencer Operation

The fourth functional logic block of the CL-SM331 is the Sector Formatter. The Sector Formatter provides the disk data and control functions. As the block diagram on the cover page indicates, the Sector Formatter is subdivided into the Format Sequencer and the Sector Formatter Data path. The Sector Formatter Operation is managed by the Format Sequencer which in turn is controlled by a user-written program. This user-written program is referred to as the Format Sequencer program and contains the control information for the disk track and sector format. This program must be loaded into the Writable Control Store (WCS) before the Format Sequencer can function properly. The Writable Control Store (WCS) consists of 124 bytes that are organized as 31 words each four bytes wide. The Format Sequencer program is then executed from the CL-SM331 Current Sequencer Word Register. Consequently, the Sector Formatter Current Sequencer Word Register actually controls the current disk operation and the disk interface output signals. Refer to Section 4.4.2 for details on the operation of the Format Sequencer.

The other main component of the Sector Formatter is the Sector Formatter Data path. The Sector Formatter Data path consists of the NRZ data handling circuitry that includes the serializer/deserializer (SERDES), the CRC error control logic, the SERDES parity logic, and the data signals to the Buffer Manager Interface. Refer to Section 4.4.1 for details on the operation of the Sector Formatter Data path.

The Sector Formatter is capable of handling NRZ Data rates up to 24 Mbits/Second. All disk data operations such as sector reads and writes, format and sector verifies are executed by one or more of these elements of the Sector Formatter.

4.4.1 Components of the Sector Formatter Data Path

The Sector Formatter Data path consists of the following seven components:

- **A serializer/deserializer (SERDES),**
- **Two eight-bit comparators,**
- **A serial synchronization detector,**
- **Comparison circuitry,**
- **Error Detection Logic,**
- **A ten-byte stack, and**
- **Buffer Memory parity logic.**

4.4.1.1 Serializer/Deserializer

Disk data is read or written from the CL-SM331 chip in a serial format. The NRZ Signal (Pin 29) provides the serial interface between the Sector Formatter Data path and the disk drive. This signal enables the CL-SM331 chip to read and write NRZ Data to and from the disk drive. The NRZ Signal (Pin 29) is the read data input signal from the disk drive when the Format Sequencer System Read Gate Signal (Pin 25) is asserted; it is the write data output signal when the Format Sequencer System Read Gate Signal (Pin 26) is asserted.

After the serial data enters the CL-SM331 it is processed through the Sector Formatter Data path Error Detection and Correction (EDAC) logic and is deserialized simultaneously by the serializer/ deserializer (SERDES). The SERDES appends a parity bit to each deserialized byte as it passes the byte on to the Buffer Manager.

Data to be written out to the disk drive is either generated by the Format Sequencer (e.g., sync bytes, ID Field bytes), or it is received from the Buffer Manager Interface in a byte-wide format with optional odd parity. The SERDES checks the parity of the deserialized byte (if parity has been enabled) and then serializes the data. Next the serialized data is passed through to the CL-SM331 NRZ Signal (Pin 29).

4.4.1.2 Eight-Bit Comparators

The Sector Formatter Data path has two eight-bit comparators that are used by the serial synchronization detector circuit, and the compare circuit. The compare circuit is not the same comparator that is used by the serial synchronization detector circuit.

The serial synchronization detector circuit uses one of the Sector Formatter comparators to search for a match between the incoming NRZ Data and the synchronization character which is 0DH (00001101B). For more details on this topic, refer to Section 4.4.1.3.

The compare circuits can use the second comparator to compare each deserialized byte received with one of the following: (1) the Data/Branch Field of the Current Sequencer Word Register, or (2) the byte received from the Buffer Memory. For more details on the comparison, refer to Section 4.4.1.4.

Both of these Sector Formatter comparators work in parallel with the Sector Formatter Data path handling of NRZ Data. Based on the results from these two eight-bit comparators the CL-SM331 makes real-time decisions.

4.4.1.3 Serial Synchronization Detector

One of the components of the Sector Formatter Data path is the serial synchronization detector circuit. The serial synchronization detector is used to synchronize the Sector Formatter with the incoming NRZ Data stream. This circuit searches for a match between the eight-bit synchronization character (0DH, 00001101B) and the incoming NRZ Data stream. When a match is detected, then the Format Sequencer logic is issued a synchronization signal. This synchronization signal enables the Format Sequencer to align itself with the incoming NRZ Data. This synchronization signal is critical because the Format Sequencer Operation is suspended until the synchronization character is found in the incoming NRZ Data stream. This synchronization signal also supplies the SERDES with the timing information that it needs to convert the incoming serial data stream to bytes. The firmware can abort the search for the

synchronization character by writing a 1FH to the Format Sequencer Start Address Register (79H). Refer to Section 4.4.2.1 for more details.

The serial synchronization detector circuit is automatically engaged when the Format Sequencer System Read Gate Signal (Pin 25) is first asserted.

4.4.1.4 Compare Circuit

The compare circuit is typically used for the Format Sequencer branch commands, and for verification of the Sector Data Field. This ability to flag specific sector or track fields for the microcontroller and then pass this information either directly or indirectly to the Format Sequencer supports special data handling and automated retry mechanisms. This comparator is not the same comparator used by the serial synchronization detector circuit. Both comparators, however, do work in parallel with the Sector Formatter Data path handling of NRZ Data.

At the beginning of a disk read or write operation the status bit for each of these compare circuits is set to the equal state. When a compare operation is performed, the status bit is updated to indicate an equal or not equal state. If the compare circuit is not used by the Format Sequencer program then the compare circuit will remain in the equal state.

In the case of a compare operation, the NRZ Read Data is compared with one of the following: (1) the Buffer Memory Data if a Sector Data Field Verify Operation has been programmed, or (2) the Current Sequencer Word Register Data/Branch Field on all bytes where the comparison was enabled (by setting the Compare Enable Bit (Writable Control Store (WCS) Control Field, Bit 1)). The status of the compare operation is available by testing the following 3 bits in Register 7AH:

- When set, Bit 0 indicates
 - COMPARE NOT EQUAL
- When set, Bit 1 indicates
 - COMPARE GREATER THAN
- When set, Bit 2 indicates
 - COMPARE LESS THAN

4.4.1.5 Ten-Byte Stack

Another component of the Sector Formatter Data path is its ten-byte, recirculating stack. If this stack is enabled during a read operation then deserialized bytes from any desired sector field can be pushed onto this stack. This storing of information enables the local microcontroller to read the information in a non-real time manner. This capability can be used for defect management or to pass the Sector Identification Field to the microcontroller.

Because it is a ten-byte stack if more than ten bytes are written to the stack only the last ten bytes are saved. The microcontroller reads this stack by reading the CL-SM331 Sector Formatter Stack Register (7FH). The microcontroller reads the data from the stack in LIFO (Last In, First Out) order. Consequently, the first microcontroller read of the Sector Formatter Stack Register (7FH) would entail the microcontroller reading the last byte that was written onto the stack. Each read of this register rotates the data in a ring fashion in the stack so that the entire stack can be read. If more than ten bytes are read from the stack then the ten bytes of data are read continuously in a circular manner. For example, if the stack is read 11 times then the stack pointer will have wrapped around to the top of the stack.

4.4.1.6 Buffer Memory Parity Logic

Buffer Memory parity is an optional error detection feature supported by the Sector Formatter Data path. This Buffer Memory parity function is enabled by setting the Buffer Memory Parity Enable Bit (Register 53H, Bit 3). For more details refer to Section 4.3.2.

4.4.1.7 Error Detection Logic

The Sector Formatter Data Path Error Detection logic includes a 8-bit CRC circuit. This circuit includes synchronization framing error protection. The Formatter Sequencer can enable the CRC circuit while it is executing the Formatter Sequencer program from the write Control Store (WCS).

The 8-bit CRC circuit in CL-SM331 is intended to protect the serial link to the CL-SM330 from transmission errors, such as may be induced by noise. The 8-bit CRC circuit is used for error detection only and is not used for error correction. Media errors are detected and decoded in the companion chip, the CL-SM330.

During a read data operation, the CRC circuit coverage includes the Synchronization byte, Sector Data bytes and the CRC redundancy.

During a write data operation, the CRC circuit generates the CRC redundancy for only the Sector Data bytes.

If a CRC error is detected after a read data operation then the Data Field CRC Error Bit (Register 7AH, Bit 3) will be set.

The following is the 8-bit CRC polynomial:

$$(x^8+x^7+x^2+1).$$

4.4.2 The Format Sequencer Operation

The second major component of the Sector Formatter is the Format Sequencer. The Format Sequencer controls the processing of serial data across the disk interface. The Format Sequencer Operation is controlled by a user-written program called the Format Sequencer program. This program controls the timing relationships between the disk interface output signals. It also monitors the disk interface input lines and based on their value it makes decisions to branch to different locations within the Format Sequencer program. The Format Sequencer program can be programmed to sequence through such types of operations as sector read, sector write, and sector verify. The Format Sequencer can also be programmed for various types of automatic retry algorithms and defect management schemes.

As the block diagram on the cover page indicates, one of the main components of the Format Sequencer is the Writable Control Store (WCS). The Writable Control Store (WCS), used to hold this Format Sequencer program, consists of 124 bytes that are organized as 31 words each four bytes wide. Each Writable Control

Store (WCS) word can be broken down into the following four eight-bit fields: (1) the Next Address Field, (2) the Control Field, (3) the Count Field, and (4) the Data/Branch Field. Refer to the description of the Writable Control Store (WCS) fields in Section 9 for details on each of these four fields. For details on the other major components of the Format Sequencer, refer to Section 4.4.3.

The track layout such as gap lengths, sector size, and sector data fill character can be flexibly defined in the Format Sequencer Writable Control Store (WCS).

The Format Sequencer is started by writing a starting address (where the Format Sequencer should start executing at) to the Format Sequencer Start Address Register (79H). The user can stop the Format Sequencer by writing the address 1FH to Register 79H. Refer to Section 4.4.2.1 for more details on the address flow of the Format Sequencer.

4.4.2.1 Format Sequencer Address Flow

The starting address (where the Format Sequencer is to begin execution) must be loaded into the Format Sequencer Start Address Register (79H). A write to Register 79H causes the four bytes at that Writable Control Store (WCS) word to be fetched from the WCS and then written into the Format Sequencer Current Sequencer Word Register. The Current Sequencer Word Register is a 32-bit register that consists of the following four eight-bit fields – the Next Address Field (9FH), the Control Field (BFH), the Count Field (DFH), and the Data/Branch Field (FFH). After the Writable Control Store (WCS) word is loaded into the Current Sequencer Word Register, it is executed. Consequently, this 32-bit Current Sequencer Word Register controls the current disk operation and the disk interface output signals.

Each time the Sector Formatter Data path reads or writes an eight-bit byte the count in the Current Sequencer Word Register Count Field is decremented by one. When this Count Field decrements past zero (to minus one or underflows), another instruction word is fetched from the Writable Control Store (WCS) and then

loaded into the Current Sequencer Word Register.

After the current instruction is executed, the source of the next address to be executed is dependent on the programmed branch command. The branch command is programmed in the Next Address Field (Bits 7-5) of the Writable Control Store (WCS), and the Alternate Branch Command Select Bit (Bit 7 of the Writable Control Store (WCS) Control Field).

The next address that the Format Sequencer should go to can be obtained from any one of the following sources: (1) the Next Address Field, or (2) the Data/Branch Field, or (3) the Branch Address Register (78H), or (4) an implied address of 1FH. (Any fetch of the Writable Control Store (WCS) address 1FH stops the Format Sequencer. Therefore, the user can stop the Format Sequencer by writing the address 1FH to the Format Sequencer Start Address Register (79H).)

4.4.2.2 Variable Sector Data Field Size

The CL-SM331 supports variable Sector Data Field sizes. The CL-SM331 uses an eight-bit Sector Data Field length counter to support this feature. When the Data Transfer Bit (Bit 0 of the Control Field of the Writable Control Store (WCS)) is set, the Count Field of the Current Sequencer Word Register is an eight-bit programmable counter. By setting the Count Field to any value from 00H to FFH a sector length of up to 256 bytes can be transferred (read from or written to the disk drive). The value of this counter should be programmed to be one less than the required sector length.

For sector sizes greater than 256 bytes there are several different methods that can be used to define the Sector Data Field size. The most direct approach is to use additional Writable Control Store (WCS) words with each word processing up to 256 bytes of the Data Field.

Another approach uses the Inhibit Data Field Carry Bit (Bit 4) in the Sector Formatter Operation Control Register (77H) and the Sector Size Counter (initialized by the value in the Sector Size Register (4EH)). In this approach

the Inhibit Data Field Carry Bit (Register 77H, Bit 4) is set before the count of the Sequencer instruction word (that has the Data Transfer Bit (Control Field, Bit 0) set) has expired. The Format Sequencer is inhibited from going on to the next Sequencer word even though the Sector Size Counter has decremented to the last byte or has generated an underflow. Consequently, another 256 bytes of data are transferred. The initial value of the Sector Size Counter should be one less than the actual number of Count Field underflows that are to be suppressed. Each inhibited Count Field underflow decrements the Sector Size Counter. The Inhibit Data Field Carry Bit (Register 77H, Bit 4) is automatically reset when the Sector Size Counter underflows.

The Sector Size Counter is automatically initialized to the sector size value programmed in Register 4EH before any Sector Data Field is processed. Therefore, the sector size needs to be written only once in an initialization routine and only the Inhibit Data Field Carry Bit (Register 77H, Bit 4) must be set for each Sector Data Field transfer.

4.4.3 Format Sequencer Components

The following are the main components of the Format Sequencer:

- **The Writable Control Store (WCS),**
- **The Current Sequencer Word Register,**
- **A Synchronization Timer,**
- **An Input Synchronization Circuit, and**
- **A Disk/Buffer Parity Circuit.**

For more information on the Writable Control Store (WCS) and the Current Sequencer Register, refer to Section 4.4.2.

4.4.3.1 Synchronization Timer

The Synchronization Timer is used to set a limit on the amount of time that the Format Sequencer is allowed to synchronize itself with the signals from the CL-SM330. This limit is programmed in the CL-SM331 Synchronization Byte-Count Limit Register (70H). The limit is specified in terms of a byte-count limit that can be from 0 to 255. Only

one value can be programmed into Register 70H. When the Synchronization Timer is activated by the Format Sequencer program, the value in Register 70H is decremented for each byte time that passes. If the value within Register 70H reaches zero a time-out occurs. The Synchronization Time-out has no direct effect on the Format Sequencer.

The Synchronization Timer can be used with two different synchronization circuits. The first circuit uses this timer when the Format Sequencer is trying to synchronize itself to the incoming NRZ Data stream. The second circuit uses this timer when the sequencer is trying to synchronize itself to the rising edge of the IDF Signal (Pin 31).

The first synchronization circuit freezes the Format Sequencer until the incoming NRZ Data stream matches the Synchronization character 0DH (00001101B). The amount of time allowed for synchronization can be limited by the Synchronization Timer. The Synchronization Timer is activated by setting the Count/ Process CRC/Start Synchronization Timer Bit (Bit 6 of the Writable Control Store (WCS) Count Field) in the instruction word with Read Gate On active (Bits 6-5 of the Writable Control Store (WCS) Control Field). If the Format Sequencer achieves synchronization before the Synchronization Timer reaches its limit, then the Format Sequencer proceeds normally. If the Synchronization Timer reaches its limit before the Format Sequencer achieves synchronization, then the Format Sequencer is immediately stopped. There is a branch command which modifies the reaction to a Synchronization Time-out. If this branch is used, then the Synchronization Time-out will cause the Format Sequencer to resume operations and fetch its next instruction using the Branch Address either specified in the Data/Branch Field (Register E0H-FEH, Bits 4-0) or the Branch Address Register (78H).

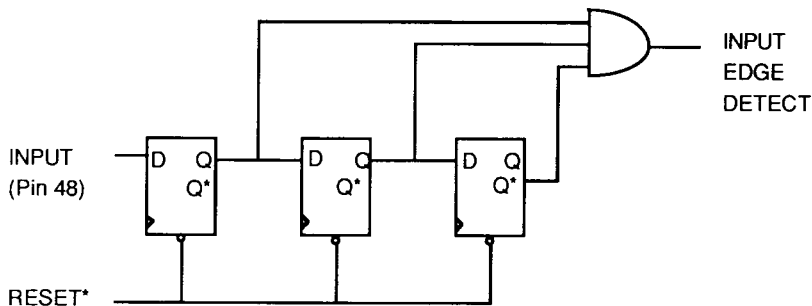
The second synchronization circuit is activated by a branch condition 011 (control field Bit 7 = 1, and RG*CRC = 0) which freezes the Sequencer Operation until the rising edge of IDF Signal (Pin 31) is detected. If the Format Sequencer achieves synchronization before the Synchronization Timer reaches its limit, then the Format Sequencer continues its flow using the

Next Address Field (Register 80H-9EH, Bits 7-5). If the Synchronization Timer reaches its limit before the Format Sequencer achieves synchronization, then the Format Sequencer continues its flow using the Branch Address either specified in the Data/Branch Field (Register E0H-FEH, Bits 4-0) or the Branch Address Register (78H).

The Synchronization Timer is reset when the RST* Signal (Pin 19) is asserted. It is automatically re-loaded from the Synchronization Byte-Count Limit Register (70H) after each use.

4.4.3.2 Input Synchronization Circuit

The Input Synchronization Timer can be used when the Format Sequencer is trying to synchronize itself to the rising edge of the IDF Signal (Pin 31). There is a branch condition 011 (control field Bit 7 = 1, and RG*CRC = 0) which freezes the Sequencer Operation until the rising edge of IDF Signal (Pin 31) is detected. During this branch the Input Synchronization circuit can detect the rising edge of the Input Signal and protect the Input Signal from the noise. The following diagram shows the implementation of the Input rising edge detection circuit:



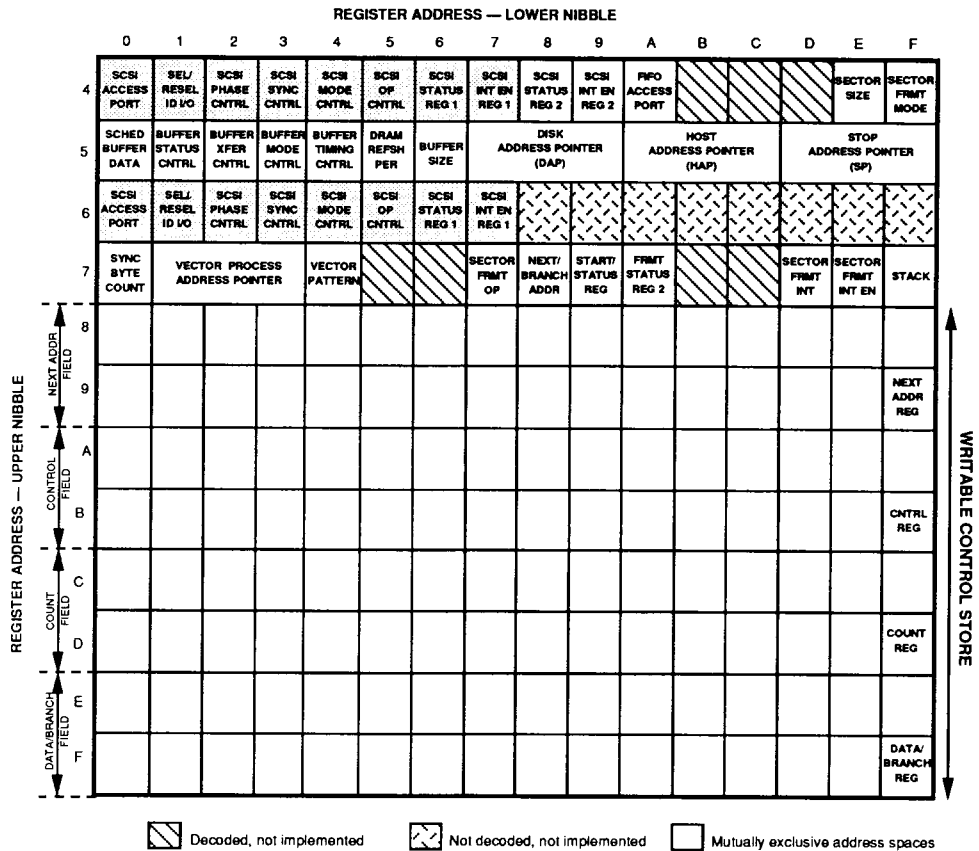
4.4.3.3 Disk/Buffer Parity Circuit

The disk/buffer parity circuit is another component of the Format Sequencer. This circuit enables the CL-SM331 to support data parity on the external RAM Data Buffer. This circuit can detect a parity error at the Sector Formatter Data path serializer/deserializer (SERDES) during either of the following operations: (1) an NRZ Write Operation, or (2) a Sector Data Verify Operation (a read of the RAM Data Buffer).

If the Buffer Memory Parity Enable Bit (Register 53H, Bit 3) is set and a parity error is detected at the serializer/deserializer (SERDES) then the Disk/Buffer Parity Error Bit (Register 7AH, Bit 6) is set. Additionally, the CL-SM331 has a branch command that can be used to stop the Format Sequencer when a disk/buffer parity error is detected. Refer to the section on RAM Data Buffer parity, Section 4.3.2, for more details.

5. REGISTER ADDRESSES AND INITIALIZATION CONDITIONS

5.1 Memory Map



5.2 Writable Control Store (WCS) Worksheet

FORMAT SEQUENCER ADDRESS	BRANCH ADDRESS REGISTER (Reg. 78H)	Microcontroller Register Addresses				DATA/ BRANCH FIELD	REG 77H BIT 1
		NEXT ADDRESS FIELD	CONTROL FIELD	COUNT FIELD			
0		80	A0	C0	E0		
1		81	A1	C1	E1		
2		82	A2	C2	E2		
3		83	A3	C3	E3		
4		84	A4	C4	E4		
5		85	A5	C5	E5		
6		86	A6	C6	E6		
7		87	A7	C7	E7		
8		88	A8	C8	E8		
9		89	A9	C9	E9		
A		8A	AA	CA	EA		
B		8B	AB	CB	EB		
C		8C	AC	CC	EC		
D		8D	AD	CD	ED		
E		8E	AE	CE	EE		
F		8F	AF	CF	EF		
10		90	B0	D0	F0		
11		91	B1	D1	F1		
12		92	B2	D2	F2		
13		93	B3	D3	F3		
14		94	B4	D4	F4		
15		95	B5	D5	F5		
16		96	B6	D6	F6		
17		97	B7	D7	F7		
18		98	B8	D8	F8		
19		99	B9	D9	F9		
1A		9A	BA	DA	FA		
1B		9B	BB	DB	FB		
1C		9C	BC	DC	FC		
1D		9D	BD	DD	FD		
1E		9E	BE	DE	FE		

BITS [0:4] = NEXT ADDRESS
 BITS [5:7]

- 0 = DATA XFER
- 1 = COMP ENBL
- 2 = OUTPUT
- 3 = INVALID NRZ
- 4 = STACK ENBL
- 6, 5 = 00 - NO CHANGE
 - 01 - WG ON
 - 10 - RG ON
 - 11 - WG OFF
- 7 = ALT BRANCH CMD5

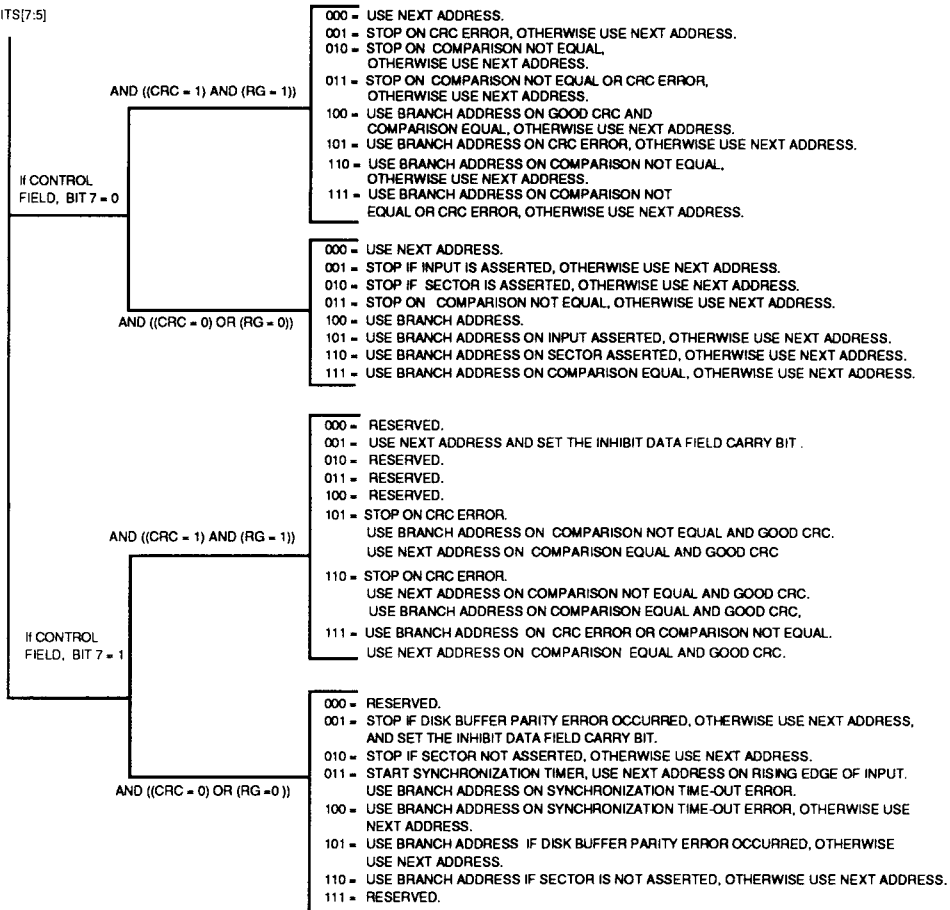
BITS [0:5] = CNT
 6 = CNT/PROCESS
 CRC/STRT SYNC
 TIMER
 7 = CNT/PROCESS AM

BITS [0:7] = DATA
 IF REG 77H, BIT 1 = 0
 BITS [0:4] = BRANCH ADDR
 IF REG 77H, BIT 1 = 1

(See Next Page)

Writable Control Store (WCS) Worksheet (cont.)

BITS[7:5]



5.3 Register Initialization

REGISTER ADDRESS	RST* (Pin 40)	SRST* (Pin 72)	REG 53H (Bit 5=1)	REG 4FH (Bit 0=1)	REG 71H (Bit 3=1)	REGISTER BIT VALUE							
						7	6	5	4	3	2	1	0
40H/60H W						X	X	X	X	X	X	X	X
41H/61H	✓	✓	✓			0	0	0	0	0	0	0	0
42H/62H	✓	✓	✓			0	0	0	0	0	0	0	0
43H/63H	✓	✓	✓			0	0	0	0	0	0	0	0
44H/64H	✓		✓			0	0	0	0	0	0	0	0
45H/65H	✓	✓	✓			0	0	0	0	0	0	0	0
46H/66H	✓		✓			X	X	0	0	0	0	0	0
46H/66H		✓				X	X	0	0	0	0	0	1
47H/67H	✓		✓			X	X	0	0	0	0	0	0
48H	✓	✓	✓			0	0	0	0	0	0	0	0
49H	✓		✓			0	0	0	0	0	0	0	0
4AH						X	X	X	X	X	X	X	X
4EH	✓					0	0	0	0	0	0	0	0
4FH	✓					0	0	0	0	0	0	0	1
50H	✓		✓			0	0	0	0	0	0	0	0
51H	✓		✓			0	0	0	0	0	0	0	0
52H	✓	✓	✓			0	0	0	0	0	0	0	0
53H	✓					1	1	1	0	0	0	0	0
54H	✓					0	0	0	0	0	0	0	0
55H	✓					0	0	0	0	0	0	0	0
56H	✓					0	0	0	0	0	0	0	0
57H	✓		✓			0	0	0	0	0	0	0	0
58H	✓		✓			0	0	0	0	0	0	0	0
59H	✓		✓			0	0	0	0	0	0	0	0
5AH	✓	✓	✓			0	0	0	0	0	0	0	0
5BH	✓	✓	✓			0	0	0	0	0	0	0	0
5CH	✓	✓	✓			0	0	0	0	0	0	0	0
5DH	✓	✓	✓			0	0	0	0	0	0	0	0
5EH	✓	✓	✓			0	0	0	0	0	0	0	0
5FH	✓	✓	✓			0	0	0	0	0	0	0	0
70H	✓					0	0	0	0	0	0	0	0
71-74H	✓					1	1	1	1	1	1	1	1
77H	✓			✓		X	X	0	0	0	0	0	X
78H R	✓			✓		X	X	X	1	1	1	1	1
W	✓			✓		X	X	X	0	0	0	0	0
79H R	✓			✓		0	0	0	0	0	0	0	0
W	✓			✓		X	X	X	0	0	0	0	0
7AH †	✓				Bits 3-0	X	0	0	0	0	0	0	0
7CH	✓					0	0	0	0	0	0	0	0
7DH	✓			✓		0	0	0	0	0	0	0	0
7EH	✓			✓		0	0	0	0	0	0	0	0
7FH R	✓			✓		X	X	X	X	X	X	X	X
W	✓			✓		0	0	0	0	0	0	0	0
9FH	✓			✓		0	0	0	1	1	1	1	1
BFH	✓			✓		0	0	0	0	0	0	0	0
DFH	✓			✓		0	0	0	0	0	0	0	0
FFH	✓			✓		0	0	0	0	0	0	0	0
80H-9EH						X	X	X	X	X	X	X	X
A0-BEH						X	X	X	X	X	X	X	X
C0-DEH						X	X	X	X	X	X	X	X
E0-FEH						X	X	X	X	X	X	X	X

NOTES: † Also reset by a write to Register 79H. X means indeterminate.

6. SCSI INTERFACE REGISTER DESCRIPTIONS

6.1 40H/60H — Direct SCSI Access Port (Read/Write)

This register has no initialization conditions.

Bits 0-7 Address 40H/60H decode allows the microcontroller direct access to the SCSI Data Bus. Data written to this address is stored and driven onto the SCSI Data Bus when the Microcontroller Direct SCSI Output Enable Bit (Register 45H/65H, Bit 3) is set. A microcontroller read of address 40H/60H reads the information directly from the SCSI Data Bus (the Microcontroller Direct SCSI Output Enable Bit (Register 45H/65H, Bit 3) must be reset for the SCSI Data Bus read).

6.2 41H/61H — Selection/Reselection ID Input (Read Only)

This register is reset when the SCSI Reset Signal (Pin 69) or the RST* Signal (Pin 19) is asserted low, or by a Host/Buffer Reset (Register 53H, Bit 5).

Bits 0-7 When the SCSI Automatic Selection/Reselection Enable Bit (Register 45H/65H, Bit 1) is set, after the CL-SM331 has been selected or reselected, this register contains the combined source and destination ID. The microcontroller should read this register after a selection/reselection of the device in order to determine the source ID.

6.3 41H/61H — Selection/Reselection ID Output (Write Only)

This register is reset when the SCSI Reset Signal (Pin 69) or the RST* Signal (Pin 19) is asserted low, or by a Host/Buffer Reset (Register 53H, Bit 5).

Bits 0-7 When the SCSI Automatic Selection/Reselection Enable Bit (Register 45H/65H, Bit 1) is set, then the contents of this register are automatically driven onto the SCSI Data Bus during a SCSI Selection/Reselection Phase after winning the SCSI Arbitration Phase. The microcontroller should write the logical OR of the source and destination SCSI ID to Register 41H/ 61H before the SCSI Selection/Reselection Phase can occur.

6.4 42H/62H — SCSI Phase Control (Read/Write)

This register is reset when the SCSI Reset Signal (Pin 69) or the RST* Signal (Pin 19) is asserted low, or by a Host/Buffer Reset (Register 53H, Bit 5).

Bit 0	SCSI Control/Data*: Writing to this bit stores a value which is driven onto the SCSI Command/Data Signal (Pin 73) when the Enable Target Bit (Register 45H/65H, Bit 4) is set, or stores the value of the expected state compared with the SCSI Command/Data Signal (Pin 73) when the Enable Initiator Bit (Register 45H/65H, Bit 5) is set. The value written is logically inverted before being driven onto the SCSI Command/Data Signal (Pin 73) in Target Mode or compared with the value on the SCSI Command/Data (Pin 73) Signal in Initiator Mode. Reading this bit provides the logically inverted value of the SCSI Command/Data Signal (Pin 73).
Bit 1	SCSI Input/Output*: Writing to this bit stores a value which is driven onto the SCSI Input/Output Signal (Pin 75) when the Enable Target Bit (Register 45H/65H, Bit 4) is set, or stores the value of the expected state compared with the SCSI Input/Output Signal (Pin 75) when the Enable Initiator Bit (Register 45H/65H, Bit 5) is set. The value written is logically inverted before being driven onto the SCSI Input/Output Signal (Pin 75) or compared with the value on the SCSI Input/Output (Pin 75) Signal. Reading this bit provides the logically inverted value of the SCSI Input/Output Signal (Pin 75).
Bit 2	SCSI Message: Writing to this bit stores a value which is driven onto the SCSI Message Signal (Pin 70) when the Enable Target Bit (Register 45H/65H, Bit 4) is set, or stores the value of the expected state compared with the SCSI Message Signal (Pin 70) when the Enable Initiator Bit (Register 45H/65H, Bit 5) is set. The value written is logically inverted before being driven onto the SCSI Message Signal (Pin 70) or compared with the value on the SCSI Message (Pin 70) Signal. Reading this bit provides the logically inverted value of the SCSI Message Signal (Pin 73).
Bit 3	SCSI Request: The value written to this bit is logically inverted and driven onto the SCSI Request Signal (Pin 74) when the Enable Target Bit (Register 45H/65H, Bit 4) is set. Reading this bit provides the logically inverted value of the SCSI Request Signal (Pin 74).
Bit 4	SCSI Busy: The value written to this bit is logically inverted and driven onto the SCSI Busy Signal (Pin 67). This bit controls the SCSI Busy Signal (Pin 67) ungated by any other signals. Reading this bit provides the logically inverted value of the SCSI Busy Signal (Pin 67).
Bit 5	SCSI Select: The value written to this bit is logically inverted and driven onto the SCSI Select Signal (Pin 72). This bit controls the SCSI Select Signal (Pin 72) ungated by any other signals. Reading this bit provides the logically inverted value of the SCSI Select Signal (Pin 72).
Bit 6	SCSI Attention: The value written to this bit is logically inverted and driven onto the SCSI Attention Signal (Pin 66) when the Enable Initiator Bit (Register 45H/65H, Bit 5) is set. Reading this bit provides the logically inverted value of the SCSI Attention Signal (Pin 66).

6.4 42H/62H — SCSI Phase Control (Read/Write) (cont.)

Bit 7 **SCSI Acknowledge:** The value written to this bit is logically inverted and driven onto the SCSI Acknowledge Signal (Pin 68) when the Enable Initiator Bit (Register 45H/65H, Bit 5) is set. Reading this bit provides the logically inverted value of the SCSI Acknowledge Signal (Pin 68).

6.5 43H/63H — SCSI Synchronous Control (Read/Write)

This register is reset when the SCSI Reset Signal (Pin 69) or the RST* Signal (Pin 19) is asserted low, or by a Host/Buffer Reset (Register 53H, Bit 5).

Bits 0-3 **Offset Count:** These four binary encoded bits set the synchronous transfer offset count. An offset count of one to 15 can be programmed for SCSI Bus synchronous transfers. An offset count of zero specifies an asynchronous transfer. Unlimited REQ/ACK offsets are not supported.

Synchronous Transfer Offset Count Table

Register 43H/63H					Register 43H/63H				
Bits					Bits				
3	2	1	0	Offset	3	2	1	0	Offset
0	0	0	0	= 0	1	0	0	0	= 8
0	0	0	1	= 1	1	0	0	1	= 9
0	0	1	0	= 2	1	0	1	0	= 10
0	0	1	1	= 3	1	0	1	1	= 11
0	1	0	0	= 4	1	1	0	0	= 12
0	1	0	1	= 5	1	1	0	1	= 13
0	1	1	0	= 6	1	1	1	0	= 14
0	1	1	1	= 7	1	1	1	1	= 15

Bits 4-7 **Synchronous Transfer Rate:** These bits, in combination with the SYSCLK clock frequency, set the SCSI Bus synchronous transfer rate. The equation for determining the synchronous transfer period is shown below.

$$t = \text{SYSCLK Period}$$

$$\text{Synchronous Transfer Period} = (P * t)$$

Synchronous Transfer Multiplier Table

Register 43H/63H					Register 43H/63H				
Bits					Bits				
7	6	5	4	P	7	6	5	4	P
0	0	0	0	= Reset State	1	0	0	0	= 9
				-RESERVED					
0	0	0	1	= RESERVED	1	0	0	1	= 10
0	0	1	0	= RESERVED	1	0	1	0	= 11
0	0	1	1	= 4	1	0	1	1	= 12
0	1	0	0	= 5	1	1	0	0	= 13
0	1	0	1	= 6	1	1	0	1	= 14
0	1	1	0	= 7	1	1	1	0	= 15
0	1	1	1	= 8	1	1	1	1	= RESERVED

6.6 44H/64H — SCSI Mode Control (Read/Write)

This register is reset when the RST* Signal (Pin 19) is asserted low, or by a Host/Buffer Reset (Register 53H, Bit 5).

Bits 0-2 **SCSI ID Bits:** These bits are the CL-SM331 encoded SCSI ID. An ID of 7 has the highest priority and an ID of 0 has the lowest.

Register 44H/64H		
Bits		
2	1	0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

SCSI ID
0
1
2
3
4
5
6
7

Bit 3 **SCSI Parity Enable:** Setting this bit enables the SCSI parity checking circuitry. The CL-SM331 always generates odd parity onto the SCSI Bus.

Bit 4 **SCSI Logic Clock Disable:** The user must program this bit to be reset. When this bit is set, the internal SCSI logic clock is disabled. It is used for test purposes.

Bits 5-7 **SCSI Logic Clock Prescalar:** These bits specify the clock used for the SCSI Phase logic. The specified clock period should be within the range of 200 ns - 400 ns.

Register 44H/64H		
Bits		
7	6	5
0	0	0
0	0	1
0	1	0
0	1	1

Register 44H/64H		
Bits		
7	6	5
1	0	0
1	0	1
1	1	0
1	1	1

=	SYSCLK/2
=	SYSCLK/4
=	SYSCLK/6
=	SYSCLK/8

=	SYSCLK/10
=	SYSCLK/12
=	SYSCLK/14
=	SYSCLK/16

6.7 45H/65H — SCSI Operation Control (Read/Write)

This register is reset when the SCSI Reset Signal (Pin 69) or the RST* Signal (Pin 19) is asserted low, or by a Host/Buffer Reset (Register 53H, Bit 5).

Bit 0	Arbitration/Selection Start: When this bit is set, the CL-SM331 will proceed to gain control of the SCSI Bus through automatic implementation of a successful SCSI Arbitration Phase. As long as arbitration is impossible due to SCSI Bus activity or a SCSI Arbitration Phase has been lost, the CL-SM331 will continue to monitor the SCSI Bus to attempt arbitration until a SCSI Arbitration Phase is won or until this bit is reset.
Bit 1	SCSI Automatic Selection/Reselection Enable: When set, this bit enables the CL-SM331 to respond automatically to being selected or reselected. Also when this bit is set, the CL-SM331 is able to proceed automatically to either a SCSI Selection or Reselection Phase after winning the SCSI Arbitration Phase. A microcontroller reset of this bit will abort the selection/reselection process.
Bit 2	SCSI Automatic Selection/Reselection Mode: If the SCSI Automatic Selection /Reselection Enable Bit (Bit 1) is set and this bit is set, the CL-SM331 will automatically proceed to a SCSI Selection Phase after arbitration is won; and if this bit is reset, the CL-SM331 will proceed to a SCSI Reselection Phase.
Bit 3	Microcontroller Direct SCSI Output Enable: When this bit is set and the Enable Target or the Enable Initiator Bit (Bit 4 and Bit 5, respectively) is set, the CL-SM331 will drive the contents of the Direct SCSI Access Port (Register 40H/60H) onto the SCSI Data Bus (Pins 54-57, 59-62). Parity will be gated onto the SCSI Data Bus Parity Signal (Pin 63).
Bit 4	Enable Target: SCSI outputs on phase and handshake signals controlled by a Target are enabled when this bit is set. This bit need only be set by the local microcontroller for firmware controlled operations, as this will be set and reset throughout real-time automatic operations under the control of the CL-SM331 logic. A SCSI Bus Free Phase will inhibit setting this bit, either the SCSI Busy Signal (Pin 67) or the SCSI Select Signal (Pin 72) must be asserted low on the SCSI Bus to allow this bit to be set.
Bit 5	Enable Initiator: SCSI outputs on control and handshake signals controlled by an Initiator are enabled when this bit is set. This bit need only be set by the local microcontroller for firmware controlled operations, as this will be set and reset throughout real-time automatic operations under the control of the CL-SM331 logic. A SCSI Bus Free Phase will inhibit setting this bit, either the SCSI Busy Signal (Pin 67) or the SCSI Select Signal (Pin 72) must be asserted low on the SCSI Bus to allow this bit to be set.
Bit 6	SCSI Active Pull-Up Select: Setting this bit enables the active pull-up on SCSI Bus signals. Resetting this bit selects open drain on all SCSI outputs except REQ* (pin 74) and ACK* (pin 68).
Bit 7	SCSI Reset Out: When this bit is set, the SCSI Reset Signal (Pin 69) will be asserted low.

6.8 46H/66H — SCSI Status Register 1 (Read/Write)

When the SCSI Reset Signal (Pin 69) is asserted low, it sets Bit 0 and resets Bits 1-5 of this register. Bits 0-5 are reset when the RST* Signal (Pin 19) is asserted low, or by a Host/Buffer Reset (Register 53H, Bit 5). Bits 0-5 must be reset by the microcontroller by writing a one to that bit, thus clearing interrupts (if enabled in Register 47H/67H and Register 4FH, Bits 1 and 6) and receiving further updated status.

Bit 0	SCSI Reset Detected: This bit reflects the SCSI Reset Signal (Pin 69) history. When this bit is set, a SCSI Reset has occurred and can still be in effect since this bit was last reset.
Bit 1	SCSI Attention Detected: This bit reflects the SCSI Attention Signal (Pin 66) history. When this bit is set, a SCSI Attention assertion has been detected and can still be in effect since this bit was last reset.
Bit 2	SCSI Offset Overrun/Underrun Detected: When this bit is set, it indicates that in SCSI synchronous transfer mode an offset overrun/ underrun was detected.
Bit 3	SCSI Bus Free Detected: When this bit is set, it indicates that a SCSI Bus Free Phase has been detected since this bit was last reset.
Bit 4	SCSI/Buffer Parity Error Detected: This bit reflects the error history for transfers from the buffer memory to the SCSI interface. When this bit is set, a parity error was detected transferring data from the buffer memory to the internal SCSI interface.
Bit 5	SCSI Bus Parity Error Detected: This bit reflects the SCSI Bus parity error history. When this bit is set, a SCSI Bus parity error was detected.
Bit 6	SCSI Parity Error: This bit reflects odd parity of the internal SCSI Bus. The user is responsible to ensure that data is stable on the internal SCSI Bus for this signal to have a valid state.
Bit 7	SCSI RST In: This bit reflects the logically inverted state of the SCSI Reset Signal (Pin 69).

6.9 47H/67H — SCSI Interrupt Enable Register 1 (Read/Write)

This register is reset when the RST* Signal (Pin 19) is asserted low or by a Host/Buffer Reset (Register 53H, Bit 5).

Bit 0	SCSI Reset Detected Enable: When this bit set, it causes the HINT Signal (Pin 33) to be asserted low when the SCSI Reset Detected Bit (Register 46H/66H, Bit 0) is set.
Bit 1	Attention Detected Enable: When this bit is set, it causes the HINT Signal (Pin 33) to be asserted low when the SCSI Attention Detected Bit (Register 46H/66H, Bit 1) is set.
Bit 2	Offset Overrun/Underrun Enable: When this bit is set, it causes the HINT Signal (Pin 33) to be asserted low when the SCSI Offset Overrun/Underrun Detected Bit (Register 46H/66H, Bit 2) is set.
Bit 3	SCSI Bus Free Detected Enable: When this bit is set, it causes the HINT Signal (Pin 33) to be asserted low when the SCSI Bus Free Detected Bit (Register 46H/66H, Bit 3) is set.
Bit 4	SCSI/Buffer Parity Error Enable: When this bit is set, it causes the HINT Signal (Pin 33) to be asserted low when the SCSI/Buffer Parity Error Detected Bit (Register 46H/66H, Bit 4) is set.
Bit 5	SCSI Bus Parity Error Enable: When this bit is set, it causes the HINT Signal (Pin 33) to be asserted low when the SCSI Bus Parity Error Detected Bit (Register 46H/66H, Bit 5) is set.
Bits 6-7	RESERVED.

6.10 48H — SCSI Status Register 2 (Read/Write)

This register is reset when the SCSI Reset Signal (Pin 69) or the RST* Signal (Pin 19) is asserted low, or by a Host/Buffer Reset (Register 53H, Bit 5). Each bit must be reset by the microcontroller by writing a one to that bit, thus clearing interrupts (if enabled in Register 49H and Register 4FH, Bits 1 and 6) and receiving further updated status.

Bit 0 **Device Selected:** When this bit is set, the CL-SM331 has answered a SCSI selection attempt since this bit was last reset. When the SCSI Automatic Selection/Reselection Enable Bit (Register 45H/65H, Bit 1) is set, the CL-SM331 will detect the combination of:

- the SCSI Select Signal (Pin 72) asserted low,
- the SCSI Busy Signal (Pin 67) deasserted high,
- the SCSI Input/Output Signal (Pin 75) deasserted high,
- the CL-SM331 SCSI ID (Register 44H/64H, Bits 0-2) is asserted on the SCSI Data Bus (Pins 54-57, 59-62),
- no more than two ID bits are asserted on the SCSI Data Bus (Pins 54- 57, 59-62),
- SCSI parity is correct (if the SCSI Parity Enable Bit (Register 44H/64H, Bit 3) is set) and
- the SCSI Reset Signal (Pin 69) is deasserted high.

The detection of the above combination will:

- set this bit (Device Selected),
- set the Enable Target Bit (Register 45H/65H, Bit 4)
- assert low the SCSI Busy Signal (Pin 69 and Register 42H/62H, Bit 4) and
- latch the SCSI Data Bus (Pins 54-57, 59-62) (accessible in the Selection/Reselection ID Input Register (41H/61H)).

Bit 1 **Device Reselected:** When this bit is set, the CL-SM331 has answered a SCSI reselection attempt since this bit was last reset. When the SCSI Automatic Selection/Reselection Enable Bit (Register 45H/65H, Bit 1) is set, the CL-SM331 will detect the combination of:

- the SCSI Select signal (Pin 72) asserted low,
- the SCSI Busy Signal (Pin 67) deasserted high,
- the SCSI Input/Output Signal (Pin 75) asserted low,
- the CL-SM331 SCSI ID (Register 44H/64H, Bits 0-2) is asserted on the SCSI Data Bus (Pins 54-57, 59-62),
- exactly two ID bits are asserted on the SCSI Data Bus (Pins 54-57, 59-62),
- SCSI parity is correct (if the SCSI Parity Enable Bit (Register 44H/64H, Bit 3) is set) and
- the SCSI Reset Signal (Pin 69) is deasserted high.

The detection of the above combination will:

- set this bit (Device Reselected),
- assert low the SCSI Busy Signal (Pin 69 and Register 42H/62H, Bit 4) until the SCSI Select Signal (Pin 72) is asserted low
- set the Enable Initiator Bit (Register 45H/65H, Bit 5) and
- latch the SCSI Data Bus (Pins 54-57, 59-62) (accessible in the Selection/Reselection ID Input Register (41H/61H)).

6.10 48H — SCSI Status Register 2 (Read/Write) (cont.)

Bit 2	Arbitration Won: When this bit is set, it indicates that a requested SCSI Arbitration Phase has been won by the CL-SM331 since this bit was last reset. If the SCSI Automatic Selection/ Reselection Enable Bit (Register 45H/65H, Bit 1) is set then the CL-SM331 will proceed to the SCSI Selection or Reselection Phase depending on the value programmed on the SCSI Automatic Selection/Reselection Mode Bit (Register 45H/65H, Bit 2).
Bit 3	Automatic Selecting/Reselecting Done: When this bit is set, it indicates that the automatic SCSI Selection/Reselection Phase is completed.
Bit 4	Transfer Done: When this bit is set, it indicates the completion of a SCSI transfer. Note that when this bit is set, it also means that the last SCSI handshake has been completed, and/or the last buffer memory cycle is completed. This is valid for DMA or Programmed I/O (PIO) transfers.
Bit 5	Transfer Halted: When this bit is set, it indicates that a SCSI transfer was halted due to either a microcontroller halt request done by resetting the DMA Start Bit (Register 52H, Bit 1) or a phase mismatch in Initiator Mode.
Bit 6	SCSI Phase Mismatch: When this bit is set, it indicates that SCSI Command/Data Signal (Pin 73), the SCSI Input/Output Signal (Pin 79), and the SCSI Message Signal (Pin 70) do not match the expected phase (Register 42H/62H, Bits 0-2) as programmed by the Initiator (the Enable Initiator Bit (Register 45H/65H, Bit 5) is set).
Bit 7	Req-On: When this bit is set, it indicates that assertion low of the SCSI Request Signal (Pin 74) has been detected since this bit was last reset. This function is enabled only when the Enable Initiator Bit (Register 45H/65H, Bit 5) is set.

6.11 49H — SCSI Interrupt Enable Register 2 (Read/Write)

This register is reset when the RST* Signal (Pin 19) is asserted low or by a Host/Buffer Reset (Register 53H, Bit 5).

Bit 0	Device Selected Enable: When this bit is set, it causes the HINT Signal (Pin 33) to be asserted low when the Device Selected Bit (Register 48H, Bit 0) is set.
Bit 1	Device Reselected Enable: When this bit is set, it causes the HINT Signal (Pin 33) to be asserted low when the Device Reselected Bit (Register 48H, Bit 1) is set.
Bit 2	Arbitration Won Enable: When this bit is set, it causes the HINT Signal (Pin 33) to be asserted low when the Arbitration Won Bit (Register 48H, Bit 2) is set.
Bit 3	Automatic Selecting/Reselecting Enable: When this bit is set, it causes the HINT Signal (Pin 33) to be asserted low when the Automatic Selecting/Reselecting Done Bit (Register 48H, Bit 3) is set.
Bit 4	Transfer Done Enable: When this bit is set, it causes the HINT Signal (Pin 33) to be asserted low when the Transfer Done Bit (Register 48H, Bit 4) is set.
Bit 5	Transfer Halted: When this bit is set, it causes the HINT Signal (Pin 33) to be asserted low when the Transfer Halted Bit (Register 48H, Bit 5) is set.
Bit 6	SCSI Phase Mismatch Enable: When this bit is set, it causes the HINT Signal (Pin 33) to be asserted low when the SCSI Phase Mismatch Bit (Register 48H, Bit 6) is set.
Bit 7	Req-On Enable: When this bit is set, it causes the HINT Signal (Pin 33) to be asserted low when the Req-On Bit (Register 48H, Bit 7) is set.

6.12 4AH — Microcontroller SCSI FIFO Access Port (Read/Write)

This register has no initialization conditions.

Bits 0-7	The register is the microcontroller SCSI FIFO access port. Writing to this address writes the microcontroller data to the FIFO, and reading this address puts the FIFO output onto the microcontroller Data Bus.
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7. BUFFER MANAGER REGISTER DESCRIPTIONS

7.1 50H — Scheduled Buffer Data (Read/Write)

This register is reset when the RST* Signal (Pin 19) is asserted low, or by a Host/Buffer Reset (Register 53H, Bit 5).

Bits 0-7 The local microcontroller uses this register to access the buffer memory (using the Disk Address Pointer). Data can be either read or written through this register. Additionally, the configuration switches on the buffer memory Data Bus are also read through this register (using the MOE Disable Bit (Register 53H, Bit 4)).

7.2 51H — Buffer Status/Control Register (Read/Write)

This register is reset when the RST* Signal (Pin 19) is asserted low, or by a Host/Buffer Reset (Register 53H, Bit 5).

Bits 0-3 **Synchronous Data Transfer Offset:** A microcontroller read of Bits 0-3 give the running synchronous offset count (Read Only).

Register 51H					Register 51H				
3	2	1	0	Current Offset	3	2	1	0	Current Offset
0	0	0	0	= 0	1	0	0	0	= 8
0	0	0	1	= 1	1	0	0	1	= 9
0	0	1	0	= 2	1	0	1	0	= 10
0	0	1	1	= 3	1	0	1	1	= 11
0	1	0	0	= 4	1	1	0	0	= 12
0	1	0	1	= 5	1	1	0	1	= 13
0	1	1	0	= 6	1	1	1	0	= 14
0	1	1	1	= 7	1	1	1	1	= 15

Bit 4 **Clear FIFO:** When this bit is set, it causes the FIFO to be cleared. This bit must be reset before any access to the FIFO is attempted.

Bit 5 **SCSI Data Set Up Select:** This bit selects the SCSI Data set-up time in asynchronous mode, referenced to the SYSCLK period, *t*.

Bit 5	SCSI Data Set-Up Time
0	<i>t</i>
1	2 <i>t</i>

NOTE: This is a logical value rather than an absolute value. See the AC parameters (Section 11.3) for specific data set-up times.

7.2 51H — Buffer Status/Control Register (Read/Write) (cont.)

Bit 6	DRAM Burst Enable: When this bit is set, it forces the Buffer Manager logic to perform disk and host DRAM page mode accesses in bursts of four (except for the last burst of the transfer). If this bit is reset, DRAM page mode accesses are issued as required depending on the host and disk transfer rates. This bit must be disabled (set to 0) when in SRAM Mode or when in Initiator Mode performing synchronous data transfers with a programmed offset, Bits 0-3, less than four.
Bit 7	Reserved for test purposes. This bit should be reset.

7.3 52H — Buffer Transfer Control (Read/Write)

This register is reset when the SCSI Reset Signal (Pin 69) or the RST* Signal (Pin 19) is asserted low, or by a Host/Buffer Reset (Register 53H, Bit 5).

Bit 0	Enable Buffer Segmentation: When this bit is set, it configures the buffer memory as 64K bytes segments on 64K bytes boundaries with the 4 MSBs of the address designating the segment.
Bit 1	DMA Start: When this bit is set, the CL-SM331 starts a DMA transfer. The direction is programmed in the SCSI R/W* Transfer Direction Bit (Bit 3). This bit is reset when (a) the transfer is completed, or (b) the CL-SM331 is in the Initiator Mode, the SCSI Phase does not match the expected phase, and the SCSI Request Signal (Pin 74) is asserted low on the SCSI Bus. A reset of this bit by the microcontroller causes a DMA halt in Target Mode only.
Bit 2	PIO Start: When this bit is set, the CL-SM331 starts transfers through the FIFO. The transfer byte count is specified by the PIO Transfer Count, Bits 4-7. This bit is reset when (a) the transfer is completed, or (b) the CL-SM331 is in the Initiator Mode, the SCSI Phase does not match the expected phase, and the SCSI Request Signal (Pin 74) is asserted low on the SCSI Bus.
Bit 3	SCSI R/W* Transfer Direction: This bit indicates the direction of information transfer on the SCSI Bus in both the Programmed I/O (PIO) and DMA transfer modes. When this bit is set, information is transferred from the CL-SM331. When this bit is reset, information is transferred to the CL-SM331.

7.3 52H — Buffer Transfer Control (Read/Write) (cont.)

Bits 4-7 **PIO Transfer Count:** The value written to these bits is the number of bytes to be transferred under Programmed I/O (PIO). A microcontroller read of these bits gives the running count of bytes to be transferred under Programmed I/O (PIO).

Register 52H					Register 52H				
Bits				PIO	Bits				PIO
7	6	5	4	Transfer Count	7	6	5	4	Transfer Count
0	0	0	0	= 0	1	0	0	0	= 8
0	0	0	1	= 1	1	0	0	1	= 9
0	0	1	0	= 2	1	0	1	0	= 10
0	0	1	1	= 3	1	0	1	1	= 11
0	1	0	0	= 4	1	1	0	0	= 12
0	1	0	1	= 5	1	1	0	1	= 13
0	1	1	0	= 6	1	1	1	0	= 14
0	1	1	1	= 7	1	1	1	1	= 15

7.4 53H — Buffer Mode Control (Read/Write)

When the RST* Signal (Pin 19) is asserted low, Bits 5-7 of this register are set and Bits 0-4 are reset.

Bit 0 **DRAM/SRAM*:** This bit selects the Buffer Manager Mode of operation. When this bit is set, the DRAM Mode is selected. When this bit is reset, the SRAM Mode is selected.

Bits 1-2 **DRAM Type:** These bits select the size of DRAM for buffer memory. The sizes supported are 64K, 256K, and 1M DRAMS as shown below:

Register 53H	
Bits	Description
2 1	
0 0	64K DRAM
0 1	256K DRAM
1 0	1M DRAM
1 1	4M DRAM

Bit 3 **Buffer Memory Parity Enable:** Setting this bit enables the buffer memory parity checking circuit on every read access of the buffer memory. The checking is enabled for buffer memory reads whether the destination is the Host SCSI port or the disk SERDES logic. The CL-SM331 generates odd parity on every buffer memory write access regardless of the state of this bit. The SCSI Bus parity value is passed through the CL-SM331 to the Buffer Data Parity Signal if the SCSI Parity Enable Bit (Register 44H/64H, Bit 3) is set; otherwise, the odd parity value from the SCSI Bus Data is generated. Odd parity is always generated from the 8-bit deserialized data from the disk.

7.4 53H — Buffer Mode Control (Read/Write) (cont.)

Bit 4 **MOE Disable:** When this bit is set, the MOE* Signal (Pin 16) in SRAM Mode and the MOE* Signal (Pin 16), the BA16/RAS* Signal (Pin 14), and the BA17/CAS* Signal (Pin 15) in DRAM Mode are disabled. This is intended to support switch reads (via the Scheduled Buffer Data Register (50H)) of the buffer memory Data Bus.

Bit 5 **Host/Buffer Reset:** Assertion of the RST* Signal (Pin 19) sets this bit and generates a hardware reset condition. When this bit is set by the microcontroller, a software reset condition is generated. Either reset stops all operations in the Buffer Manager and SCSI Host Logic. The software reset initializes Registers 40H/60H-47H/67H, 48H, 49H, 50H, 52H, and 57H-5FH. All SCSI signals are switched to a high-impedance state. The Buffer Manager signals are unaffected by a software reset.

Bits 6-7 **Wait States:** These bits select the number of wait states the Ready Signal (Pin 38) is deasserted for accessing the CL-SM331 internal registers. One wait state is defined to be 't', the period of the SYSCLK Signal (Pin 24). The Ready Signal (Pin 38) is asserted with respect to the ALE Signal (Pin 51). The number of wait states as listed below is measured from the assertion of the Read Strobe Signal (Pin 37), the Write Strobe Signal (Pin 36), or the Data Strobe Signal (Pin 37).

Register 53H	
Bits	Description
7 6	
0 0	No wait States
0 1	1-2 wait States
1 0	2-3 wait States
1 1	3-4 wait States

7.5 54H — Buffer Manager Timing Control (Read/Write)

This register is reset when the RST* Signal (Pin 19) is asserted low.

Bits 0-1 RAS* Low Time/SRAM Cycle Time: When DRAM is used, this field specifies the number of SYSCLK cycles the BA16/RAS* Signal (Pin 14) is asserted in a non-page mode DRAM access cycle. When SRAM is used, this field specifies the SRAM cycle time.

t = SYSCLK Period

RAS* Low Time, tWRL =

Bits	Bits	Bits	Bits
1 0	1 0	1 0	1 0
0 0 = 2t	0 1 = 3t	1 0 = 4t	1 1 = 5t

SRAM Buffer Access Time, tWBA =

Bits	Bits	Bits	Bits
1 0	1 0	1 0	1 0
0 0 = 2t	0 1 = 3t	1 0 = 4t	1 1 = 5t

Bits 2-3 RAS* High Time: When DRAM is used, this field specifies the minimum number of SYSCLK cycles the BA16/RAS* Signal (Pin 14) is deasserted (RAS precharge time).

t = SYSCLK Period

RAS* High Time, tWRH =

Bits	Bits	Bits	Bits
3 2	3 2	3 2	3 2
0 0 = t	0 1 = 2t	1 0 = 3t	1 1 = 4t

Bits 4-5 CAS* Low Time: When DRAM is used, this field specifies the number of SYSCLK cycles the BA17/CAS* Signal (Pin 15) is asserted in a DRAM page mode access.

t = SYSCLK Period

CAS* Low Time, tWCL =

Bits	Bits	Bits	Bits
5 4	5 4	5 4	5 4
0 0 = t	0 1 = 2t	1 0 = 3t	1 1 = 4t

Bits 6-7 CAS* High Time: When DRAM is used, this field specifies the minimum number of SYSCLK cycles the BA17/CAS* Signal (Pin 15) is deasserted in a DRAM page mode access.

t = SYSCLK Period

CAS* High Time, tWCH =

Bits	Bits	Bits	Bits
7 6	7 6	7 6	7 6
0 0 = t	0 1 = 2t	1 0 = 3t	1 1 = 4t

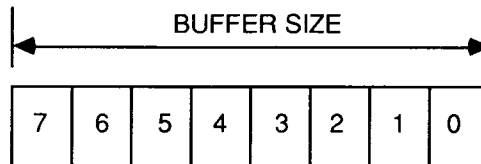
7.6 55H — DRAM Refresh Period (Read/Write)

This register is reset when the RST* Signal (Pin 19) is asserted low.

Bits 0-7 This register holds the most significant 8 bits of the 9-bit refresh period, the one least significant bit (inaccessible) is always set. The refresh period is specified in the number of SYSCLK cycles.

7.7 56H — Buffer Size (Read/Write)

This register is reset when the RST* Signal (Pin 19) is asserted low.



- 00H = 2K bytes
- 01H = 8K bytes
- 03H = 16K bytes
- 07H = 32K bytes
- 0FH = 64K bytes
- 1FH = 128K bytes
- 3FH = 256K bytes
- 7FH = 1 Mbytes
- FFH = 4 Mbytes

Bits 0-7 This register specifies the size of the physical buffer memory (in bytes) where the codes for a given buffer size are in the table above. The value programmed in this register controls the comparison of the Host Address Pointer (HAP—Registers 5AH-5CH) and the Stop Address Pointer (SAP—Registers 5DH-5FH).

7.8 57H — Disk Address Pointer Low (DAPL) (Read/Write)

This register is reset when the RST* Signal (Pin 19) is asserted low, or by a Host/Buffer Reset (Register 53H, Bit 5).

Bits 0-7	This register is the low-order byte of the buffer memory address for disk and microcontroller accesses.
----------	---

7.9 58H — Disk Address Pointer Middle (DAPM) (Read/Write)

This register is reset when the RST* Signal (Pin 19) is asserted low, or by a Host/Buffer Reset (Register 53H, Bit 5).

Bits 0-7	This register is the middle-order byte of the buffer memory address for disk and microcontroller accesses.
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7.10 59H — Disk Address Pointer High (DAPH) (Read/Write)

This register is reset when the RST* Signal (Pin 19) is asserted low, or by a Host/Buffer Reset (Register 53H, Bit 5).

Bits 0-5	These bits are the high-order byte of the buffer memory address for disk and microcontroller accesses.
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Bits 6-7	RESERVED.
----------	------------------

7.11 5AH — Host Address Pointer Low (HAPL) (Read/Write)

This register is reset when the SCSI Reset Signal (Pin 69) or the RST* Signal (Pin 19) is asserted low, or by a Host/Buffer Reset (Register 53H, Bit 5).

Bits 0-7	This register is the low-order byte of the buffer memory address for host accesses.
----------	---

7.12 5BH — Host Address Pointer Middle (HAPM) (Read/Write)

This register is reset when the SCSI Reset Signal (Pin 69) or the RST* Signal (Pin 19) is asserted low, or by a Host/Buffer Reset (Register 53H, Bit 5).

Bits 0-7	This register is the middle-order byte of the buffer memory address for host accesses.
----------	--

7.13 5CH — Host Address Pointer High (HAPH) (Read/Write)

This register is reset when the SCSI Reset Signal (Pin 69) or the RST* Signal (Pin 19) is asserted low, or by a Host/Buffer Reset (Register 53H, Bit 5).

Bits 0-5	These bits are the high-order byte of the buffer memory address for host accesses.
----------	--

Bits 6-7	RESERVED.
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7.14 5DH — Stop Address Pointer Low (SAPL) (Read/Write)

This register is reset when the SCSI Reset Signal (Pin 69) or the RST* Signal (Pin 19) is asserted low, or by a Host/Buffer Reset (Register 53H, Bit 5).

Bits 0-7	This register is the low-order byte of the Stop Address Pointer (SAP) for host accesses.
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7.15 5EH — Stop Address Pointer Middle (SAPM) (Read/Write)

This register is reset when the SCSI Reset Signal (Pin 69) or the RST* Signal (Pin 19) is asserted low, or by a Host/Buffer Reset (Register 53H, Bit 5).

Bits 0-7	This register is the middle-order byte of the Stop Address Pointer (SAP) for host accesses.
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7.16 5FH — Stop Address Pointer High (SAPH) (Read/Write)

This register is reset when the SCSI Reset Signal (Pin 69) or the RST* Signal (Pin 19) is asserted low, or by a Host/Buffer Reset (Register 53H, Bit 5).

Bits 0-5	These bits are the high-order byte of the Stop Address Pointer (SAP) for host accesses.
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Bits 6-7	RESERVED.
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8. SECTOR FORMATTER REGISTER DESCRIPTIONS

8.1 4EH — Sector Size (Read/Write)

This register is reset when the RST* Signal (Pin 19) is asserted low.

Bits 0-7	<p>Writing to this register sets the number of 256 byte data blocks to be transferred by the Format Sequencer when the Inhibit Data Field Carry Bit (Register 77H, Bit 4) is used. The value programmed should be one less than the number of underflows of the Current Sequencer Word Count Field that will be inhibited. With this register set to 00H, and the Inhibit Data Field Carry Bit (Register 77H, Bit 4) set, only one underflow of the Current Sequencer Word Count Field will be inhibited.</p> <p>For a 532-byte Data Field, set the Count Field of the Format Sequencer word to 13H, set this register to 01H, and set the Inhibit Data Field Carry Bit (Register 77H, Bit 4).</p> <p>For a 4096-byte Data Field, set the Count Field of the Format Sequencer word to FFH, set this register to 0EH, and set the Inhibit Data Field Carry Bit (Register 77H, Bit 4).</p>
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8.2 4FH — Sector Formatter Mode Control (Read/Write)

This register is reset (except for Bit 0 which will be set) when the RST* Signal (Pin 19) is asserted low.

Bit 0	Sector Formatter Reset: When the RST* Signal (Pin 19) is asserted low, this bit is set and generates a hardware Reset condition. When this bit is set by the microcontroller, a software Reset condition is generated. Either reset stops all operations in the Sector Formatter. The software Reset initializes Registers 71H-76H, 78H-7EH, 9FH, BFH, DFH, FFH, deasserts the Read Gate Signal (Pin 25), the Write Gate Signal (Pin 26), and switches the NRZ Signal (Pin 29) to a high-impedance state. The Sector Formatter will remain in the Reset condition as long as this bit is set. The Reset condition can be removed by resetting this bit. Refer to the section on register reset conditions (Section 5.3).
Bit 1	Local HINT Enable: When this bit is set, it enables local interrupt capability on the HINT Signal (Pin 33). The individual sources of interrupts can still be disabled by the Interrupt Enable Registers (Registers 47H/67H and 49H).
Bit 2	Local DINT Enable: When this bit is set, it enables local interrupt capability on the DINT Signal (Pin 32). The individual sources of interrupts can still be disabled by the Sector Formatter Interrupt Enable Register (7EH).
Bit 3	Local Int Pin Pull-Up Disable: When this bit is set, it disables the pull-up on both the HINT Signal (Pin 33) and the DINT Signal (Pin 32), leaving an open drain output. This is intended to support system-level, multiple interrupt sources.
Bit 4	SCSI Interface Register Decode Select: When this bit is set, the address space 40H-47H is decoded. When this bit is reset, the address space 60H-67H is decoded. After a Sector Formatter Reset, decode of both address spaces is disabled until this register is written.
Bit 5	Interrupt Polarity: When this bit is set, it selects active low on the interrupt pins DINT (Pin 32) and HINT (pin 33). When this bit is reset, which is the default condition, it selects active high on the interrupt pins DINT (pin 32) and HINT (pin 33). When the interrupt pins are programmed active high, it will override the open drain configuration even if the pull-ups are disabled by the Local Int Pin Pull-Up Disable Bit (Register 4F, Bit 3).
Bit 6	Local Int Mode Enable: When this bit is set, it routes both the HINT and DINT internal Signals to the DINT Signal (Pin 32) and disables any output to the HINT Signal (Pin 28).
Bit 7	RESERVED.

8.3 70H — Synchronization Byte-Count Limit (Read/Write)

This register is reset when the RST* Signal (Pin 19) is asserted low.

Bits 0-7 This register holds the byte-count limit for NRZ Read Data synchronization attempts. This value is programmable from 0 to 255. Refer to the description of the Count/Process CRC/Start Synchronization Timer(Bit 6 of the Writable Control Store (WCS) Count Field) (Section 9.3). When the timer has been activated, the value is decremented for each byte time that passes. If the value reaches zero, the Synchronization Time-Out Error Bit (Register 7AH, Bit 4) is set. Reading this register provides the running count (if the timer is active), or the programmed limit if the timer is inactive.

8.4 71H — Vector Process Address Pointer (VAPL) (Read Only)

This register is reset when the RST* Signal (Pin 19) is asserted low.

Bits 0-7 This register is the low-order byte of the buffer memory address for vector process.

8.5 72H — Vector Process Address Pointer (VAPM) (Read Only)

This register is reset when the RST* Signal (Pin 19) is asserted low.

Bits 0-7 This register is the middle-order byte of the buffer memory address for vector process.

8.6 73H — Vector Process Address Pointer (VAPH) (Read Only)

This register is reset when the RST* Signal (Pin 19) is asserted low.

Bits 0-5 This register is the high-order byte of the buffer memory address for vector process.

Bits 6-7 **RESERVED.**

8.7 74H — Vector Process Error Pattern (Read Only)

This register is reset when the RST* Signal (Pin 19) is asserted low.

Bits 0-7 This register is the error pattern for vector process.

8.8 77H — Sector Formatter Operation Control (Read/Write)

This register is reset when the RST* Signal (Pin 19) is asserted low, or by a Sector Formatter Reset (Register 4FH, Bit 0).

Bit 0	RESERVED.
Bit 1	Data/Branch Field Mode Enable: When this bit is set, the Format Sequencer uses the Data/Branch Field (Register FFH) as a source for branch addresses instead of Bits 0-4 of the Branch Address (Register 78H). When this bit is reset, the Format Sequencer uses Bits 0-4 of the Branch Address Register (78H) as a source for branch addresses. This bit does not alter the address source for branch commands that use both the Branch Address (Register 78H) and the Data/Branch Field (Register FFH) for potential address sources.
Bit 2	Suppress Transfer: When this bit is set, the buffer access mechanism of Data Transfer (Current Sequencer Word Control Field, Bit 0) is disabled. During a write operation, the NRZ Data Field will be written with the pattern of the Current Sequencer Word Data/Branch Field (Register FFH). During a read operation, the incoming NRZ Data will have CRC verified, but no data will be transferred to the buffer memory.
Bit 3	Buffer/Disk R/W* Transfer Direction: This bit indicates the direction of information transfer to/from the Sector Formatter when disk data transfer is initiated by the Sector Formatter. When this bit is reset, the data transfer direction is from the Sector Formatter to the buffer memory. When this bit is set, the data transfer direction is from the buffer memory to the Sector Formatter.
Bit 4	Inhibit Data Field Carry: When this bit is set, the Format Sequencer Byte Counter carry normally used to trigger the next fetch of a Writable Control Store (WCS) Word will be inhibited. This bit will be automatically reset whenever a carry has occurred and the Sector Size (Register 4EH) has previously been decremented to zero. This bit can be both set and reset by the Format Sequencer branch commands. When the Format Sequencer is running, writes to this register must be synchronized with the Format Sequencer activities.
Bit 5	Edge Detect Sensitivity Selection: This bit specifies which edge (rising or falling) triggers the SMDet edge detect circuit. This bit modifies the Format Sequencer branch logic, the Sector Detected (Register 7DH, Bit 0) logic. When this bit is reset, only rising edges will trigger the edge detect circuitry. When this bit is set, only falling edges will trigger the edge detect circuitry.
Bits 6-7	RESERVED.

8.9 78H — Next Format Sequencer Address (Read)

This register is reset when the RST* Signal (Pin 19) is asserted low, or by a Sector Formatter Reset (Register 4FH, Bit 0).

Bits 0-4 **Next Active Format Sequencer Address:** Bits 0-4 provide the next Writable Control Store (WCS) address to be executed by the Format Sequencer. This address could read the contents of the Format Sequencer Start Address Register (79H), or the Branch Address Register (78H), or the Current Sequencer Word Next Address Field (Register 9FH) or the Data/Branch Field (Register FFH).

Bits 5-7 **RESERVED.**

8.10 78H — Branch Address (Write)

This register is reset when the RST* Signal (Pin 19) is asserted low, or by a Sector Formatter Reset (Register 4FH, Bit 0).

Bits 0-4 **Branch Address:** The Format Sequencer jumps to the address specified in these bits when a branch condition is programmed and met.

Bits 5-7 **RESERVED.**

8.11 79H — Format Sequencer Status Register 1 (Read)

This register is reset when the RST* Signal (Pin 19) is asserted low, or by a Sector Formatter Reset (Register 4FH, Bit 0).

Bit 0	Format Sequencer Active: This bit is set while the Format Sequencer is in an active processing state.
Bit 1	AM Active: This bit is set when the Data Transfer Bit (Writable Control Store (WCS) Control Field, Bit 0) is reset and the Count/ Process AM Bit (Writable Control Store (WCS) Count Field, Bit 7) is set. It is reset after reading or writing of the ECC bytes. It is also reset when the Format Sequencer stops.
Bit 2	Data Transfer: This bit is set during data transfers between the buffer memory and the disk, that is any time the Data Transfer Bit (Writable Control Store (WCS) Control Field, Bit 0) is set even if the Suppress Transfer Bit (Register 77H, Bit 2) is set.
Bit 3	Branch Active: This bit is set when a branch condition is met. Reading this register resets this bit.
Bit 4	Synchronization Detect Status: This bit is set during a disk Read operation when the internal serializer/deserializer has been synchronized with the NRZ Read Data (a match has been found between the NRZ Read Data and the preprogrammed sync character (0DH, 00001011B)). This bit is reset on the falling (trailing) edge of the Read Gate Signal (Pin 25).
Bit 5	Format Sequencer Input: This bit indicates the status of the IDF Signal (Pin 31).
Bit 6	Format Sequencer Output: This bit indicates the status of the Output Bit (Writable Control Store (WCS) Control Field, Bit 2).
Bit 7	Byte Ready: When this bit is set, it indicates that the scheduled buffer memory access is completed, and that another scheduled buffer memory access may be started.

8.12 79H — Format Sequencer Start Address (Write)

This register is reset when the RST* Signal (Pin 19) is asserted low, or by a Sector Formatter Reset (Register 4FH, Bit 0).

Bits 0-4	Start Address: A write to this register starts the Format Sequencer at the address written to this register.
Bits 5-7	RESERVED.

8.13 7AH — Format Sequencer Status Register 2 (Read Only)

This register is reset when the RST* Signal (Pin 19) is asserted low, or by a Sector Formatter Reset (Register 4FH, Bit 0), or by a Format Sequencer start (a write to the Format Sequencer Start Address Register (79H)).

Bit 0	Compare Not Equal: This bit is set when the result of the compare operation is not equal. The comparison is performed between the NRZ Read Data and either the buffer memory data or the Data/Branch Field in the Current Sequencer Word on all bytes where comparison was enabled in the Compare Enable Bit (Writable Control Store (WCS) Control Field, Bit 1). Compare Equal is only valid after the Format Sequencer has completed processing the CRC Field. This status is reset upon a Format Sequencer start (Register 79H) or a format sequencer read operation.
Bit 1	Compare Greater Than: This bit is set when the NRZ Read Data is greater than either the buffer memory data or the Data/Branch Field in the Current Sequencer Word on the first byte where comparison was enabled in the Compare Enable Bit (Writable Control Store (WCS) Control Field, Bit 1). Compare Greater Than is only valid after the Format Sequencer has completed processing the CRC Field. This status is reset upon a Format Sequencer start (Register 79H) or a format sequencer read operation.
Bit 2	Compare Less Than: This bit is set when the NRZ Read Data is less than either the buffer memory data or the Data/Branch Field in the Current Sequencer Word on the first byte where comparison was enabled in the Compare Enable Bit (Writable Control Store (WCS) Control Field, Bit 1). Compare Less Than is only valid after the Format Sequencer has completed processing the CRC Field. This status is reset upon a Format Sequencer start (Register 79H) or a format sequencer read operation.
Bit 3	Data Field CRC Error: This bit is set after the last CRC Bit is read if there is a non-zero CRC syndrome indicating a read error in a Data Field. The read error was generated in the read transmission from the companion CL-SM330 chip. This status is reset upon a format sequencer start (Register 79H) or the start of a Format Sequencer read or write operation.
Bit 4	Synchronization Time-Out Error: This bit is set after a time-out occurs and read synchronization has not occurred. The timer limit is held in the Synchronization Byte-Count Limit (Register 70H). The timer is enabled in the Current Sequencer Word.
Bit 5	RESERVED.
Bit 6	Disk/Buffer Parity Error: This bit is set by a buffer parity error during a buffer read (disk data read by the Format Sequencer or the microcontroller) with the Buffer Memory Parity Enable Bit (Register 53H, Bit 3) set.
Bit 7	RESERVED.

8.14 7DH — Sector Formatter Interrupt (Read/Write Reset)

This register is reset when the RST* Signal (Pin 19) is asserted low, or by a Sector Formatter Reset (Register 4FH, Bit 0). Each bit must be reset by the microcontroller by writing a one to that bit, thus clearing interrupts (if enabled in Register 4FH, Bits 1 and 6, and Register 7EH), and receiving further updated status.

Bit 0	SMDet Detected: This bit is set by the edge programmed by the Edge Detect Sensitivity Selection Bit (Register 77H, Bit 5) of the SMDet Signal (Pin 18).
Bit 1	Vector Transmission Error Detected: This bit is set upon the detection of a CRC error in an Error Correction Vector Packet.
Bit 2	Input Detected: This bit is set by the edge programmed by the Edge Detect Sensitivity Bit.(Register 77, Bit 5) of the input Signal.
Bit 3	Sequencer Stopped Detected: This bit is set by the Format Sequencer cycling to the stopped condition.
Bit 4	Branch Active Detected: This bit is set by the Format Sequencer meeting a programmed branch or stop condition.
Bit 5	Data Transfer Detected: This bit is set by the Format Sequencer executing a Current Sequencer Word with Bit 0 of the Writable Control Store (WCS) Control Field set.
Bit 6	Sequencer Output Detected: This bit is set by the Format Sequencer executing a Current Sequencer Word with Bit 2 of the Writable Control Store (WCS) Control Field set.
Bit 7	Vector Parity Error: This bit is set upon the detection of a parity error in the data read from buffer memory during the vector processing sequence.

8.15 7EH — Sector Formatter Interrupt Enable (Read/Write)

This register is reset when the RST* Signal (Pin 19) is asserted low, or by a Sector Formatter Reset (Register 4FH, Bit 0).

Bit 0	SMDDET Detected Enable: When this bit is set, it enables the DINT Signal (Pin 32) to be asserted low when the SMDDET Detected Bit (Register 7DH, Bit 0) is set.
Bit 1	Vector Transmission Error Detected Enable: When this bit is set, it enables the DINT Signal (Pin 32) to be asserted low when the Vector Transmission Error Detected Bit (Register 7DH, Bit 1) is set.
Bit 2	Input Detected Enable: When this bit is set, it enables the DINT Signal (Pin 32) to be asserted low when the Input Detected Bit (Register 7DH, Bit 2) is set.
Bit 3	Sequencer Stopped Detected Enable: When this bit is set, it enables the DINT Signal (Pin 32) to be asserted low when the Sequencer Stopped Detected Bit (Register 7DH, Bit 3) is set.
Bit 4	Branch Active Detected Enable: When this bit is set, it enables the DINT Signal (Pin 32) to be asserted low when the Branch Active Detected Bit (Register 7DH, Bit 4) is set.
Bit 5	Data Transfer Detected Enable: When this bit is set, it enables the DINT Signal (Pin 32) to be asserted low when the Data Transfer Detected Bit (Register 7DH, Bit 5) is set.
Bit 6	Sequencer Output Detected Enable: When this bit is set, it enables the DINT Signal (pin 32) to be asserted low when the Sequencer Output Detected Bit (Register 7DH, Bit 6) is set.
Bit 7	Vector Parity Error Detected Enable: When this bit is set, it enables the DINT Signal (Pin 32) to be asserted low when the Vector Parity Error Detected Bit (Register 7DH, Bit 7) is set.

8.16 7FH — Sector Formatter Stack (Read Only)

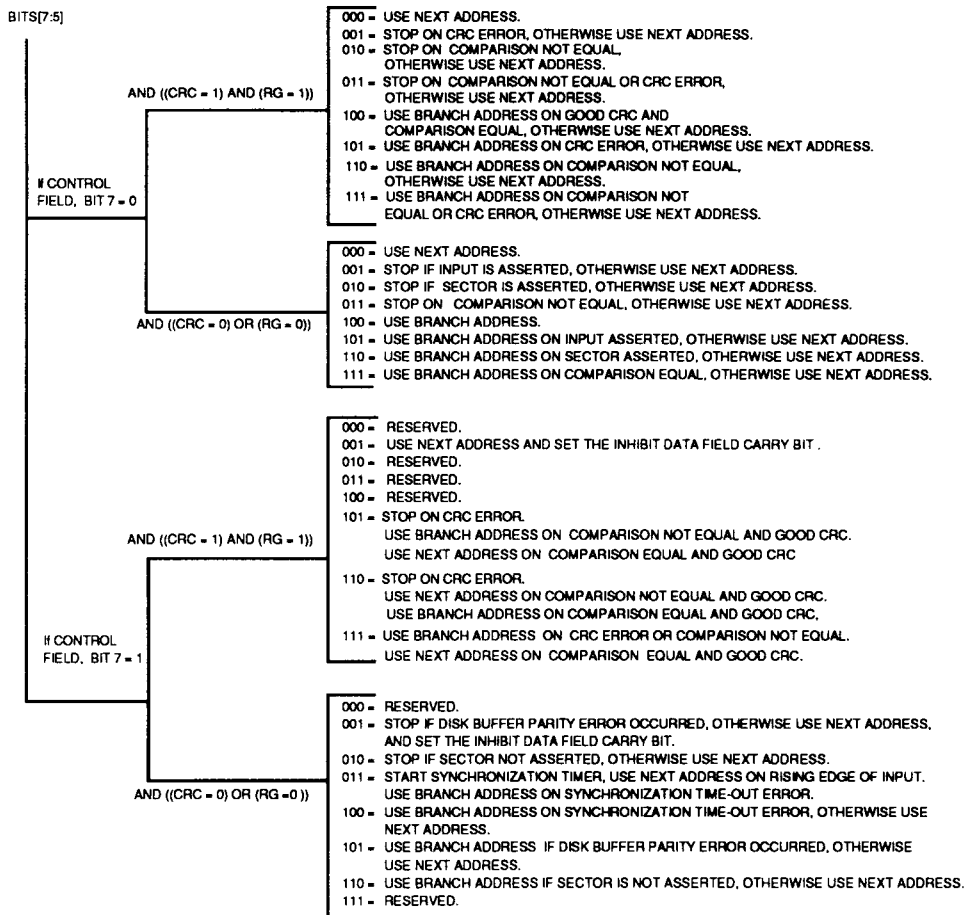
This register has no initialization conditions.

Bits 0-7	<p>The first microcontroller read of this address after a Format Sequencer operation reads the last byte that was written (enabled by the Stack Enable Bit (Bit 4) of the Writable Control Store (WCS) Control Field) onto the stack.</p> <p>Each read of this address rotates the data in a ring fashion in the stack so the entire stack can be read. The data is read in LIFO (Last In, First Out) order.</p> <p>The stack is ten bytes deep. If more than ten bytes are written to the stack only the last ten bytes are saved. If more than ten bytes are read from the stack then the ten bytes of data are read continuously in a circular manner.</p>
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9.0 WRITABLE CONTROL STORE (WCS) FIELD DESCRIPTIONS

9.1 80H-9EH — Next Address Field (Read/Write)

The Writable Control Store (WCS) has no initialization conditions.



9.1 80H-9EH — Next Address Field (Read/Write) (cont.)

Bits 0-4 **Next Address:** This is the address the Format Sequencer will go to after the down counter for the Count Field has reached zero and a branch has not been taken. There are 31 possible next address locations (00H-1EH). Fetching address 1FH stops the Format Sequencer.

Bits 5-7 **Branch Command:** All branch commands are evaluated at the end of execution of the Current Sequencer Word.

NOTE: The Branch Address can be the Branch Address Register (78H) or the Data/Branch Field unless otherwise explicitly stated.

Branch commands when the Alternate Branch Command Select Bit (Bit 7) of the Writable Control Store (WCS) Control Field is reset and all of the following conditions are true:

- the Process CRC Bit (Bit 6) of the Writable Control Store (WCS) Count Field is set and
- the Read Gate Signal (Pin 25) is asserted:

- 000 = Use the Next Address Field.
- 001 = Stop on CRC error, otherwise use the Next Address Field.
- 010 = Stop on comparison not equal, otherwise use the Next Address Field.
- 011 = Stop on comparison not equal or CRC error, otherwise use the Next Address Field.
- 100 = Use the branch Address on good CRC and comparison equal, otherwise use the Next Address Field.
- 101 = Use the branch Address on CRC error, otherwise use the Next Address Field.
- 110 = Use the Branch Address on comparison not equal, otherwise use the Next Address Field.
- 111 = Use the Branch Address on comparison not equal or CRC error, otherwise use the Next Address Field.

Branch commands when the Alternate Branch Command Select Bit (Bit 7) of the Writable Control Store (WCS) Control Field is reset and any of the following conditions are true:

- the Process CRC Bit (Bit 6) of the Writable Control Store (WCS) Count Field is reset or
- the Read Gate Signal (Pin 25) is deasserted:

- 000 = Use the Next Address Field.
 - 001 = Stop if the IDF Signal (Pin 31) is asserted, otherwise use the Next Address Field.
 - 010 = Stop if the SMDDET Signal (Pin 18) is asserted, otherwise use the Next Address Field.
 - 011 = Stop on comparison not equal, otherwise use the Next Address Field.
 - 100 = Use the branch address.
 - 101 = Use the branch address when the IDF Signal (Pin 31) is asserted, otherwise use the Next Address Field.
-

9.1 80H-9EH — Next Address Field (Read/Write) (cont.)

-
- Bits 5-7 (cont.) 110 = Use the Branch Address when the SMDDET Signal (Pin 18) is asserted, otherwise use the next Address Field.
111 = Use the Branch Address on comparison equal, otherwise use the Next Address Field.

Branch Commands when the Alternate Branch Command Select Bit (Bit 7) of the Writable Control Store (WCS) Control Field is set and all of the following conditions are true:

- the Process CRC Bit (Bit 6) of the Writable Control Store (WCS) Count Field is set and
- the Read Gate Signal (Pin 25) is asserted:

- 000 = RESERVED.
001 = Use the Next Address Field and set the Inhibit Data Field Carry Bit(Register 77H, Bit 4).
010 = RESERVED.
011 = RESERVED.
100 = RESERVED.
101 = Stop on CRC error.
Use the Branch Address on comparison not equal, and good CRC.
Use the next Address Field on comparison equal and good CRC.
110 = Stop on CRC error.
Use the next Address Field on comparison not equal and good CRC.
Use the Branch address on comparison equal and good CRC.
111 = Use the Branch Address on CRC error or comparison not equal.
Use the Next Address Field on comparison equal and good CRC.

Branch commands when the Alternate Branch Command Select Bit (Bit 7) of the Writable Control Store (WCS) Control Field is set and any of the following conditions are true:

- the Process CRC Bit (Bit 6) of the Writable Control Store (WCS) Count Field is reset or
 - the Read Gate Signal (Pin 25) is deasserted:
- 000 = RESERVED.
001 = Stop if disk buffer parity error occurred, otherwise use the next Address Field and set the Inhibit Data Field Carry Bit (Register 77H, Bit 4).
010 = Stop if the SMDDET Signal (Pin 18) is asserted, otherwise use the next Address Field.
011 = Start the synchronization timer, use the Next Address Field on the rising edge of IDF Signal (Pin 31).
Use the branch address if the Synchronization Time-Out Error Bit (Register 7DH, Bit 4) is set.
100 = Use the branch address if the Synchronization Time-Out Error Bit (Register 7DH, Bit 4) is set, otherwise use the next Address Field.
101 = Use the Branch Address if a disk buffer parity error occurred, otherwise use the next Address Field.
110 = Use the branch address if the SMDDET Signal (Pin 18) are deasserted, otherwise use the next Address Field.
111 = RESERVED.
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9.2 A0H-BEH — Control Field (Read/Write)

The WCS has no initialization conditions.

Bit 0	Data Transfer: When this bit is set, the Count Field is used as an eight-bit counter. Each byte cycle that this bit is set, a byte of data will be accessed for the serializer/deserializer from the buffer memory if the Suppress Transfer Bit (Register 77H, Bit 2) is reset, or from the Writable Control Store (WCS) Data/Branch Field if the Suppress Transfer Bit (Register 77H, Bit 2) is set. If the Write Gate Signal (Pin 26) is asserted then a byte of data is read from the appropriate source. If the Read Gate signal (Pin 25) is asserted then a byte of data is written to the buffer memory (if the Suppress Transfer Bit (Register 77H, Bit 2) is reset).
Bit 1	Compare Enable: Each byte cycle that this bit is set and the Read Gate Signal (Pin 25) is asserted then the deserialized NRZ Read Data will be compared against the Writable Control Store (WCS) Data/Branch Field or against the buffer memory data if a sector Data Field verify operation has been programmed.
Bit 2	Output: This bit is connected to the Output Signal (Pin 30) and can be used to synchronize the external circuitry or the microcontroller (through the internal interrupt circuitry, see Register 7DH, Bit 6).
Bit 3	Invalid NRZ Control: When this bit is set and the Read Gate Signal (Pin 25) is asserted, the NRZ Read Data synchronization circuit is prevented from starting.
Bit 4	Stack Enable: When this bit is set, read data is pushed onto the ten-byte recirculating stack.

9.2 A0H-BEH — Control Field (Read/Write) (cont.)

Bits 5-6 **Control Field:** Bits 5-6 are encoded as follows:

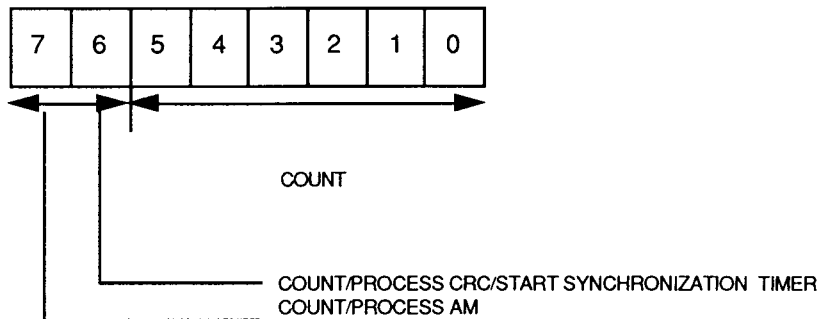
Encoded Control Field Bits 5-6

Bit 6	Control Field		DESCRIPTION
	Bit 5	CODED AS	
0	0	No Change	The state of the Write Gate Signal (Pin 26) and the Read Gate Signal (Pin 25) is not affected.
0	1	Write Gate-On	This code is used to assert the Write Gate Signal (Pin 26). The Write Gate Signal (Pin 26) is asserted during the first count of the execution of the Format Sequencer word with this bit combination set. The Write Gate Signal (Pin 26) is not asserted if the Read Gate Signal (Pin 25) is asserted when this bit combination is executed.
1	0	Read Gate-On	This code is used to assert the Read Gate Signal (Pin 25). The Read Gate Signal (Pin 25) is asserted during the first count of the execution of the Format Sequencer word with this bit combination set. The Read Gate Signal (Pin 25) is not asserted if the Write Gate Signal (Pin 26) is asserted when this bit combination is executed. The Read Gate Signal (Pin 25) is deasserted at the end of CRC processing, or when the Format Sequencer goes to the stopped state.
1	1	Write Gate-Off	This code is used to deassert the Write Gate Signal (Pin 26). The Write Gate Signal (Pin 26) is cleared during the last count of the execution of the Format Sequencer word with this bit combination set. The Write Gate Signal (Pin 26) is also deasserted when the Format Sequencer comes to the stop state.

Bit 7 **Alternate Branch Command Select:** When this bit is set, the branch conditions in the Next Address Field are redefined as described in Section 9.1).

9.3 C0H-DEH — Count Field (Read/Write)

This is the Count Field of the Writable Control Store (WCS) word. This sets the initial value of the Sequencer Counter when a new state is entered. The WCS has no initialization conditions.



Bits 0-5 **Count:** These bits are always used for the initial value of the low-order bits of the Format Sequencer Byte Counter for the execution of the Current Sequencer Word. The counter is decremented each byte time. When it reaches zero, a new Format Sequencer word will be fetched from the Writable Control Store (WCS). The byte counter is used in three modes of operation where unused bits are used as special control bits.

Bit 6 **Count/Process CRC/Start Synchronization Timer:** This bit is used for three functions.

Count: In this mode, this bit is used for the initial value of the Format Sequencer Byte Counter for the execution of the Current Sequencer Word. This mode is selected when the Data Transfer Bit (Bit 0 of the Writable Control Store (WCS) Control Field) is set.

Process CRC: When this bit is set, the Format Sequencer will process the current NRZ Data as the CRC Field. In a write operation, the generated remainder is appended to the outgoing NRZ Data stream. In a read operation, the circuit is set up to evaluate the recomputed remainder for a zero syndrome. This mode is selected when the Data Transfer Bit (Bit 0 of the Writable Control Store (WCS) Control Field) is reset, and the Read Gate-On Bit code is not set.

Start Synchronization Timer: In this mode, this bit is used to reset and start the Synchronization Timer. This counter is used to limit the amount of time that the Format Sequencer will wait for synchronization with the NRZ Read Data. The Synchronization Byte-Count Limit (Register 70H) holds a limit for the counter. If the count limit is exhausted, the current read operation will be aborted (the Format Sequencer stopped) and the Synchronization Time-Out Error Bit (Register 7AH, Bit 4) will be set. This mode is selected when the Read Gate-On Bit code (Bit 5 reset and Bit 6 set of the Writable Control Store (WCS) Control Field) is set, and the Data Transfer Bit (Bit 0 of the Writable Control Store (WCS) Control Field) is reset.

9.3 C0H-DEH — Count Field (Read/Write) (cont.)

Bit 7 **Count/Process AM:** This bit is used for two functions.

Count: In this mode, this bit is used for the initial value of the Format Sequencer Byte Counter for the execution of the Current Sequencer Word. This mode is selected when the Data Transfer Bit (Bit 0 of the Writable Control Store (WCS) Control Field) is set.

Process AM: When this bit is set, the AM Active Bit (Register 79H, Bit 1) will be set. This mode is selected when the Data Transfer Bit (Bit 0 of the Writable Control Store (WCS) Control Field) is reset.

9.4 E0H-FEH — Data/Branch Field (Read/Write)

Bits 0-7 This field has two functions.

In any mode, the Data/Branch Field is used for data. This register is the source for all overhead bytes (bytes without the Data Transfer Bit (Control Field, Bit 0) set) of data used by the device during write operations. During read operations, it is one of the operands to the comparison logic. When the Data Transfer Bit (Control Field, Bit 0) is set with the Write Gate Signal (Pin 44) asserted, the source for write data will be the external buffer. When the Suppress Transfer Bit (Register 77H, Bit 2) is set with the Write Gate Signal (Pin 26) asserted, the source for Write Data will be the contents of this register.

When the Data/Branch Field Enable Bit (Register 77H, Bit 1) is set, Bits 0-4 will be used as the branch address if a branch command is programmed and the condition is met.

NOTE: This option provides the Format Sequencer programmer with an extremely flexible branch addressing option. However, if a branch command is programmed in the same Format Sequencer word that uses the Writable Control Store (WCS) Data/Branch Field then the contents of this field must be appropriate for both uses. This dual use is improbable, and the problem should be avoided.

10.0 SEQUENCER REGISTER DESCRIPTIONS

These registers contain the value of the currently executing Writable Control Store (WCS) word.

10.1 9FH — Current Sequencer Word — Next Address Field (Read/Write)

This register is set when the RST* Signal (Pin 19) is asserted low, or by a Sector Formatter Reset (Register 4FH, Bit 0).

10.2 BFH — Current Sequencer Word — Control Field (Read/Write)

This register is reset when the RST* Signal (Pin 19) is asserted low, or by a Sector Formatter Reset (Register 4FH, Bit 0).

10.3 DFH — Current Sequencer Word — Count Field (Read/Write)

This register is reset when the RST* Signal (Pin 19) is asserted low, or by a Sector Formatter Reset (Register 4FH, Bit 0).

10.4 FFH — Current Sequencer Word — Data/Branch Field (Read/Write)

This register is reset when the RST* Signal (Pin 19) is asserted low, or by a Sector Formatter Reset (Register 4FH, Bit 0).

11. ELECTRICAL SPECIFICATION

11.1 Absolute Maximum Ratings

Ambient Temperature Under Bias.....	0° C to 70° C
Storage Temperature	- 65° C to 150° C
Voltage On Any Pin With Respect To Ground....	GND - 0.5 to V _{CC} + 0.5 Volts
Power Dissipation.....	0.500 Watt
Power Supply Voltage.....	7 Volts

NOTE:

Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

11.2 DC Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V _{CC}	Power Supply Voltage	4.75	5.25	Vdc	Operating
V _{IL}	Input Low Voltage	-0.5	0.8	Vdc	
V _{IH}	Input High Voltage	2.0	V _{CC} + 0.5	Vdc	
V _{OL} ^{1,3}	Output Low Voltage		0.4	Vdc	I _{OL} = 2 mA
V _{OL} ²	Output Low Voltage		0.5	Vdc	I _{OL} = 48 mA
V _{OH} ¹	Output High Voltage	2.4		Vdc	I _{OH} = -400 μA
I _{CC}	Supply Current		50	mA	Operating
I _L	Input Leakage	-10	10	μA	0 < V _{IN} < V _{CC}
I _{/OL}	I/O Leakage Current	-10	10	μA	0 < V _{IN} < V _{CC}
C _{IN}	Input Capacitance		10	pF	
C _{OUT}	Output Capacitance		10	pF	

NOTES:

- 1) All output pins except for the SCSI bus signals.
- 2) All SCSI bus output or I/O signals.
- 3) I_{OL} = 4 mA for the READ GATE signal (Pin 43) and the WRITE GATE signal (Pin 44).
- 4) All unused inputs must be tied to the inactive state to GND or V_{CC} appropriately.

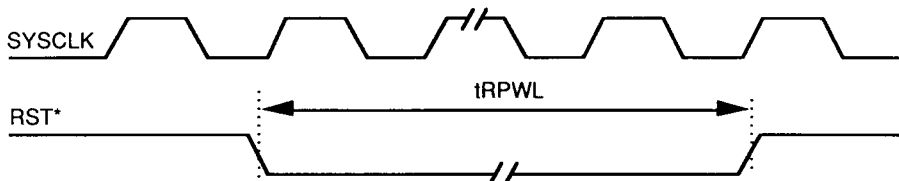
11.3 AC Characteristics

Unless otherwise specified the following timings are operating under the assumption that all non-SCSI outputs will drive one Schottky TTL load in parallel with 50 pF and all inputs are at TTL level. The MIN and MAX timings are conforming to the operating ranges of power supply voltage of 5V +/-5% and ambient temperature of 0° C to 70° C. The rise and fall times for clock signals should be kept at or below 15% of the clock period.

11.3.1 RESET Assertion Timing Parameters

SYMBOL	PARAMETER	MIN	MAX	UNITS
tRPWL	RST* pulse width low	500		ns

11.3.1.1 RESET Assertion Timing

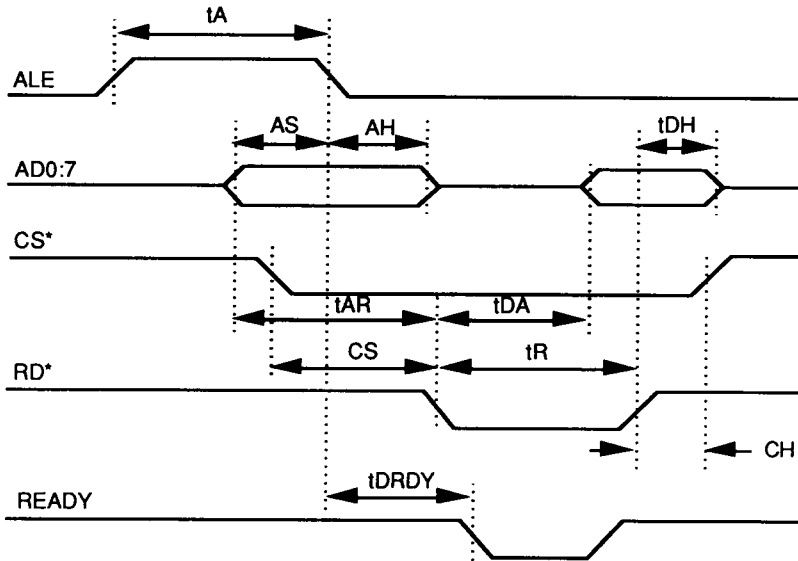


11.3.2 Microcontroller Interface Timing Parameters

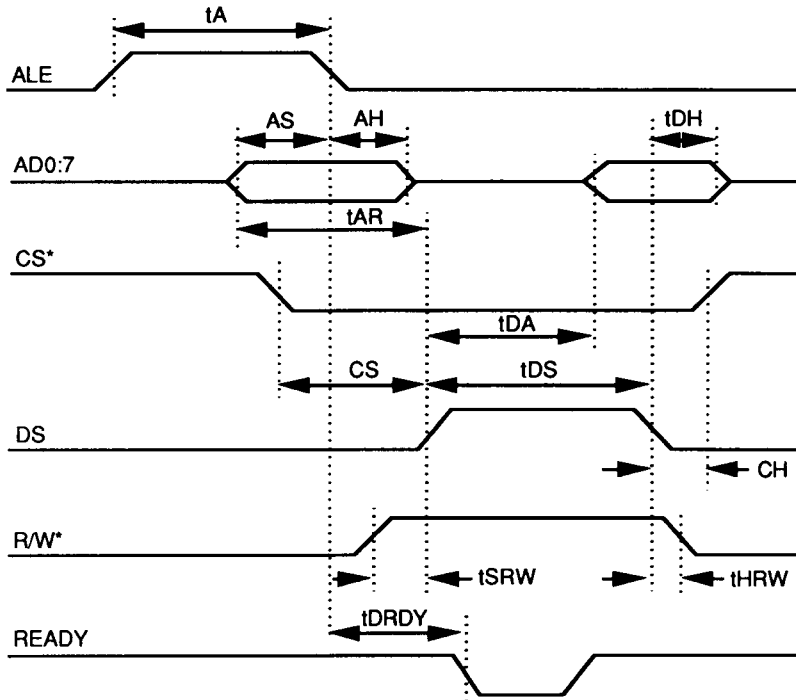
SYMBOL	PARAMETER	MIN	MAX	UNITS
tA	ALE width	20		ns
tAW	Address valid to WR* ↓ or DS ↑	30		ns
tAR	Address valid to RD* ↓ or DS ↑	20		ns
tW	WR* width	120		ns
tR	RD* width	120		ns
AS	Address valid to ALE ↓	5		ns
AH	ALE ↓ to address invalid	12		ns
CS	CS ↑ to RD* ↓ WR* ↓ or DS ↑	20		ns
CH	RD* ↓, WR* ↑ or DS ↓ to CS ↓	5		ns
WDS	Write data valid to WR* ↑ or to DS ↓	55		ns
WDH	WR* ↑ or DS ↓ to Write data invalid	10		ns
tDA	RD* ↓ or DS ↑ to Read data valid		100	ns
tDH	RD* ↑ or DS ↓ to Read data invalid	10		ns
tDZ	RD* ↑ or DS ↓ to Read data undriven		50	ns
tDS	DS width	120		ns
tDRDY	ALE ↓ to READY valid		40	ns
tSRW	R/W* valid to DS ↑	30		ns
tHRW	DS ↓ to R/W* invalid	20		ns

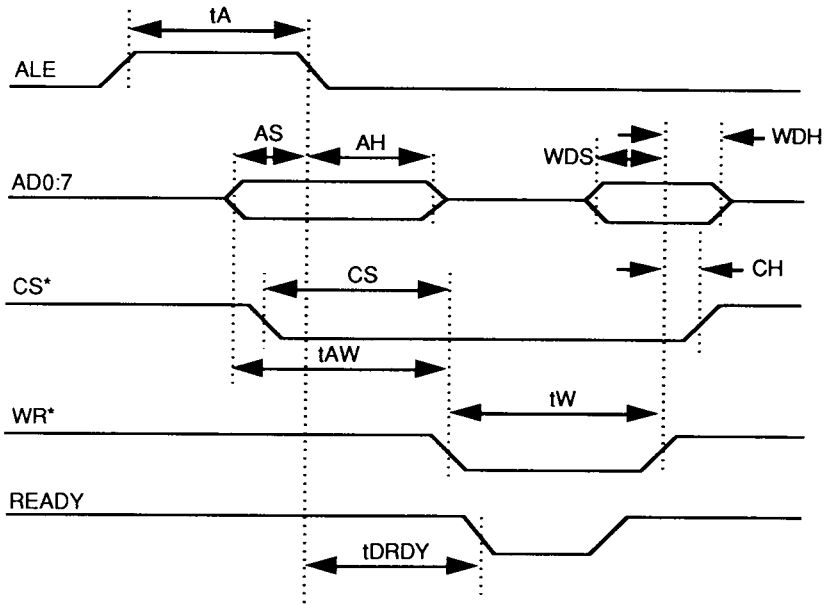
NOTES:

- 1) ↑ dicates rising edge. ↓ indicates falling edge.
- 2) When the I/MC* signal (Pin 24) is asserted high, the Intel bus control interface is selected. The timing diagram in Sections 11.3.2.1 and 11.3.2.3 depict a register read and write respectively with this interface selected.
- 3) When the I/MC* signal (Pin 24) is deasserted low, the Motorola bus control interface is selected. The timing diagrams in Section 11.3.2.2 and 11.3.2.4 depict a register read and write respectively with this interface selected.

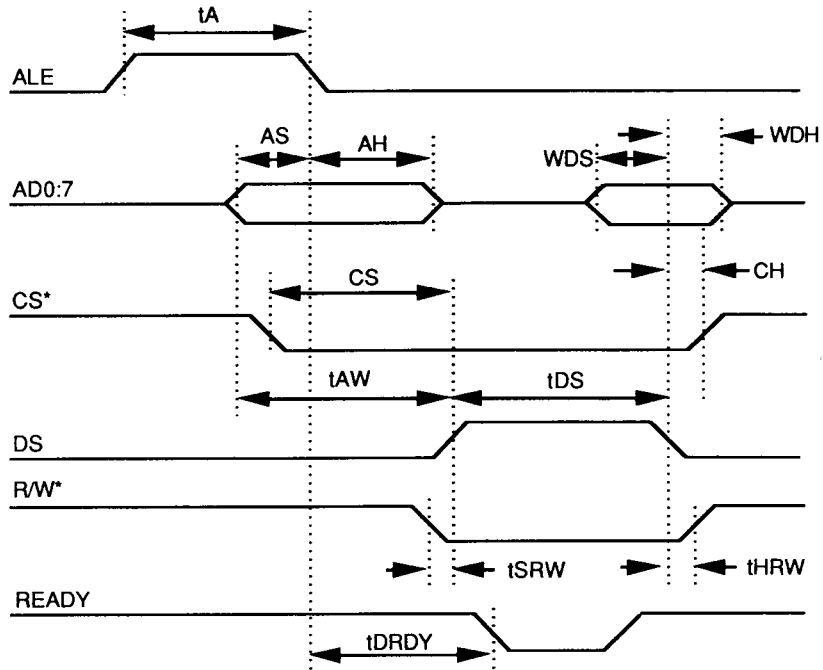
11.3.2.1 Register Read Operation in Intel Mode (AC2)


11.3.2.2 Register Read Operation in Motorola Mode (AC3)



11.3.2.3 Register Write Operation in Intel Mode (AC4)


11.3.2.4 Register Write Operation in Motorola Mode (AC5)

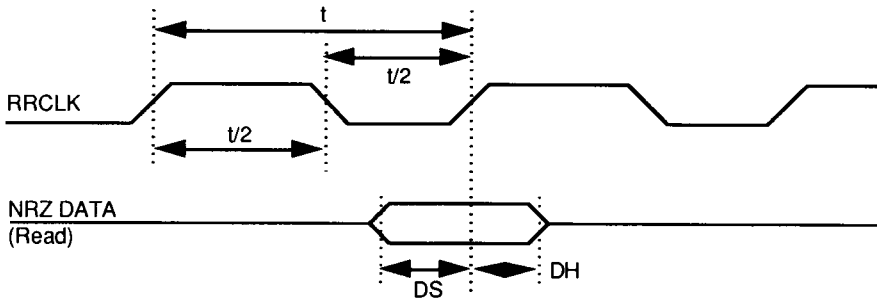
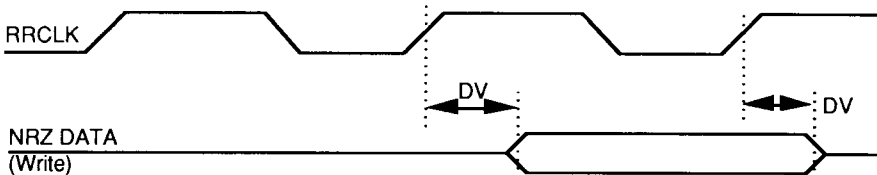


11.3.3 Disk Read/Write Timing Parameters

SYMBOL	PARAMETER	MIN	MAX	UNITS
t	RRCLK period	41		ns
t/2	RRCLK high/low time	16		ns
DS	NRZ in valid to RRCLK ↑	10		ns
DH	RRCLK ↑ to NRZ in invalid	5		ns
DV	RRCLK ↑ to NRZ out	10	25	ns

NOTES:

- 1) ↑ indicates rising edge.
- 2) ↓ indicates falling edge.

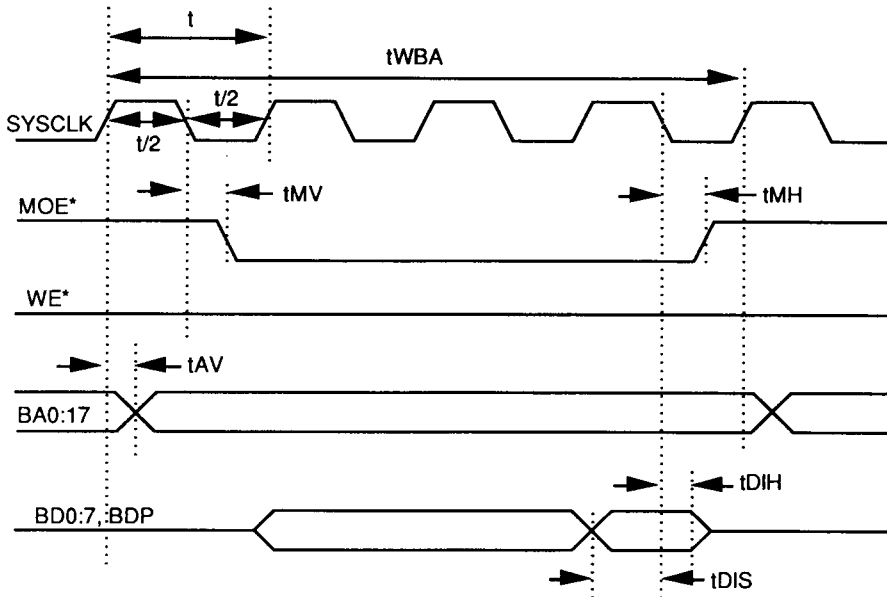
11.3.3.1 Disk Read Timing (AC7)

11.3.3.2 Disk Write Timing (AC8)


11.3.4 Buffer Memory Read/Write Timing Parameters

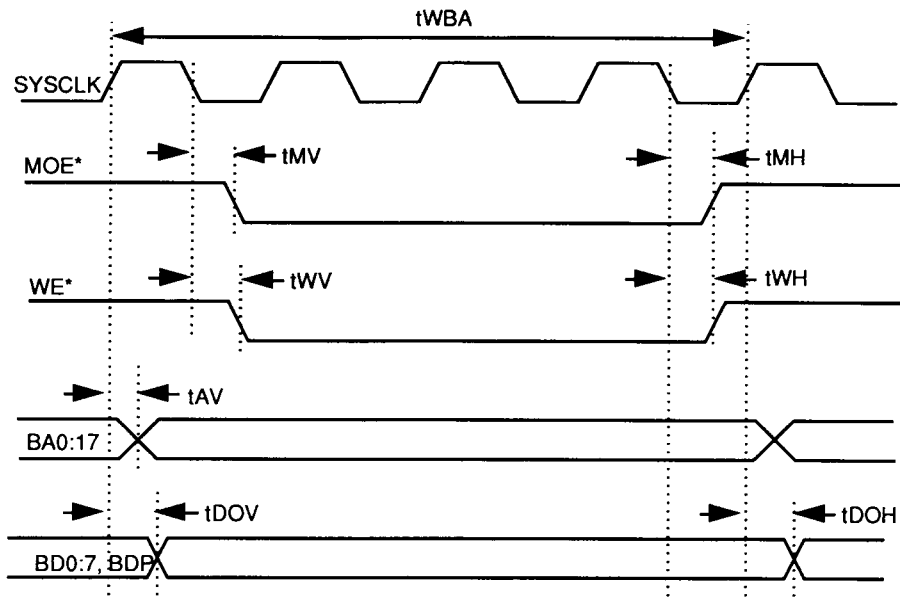
SYMBOL	PARAMETER	MIN	MAX	UNITS
t	SYSClk period	40		ns
t/2	SYSClk high/low time	16		ns
tAV	SYSClk ↑ to address valid		30	ns
tMV	SYSClk ↓ to MOE* ↓		30	ns
tMH	SYSClk ↓ to MOE* ↑		30	ns
tWV	SYSClk ↓ to WE* ↓		30	ns
tWH	SYSClk ↓ to WE* ↑		30	ns
tDOV	SYSClk ↑ to data out valid		40	ns
tDOH	SYSClk ↑ to data out invalid	0		ns
tDIS	Data in valid to SYSClk ↓	5		ns
tDIH	SYSClk ↓ to data in invalid	20		ns
tRV	SYSClk ↓ to RAS* ↓		30	ns
tRH	SYSClk ↓ to RAS* ↑		30	ns
tRAV	SYSClk ↑ to row address valid		30	ns
tRAH	SYSClk ↑ to row address invalid		30	ns
tCV	SYSClk ↓ to CAS* ↓		30	ns
tCH	SYSClk ↓ to CAS* ↑		30	ns
tCAV	SYSClk ↑ to column address valid		30	ns
tCAH	CAS* ↓ to column address invalid	(2)		

NOTES:

- 1) ↑ indicates rising edge. ↓ indicates falling edge.
- 2) Column address remains valid throughout CAS* low time.

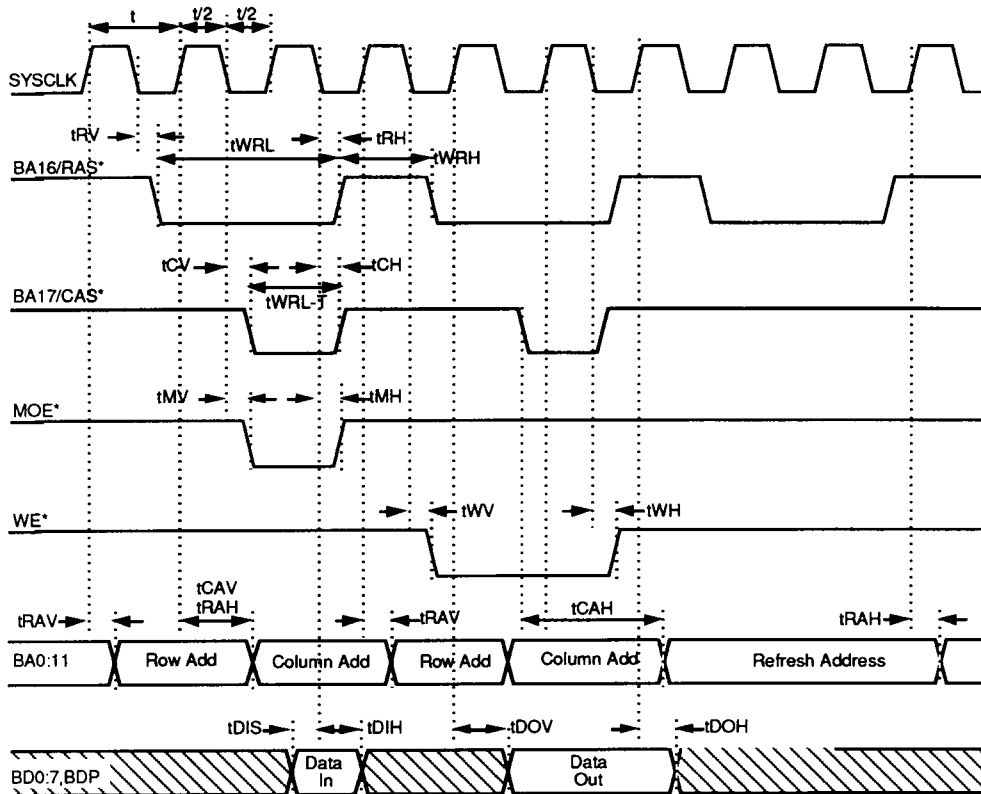
11.3.4.1 SRAM Read Timing (AC10)


11.3.4.2 SRAM Write Timing (AC11)



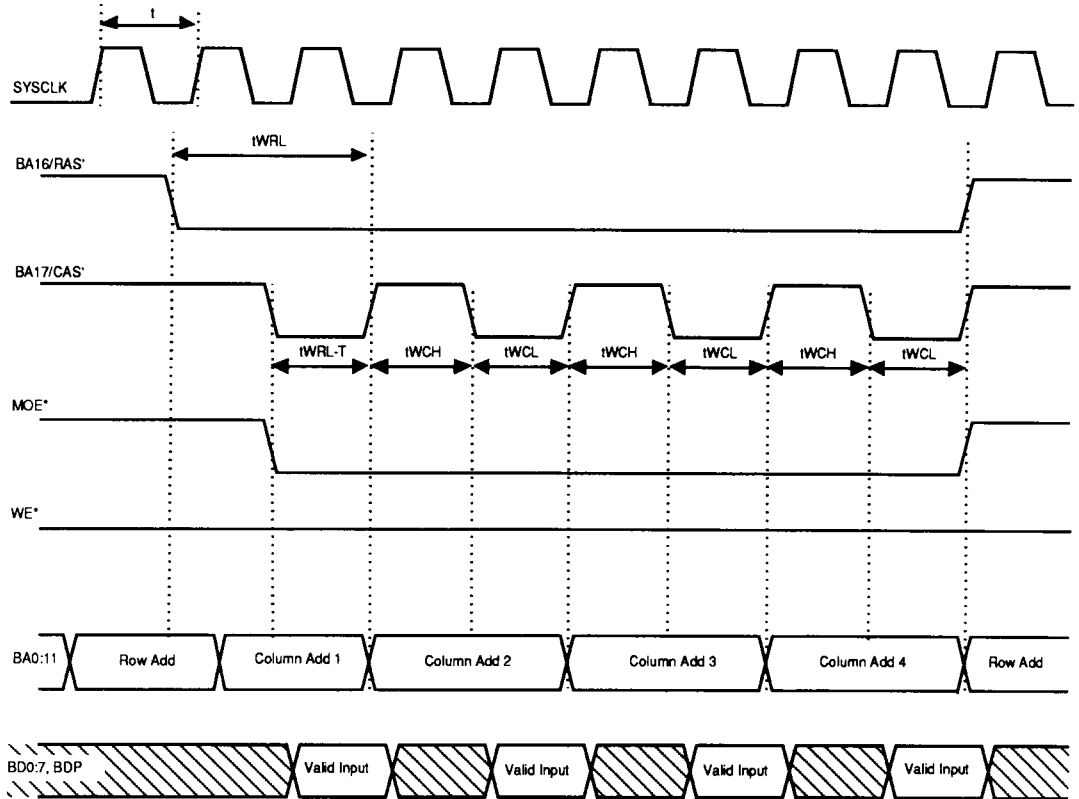
NOTE:

$tWBA$ is a functional parameter that gives the duration of one RAM data buffer access cycle in SYSCLK periods. The value is programmed in Bits 1-0 of Register 54H. These examples show $tWBA = 4t$.

11.3.4.3 Normal DRAM Read, Write, and Refresh Cycles (AC12)

NOTES:

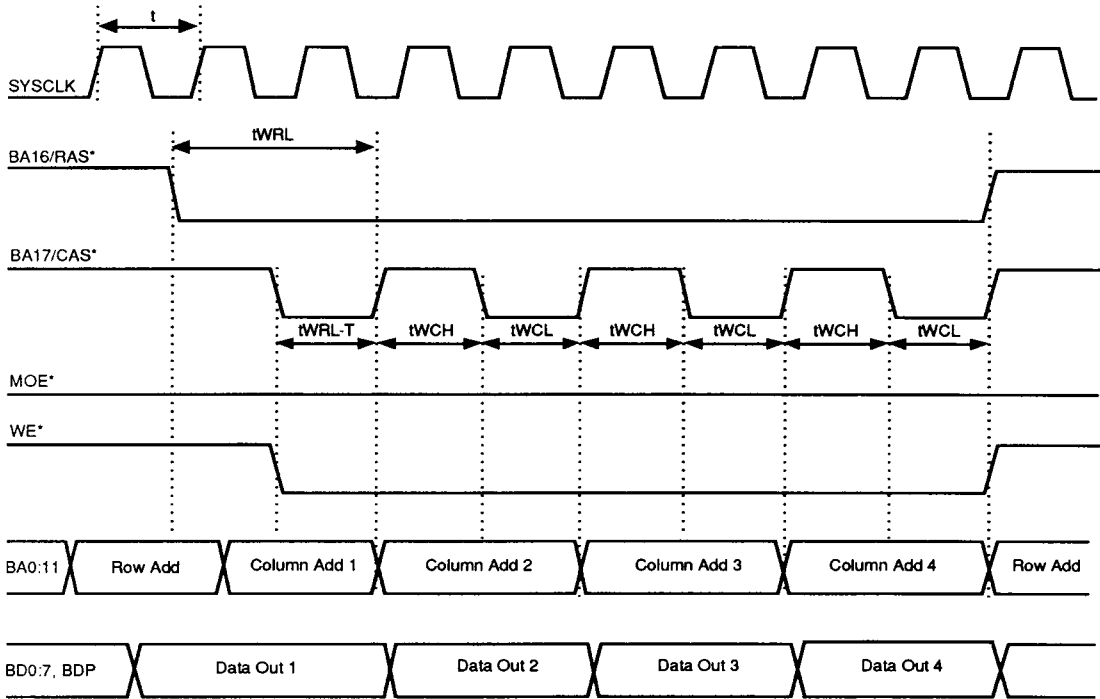
- 1) t_{WRL} and t_{WRH} are functional parameters that specify the duration of the BA16/RAS* signal (Pin 14) width low and the BA16/RAS* signal (Pin 14) width high (in SYSCLK periods) for a normal RAM data buffer access cycle. These values are programmed in Bits 3 - 0 of Register 54H. This example shows values of $t_{WRL}=2$ and $t_{WRH}=1$.
- 2) The BA17/CAS* signal (Pin 5) is asserted low one SYSCLK cycle after the BA16/RAS* signal (Pin 14) is asserted low. The BA17/CAS* signal (Pin 5) is deasserted high when the BA16/RAS* signal (Pin 14) is deasserted high.
- 3) The MOE* signal (Pin 15) is asserted low and deasserted high along with the BA17/CAS* signal (Pin 5) in a Read access. The MOE* signal (Pin 15) is deasserted high throughout Write and Refresh cycles.
- 4) A Write cycle is always an early Write cycle. The WE* signal (Pin 16) is asserted low and deasserted high along with the BA16/RAS* signal (Pin 14). Data out is valid by the falling (leading) edge of the BA17/CAS* signal (Pin 5) and is held valid while the BA17/CAS* signal (Pin 5) is asserted low.

11.3.4.4 Page Mode DRAM Read Cycle (ACB3)



NOTES:

- 1) $t_{WRL} = 2$, $t_{WRH} = 1$, $t_{WCL} = 1$, $t_{WCH} = 1$.
- 2) This is only a functional timing diagram and does not depict AC-tested parameters.

11.3.4.5 Page Mode DRAM Write Cycle (ACB4)

NOTES:

- 1) $tWRL = 2$, $tWRH = 1$, $tWCL = 1$, $tWCH = 1$.
- 2) This is only a functional timing diagram and does not depict AC-tested parameters.

11.3.5 SCSI Arbitration Timing Parameters

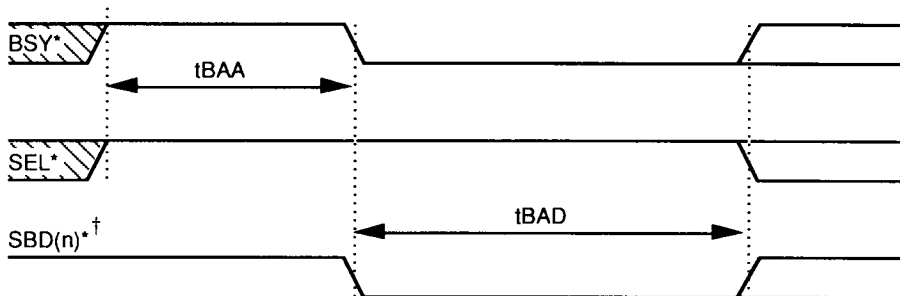
SYMBOL	PARAMETER	MIN	MAX	UNITS
tBAA	BSY* and SDB(n)* assertion delay from bus free detected		7ts + 40††	ns
tBAD	Bus arbitration assertion or deassertion delay		12ts + 40††	ns

NOTES:

† The CL-SH350 SCSI ID signal asserted on the SCSI data bus for arbitration.

†† ts is the SCSI clock period, a function of SYSCLK as defined in Register 44H/64H, Bits 5-7.

11.3.5.1 SCSI Arbitration Timing (ACB6)



NOTE:

This is only a functional timing diagram and does not depict AC-tested parameters.

11.3.6 SCSI Select/Reselect Timing

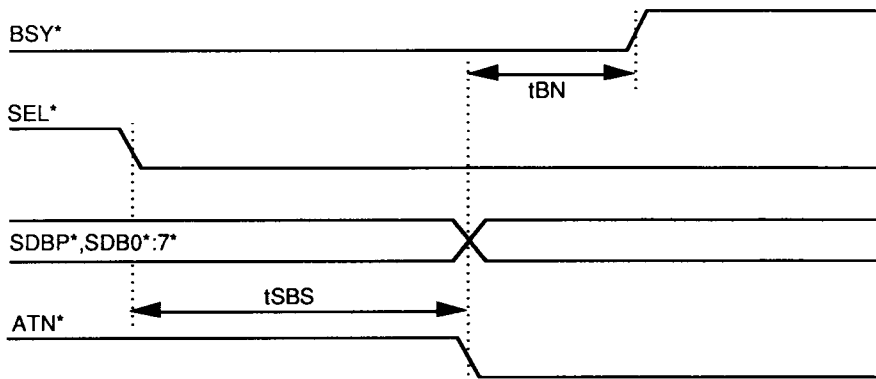
11.3.6.1 SCSI Selection Timing Parameters

SYMBOL	PARAMETER	MIN	MAX	UNITS
tSBS	SCSI bus SELECTION data assertion		6ts + 40†	ns
tBN	SCSI BSY* deasserted high		2ts + 40†	ns

NOTE:

† ts is the SCSI clock period, a function of SYSCLK as defined in Register 44H/64H, Bits 5-7.

11.3.6.2 SCSI Selection Timing (ACB8)



NOTE:

This is only a functional timing diagram and does not depict AC-tested parameters.

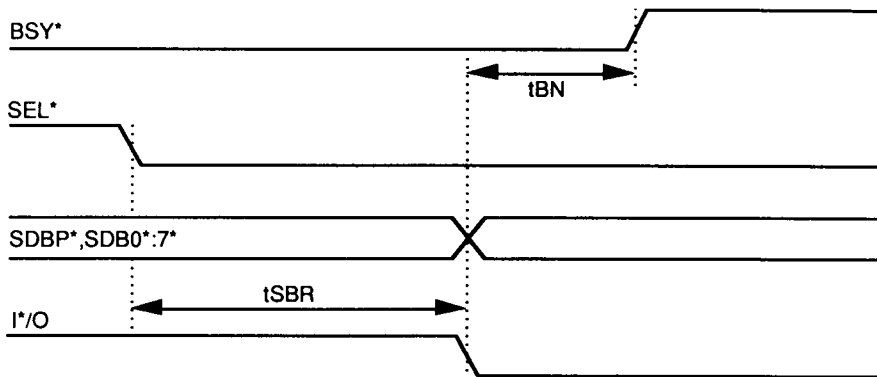
11.3.6.3 SCSI Reselection Timing Parameters

SYMBOL	PARAMETER	MIN	MAX	UNITS
tSBR	SCSI bus RESELECTION data assertion		6ts + 40†	ns
tBN	SCSI BSY* deasserted high		2ts + 40†	ns

NOTE:

† ts is the SCSI clock period, a function of SYSClk as defined in Register 44H/64H, Bits 5-7.

11.3.6.4 SCSI Reselection Timing (ACB10)

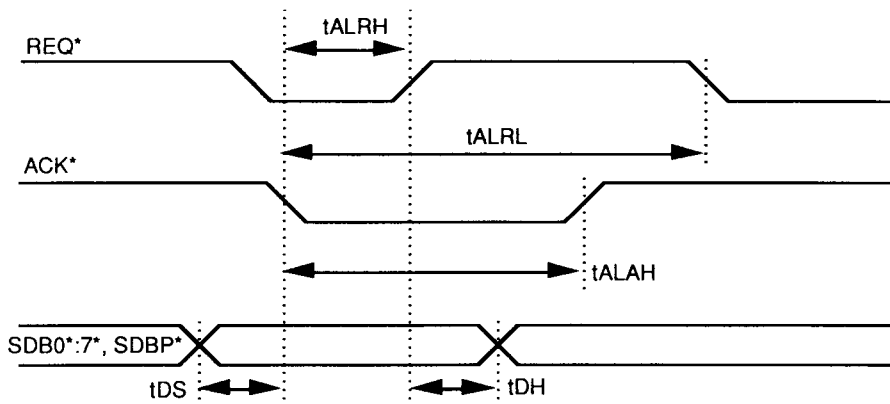


NOTE:

This is only a functional timing diagram and does not depict AC-tested parameters.

11.3.7 Target Mode Asynchronous Data Transfers
11.3.7.1 Data Out Phase Timing Parameters

SYMBOL	PARAMETER	MIN	MAX	UNITS
tALRH	ACK* ↓ to REQ* ↑		55	ns
tALRL	ACK* ↓ to REQ* ↓		2T + 55 if tALAH ≤ 2T tALAH + 55 if tALAH > 2T	ns
tDS	SDB0*:7*, SDBP* setup to ACK* ↓	40		ns
tDH	SDB0*:7*, SDBP* hold from REQ* ↑	0		ns

11.3.7.2 Data Out Phase Timing (AC15)


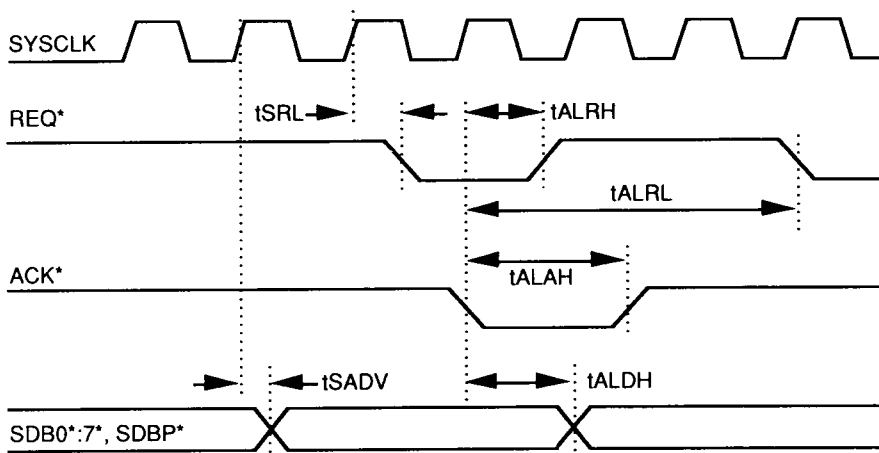
11.3.7.3 Data In Phase Timing Parameters

SYMBOL	PARAMETER	MIN	MAX	UNITS
tALRH	ACK* ↓ to REQ* ↑		55	ns
tALRL	ACK* ↓ to REQ* ↓		3T (4t) [†] + 55 if tALAH ≤ 3t (4t)	ns
			tALAH + 55 if tALAH > 3t (4t)	ns
tSRL	SYSCLK ↑ to REQ* ↓		70 ^{††}	ns
tSADV	SYSCLK ↑ to SDB0*:7*, SDBP* valid delay		60	ns
tALDH	SDB0*:7*, SDBP* hold from ACK* ↓	t-10		ns

NOTES:

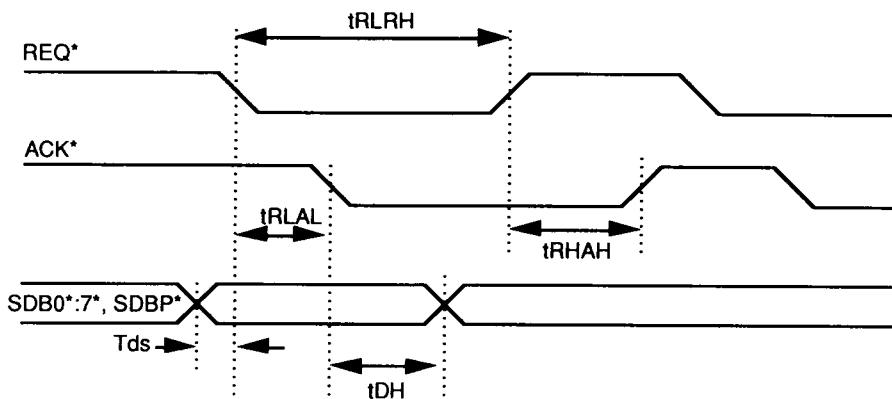
- † This time is 3t if the SCSI DATA SET UP SELECT bit (Register 51H, Bit 5) is reset or the time is 4t if the SCSI DATA SET UP SELECT bit is set.
- †† For reference only, tSRL and tSADV together guarantee a data setup time of 55ns.

11.3.7.4 Data In Phase Timing (AC17)



11.3.8 Initiator Mode Asynchronous Data Transfers
11.3.8.1 Data In Phase Timing Parameters

SYMBOL	PARAMETER	MIN	MAX	UNITS
tRLAL	REQ* ↓ to ACK* ↓		55	ns
tRHAH	REQ* ↑ to ACK* ↑		2t + 55 if tRLRH < 2t tRLRH + 55 if tRLRH ≥ 2t	ns
tDS	SDB0*:7*, SDBP* setup to REQ* ↓	40		ns
tDH	SDB0*:7*, SDBP* hold from ACK* ↓	0		ns

11.3.8.2 Data In Phase Timing (AC19)


11.3.8.3 Data Out Phase Timing Parameters

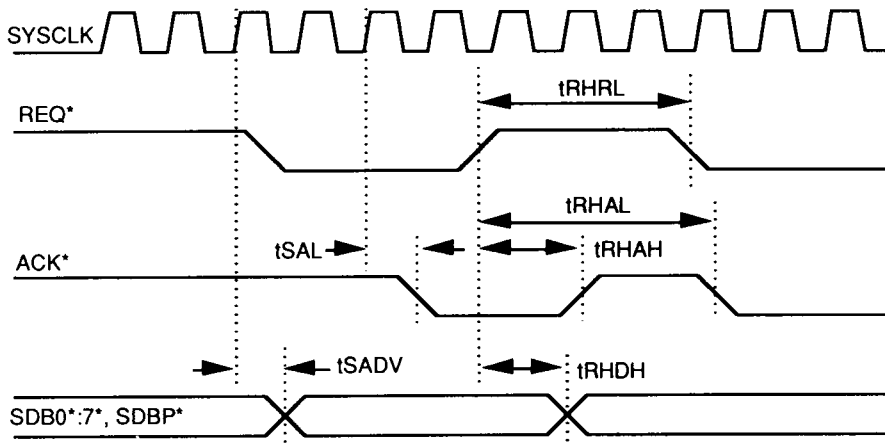
SYMBOL	PARAMETER	MIN	MAX	UNITS
tRHAH	REQ* ↑ to ACK* ↑		55	ns
tRHAL	REQ* ↑ to ACK* ↓		3t (4t) [†] + 55 if tRHRL ≤ 3t tRHRL + 55 if tRHRL > 3t	ns
tSAL	SYSCLK ↑ to ACK* ↓		75 ^{††}	ns
tSADV	SYSCLK ↑ to SDB0*:7*, SDBP* valid delay		55	ns
tRHDL	SDB0*:7*, SDBP* hold from REQ* ↑	0		ns

NOTES:

† This time is 3t if the SCSI DATA SET UP SELECT bit (Register 51H, Bit 5) is reset or the time is 4t if the SCSI DATA SET UP SELECT bit is set.

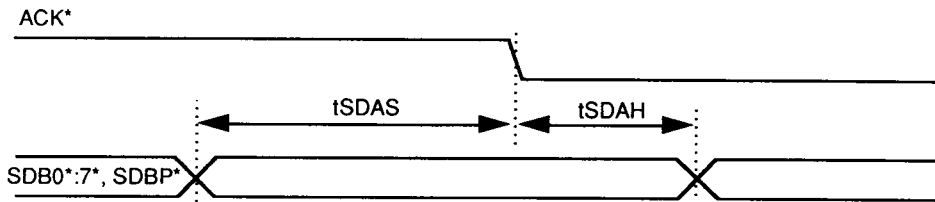
†† For reference only, tSAL and tSADV together guarantee a data setup time of 55 ns.

11.3.8.4 Data Out Phase Timing (AC21)



11.3.9 Target Mode Synchronous Data Transfers
11.3.9.1 Data Out Phase Timing Parameters

SYMBOL	PARAMETER	MIN	MAX	UNITS
tSDAS	SDB0 [*] :7 [*] , SDBP [*] set-up time to ACK [*] ↓	40		ns
tSDAH	ACK [*] ↓ to SDB0 [*] :7 [*] , SDBP [*] hold time	100		ns

11.3.9.2 Data Out Phase Timing (AC23)


11.3.9.3 Data In Phase Timing Parameters

SYMBOL	PARAMETER	MIN	MAX	UNITS
tSRRF	SYSCLK ↑ to REQ* ↓ delay		45	ns
tSRRR	SYSCLK ↑ to REQ* ↑ delay		45	ns
tSFRR	SYSCLK ↓ to REQ* ↑ delay		35	ns
tSDV	SYSCLK ↑ to SDB0*:7*, SDBP* valid delay		55	ns

NOTE:

For the Data In phase, the SCSI data bus set-up and hold times in synchronous transfer mode are dependent on the SYSCLK period *t*, in ns, and the value *P* which sets the synchronous transfer rate in Register 43H/63H, Bits 4-7.

If *P* is chosen as an even number then:

$$\text{SDB0}^*:7^*, \text{SDBP}^* \text{ set-up time to REQ}^* \downarrow = \frac{P}{2} \cdot (t-15)$$

$$\text{SDB0}^*:7^*, \text{SDBP}^* \text{ hold time from REQ}^* \downarrow = \frac{P}{2} \cdot (t-5)$$

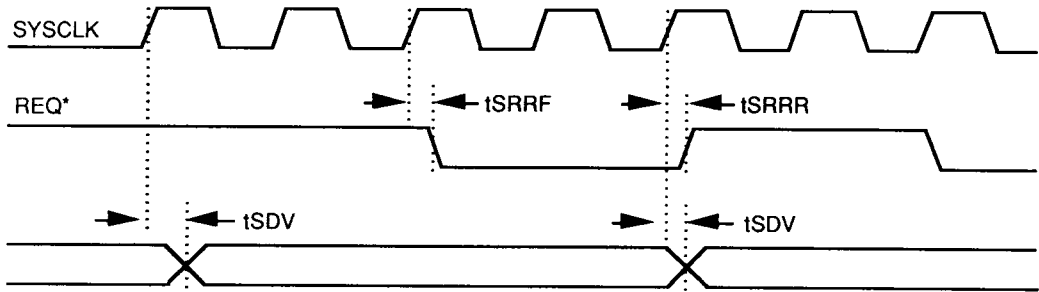
If *P* is chosen as an odd number then:

$$\text{SDB0}^*:7^*, \text{SDBP}^* \text{ set-up time to REQ}^* \downarrow = \frac{P-1}{2} \cdot (t-15)$$

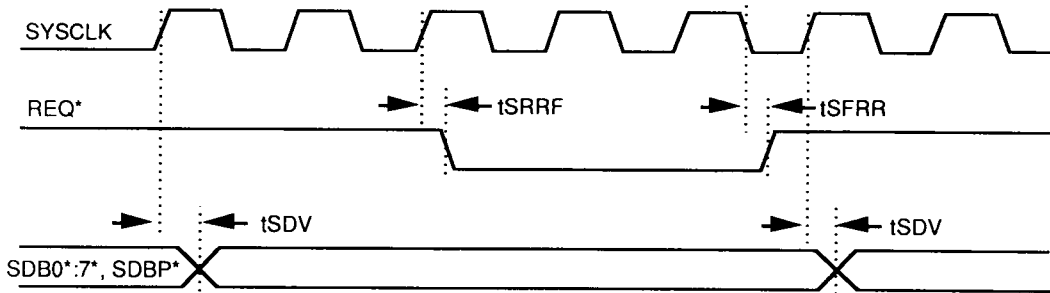
$$\text{SDB0}^*:7^*, \text{SDBP}^* \text{ hold time from REQ}^* \downarrow = \frac{P+1}{2} \cdot (t-5)$$

11.3.9.4 Data In Phase Timing (AC26)

Even Number of SYSCLK Cycles per SCSI Synchronous Transfer Period



Odd Number of SYSCLK Cycles per SCSI Synchronous Transfer Period

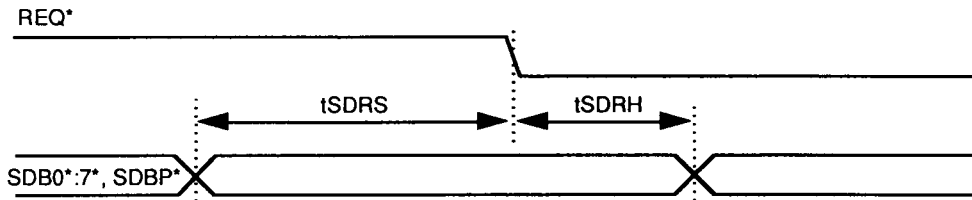


11.3.10 Initiator Mode Synchronous Data Transfers

11.3.10.1 Data In Phase Timing Parameters

SYMBOL	PARAMETER	MIN	MAX	UNITS
tSDRS	SDB0 [*] :7 [*] , SDBP [*] set-up time to REQ [*] ↓	40		ns
tSDRH	REQ [*] ↓ to SDB0 [*] :7 [*] , SDBP [*] hold time	100		ns

11.3.10.2 Data In Phase Timing (AC29)



11.3.10.3 Data Out Phase Timing Parameters

SYMBOL	PARAMETER	MIN	MAX	UNITS
tSRAF	SYSCLK ↑ to ACK* ↓ delay		45	ns
tSRAR	SYSCLK ↑ to ACK* ↑ delay		45	ns
tSFAR	SYSCLK ↓ to ACK* ↑ delay		35	ns
tSDV	SYSCLK ↑ to SDB0*:7*, SDBP* valid delay		35	ns

NOTES:

For the Data Out phase, the SCSI data bus set-up and hold times in synchronous transfer mode are dependent on the SYSCLK period t , in ns, and the value P which sets the synchronous transfer rate in Register 43H/63H, Bits 4-7.

If P is chosen as an even number then:

$$\text{SDB0}^*:7^*, \text{SDBP}^* \text{ set-up time to REQ}^* \downarrow = \frac{P}{2} \cdot (t-15)$$

$$\text{SDB0}^*:7^*, \text{SDBP}^* \text{ hold time from REQ}^* \downarrow = \frac{P}{2} \cdot (t-5).$$

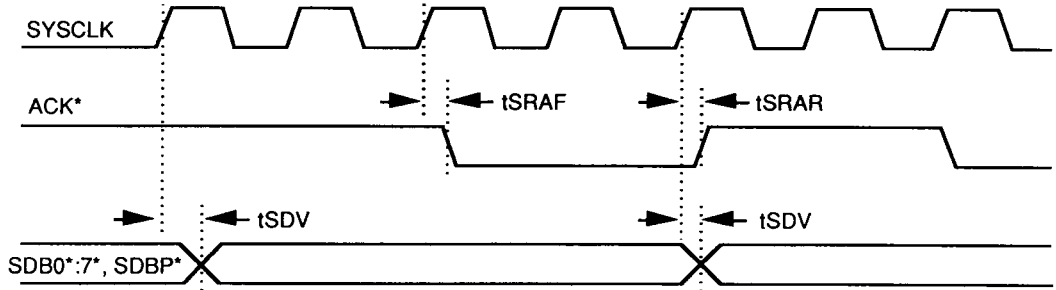
If P is chosen as an odd number then:

$$\text{SDB0}^*:7^*, \text{SDBP}^* \text{ set-up time to REQ}^* \downarrow = \frac{P-1}{2} \cdot (t-15)$$

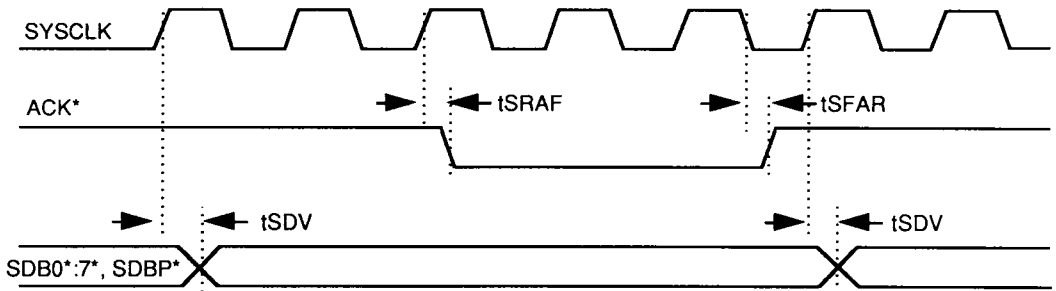
$$\text{SDB0}^*:7^*, \text{SDBP}^* \text{ hold time from REQ}^* \downarrow = \frac{P+1}{2} \cdot (t-5).$$

11.3.10.4 Data Out Phase Timing (AC31)

Even Number of SYSCLK Cycles per SCSI Synchronous Transfer Period

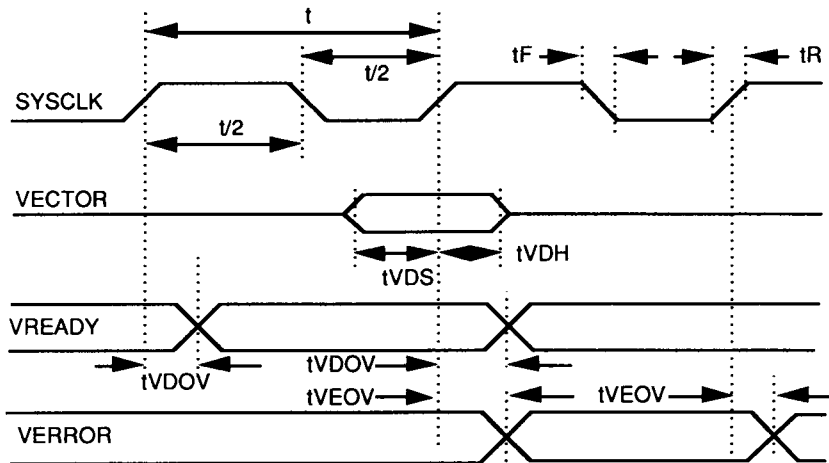


(AC32) Odd Number of SYSCLK Cycles per SCSI Synchronous Transfer Period



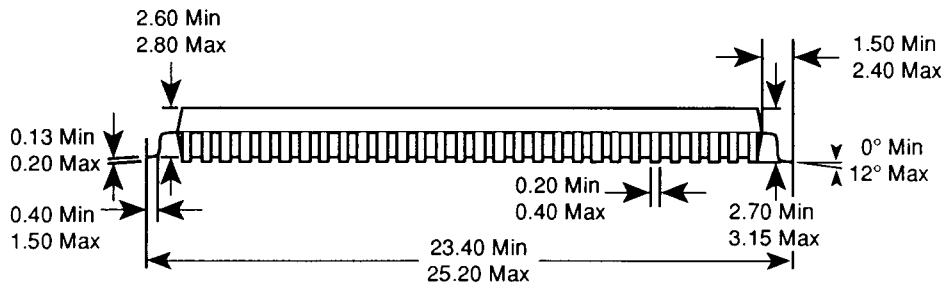
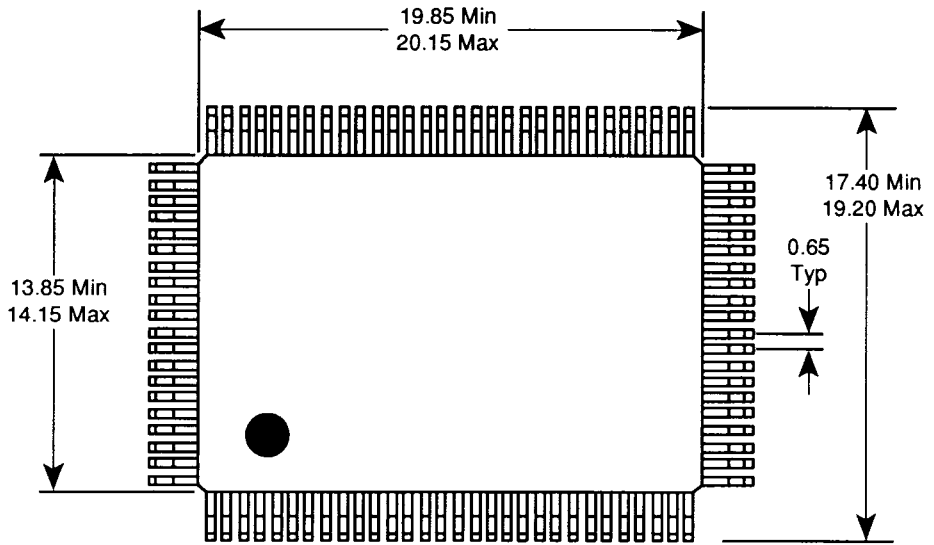
11.3.11 Vector Process
11.3.11.1 Vector Process Timing Parameters

SYMBOL	PARAMETER	MIN	MAX	UNITS
tVDS	VECTOR in valid to SYSCLK ↑	10		ns
tVDH	SYSCLK ↑ to VECTOR in invalid	5		ns
tVDOV	SYSCLK ↑ to VREADY out valid	10	25	ns
tVEOV	SYSCLK ↑ to VERROR out valid	10	25	ns

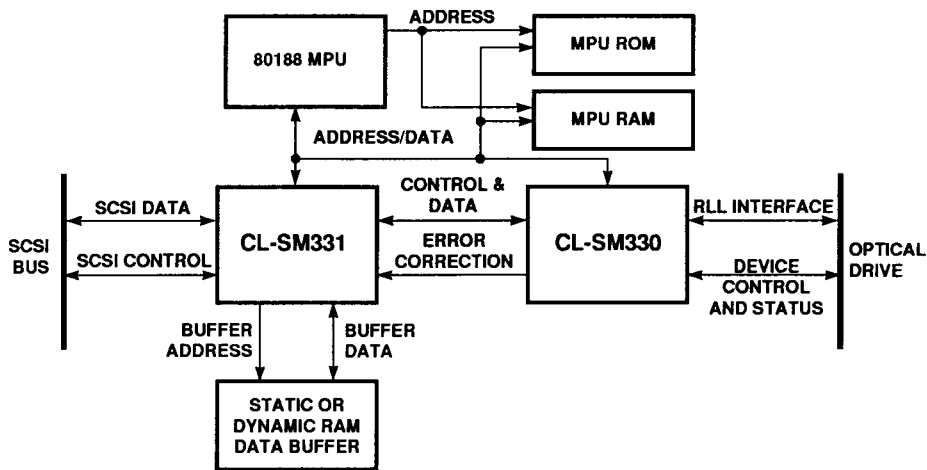
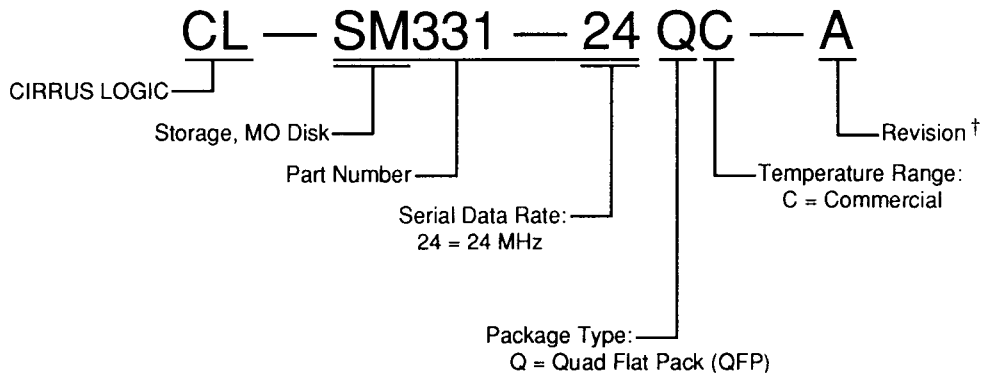
11.3.11.2 Vector Process Timing


12. SAMPLE PACKAGE

12.1 100-Pin Quad Flat Pack (QFP) Sample Package



NOTE: Dimensions for the QFP package are in millimeters.

13. TYPICAL APPLICATION

Single-Ended Direct SCSI System Implementation
14. ORDERING INFORMATION
Numbering Guide


† Contact CIRRUS LOGIC for up-to-date information on revisions.

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The Company

Cirrus Logic, Inc., produces high-integration peripheral controller circuits for mass storage, graphics, and data communications. Our products are used in leading-edge personal computers, engineering workstations, and office automation equipment.

The Cirrus Logic formula combines proprietary S/LA™+ IC design automation with system design expertise. The S/LA design system is a proven tool for developing high-performance logic circuits in half the time of most semiconductor companies. The results are better VLSI products, on-time, that help you win in the marketplace.

Cirrus Logic's fabless manufacturing strategy, unique in the semiconductor industry, employs a full manufacturing infrastructure to ensure maximum product quality, availability and value for our customers.

Talk to our systems and applications specialists; see how you can benefit from a new kind of semiconductor company.

† U.S. Patent No. 4,293,783

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