

74AC/ACT11030 8-Input NAND Gate Product Specification

ACL Products

FEATURES

- Output capability: ± 24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: SSI

DESCRIPTION

The 74AC/ACT11030 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11030 provides one 8-input NAND gate function.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS $T_A = 25^\circ\text{C}; \text{GND} = 0\text{V};$ $V_{CC} = 5.0\text{V}$	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay A through H to \bar{Y}	$C_L = 50\text{pF}$	4.8	5.7	ns
C_{PD}	Power dissipation capacitance per gate ¹	$f = 1\text{MHz}; C_L = 50\text{pF}$	42	41	pF
C_{IN}	input capacitance	$V_I = 0\text{V}$ or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jeduc JC40.2 Standard 17	500	500	mA

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$

f_i = input frequency in MHz, C_L = output load capacitance in pF,

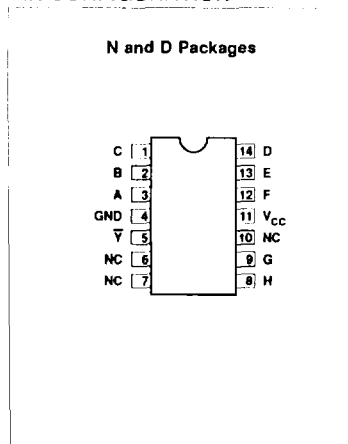
f_o = output frequency in MHz, V_{CC} = supply voltage in V,

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

ORDERING INFORMATION

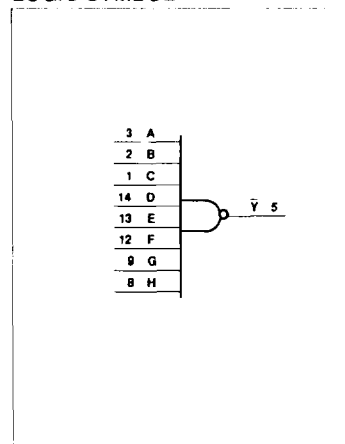
PACKAGES	TEMPERATURE RANGE	ORDER CODE
14-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11030N 74ACT11030N
14-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11030D 74ACT11030D

PIN CONFIGURATION



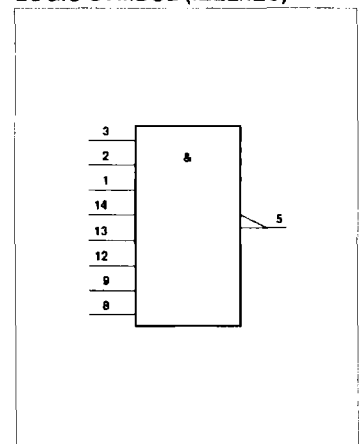
April 14, 1988

LOGIC SYMBOL



5-58

LOGIC SYMBOL (IEEE/IEC)



853-1338 92942

8-Input NAND Gate

74AC/ACT11030

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
3, 2, 1, 14 13, 12, 9, 8	A, B, C, D, E, F, G, H	Data inputs
5	\bar{Y}	Data output
4	GND	Ground (0V)
11	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS	OUTPUT
A through H	\bar{Y}
All inputs H	L
One or more inputs L	H

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11030			74ACT11030			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0 ¹	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

- No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK} or V_I	DC input diode current ²	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to $V_{CC} + 0.5$	V
I_{OK} or V_O	DC output diode current ²	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to $V_{CC} + 0.5$	V
I_O	DC output source or sink current per output pin	$V_O = 0$ to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C: derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C: derate linearly by 6mW/K	400	mW

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8-Input NAND Gate

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	V _{CC}	74AC11030				74ACT11030				UNIT
				T _A = +25°C		T _A = -40°C to +85°C		T _A = +25°C		T _A = -40°C to +85°C		
				Min	Max	Min	Max	Min	Max	Min	Max	
V _{IH}	High-level input voltage		3.0	2.10		2.10		2.0		2.0	V	
			4.5	3.15		3.15		2.0		2.0		
			5.5	3.85		3.85		2.0		2.0		
V _{IL}	Low-level input voltage		3.0		0.90		0.90				V	
			4.5		1.35		1.35	0.8		0.8		
			5.5		1.65		1.65	0.8		0.8		
V _{OH}	High-level output voltage	V _I = V _{IL} or V _{IH}	I _{OH} = -50μA	3.0	2.9		2.9				V	
				4.5	4.4		4.4		4.4			4.4
				5.5	5.4		5.4		5.4			5.4
				4.5	3.94	3.8	3.94	3.8				
									5.5	4.94		4.8
5.5			3.85				3.85					
V _{OL}	Low-level output voltage	V _I = V _{IL} or V _{IH}	I _{OL} = 50μA	3.0		0.1		0.1			V	
				4.5		0.1		0.1	0.1			0.1
				5.5		0.1		0.1	0.1			0.1
				3.0	0.36	0.44	0.36	0.44				
									4.5	0.36		0.44
5.5		0.36		0.44	0.36		0.44					
5.5			1.65			1.65		1.65				
I _I	Input leakage current	V _I = V _{CC} or GND	5.5		±0.1		±1.0		±0.1	±1.0	μA	
I _{CC}	Quiescent supply current	V _I = V _{CC} or GND, I _O = 0	5.5		4.0		4.0		4.0	4.0	μA	
ΔI _{CC}	Supply current, TTL inputs High ²	One input at 3.4V, other inputs at V _{CC} or GND	5.5						0.9	1.0	mA	

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
- This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

8-Input NAND Gate

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AC ELECTRICAL CHARACTERISTICS AT 3.3V $\pm 0.3V$

SYMBOL	PARAMETER	WAVEFORM	74AC11030					UNIT
			$T_A = +25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B, C, D, E, F, G, H to \bar{Y}	1	1.5 1.5	6.9 6.4	9.1 8.8	1.5 1.5	9.9 9.8	ns

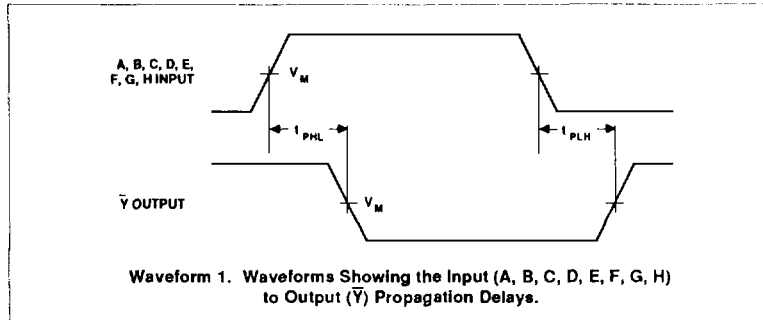
AC ELECTRICAL CHARACTERISTICS AT 5.0V $\pm 0.5V$

SYMBOL	PARAMETER	WAVEFORM	74AC11030					UNIT
			$T_A = +25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B, C, D, E, F, G, H to \bar{Y}	1	1.5 1.5	4.8 4.8	6.7 6.7	1.5 1.5	7.2 7.4	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V $\pm 0.5V$

SYMBOL	PARAMETER	WAVEFORM	74ACT11030					UNIT
			$T_A = +25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B, C, D, E, F, G, H to \bar{Y}	1	1.5 1.5	5.4 5.9	8.1 7.8	1.5 1.5	8.5 8.7	ns

AC WAVEFORMS



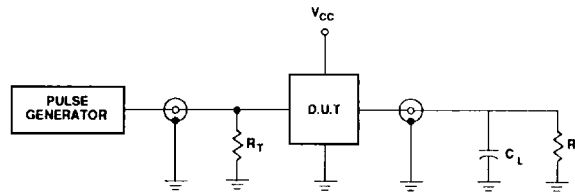
WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	$V_{IN} = \text{GND to } V_{CC}$ $V_M = 50\% V_{CC}$	$V_{OUT} = V_{OL} \text{ to } V_{OH}$
ACT	$V_{IN} = \text{GND to } 3.0V$ $V_M = 1.5V$	$V_M = 50\% V_{CC}$

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TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500 Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR \leq 10MHz

$t_r = t_f = 3ns$