EPC1064/EPC1064V Configuration EPROMs

December 1993, ver. 1 — Data Sheet Supplement

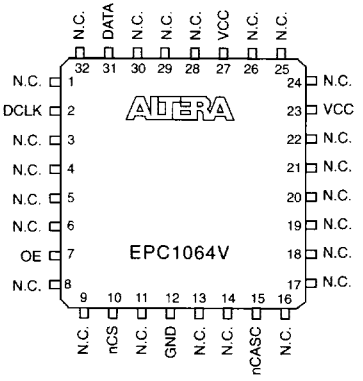
This data sheet supplement must be used together with the *Configuration EPROMs for FLEX 8000 Devices Data Sheet* in the Altera 1993 ***Data Book***. This supplement provides specifications for the 3.3-V EPC1064V device, and the dimensions for the 32-pin thin quad flat pack (TQFP) package available for EPC1064 and EPC1064V devices.

Features

- Serial EPROMs designed to configure FLEX 8000 devices
- 3.3-V operation provided by EPC1064V
- Available in the following one-time programmable (OTP) packages:
  - 32-pin thin quad flat pack (TQFP) (see Figure 1)
  - 8-pin plastic dual in-line (PDIP)
  - 20-pin plastic J-lead chip carrier (PLCC)
- Simple 4-wire interface to FLEX 8000 devices for ease of use
- Low current during configuration (10 mA) and near-zero standby current (100 µA)
- Software design support with Altera's MAX+PLUS II development system for IBM PC-AT, PS/2, and compatible computers, as well as for Sun SPARCstation, HP 9000 Series 700, and DEC Alpha AXP workstations
- Programming support with Altera's Master Programming Unit (MPU) and programming hardware from other manufacturers, including Data I/O

Figure 1. EPC1064/EPC1064V 32-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.



32-Pin TQFP

A-DSS-EPC1064V-01

EPC1064V Absolute Maximum Ratings

See *Operating Requirements for Altera Devices* in the 1993 ***Data Book***.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			20	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			100	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

EPC1064V Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	3.0	3.6	V
V_I	Input voltage	*Note (1)*	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			20	ns
t_F	Input fall time			20	ns

EPC1064V DC Operating Conditions *Notes (2), (3)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA DC	V_{CC} – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC		0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10	10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–10	10	µA

EPC1064V Supply Current

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC0}	V_{CC} supply current (standby)			100		µA
I_{CC1}	V_{CC} supply current (during configuration)	DCLK = 8 MHz		10		mA

EPC1064V Capacitance *Note (4)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

EPC1064V Timing Parameters

Symbol	Parameter	Conditions	Min	Max	Unit
t_{OEZX}	OE high to DATA output enabled			75	ns
t_{CSZX}	nCS low to DATA output enabled			75	ns
t_{CSXZ}	nCS high to DATA output disabled			75	ns
t_{CSS}	nCS low setup time to first DCLK rising edge		250		ns
t_{CSH}	nCS low hold time after DCLK rising edge		0		ns
t_{DSU}	Data setup time before rising edge on DCLK		75		ns
t_{DH}	Data hold time after rising edge on DCLK		0		ns
t_{CO}	DCLK to DATA out delay, *Note (5)*			100	ns
t_{CK}	Clock period		240		ns
f_{CK}	Clock frequency			4	MHz
t_{CL}	DCLK low time		120		ns
t_{CH}	DCLK high time		120		ns
t_{XZ}	OE low or nCS high to DATA output disabled			75	ns
t_{OEW}	OE pulse width to guarantee counter reset		150		ns
t_{CASC}	Last DCLK + 1 to nCASC low delay			90	ns
t_{CKXZ}	Last DCLK + 1 to DATA tri-state delay			75	ns
t_{CEOUT}	nCS high to nCASC high delay			150	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.

(2) Typical values are for T_A = 25° C and V_{CC} = 3.3 V.

(3) Operating conditions: V_{CC} = 3.3 V ± 10%, T_A = 0° C to 70° C for commercial use.

(4) Capacitance is sample-tested only.

(5) Eight Clock cycles are required after the t_{CSS} setup time has been met to clock out the first eight bits. These bits are all high and are used to synchronize the configuration process. The ninth Clock cycle presents the first configuration data bit.

Product Availability

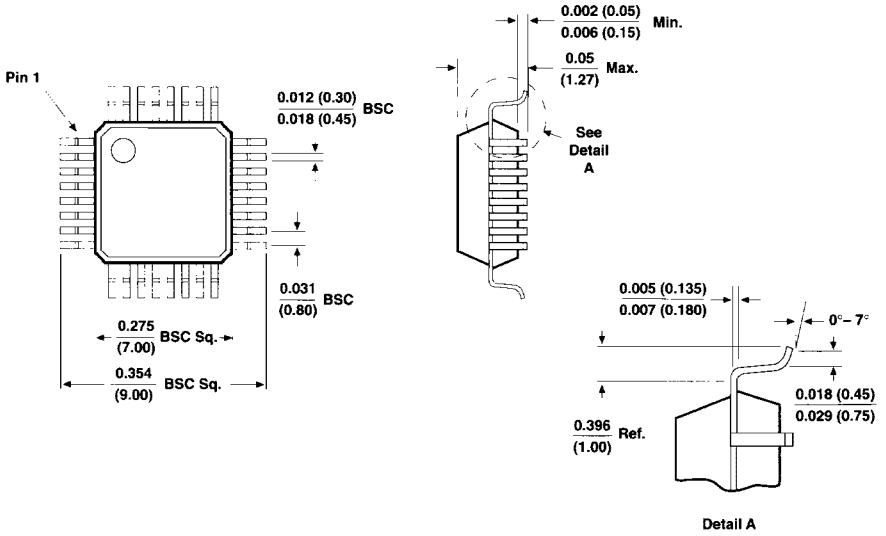
Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EPC1064V
Industrial Temp.	(–40° C to 85° C)	Consult factory
Military Temp.	(–55° C to 125° C)	Consult factory

Package Outlines

Figure 2 shows the package outlines for the 32-pin TQFP package. For dimensions of the 8-pin PDIP and 20-pin PLCC packages, see the *Altera Device Package Outlines Data Sheet* in the 1993 ***Data Book***.

Figure 2. 32-Pin Thin Plastic Quad Flat Pack (TQFP)

For an explanation of the package outline dimensions, refer to "Introduction" in the Altera Device Package Outlines Data Sheet in the 1993 ***Data Book****. Controlling measurement is in millimeters.*



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