FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-30327-2E

MEMORY

LOW POWER SRAM CARD

PCMCIA Rel.2/JEIDA Ver.4 conformable

MB98A9083x/9093x/9103x/9113x-20

LOW POWER STATIC RANDOM ACCESS MEMORY CARD
256 K/512 K/1 M/2 M-BYTE

■ DESCRIPTION

The Fujitsu MB98A9083x, 9093x, 9103x and 9113x are Static Random Access Memory (SRAM) cards capable of storing and retrieving large amounts of data. The memory circuits are housed in a credit-card sized 68-pin package. Internal circuitry is protected by two metal panels, each one at the top and the bottom of the card, that help to reduce chip damage from electrostatic discharge.

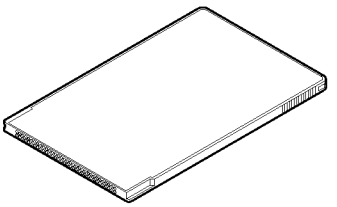
When the SRAM card is not powered by its system, an on-board, replaceable lithium battery (coin-type) is used to retain data. When the lithium battery must be replaced, rechargeable battery that are built in the SRAM card, maintain data. (See the BLOCK DIAGRAM for location of batteries.)

A unique feature of the Fujitsu memory cards allows the user to organize the card into either an 8-bit or a 16-bit bus configuration. All cards are portable and operate on low power at high speed.

In accordance with the Personal Computer Memory Card International Association (PCMCIA) and Japan Electrical Industry Development Association (JEIDA) industry standard specifications, SRAM cards offer additional EEPROM memory that is used to store attribute data. The attribute memory is an SRAM card option. (See page 3 for a description of the three available options.)

- Credit card size: 85.6 mm (length) × 54.0 mm (width) × 3.3 mm (thick).
- PCMCIA/JEIDA conformed two-piece 68-pin connector (with a two-row built-in 68-pin receptacle)
- Low operating and standby power consumption
- Built-in, rechargeable batteries for data retention during lithium battery replacement
- Battery voltage detect and write protect function

■ PACKAGE



CRD-68P-M04

■ ATTRIBUTE MEMORY OPTIONS

PCMCIA and JEIDA standard memory cards from Fujitsu provide a separate EEPROM memory address space for recording fundamental card information. It is used by the card manufacturers to record basic configuration information such as device type, size, speed, etc.

The attribute memory is selected by asserting the $\overline{\text{REG}}$ pin on the card interface. Option descriptions as follows:

OPTION 1: Attribute memory is not supported.
$\overline{\text{REG}}$ Pin: Not Contacted

(JEIDA Ver.3 conformable)

Part Number	Main Memory		Attribute Memory		Memory Organization*
	Memory Device	Access Time	Memory Device	Access Time	
MB98A90831	1M SRAM × 2 pcs	200 ns	—	—	256 K × 8 bits/128 K × 16 bits
MB98A90931	1M SRAM × 4 pcs	200 ns	—	—	512 K × 8 bits/256 K × 16 bits
MB98A91031	1M SRAM × 8 pcs	200 ns	—	—	1 M × 8 bits/512 K × 16 bits
MB98A91131	1M SRAM × 16 pcs	200 ns	—	—	2 M × 8 bits/1 M × 16 bits

OPTION 2: Attribute memory in a separate location is not supported.

When the $\overline{\text{REG}}$ line is asserted, "FF" is output to the data bus to indicate that attribute data may be stored in main memory.

(PCMCIA Rel.2/JEIDA Ver.4 conformable)

Part Number	Main Memory		Attribute Memory		Memory Organization*
	Memory Device	Access Time	Memory Device	Access Time	
MB98A90832	1M SRAM × 2 pcs	200 ns	—	—	256 K × 8 bits/128 K × 16 bits
MB98A90932	1M SRAM × 4 pcs	200 ns	—	—	512 K × 8 bits/256 K × 16 bits
MB98A91032	1M SRAM × 8 pcs	200 ns	—	—	1 M × 8 bits/512 K × 16 bits
MB98A91132	1M SRAM × 16 pcs	200 ns	—	—	2 M × 8 bits/1 M × 16 bits

OPTION 3: Attribute memory is supported. The data is stored in an 16K-bit EEPROM.

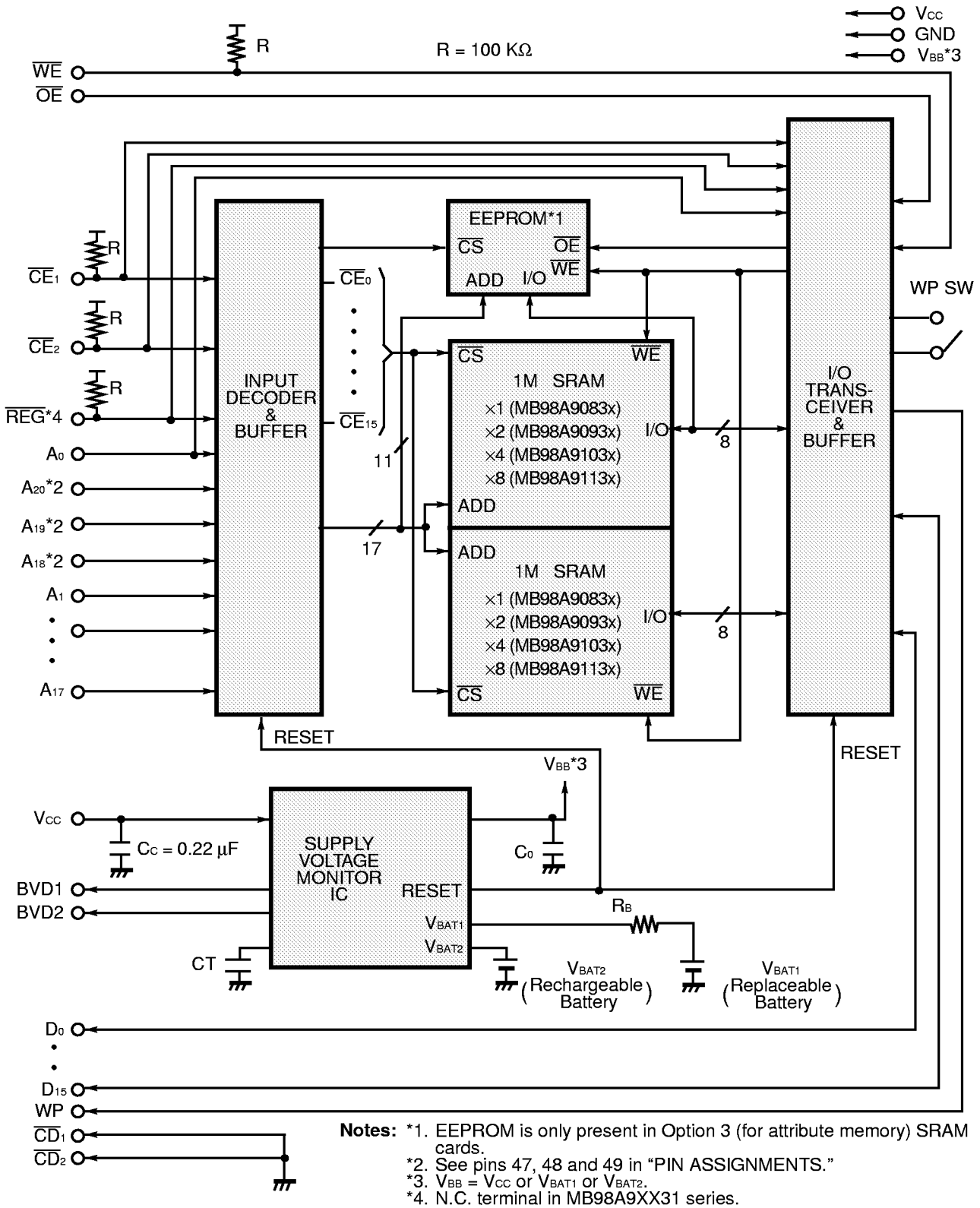
When the $\overline{\text{REG}}$ line is asserted, data stored in EEPROM is output to the data bus.

(PCMCIA Rel.2/JEIDA Ver.4 conformable)

Part Number	Main Memory		Attribute Memory		Memory Organization*
	Memory Device	Access Time	Memory Device	Access Time	
MB98A90833	1M SRAM × 2 pcs	200 ns	EEPROM × 1 pcs	300 ns	256 K × 8 bits/128 K × 16 bits
MB98A90933	1M SRAM × 4 pcs	200 ns	EEPROM × 1 pcs	300 ns	512 K × 8 bits/256 K × 16 bits
MB98A91033	1M SRAM × 8 pcs	200 ns	EEPROM × 1 pcs	300 ns	1 M × 8 bits/512 K × 16 bits
MB98A91133	1M SRAM × 16 pcs	200 ns	EEPROM × 1 pcs	300 ns	2 M × 8 bits/1 M × 16 bits

Note: * To be configured by user.

Fig. 1 – MB98A9083x/9093x/9103x/9113x BLOCK DIAGRAM



Notes: *1. EEPROM is only present in Option 3 (for attribute memory) SRAM cards.
*2. See pins 47, 48 and 49 in "PIN ASSIGNMENTS."
*3. $V_{BB} = V_{CC}$ or V_{BAT1} or V_{BAT2}.
*4. N.C. terminal in MB98A9XX31 series.

■ PIN ASSIGNMENTS

MB98A9083x	MB98A9093x	MB98A9103x	MB98A9113x	Pin No.		MB98A9083x	MB98A9093x	MB98A9103x	MB98A9113x
GND	GND	GND	GND	1	35	GND	GND	GND	GND
D_3	D_3	D_3	D_3	2	36	$\overline{CD_1}$	$\overline{CD_1}$	$\overline{CD_1}$	$\overline{CD_1}$
D_4	D_4	D_4	D_4	3	37	D_{11}	D_{11}	D_{11}	D_{11}
D_5	D_5	D_5	D_5	4	38	D_{12}	D_{12}	D_{12}	D_{12}
D_6	D_6	D_6	D_6	5	39	D_{13}	D_{13}	D_{13}	D_{13}
D_7	D_7	D_7	D_7	6	40	D_{14}	D_{14}	D_{14}	D_{14}
$\overline{CE_1}$	$\overline{CE_1}$	$\overline{CE_1}$	$\overline{CE_1}$	7	41	D_{15}	D_{15}	D_{15}	D_{15}
A_{10}	A_{10}	A_{10}	A_{10}	8	42	$\overline{CE_2}$	$\overline{CE_2}$	$\overline{CE_2}$	$\overline{CE_2}$
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	9	43	N.C.	N.C.	N.C.	N.C.
A_{11}	A_{11}	A_{11}	A_{11}	10	44	N.C.	N.C.	N.C.	N.C.
A_9	A_9	A_9	A_9	11	45	N.C.	N.C.	N.C.	N.C.
A_8	A_8	A_8	A_8	12	46	A_{17}	A_{17}	A_{17}	A_{17}
A_{13}	A_{13}	A_{13}	A_{13}	13	47	N.C.	A_{18}	A_{18}	A_{18}
A_{14}	A_{14}	A_{14}	A_{14}	14	48	N.C.	N.C.	A_{19}	A_{19}
$\overline{WE}$	$\overline{WE}$	$\overline{WE}$	$\overline{WE}$	15	49	N.C.	N.C.	N.C.	A_{20}
N.C.	N.C.	N.C.	N.C.	16	50	N.C.	N.C.	N.C.	N.C.
V_{CC}	V_{CC}	V_{CC}	V_{CC}	17	51	V_{CC}	V_{CC}	V_{CC}	V_{CC}
N.C.	N.C.	N.C.	N.C.	18	52	N.C.	N.C.	N.C.	N.C.
A_{16}	A_{16}	A_{16}	A_{16}	19	53	N.C.	N.C.	N.C.	N.C.
A_{15}	A_{15}	A_{15}	A_{15}	20	54	N.C.	N.C.	N.C.	N.C.
A_{12}	A_{12}	A_{12}	A_{12}	21	55	N.C.	N.C.	N.C.	N.C.
A_7	A_7	A_7	A_7	22	56	N.C.	N.C.	N.C.	N.C.
A_6	A_6	A_6	A_6	23	57	N.C.	N.C.	N.C.	N.C.
A_5	A_5	A_5	A_5	24	58	N.C.	N.C.	N.C.	N.C.
A_4	A_4	A_4	A_4	25	59	N.C.	N.C.	N.C.	N.C.
A_3	A_3	A_3	A_3	26	60	N.C.	N.C.	N.C.	N.C.
A_2	A_2	A_2	A_2	27	61	$\overline{REG}$/N.C.*	$\overline{REG}$/N.C.*	$\overline{REG}$/N.C.*	$\overline{REG}$/N.C.*
A_1	A_1	A_1	A_1	28	62	BVD2	BVD2	BVD2	BVD2
A_0	A_0	A_0	A_0	29	63	BVD1	BVD1	BVD1	BVD1
D_0	D_0	D_0	D_0	30	64	D_8	D_8	D_8	D_8
D_1	D_1	D_1	D_1	31	65	D_9	D_9	D_9	D_9
D_2	D_2	D_2	D_2	32	66	D_{10}	D_{10}	D_{10}	D_{10}
WP	WP	WP	WP	33	67	$\overline{CD_2}$	$\overline{CD_2}$	$\overline{CD_2}$	$\overline{CD_2}$
GND	GND	GND	GND	34	68	GND	GND	GND	GND

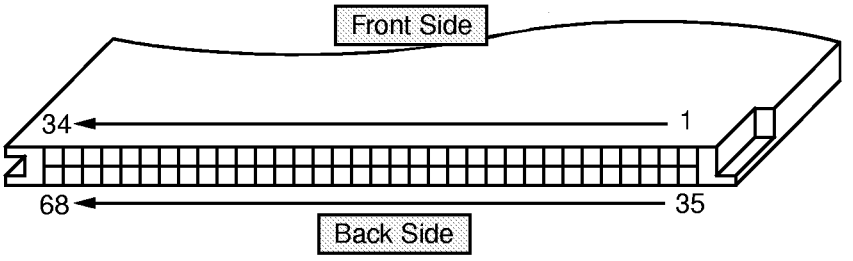
* : N.C. terminal in MB98A9XX31 series.

■ PIN DESCRIPTIONS

Symbol	Pin Name	Input/Output	Function
A_0 to A_{20}	Address Input	Input	Address Inputs, A_0 to A_{20}.
D_0 to D_{15}	Data Input/Output	Input/Output	Data Inputs/Outputs. The data bus size (8-bit or 16-bit) selected with $\overline{CE_1}$ and $\overline{CE_2}$.
$\overline{CE_1}$	Card Enable for Lower Byte	Input	Active Low – Lower byte (D_0 to D_7) is selected for read/write function of SRAM cards.
$\overline{CE_2}$	Card Enable for Upper Byte	Input	Active Low – Upper byte (D_8 to D_{15}) is selected for read/write function of SRAM cards.
$\overline{REG}$	Attribute Memory Select	Input	Active Low – Attribute memory is selected for read/write function of identification data of SRAM cards. (N.C. or "FF" data or attribute data.)
$\overline{OE}$	Output Enable	Input	Active Low – Output enable for SRAM cards.
$\overline{WE}$	Write Enable	Input	Active Low – Write enable for SRAM cards.
$\overline{CD_1}$, $\overline{CD_2}$	Card Detect	Output	These pins detect if the card has been correctly inserted. Both pins are tied to GND internally.
WP	Write Protect	Output	Write controller for SRAM cards This pin outputs the Protect / Non Protect status of "WP Switch".
BVD1	Battery Voltage Detect 1	Output	These pins indicate the battery condition of the SRAM cards. a) BVD1 = BVD2 = V_{OH} –Battery voltage is a safe level. b) BVD2 = V_{OL}, BVD1 = V_{OH} –Battery voltage is lower than 2.65 V. Battery should be replaced. c)BVD1 = BVD2 = V_{OL} –Battery voltage is lower than 2.37 V, or battery is not present.
BVD2	Battery Voltage Detect 2	Output	
V_{CC}	Power Supply	—	Power Supply Voltage (+5.0 V±5%)
GND	Ground	—	System Ground
N.C.	No Connection	—	

■ PIN LOCATIONS

Fig. 2 – BOTTOM VIEW (CONNECTOR SIDE)



■ FUNCTIONAL TRUTH TABLE

MAIN MEMORY FUNCTION *1 ($\overline{REG}$ = V_{IH})

$\overline{CE_2}$	$\overline{CE_1}$	A_0 (Byte)	$\overline{OE}$	$\overline{WE}$	WP	Mode	Data Input/Output		WP SW
							D_{15} to D_8	D_7 to D_0	
H	H	X	X	X	L	Standby	High-Z		NP
H	L	L	L	H	L	Read (×8)	High-Z	D_{OUT} (Lower Byte)	NP
H	L	H	L	H	L	Read (×8)	High-Z	D_{OUT} (Upper Byte)	NP
H	L	L	H*2	L	L	Write (×8)	High-Z	D_{IN} (Lower Byte)	NP
H	L	H	H*2	L	L	Write (×8)	High-Z	D_{IN} (Upper Byte)	NP
L	H	X	L	H	L	Read (×8)	D_{OUT} (Upper Byte)	High-Z	NP
L	H	X	H*2	L	L	Write (×8)	D_{IN} (Upper Byte)	High-Z	NP
L	L	X	L	H	L	Read (×16)	D_{OUT}		NP
L	L	X	H*2	L	L	Write (×16)	D_{IN}		NP
X	X	X	H	H	L	Output Disable	High-Z		NP
H	H	X	X	X	H	Standby	High-Z		P
H	L	L	L	H	H	Read (×8)	High-Z	D_{OUT} (Lower Byte)	P
H	L	H	L	H	H	Read (×8)	High-Z	D_{OUT} (Upper Byte)	P
H	L	L	H*2	L	H	Output Disable	High-Z		P
H	L	H	H*2	L	H	Output Disable	High-Z		P
L	H	X	L	H	H	Read (×8)	D_{OUT} (Upper Byte)	High-Z	P
L	H	X	H*2	L	H	Output Disable	High-Z		P
L	L	X	L	H	H	Read (×16)	D_{OUT}		P
L	L	X	H*2	L	H	Output Disable	High-Z		P
X	X	X	H	H	H	Output Disable	High-Z		P

Notes: *1. H = V_{IH}, L = V_{IL}, X = Either V_{IL} or V_{IH}, WP SW = Write Protect Switch, NP = Non Protect, P = Protect
*2. H-level is recommended though it is functionable at L-level.

ATTRIBUTE MEMORY FUNCTION *1 ($\overline{REG}$ = V_{IL}) *2

$\overline{CE_2}$	$\overline{CE_1}$	A_0 (Byte)	$\overline{OE}$	$\overline{WE}$	WP	Mode	Data Input/Output		WP SW
							D_{15} to D_8	D_7 to D_0	
H	H	X	X	X	L	Standby	High-Z		NP
H	L	L	L	H	L	Read (×8)	High-Z	D_{OUT} *3 (Lower Byte)	NP
H	L	H	L	H	L	Read (×8)	High-Z	H-level	NP
H	L	L	H	L	L	Write (×8)	High-Z	D_{IN} (Lower Byte)	NP
H	L	H	H	L	L	Write (×8)	High-Z	X	NP
L	H	X	L	H	L	Read (×8)	H-level	High-Z	NP
L	H	X	H	L	L	Write (×8)	High-Z	High-Z	NP
L	L	X	L	H	L	Read (×16)	H-level	D_{OUT} *3 (Lower Byte)	NP
L	L	X	H	L	L	Write (×16)	X	D_{IN} (Lower Byte)	NP
X	X	X	H	H	L	Output Disable	High-Z		NP
H	H	X	X	X	H	Standby	High-Z		P
H	L	L	L	H	H	Read (×8)	High-Z	D_{OUT} *3 (Lower Byte)	P
H	L	H	L	H	H	Read (×8)	High-Z	H-level	P
H	L	L	H	L	H	Output Disable	High-Z		P
H	L	H	H	L	H	Output Disable	High-Z		P
L	H	X	L	H	H	Read (×8)	H-level	High-Z	P
L	H	X	H	L	H	Output Disable	High-Z		P
L	L	X	L	H	H	Read (×16)	H-level	D_{OUT} *3 (Lower Byte)	P
L	L	X	H	L	H	Output Disable	High-Z		P
X	X	X	H	H	H	Output Disable	High-Z		P

Notes: *1. H = V_{IH}, L = V_{IL}, X = Either V_{IL} or V_{IH}, WP SW = Write Protect Switch, NP = Non Protect, P = Protect
*2. N.C. for MB98A90831, 90931, 91031 and 91131.
*3. H-level is output for MB98A90832, 90932, 91032 and 91132.

■ ADDRESS CONFIGURATIONS *1 (MAIN MEMORY)

8-BIT BUS ORGANIZATION ($\overline{CE}_1$ = V_{IL}, $\overline{CE}_2$ = V_{IH})

A_{20} to A_0						$\overline{CE}_2$	$\overline{CE}_1$	D_{15} to D_8	D_7 to D_0
0	0000	0000	0000	0000	0000	H	L	– – – – –	0 Add.
0	0000	0000	0000	0000	0001	H	L	– – – – –	1 Add.
0	0000	0000	0000	0000	0010	H	L	– – – – –	2 Add.
0	0000	0000	0000	0000	0011	H	L	– – – – –	3 Add.
↓	↓	↓	↓	↓	↓	↓	↓	↓ ↓	↓ ↓
1	1111	1111	1111	1111	1100	H	L	– – – – –	2,097,148 Add.
1	1111	1111	1111	1111	1101	H	L	– – – – –	2,097,149 Add.
1	1111	1111	1111	1111	1110	H	L	– – – – –	2,097,150 Add.
1	1111	1111	1111	1111	1111	H	L	– – – – –	2,097,151 Add.

8-BIT BUS ORGANIZATION ($\overline{CE}_1$ = V_{IH}, $\overline{CE}_2$ = V_{IL}) *2

A_{20} to A_0						$\overline{CE}_2$	$\overline{CE}_1$	D_{15} to D_8	D_7 to D_0
0	0000	0000	0000	0000	000x	L	H	1 Add.	– – – – –
0	0000	0000	0000	0000	001x	L	H	3 Add.	– – – – –
0	0000	0000	0000	0000	010x	L	H	5 Add.	– – – – –
0	0000	0000	0000	0000	011x	L	H	7 Add.	– – – – –
↓	↓	↓	↓	↓	↓	↓	↓	↓ ↓	↓ ↓
1	1111	1111	1111	1111	100x	L	H	2,097,145 Add.	– – – – –
1	1111	1111	1111	1111	101x	L	H	2,097,147 Add.	– – – – –
1	1111	1111	1111	1111	110x	L	H	2,097,149 Add.	– – – – –
1	1111	1111	1111	1111	111x	L	H	2,097,151 Add.	– – – – –

16-BIT BUS ORGANIZATION ($\overline{CE}_1$ = V_{IL}, $\overline{CE}_2$ = V_{IL})

A_{20} to A_0						$\overline{CE}_2$	$\overline{CE}_1$	D_{15} to D_8	D_7 to D_0
0	0000	0000	0000	0000	000x	L	L	1 Add.	0 Add.
0	0000	0000	0000	0000	001x	L	L	3 Add.	2 Add.
0	0000	0000	0000	0000	010x	L	L	5 Add.	4 Add.
0	0000	0000	0000	0000	011x	L	L	7 Add.	6 Add.
↓	↓	↓	↓	↓	↓	↓	↓	↓ ↓	↓ ↓
1	1111	1111	1111	1111	100x	L	L	2,097,145 Add.	2,097,144 Add.
1	1111	1111	1111	1111	101x	L	L	2,097,147 Add.	2,097,146 Add.
1	1111	1111	1111	1111	110x	L	L	2,097,149 Add.	2,097,148 Add.
1	1111	1111	1111	1111	111x	L	L	2,097,151 Add.	2,097,150 Add.

Notes: *1. H = V_{IH}, L = V_{IL}, X = Either 0 or 1.
*2. Even addresses are not available in this mode.

■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +6.0	V
Input Voltage	V_{IN}	–0.5 to V_{CC} +0.5	V
Output Voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Ambient Temperature	T_A	–10 to +60 *1	°C
Storage Temperature	T_{STG}	–20 to +65 *2	°C

Notes: *1. This value does not apply to the replaceable battery.
*2. This value does not apply to the replaceable battery and data retention.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Ground	GND	—	0	—	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	–0.3	—	0.8	V
Ambient Temperature *	T_A	0	—	55	°C

Note: * This value does not apply to the replaceable lithium battery. See V_{BAT1} in Fig.1.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

■ CAPACITANCE

(T_A = 25°C, f = 1 MHz, V_{IN} = $V_{I/O}$ = GND)

Parameter	Notes	Symbol	Min.	Typ.	Max.	Unit
Input Capacitance	*1	C_{IN}	—	—	50	pF
I/O Capacitance	*2	$C_{I/O}$	—	—	50	pF

Notes: *1. This value does not apply to $\overline{CE_1}$, $\overline{CE_2}$, $\overline{REG}$ and $\overline{WE}$.
*2. This value does not apply to BVD1, BVD2, $\overline{CD_1}$ and $\overline{CD_2}$.

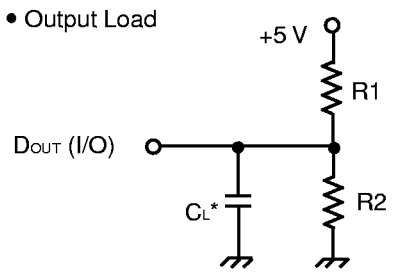
■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

Parameter		Notes	Symbol	Condition	Min.	Typ.	Max.	Unit
Standby Supply Current		*1	I_{SB1}	$\overline{CE_1}$, $\overline{CE_2} \geq V_{CC}$ –0.2 V	—	—	0.5	mA
			I_{SB2}	$\overline{CE_1}$, $\overline{CE_2} = V_{IH}$	—	—	5.0	mA
Active Supply Current			I_{CC1}	$V_{IN} = V_{IH}$ or V_{IL} $\overline{CE_1}$, $\overline{CE_2} = V_{IL}$, I_{OUT} = 0 mA	—	—	50	mA
Operating Supply Current	MB98A9083x/9093x		I_{CC2}	$V_{IN} = V_{IH}$ or V_{IL}, Cycle = Min Duty = 100%, I_{OUT} = 0 mA $\overline{OE} = V_{IH}$ during Write Cycle	—	—	180	mA
	MB98A9103x/9113x				—	—	240	
Input Leakage Current		*2	I_{LI}	V_{IN} = 0 V to V_{CC}	–10	—	10	µA
Output Leakage Current		*3	$I_{LI/O}$	V_{OUT} = 0 V to V_{CC}, $\overline{CE_1}$, $\overline{CE_2} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	–10	—	10	µA
Output High Voltage		*4	V_{OH}	I_{OH} = –1.0 mA	2.4	—	—	V
Output Low Voltage			V_{OL}	I_{OL} = 2.1 mA	—	—	0.4	V

Notes: *1. This value does not apply to recharge current from system or replaceable lithium battery to rechargeable battery.
*2. This value does not apply to $\overline{CE_1}$, $\overline{CE_2}$, $\overline{REG}$ and $\overline{WE}$.
*3. This value does not apply to BVD1, BVD2, $\overline{CD_1}$, $\overline{CD_2}$ and WP.
*4. This value does not apply to $\overline{CD_1}$ and $\overline{CD_2}$.

Fig. 3 – AC TEST CONDITIONS



- Input Pulse Levels: 0.6 V to 2.6 V
- Input Pulse Rise and Fall Times: 5 ns (Transition between 0.8 V and 2.4 V)
- Timing Reference Levels

  Input: V_{IL} = 0.8 V, V_{IH} = 2.4 V
  Output: V_{OL} = 0.8 V, V_{OH} = 2.0 V

* Including Jig and stray capacitance

	R1	R2	CL	Parameters Mesured
Load I	1.8 kΩ	990 Ω	100 pF	All parameters except t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{RCLZ}, t_{ROLZ}, t_{RCHZ}, t_{ROHZ}, t_{WLZ} and t_{WHZ}
Load II	1.8 kΩ	990 Ω	5 pF	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{RCLZ}, t_{ROLZ}, t_{RCHZ}, t_{ROHZ}, t_{WLZ} and t_{WHZ}

■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

MAIN MEMORY READ CYCLE

Parameter	Notes	Symbol	Min.	Max.	Unit
Read Cycle Time		t_{RC}	200	—	ns
Address Access Time		t_{AA}	—	200	ns
Card Enable Access Time		t_{CE}	—	200	ns
Output Enable Access Time		t_{OE}	—	100	ns
Output Hold from Address Change		t_{OH}	5	—	ns
Card Enable to Output Low-Z	*1, 2	t_{CLZ}	5	—	ns
Output Enable to Output Low-Z	*1, 2	t_{OLZ}	5	—	ns
Card Enable to Output High-Z	*1, 2	t_{CHZ}	—	50	ns
Output Enable to Output High-Z	*1, 2	t_{OHZ}	—	50	ns

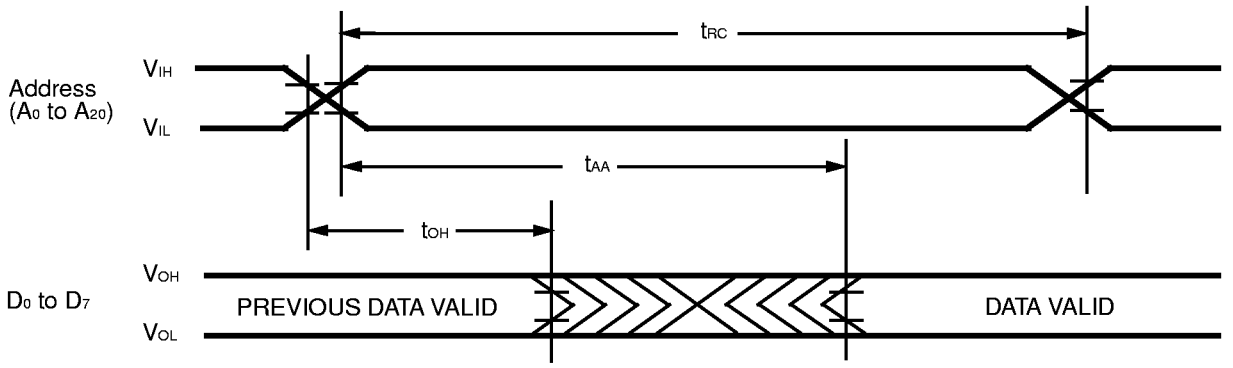
ATTRIBUTE MEMORY READ CYCLE *3

Parameter	Notes	Symbol	Min.	Max.	Unit
Read Cycle Time		t_{RRC}	300	—	ns
Address Access Time		t_{RAA}	—	300	ns
Card Enable Access Time		t_{RCE}	—	300	ns
Output Enable Access Time		t_{ROE}	—	150	ns
Output Hold from Address Change		t_{ROH}	5	—	ns
Card Enable to Output Low-Z	*1, 2	t_{RCLZ}	5	—	ns
Output Enable to Output Low-Z	*1, 2	t_{ROLZ}	5	—	ns
Card Enable to Output High-Z	*1, 2	t_{RCHZ}	—	60	ns
Output Enable to Output High-Z	*1, 2	t_{ROHZ}	—	60	ns

Notes: *1. Transition is measured at the point of ±500 mV from steady state voltage.
*2. This parameter is specified using Load II in Fig.3.
*3. This parameter is for MB98A90833, 90933, 91033 and 91133.

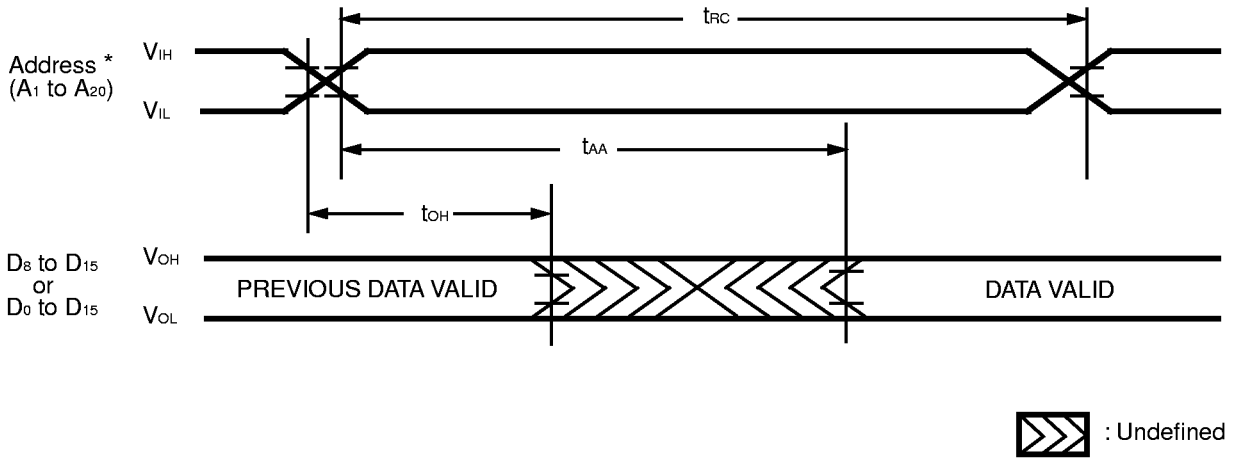
MAIN MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = V_{IH}, $\overline{REG}$ = V_{IH})

READ CYCLE 1: $\overline{CE_1}$ = $\overline{OE}$ = V_{IL}, $\overline{CE_2}$ = V_{IH} : × 8-bit Bus Organization



READ CYCLE 2: $\overline{CE_1}$ = V_{IH}, $\overline{CE_2}$ = $\overline{OE}$ = V_{IL}: × 8-bit Bus Organization

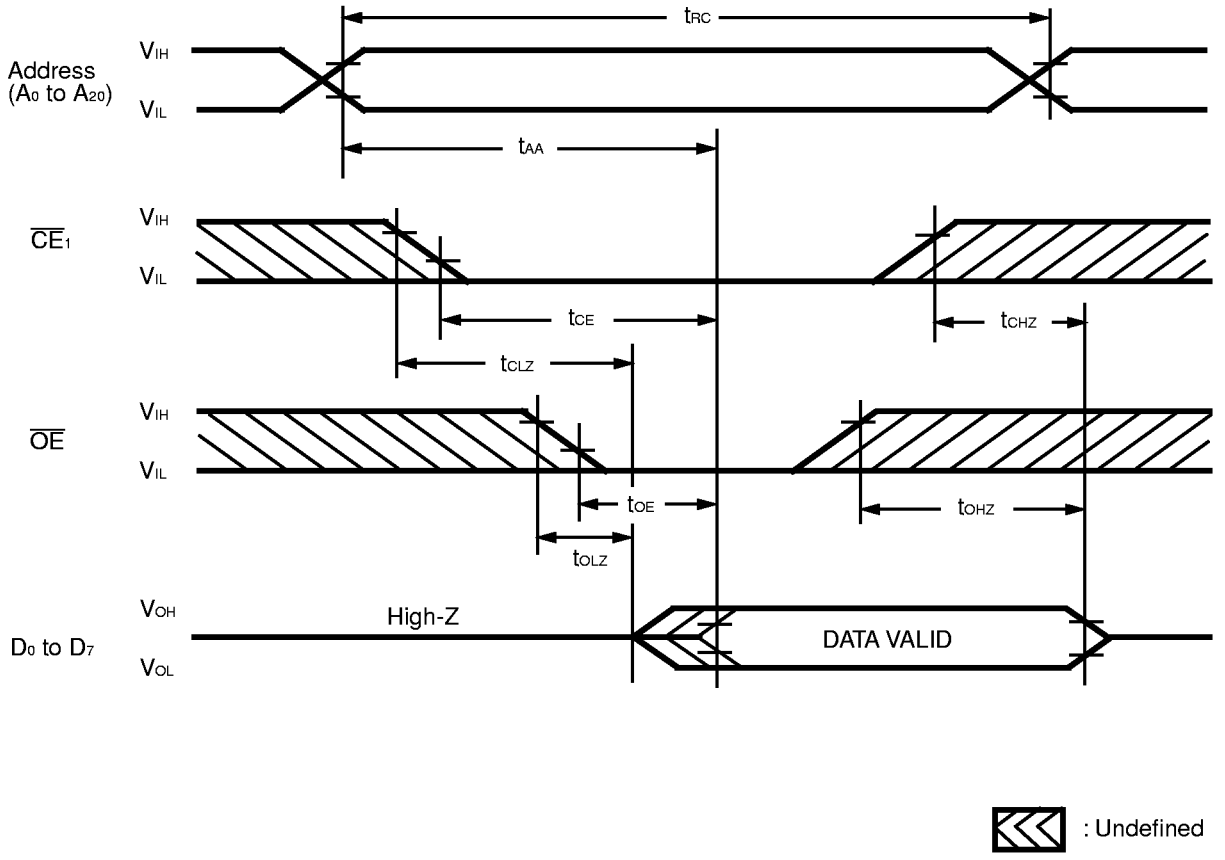
$\overline{CE_1}$ = $\overline{CE_2}$ = $\overline{OE}$ = V_{IL}: × 16-bit Bus Organization



Note: * A_0 = Either V_{IH} or V_{IL}.

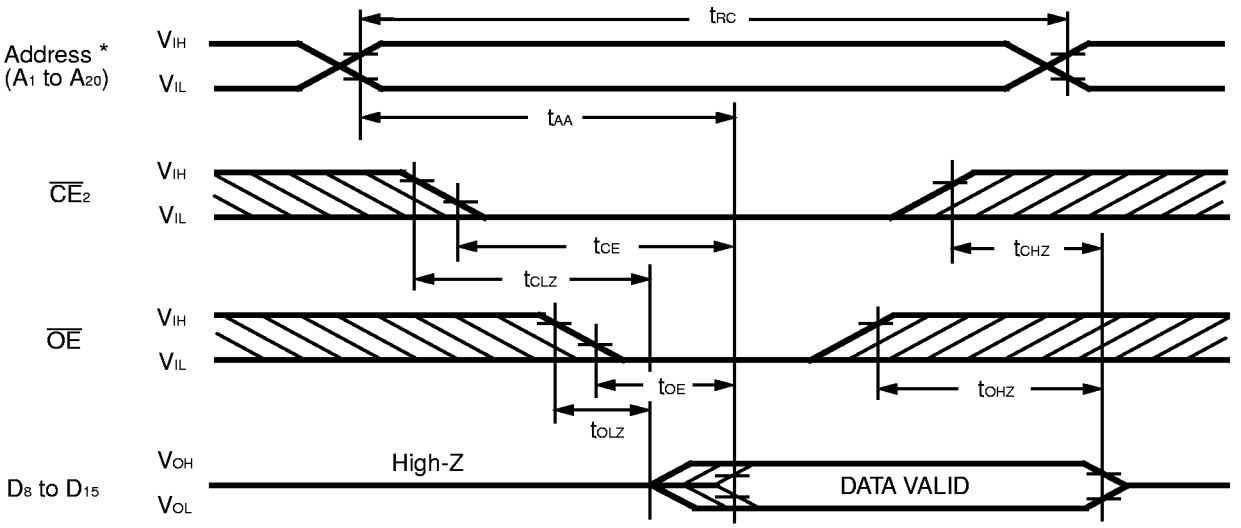
MAIN MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = V_{IH}, $\overline{REG}$ = V_{IH})

READ CYCLE 3: $\overline{CE_2}$ = V_{IH}: × 8-bit Bus Organization

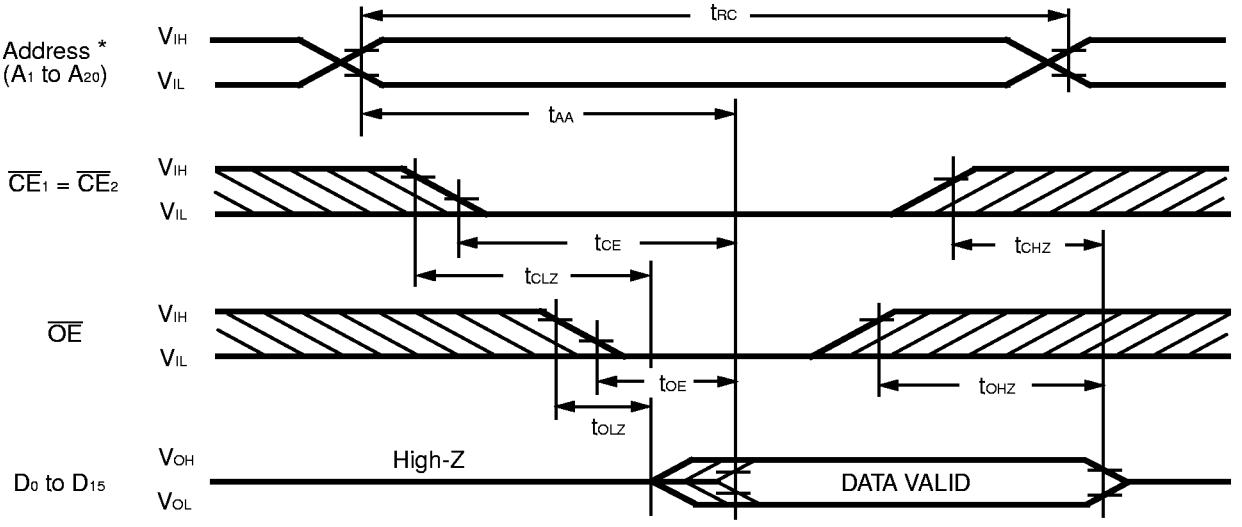


MAIN MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = V_{IH}, $\overline{REG}$ = V_{IH})

READ CYCLE 4: $\overline{CE_1}$ = V_{IH}: × 8-bit Bus Organization



READ CYCLE 5: $\overline{CE_1}$ = $\overline{CE_2}$: × 16-bit Bus Organization

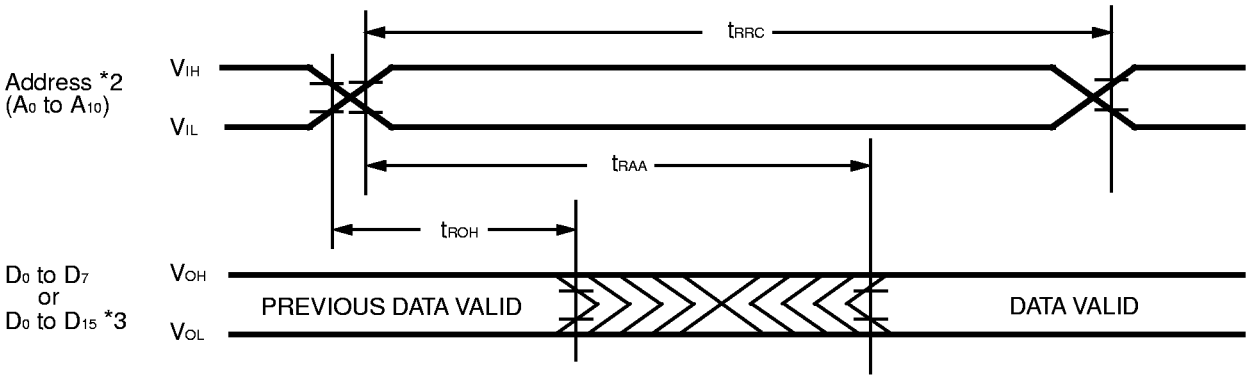


: Undefined

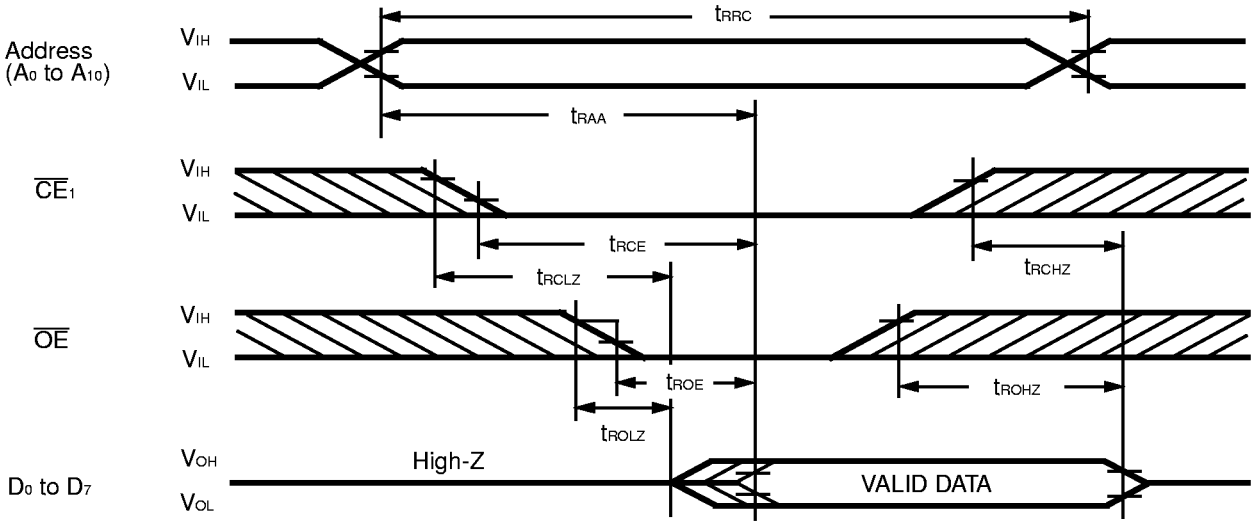
Note: * A_0 = Either V_{IH} or V_{IL}.

ATTRIBUTE MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = V_{IH}, $\overline{REG}$ = V_{IL}) *1

READ CYCLE 1: $\overline{CE_1}$ = $\overline{OE}$ = V_{IL}, $\overline{CE_2}$ = V_{IH} : × 8-bit Bus Organization
$\overline{CE_1}$ = $\overline{CE_2}$ = $\overline{OE}$ = V_{IL} : × 16-bit Bus Organization

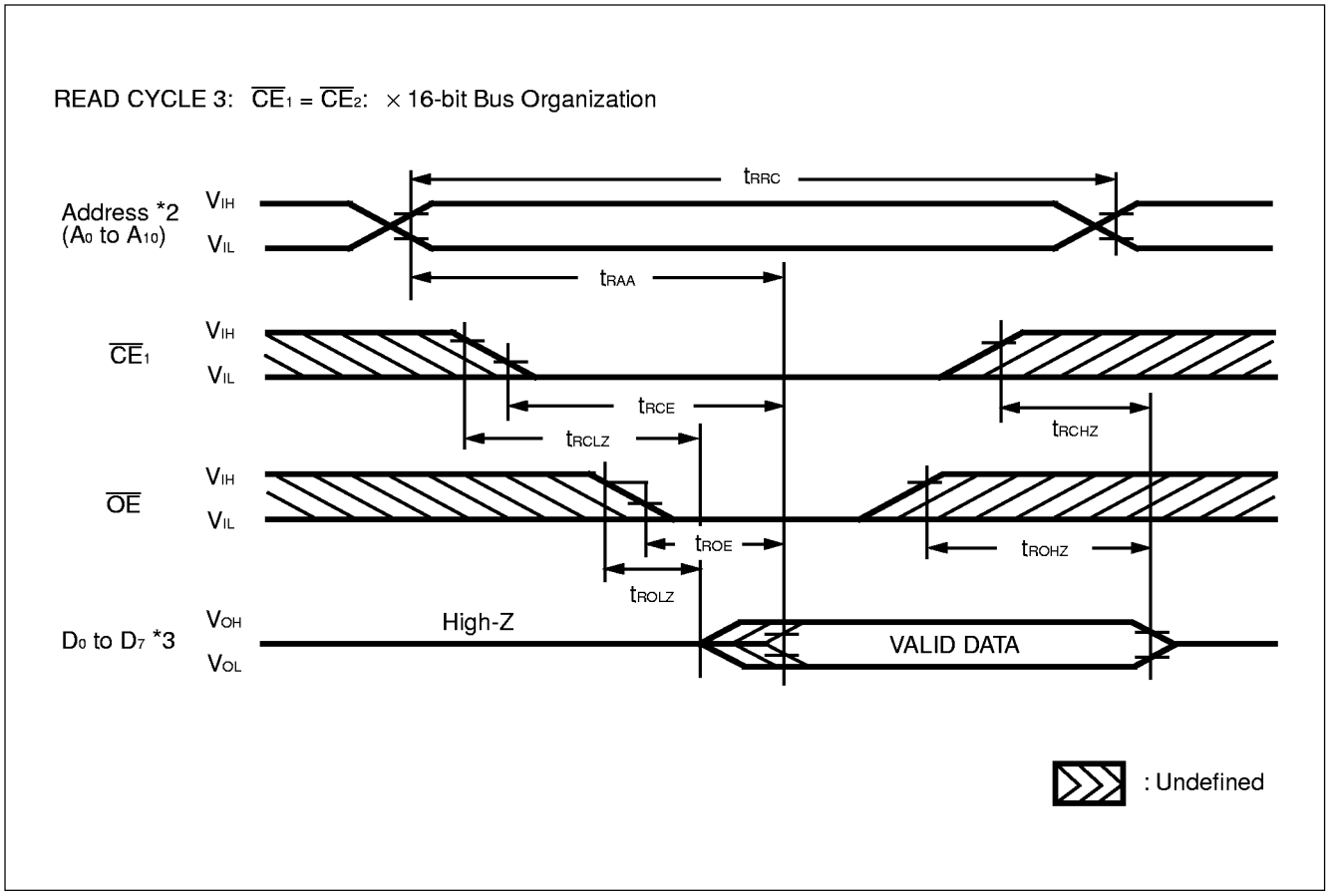


READ CYCLE 2: $\overline{CE_2}$ = V_{IH}: × 8-bit Bus Organization



Notes: *1. This timing diagram is for MB98A90833, 90933, 91033 and 91133. "FF" data is available on MB98A90832, 90932, 91032, and 91132 only.
*2. A_0 = Either V_{IH} or V_{IL} for a 16-bit bus organization.
*3. H-level is output from D_8 to D_{15}.

ATTRIBUTE MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = V_{IH}, $\overline{REG}$ = V_{IL}) *1



Notes: *1. This timing diagram is for MB98A90833, 90933, 91033, and 91133. "FF" data is available on MB98A90832, 90932, 91032, and 91132 only.

*2. A_0 = Either V_{IH} or V_{IL}.

*3. H-level is output from D_8 to D_{15}.

MAIN MEMORY WRITE CYCLE *1

Parameter	Notes	Symbol	Min.	Max.	Unit
Write Cycle Time		t_{WC}	200	—	ns
Address Valid to End of Write		t_{AW}	140	—	ns
Chip Select to End of Write		t_{CW}	140	—	ns
Data Valid to End of Write		t_{DW}	60	—	ns
Data Hold Time		t_{DH}	30	—	ns
Write Pulse Width		t_{WP}	120	—	ns
Address Set Up Time		t_{AS}	20	—	ns
Write Recovery Time		t_{WR}	30	—	ns
Output Enable to Output Low-Z	*2	t_{OLZ}	5	—	ns
Output Enable to Output High-Z	*2	t_{OHZ}	—	50	ns
Write Enable to Output Low-Z	*2, 3	t_{WLZ}	5	—	ns
Write Enable to Output High-Z	*2, 3	t_{WHZ}	—	50	ns
Output Enable Set Up Time		t_{OES}	10	—	ns
Output Enable Hold Time		t_{OEH}	10	—	ns

ATTRIBUTE MEMORY WRITE CYCLE *4

Parameter	Symbol	Min.	Max.	Unit
Byte Write Cycle Time	t_{RWR}	—	10	ms
Address Set Up Time	t_{RAS}	20	—	ns
Chip Enable Set Up Time	t_{RCS}	0	—	ns
Output Enable Set Up Time	t_{ROES}	20	—	ns
Write Pulse Width	t_{RWP}	100	—	ns
Address Hold Time	t_{RAH}	50	—	ns
Data Set Up Time	t_{RDS}	50	—	ns
Data Hold Time	t_{RDH}	20	—	ns
Chip Enable Hold Time	t_{RCH}	0	—	ns
Output Enable Hold Time	t_{ROEH}	20	—	ns
Write Recovery Time	t_{RRE}	50	—	ns
End of Write to Output Time	t_{RRBO}	—	100	ns
Number of Write per Byte	N	10000	—	Times
Write Enable Hold Time	t_{RWEH}	10	—	ns

Notes: *1. If $\overline{OE}$, $\overline{CE_1}$, and $\overline{CE_2}$ are in the Read Mode during this period, then the I/O pins are in the output state and the input signals of the phase opposite to the outputs must be applied.

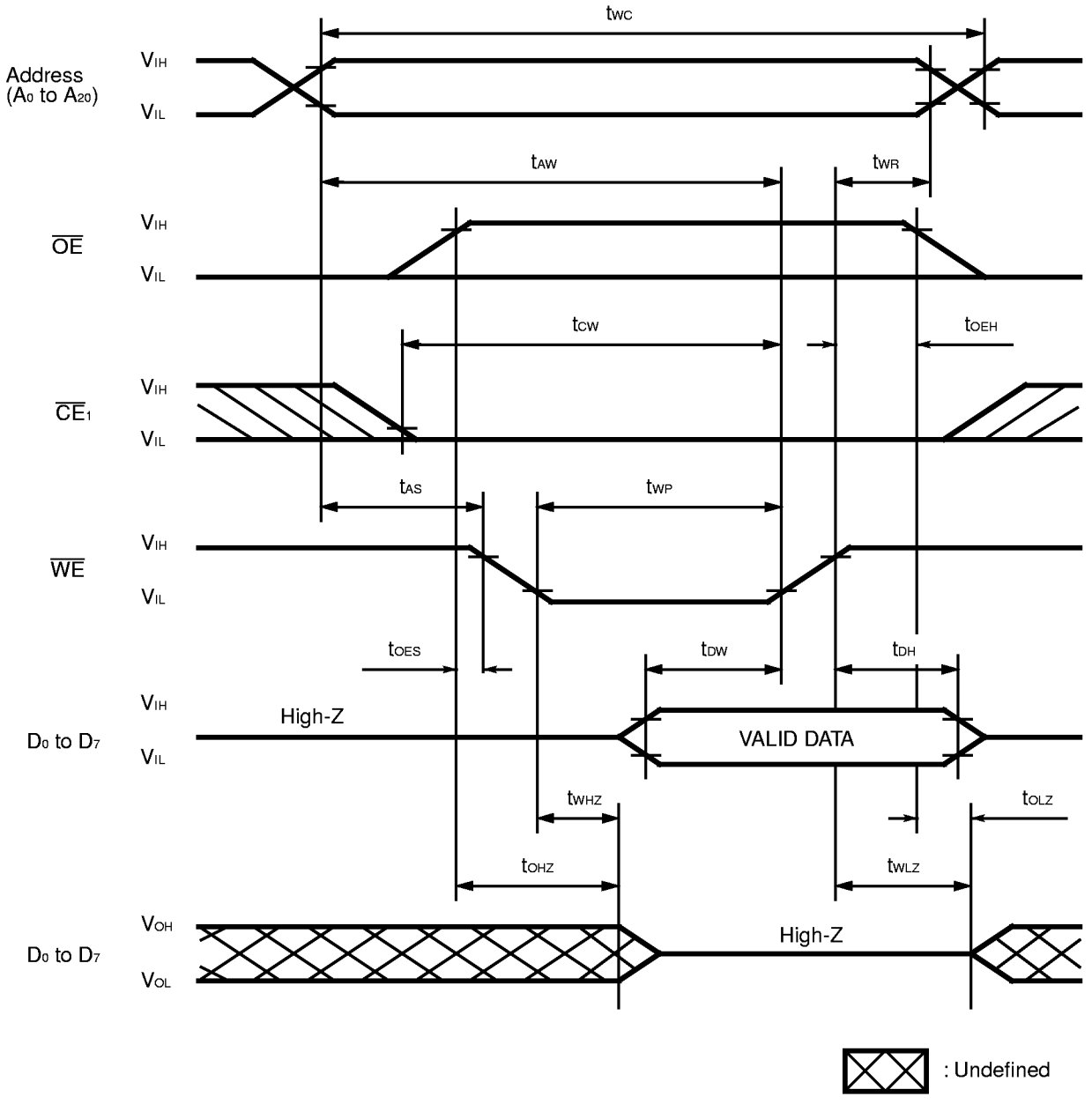
*2. Transition is measured at the point of ±500 mV from steady state voltage.

*3. This parameter is specified only during write cycle with $\overline{OE}$ = V_{IL} and specified using Load II in Fig.3.

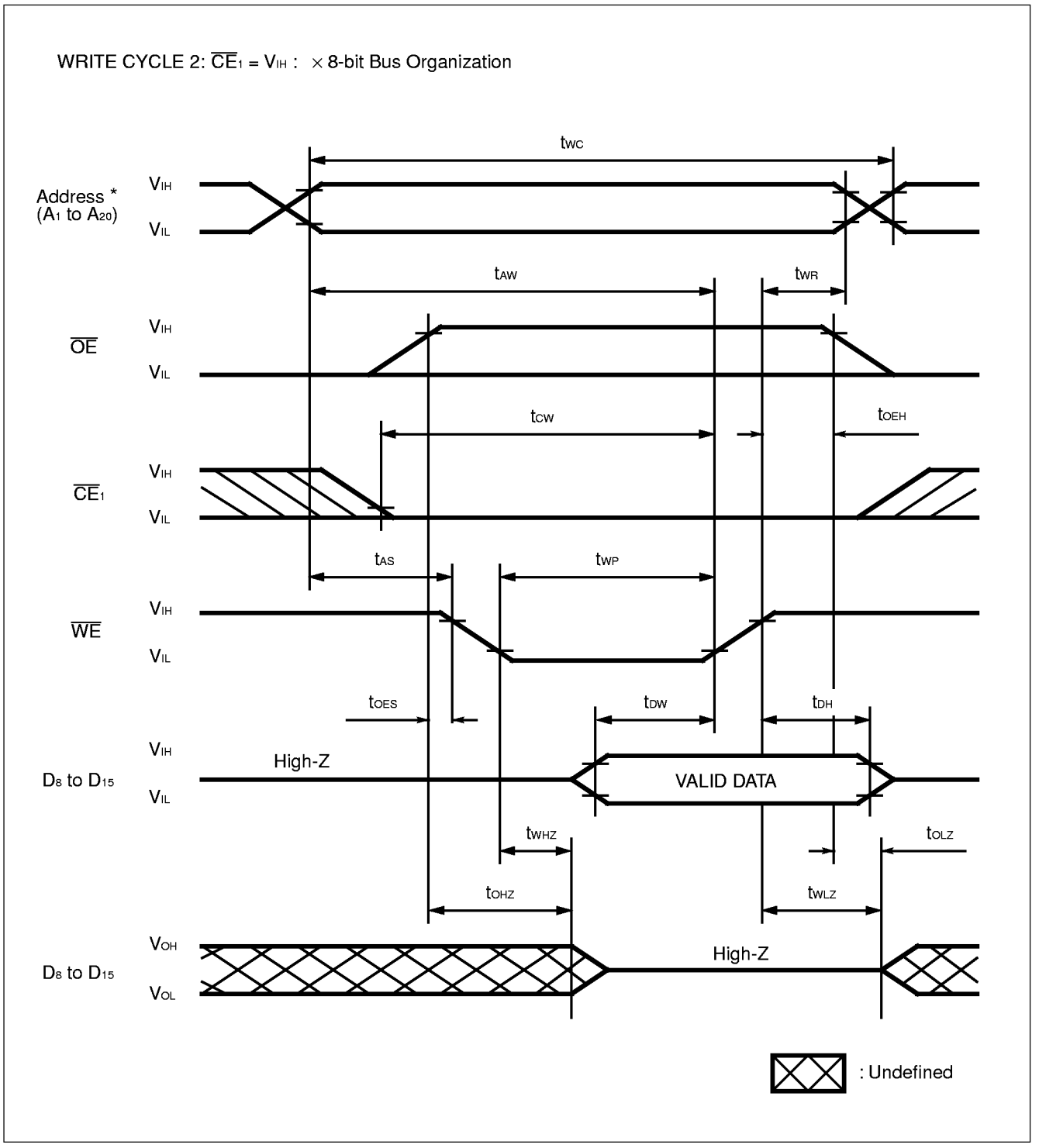
*4. This parameter is for MB98A90833, 90933, 91033 and 91133.

MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{WE}$ = CONTROLLED, $\overline{REG}$ = V_{IH})

WRITE CYCLE 1: $\overline{CE}_2 = V_{IH}$: × 8-bit Bus Organization

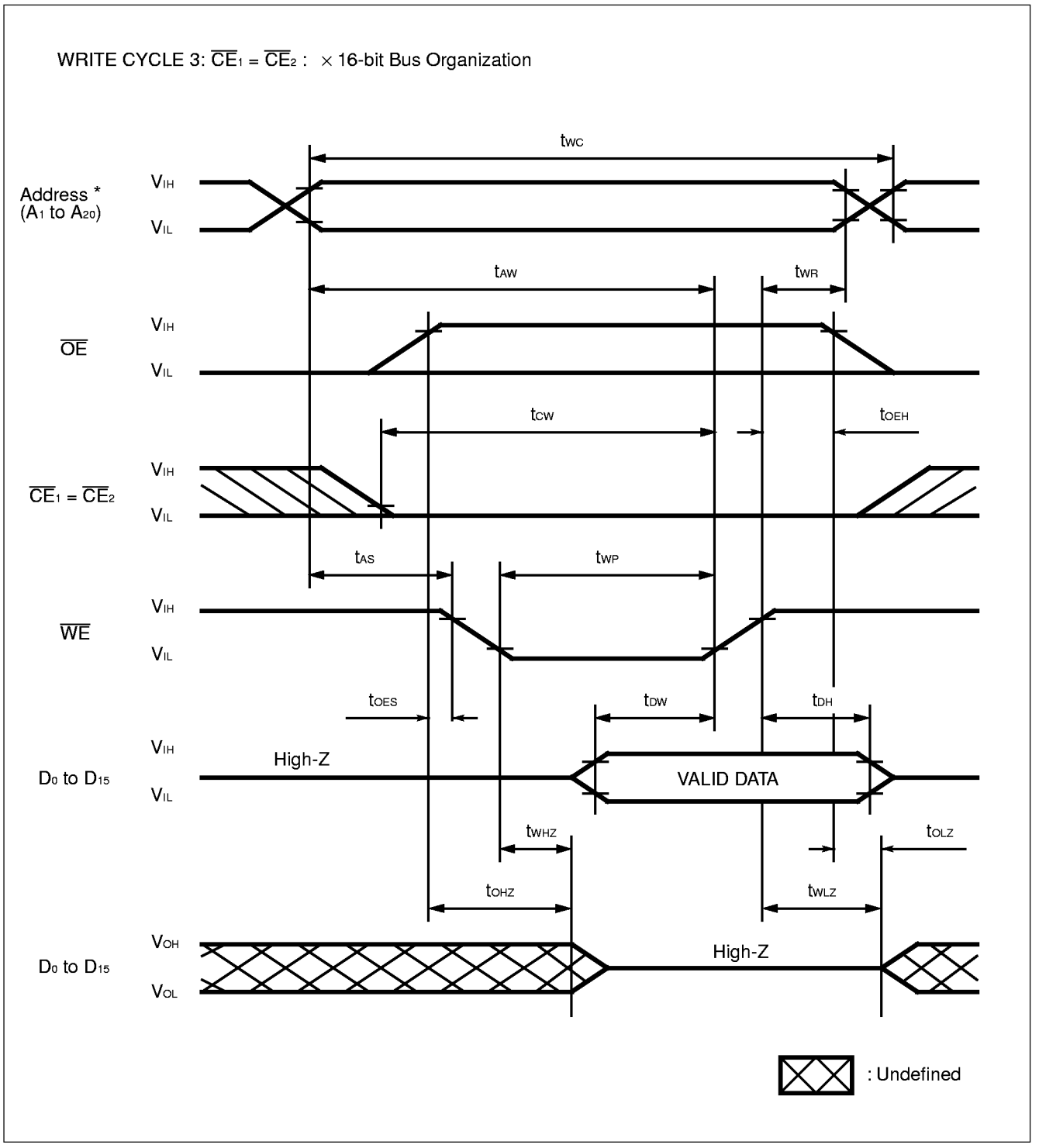


MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{WE}$ = CONTROLLED, $\overline{REG}$ = V_{IH})



Note: * A_0 = Either V_{IH} or V_{IL}.

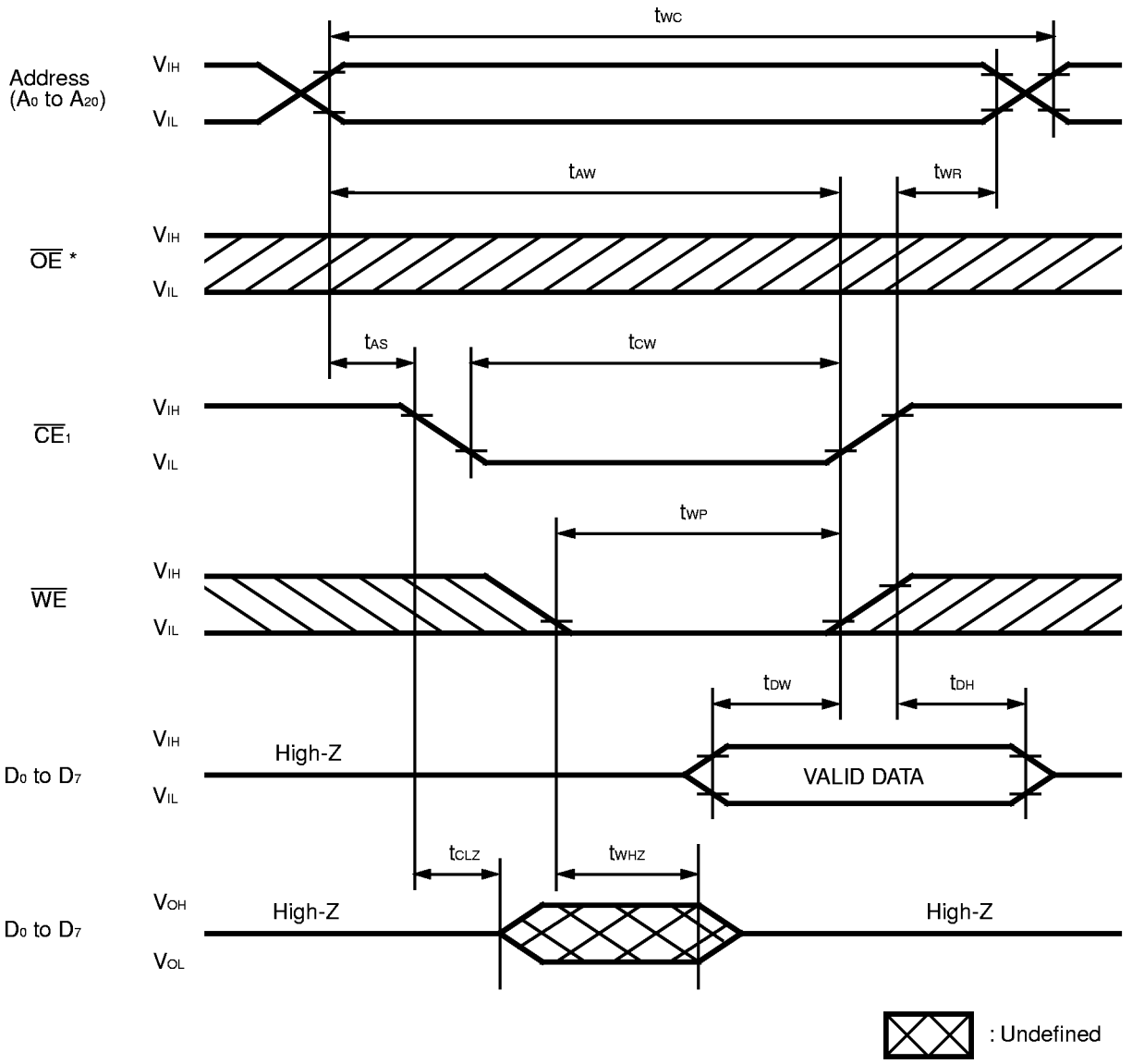
MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{WE}$ = CONTROLLED, $\overline{REG}$ = V_{IH})



Note: * A_0 = Either V_{IH} or V_{IL}.

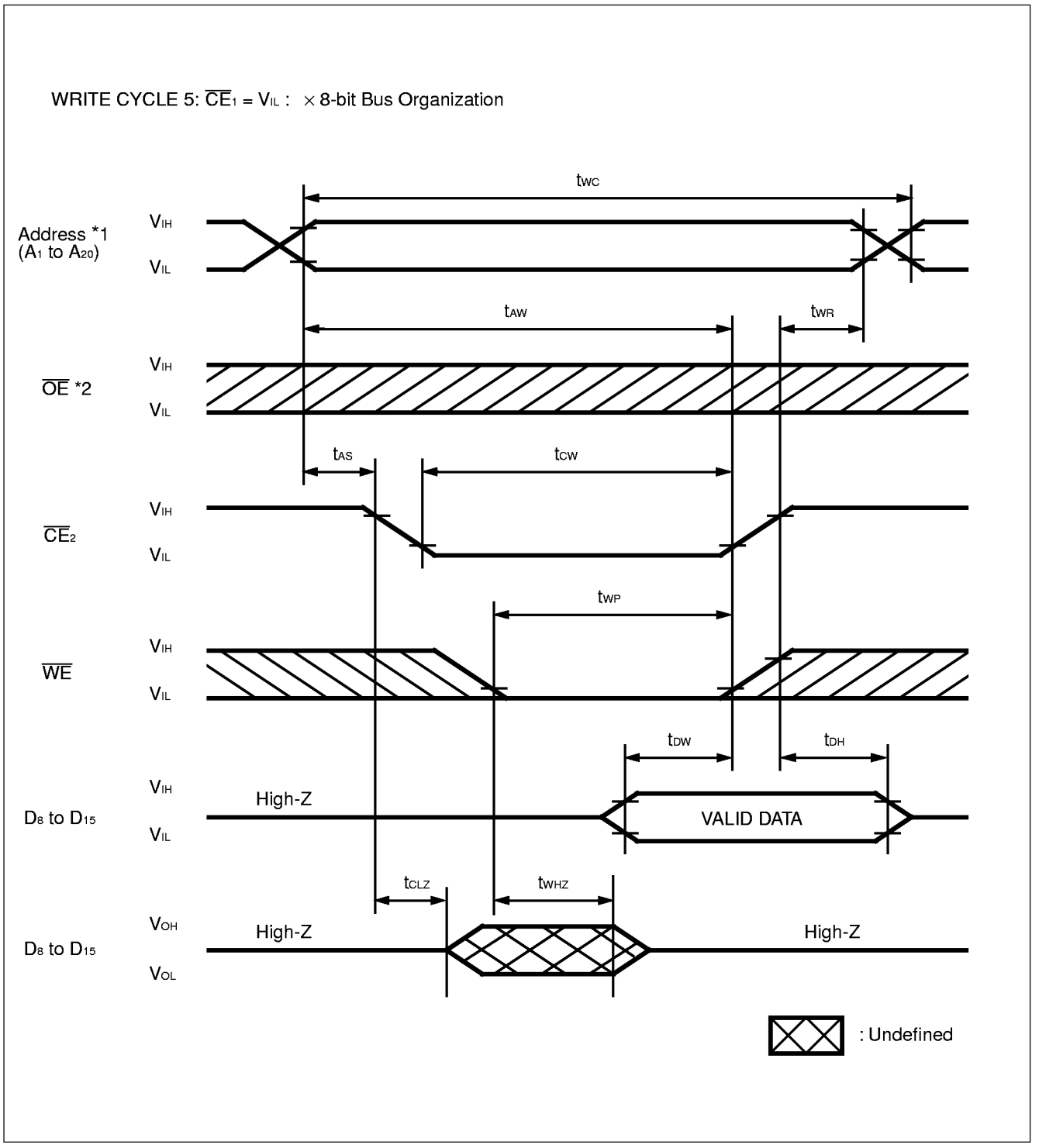
MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{CE}$ = CONTROLLED, $\overline{REG}$ = V_{IH})

WRITE CYCLE 4: $\overline{CE}_2 = V_{IL}$: × 8-bit Bus Organization



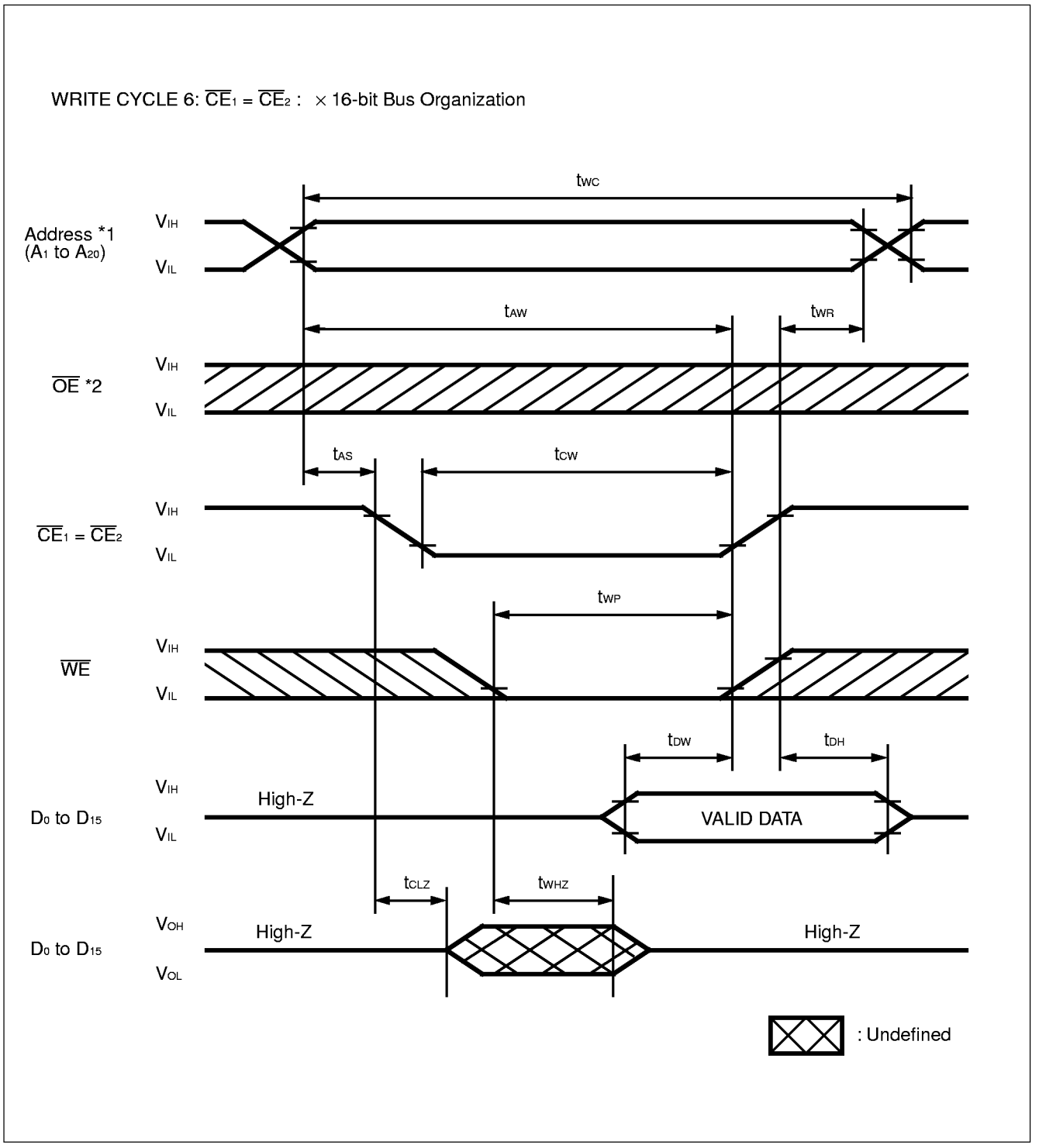
Note: * H-level is recommended for stable operation though the card is operable at L-level.

MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{CE}$ = CONTROLLED, $\overline{REG}$ = V_{IH})



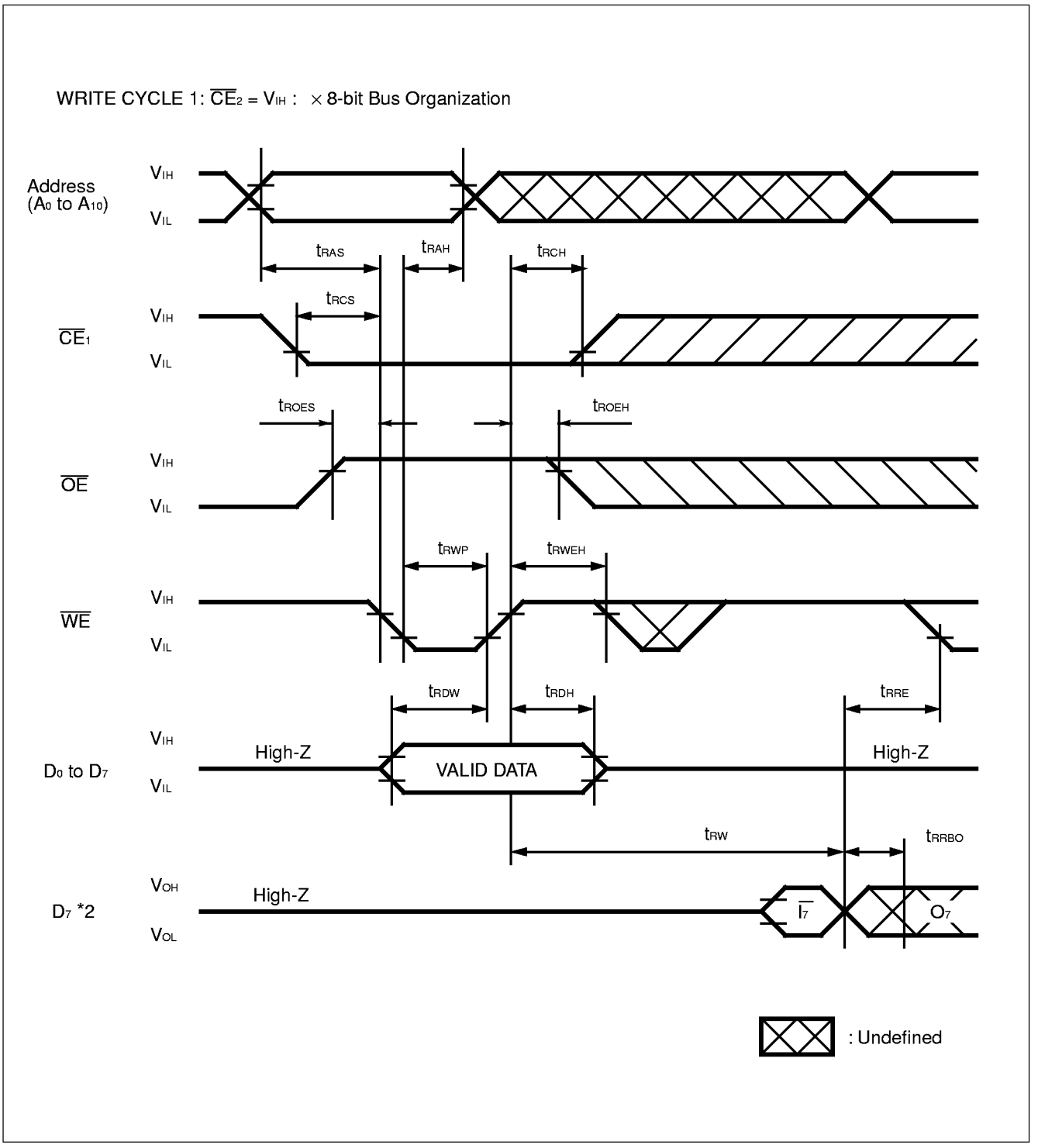
Notes: *1. A_0 = Either V_{IH} or V_{IL}.
*2. H-level is recommended for stable operation though the card is operable at L-level.

MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{CE}$ = CONTROLLED, $\overline{REG}$ = V_{IH})



Notes: *1. A_0 = Either V_{IH} or V_{IL}.
*2. H-level is recommended for stable operation though the card is operable at L-level.

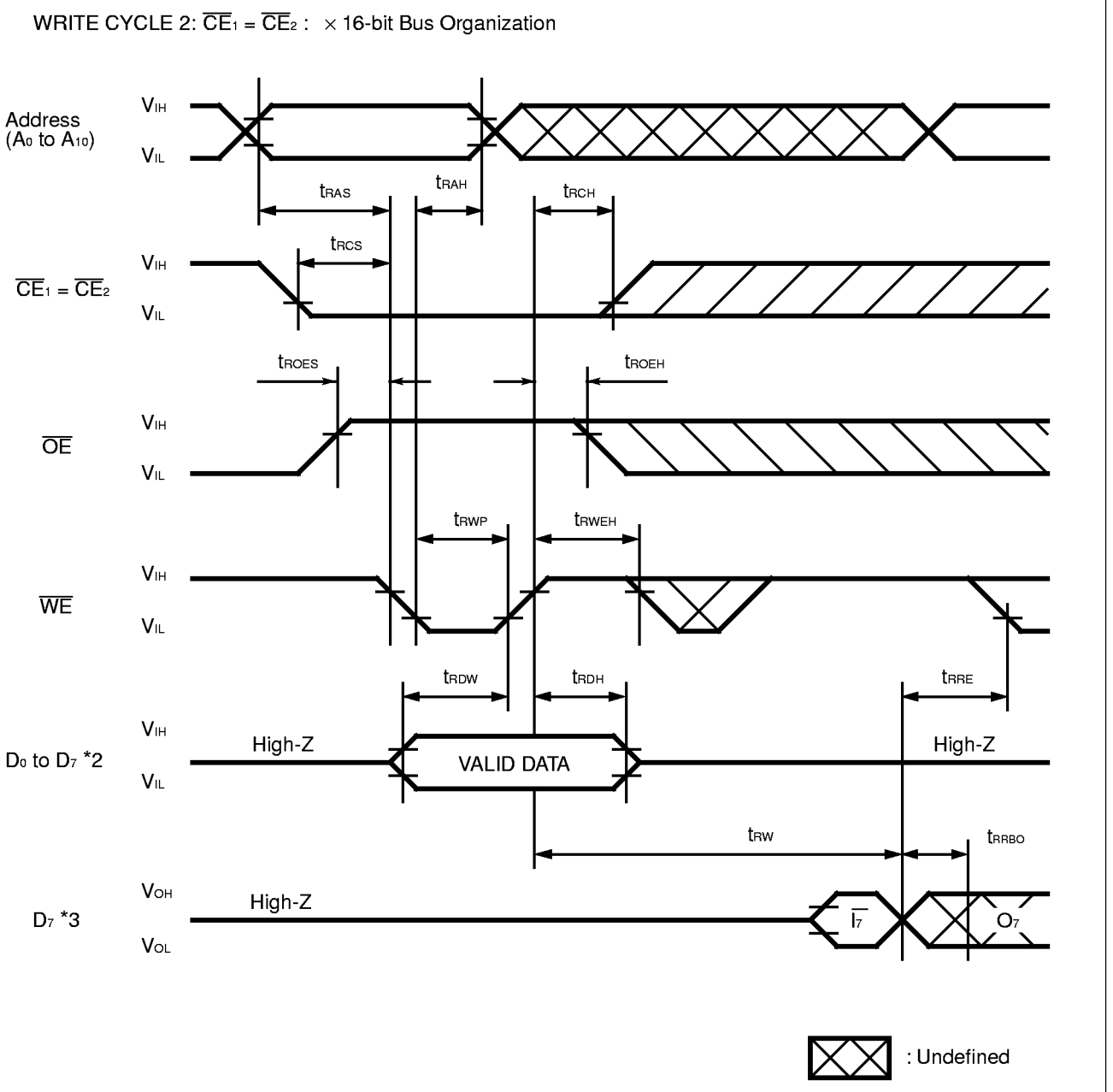
ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{WE}$ = CONTROLLED, $\overline{REG}$ = V_{IL}) *1



Notes: *1. This timing diagram is for MB98A90833, 90933, 91033, and 91133. “FF” data is available on MB98A90832, 90932, 91032, and 91132 only.

*2. Data polling operation.

ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{WE}$ = CONTROLLED, $\overline{REG}$ = V_{IL}) *1

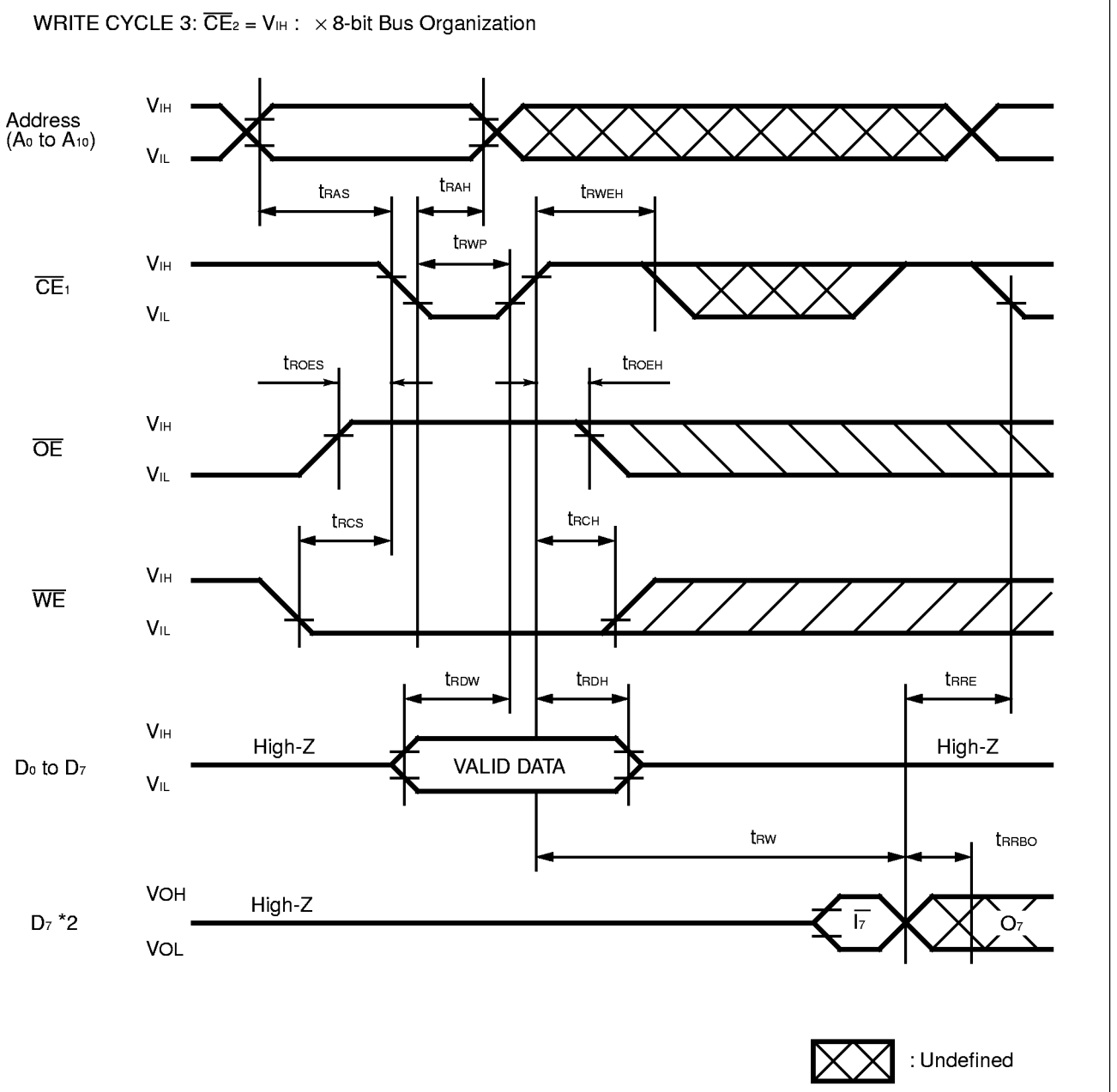


Notes: *1. This timing diagram is for MB98A90833, 90933, 91033, and 91133. “FF” data is available on MB98A90832, 90932, 91032, and 91132 only.

*2. Input levels of terminals D_8 to D_{15} are not specified.

*3. Data polling operation.

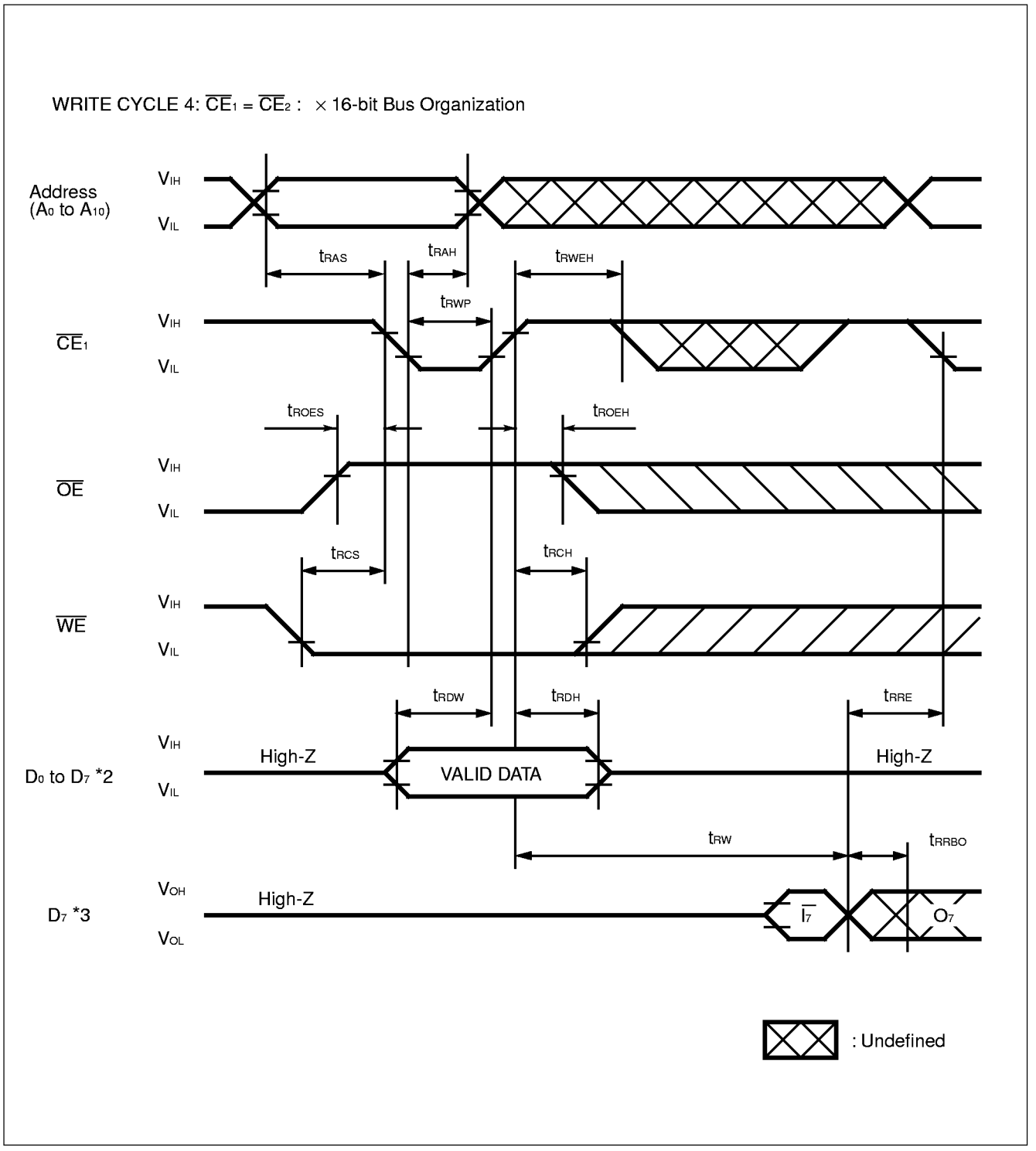
ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{CE}$ = CONTROLLED, $\overline{REG}$ = V_{IL}) *1



Notes: *1. This timing diagram is for MB98A90833, 90933, 91033, and 91133. “FF” data is available on MB98A90832, 90932, 91032, and 91132 only.

*2. Data polling operation.

ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{CE}$ = CONTROLLED, $\overline{REG}$ = V_{IL}) *1

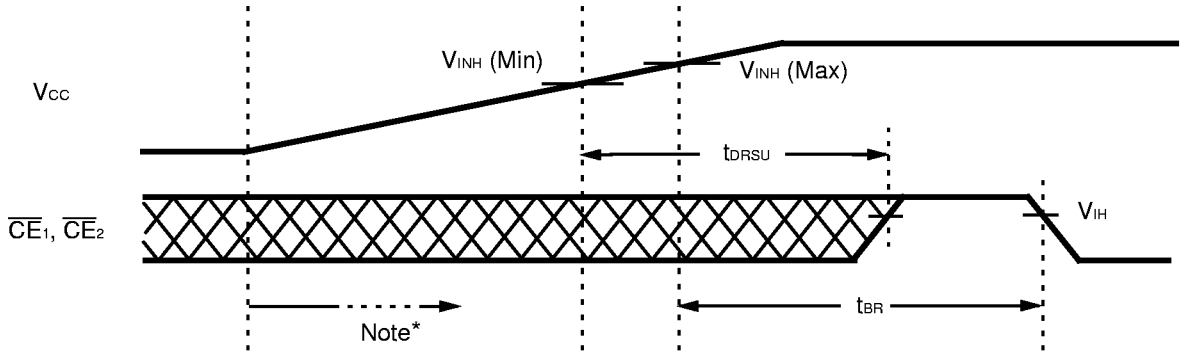


Notes: *1. This timing diagram is for MB98A90833, 90933, 91033, and 91133. "FF" data is available on MB98A90832, 90932, 91032, and 91132 only.
*2. Input levels of terminals D_8 to D_{15} are not specified.
*3. Data polling operation.

■ POWER SUPPLY SEQUENCE CHARACTERISTICS

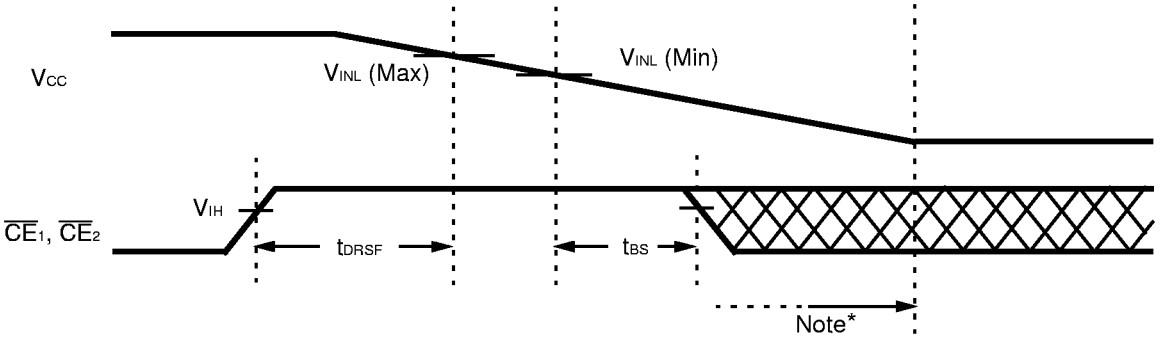
Parameter	Symbol	Min.	Typ.	Max.	Unit
Detection Rising Voltage	V_{INH}	4.2	4.3	4.4	V
Detection Falling Voltage	V_{INL}	4.1	4.2	4.3	V
Battery Backup Recovery Time	t_{BR}	3.0	—	—	ms
Data Retention Rising Time	t_{DRSU}	—	—	0.5	ms
Battery Backup Set Up Time	t_{BS}	10	—	—	µs
Data Retention Falling Time	t_{DRSF}	0	—	—	ns

POWER-ON TIMING DIAGRAM



Note: * Insertion or removal of the card is not recommended when V_{CC} is greater than 0 V.

POWER-OFF TIMING DIAGRAM



Note: * Insertion or removal of the card is not recommended when V_{CC} is greater than 0 V.

■ UNIQUE FEATURES FOR SRAM CARD

1. REPLACEABLE BATTERIES FOR THE SRAM CARD

The battery used in the SRAM Card is a 3.0 V Lithium battery (coin type) with the following specifications:

Diameter : 20.0 (mm)
Thickness : 2.5 (mm)
Weight : 2.5 (g) Approx.
Type : CR2025, or equivalent

2. APPROXIMATE DATA RETENTION TIME WITH BATTERY SUPPORT ONLY

Part Number	Approx. Data Retention Time * (T_A = 20°C)
MB98A9083x	7 years min. 15 years typ.
MB98A9093x	4 years min. 8 years typ.
MB98A9103x	2 years min. 4 years typ.
MB98A9113x	1 year min. 2 years typ.

* Determined by the memory density of the card;
i.e., greater card density means less battery time.

3. REPLACING THE BATTERY IN THE SRAM CARD

a. Insert a slender pointed object, such as the end of a paper clip, into the hole on the upper side of the card. (See Fig. 4.)

b. Release the battery holder by pressing the paper clip against the catch and pulling the battery holder straight out from the card. (The battery cavity is located at the top of the card. See Fig. 5.) When the battery holder is free from the card the battery will fall out.

c. Replace the old battery with a fresh one. Be certain to match battery polarity to the + and – shown on the holder.

d. Place the new battery into the holder, squeeze the holder containing the new battery tightly, and reinsert it into the battery cavity.

WARNING
Battery MUST be replaced within 30 minutes* or data will be lost.

Note: *With condition that the SRAM card had been inserted into application system more than 10 minutes.

Fig. 4 – SRAM CARD DRAWING (TOP VIEW)

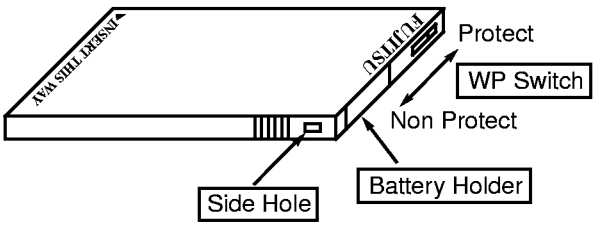
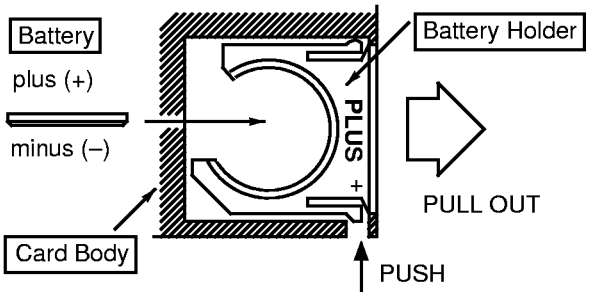


Fig.5 – BATTERY CASE DRAWING (TOP VIEW)



4. SPECIAL MONITORING PINS

4.1 BVD1, BVD2: Voltage Monitoring Pins

These pins monitor the voltage of the battery which must be maintained at 2.65 V or greater for data retention. The condition of the battery is determined by reading the output signals on BVD1 and BVD2.

1. When BVD1=BVD2=V_{OH}
   Battery voltage is sufficient to guarantee data retention; i.e., .2.65 V.

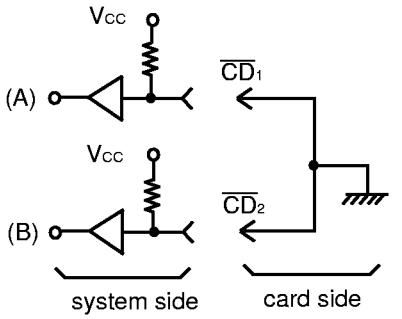
2. When BVD2=V_{OL}, BVD1=V_{OH}
   Battery voltage is lower than 2.65 V and should be replaced to safeguard data.

3. When BVD1=BVD2=V_{OL}
   Battery voltage is less than 2.37 V: the level is dangerous. There is a possibility that data has not retained.

*These functions operate over the Recommended Operating Conditions.

4.2 $\overline{CD}_1$, $\overline{CD}_2$: Card Detection Pins

These pins detect the insertion of the card into the system. (See Fig. 6.)
When the memory card has been correctly inserted, $\overline{CD}_1$ and $\overline{CD}_2$ are detected by the system. $\overline{CD}_1$, $\overline{CD}_2$ are tied to ground on the card side as shown in Fig. 6.



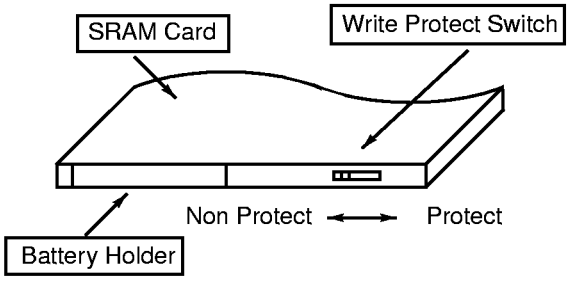
- Fig. 6 -

4.3 WP: Write Protect Pins

This pin monitors the position of the Write Protect switch. As shown in Fig. 7, the SRAM card has a Write Protect switch at the top of the card.

To write to the card, the switch must be turned to the "Non Protect" position and the $\overline{WE}$ pin low. L-level is output on the WP pin.

To prevent writing to the card, the switch must be turned to the "Protect" position. H-level is output on the WP pin.



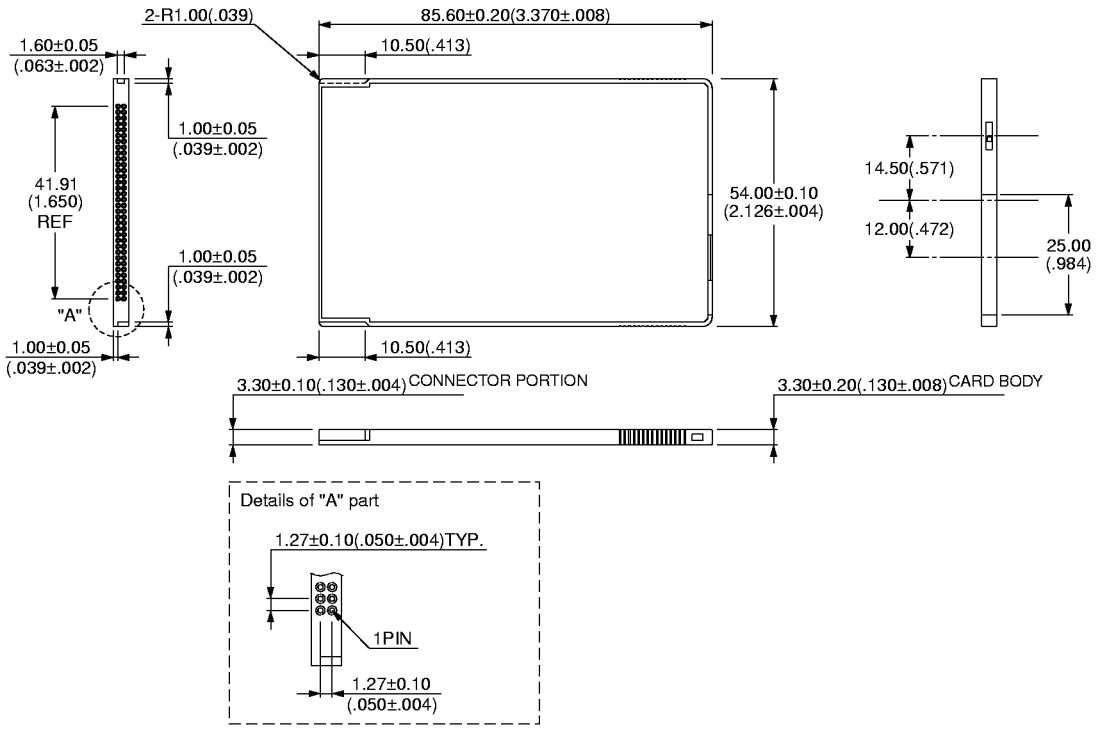
- Fig. 7 -

WP Switch	WP Pin
Protect	H
Non Protect	L

■ PACKAGE DIMENSIONS

68-PIN MEMORY CARD
(CASE No.: CRD-68P-M04)

Note: Dimensions comform with PCMCIA/JEIDA. (PC CARD STANDARD 95)



Dimensions in mm (inches)

■ DEVICE HANDLING PRECAUTIONS

This device in composed of fine electronic parts, so take care in handling or keeping it as below.

- The card is made fine, so do not keep it in the high temperature nor high humiditly, place line in the direct sunshine nor near the heater.
- The card should not be bent, scratched, dropped nor be shocked violently.
- This device should never be taken a part. It could destroy the card or your personal computer hardware.
- To help you handle this device safely, request us the device specifications when purchasing this device.