August 1993
Edition 2.0

FUJITSU

DATA SHEET

MBM27C1024A-10/-12/-15

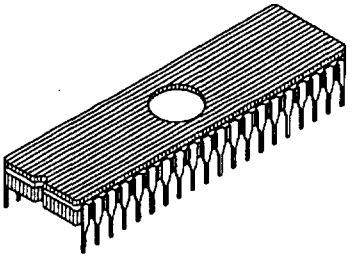
CMOS 1M-BIT UV EPROM

CMOS 1,048,576–BIT UV ERASABLE READ ONLY MEMORY (EPROM)

The Fujitsu MBM27C1024A EPROM is a high speed read-only static memory that is UV-erasable and reprogrammable. The device contains 1,048,576 programmable or reprogrammable bits organized in a 65,536-word/16-bit format. The MBM27C1024A is housed in a 40–pin DIP with a transparent lid; when the lid is properly exposed to an ultraviolet light source, a previously programmed bit pattern is erased in approximately 15 to 20 minutes. A new bit pattern can then be written into memory.

The MBM27C1024A EPROM is fabricated using CMOS double poly-silicon gate technology with stacked single–transistor gate cells. The MBM27C10024A is an excellent choice for system development work and in other applications where programmed, the device requires only a single +5V power supply; the current requirements are exceptionally low in both the active and standby modes of operation.

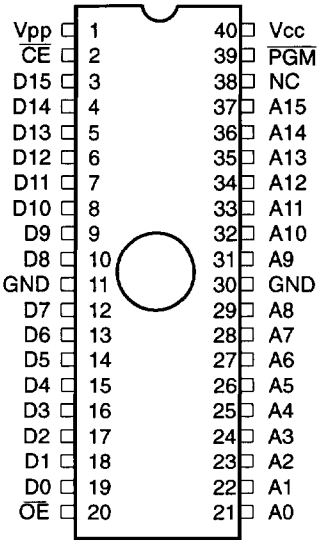
- 65,536-word/16-bit organization with on-chip decoding
- One-Word or Two-Word programming capability with high speed programming algorithm
- Static operation (no clocks required)
- Fast access time:
  - 100ns max. (MBM27C1024A-10)
  - 120ns max. (MBM27C1024A-12)
  - 150ns max. (MBM27C1024A-15)
- Easy and simple memory expansion via @pin
- Three-state output for wired-OR capability
- TTL compatible inputs/outputs
- Single =5V (± 10%) power supply with low current drain:
  - Active operation = 50mA max. (100ns/120ns)
  - Active operation = 40mA max. (150ns)
  - Standby operation = 0.1mA max.
- Programming voltage: +12.5V
- JEDEC approved pin assignment
- 40-pin ceramic DIP Package (Suffix: P)



CERAMIC PACKAGE
DIP-40C-C02

PIN ASSIGNMENT

(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage with respect to ground	V_{CC}	− 0.6 to + 7.0	V
Programming Voltage with respect to ground	V_{PP}	− 0.6 to + 14.0	V
Input/Output Voltage (except for A_9 with respect to ground)	V_{IN1}, V_{OUT}	−0.6 to V_{CC} +0.6	V
Programming Voltage with respect to ground	V_{IN2}	−0.6 to +13.5	V
Temperature under Bias	T_{BIAS}	−25 to +85	°C
Storage Temperature Range	T_{STG}	− 65 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

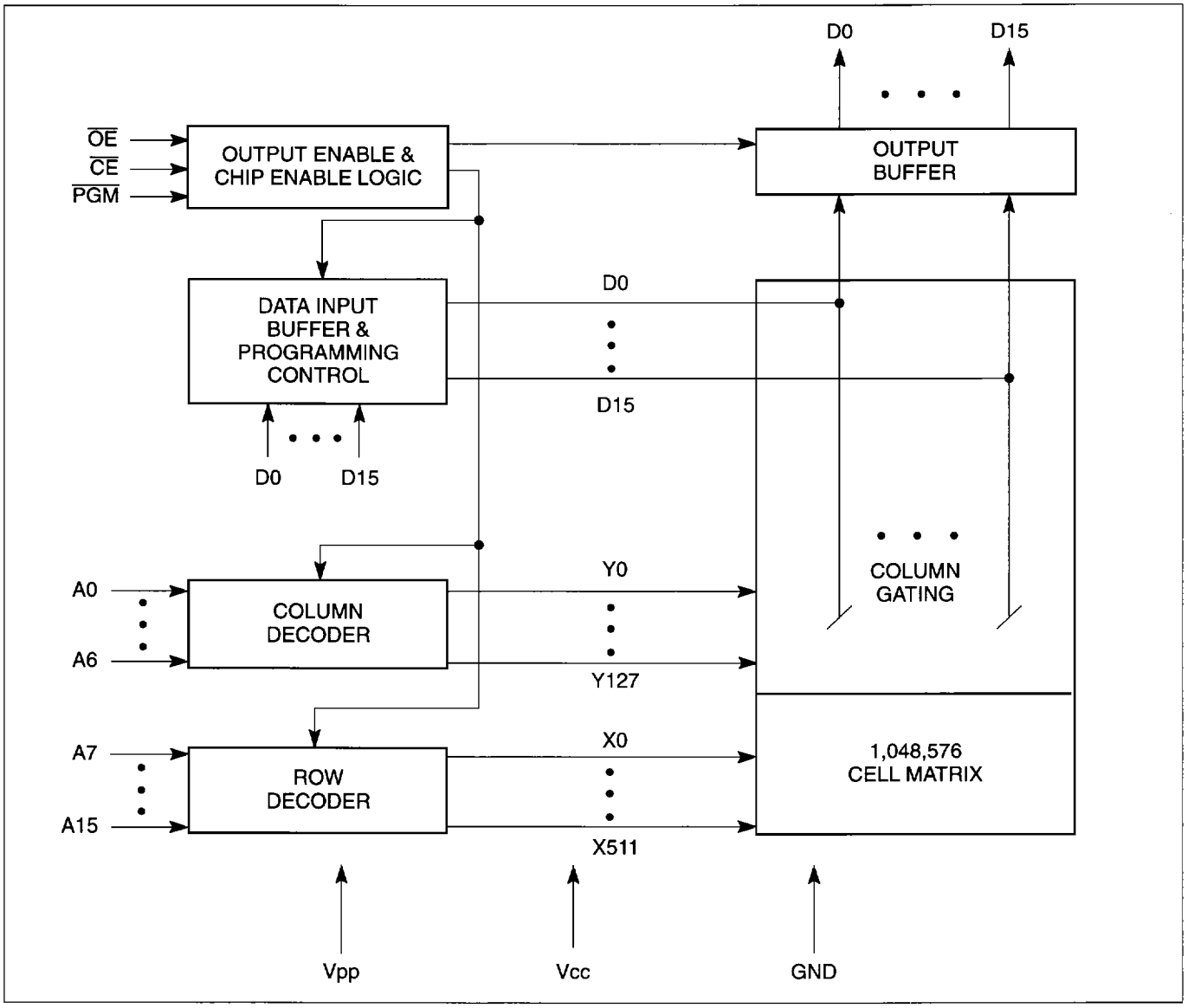


Figure 1. Block Diagram

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Input Capacitance, (V_{IN} = 0V)	C_{IN}		5	20	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}		8	20	pF

PIN DESCRIPTION

Symbol	Pin No.	Function
V_{PP}	1	+5V power supply. When +12.5V is applied, the device is enabled for programming operation.
$\overline{CE}$	2	Chip enable. When active Low, the device is enabled for data read and programming operations.
D_0 to D_{15}	3 to 10, 12 to 19	Three-state output data lines
GND	11, 30	Circuit ground
$\overline{OE}$	20	Output enable. When active Low, all output lines are enabled.
A_0 to A_{15}	21 to 29, 31 to 37	Address lines
NC	38	No connection
$\overline{PGM}$	39	When active Low, programming data from the input buffer is written into a specified address of memory.
V_{CC}	40	+5V power supply

FUNCTIONS AND PIN CONNECTIONS

OPERATING MODE	A_0 to A_8	A_9	A_{10} to A_{16}	Data	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{CC}	V_{PP}	GND
Standby	X	X	X	Hi-Z	V_{IH}	X	X	5V	5V	0V
Read	A_{IN}	A_{IN}	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	5V	5V	0V
Output Disable	A_{IN}	A_{IN}	A_{IN}	Hi-Z	V_{IL}	V_{IH}	X	5V	5V	0V
						X	V_{IL}			
Electronic Signature	Note 1	12V	A_0	CODE	V_{IL}	V_{IL}	V_{IH}	5V	5V	0V
One-Word Program	A_{IN}	A_{IN}	A_{IN}	D_{IN}	V_{IL}	V_{IH}	V_{IL}	6V	12.5V	0V
One-Word Verify	A_{IN}	A_{IN}	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	6V	12.5V	0V
One-Word Program Inhibit	A_{IN}	A_{IN}	A_{IN}	Hi-Z	V_{IL}	V_{IH}	V_{IH}	6V	12.5V	0V
Two-Word Program (Latch)	A_{IN}	A_{IN}	A_{IN}	D_{IN}	V_{IH}	V_{IH}	V_{IH}	6V	12.5V	0V
Two-Word Program	Note 2	A_{IN}	A_{IN}	HI-Z	V_{IH}	V_{IL}	V_{IL}	6V	12.5V	0V
Two-Word Verify	A_{IN}	A_{IN}	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	6V	12.5V	0V
Two-Word Program Inhibit	A_{IN}	A_{IN}	A_{IN}	HI-Z	V_{IH}	V_{IL}	V_{IH}	6V	12.5V	0V

Legend:
X = Don't care

Notes:
1. A_0 is toggling address.
2. A_0 is "X".

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage *1	V_{PP}	V_{CC} −0.6	V_{CC}	V_{CC} +0.6	V
Input High Level	V_{IH}	2.0	—	V_{CC} +0.3	V
Input Low Level	V_{IL}	−0.3	—	0.8	V
Operating Temperature	T_A	0	—	70	°C

*1: V_{PP} supply voltage is applied posterior to or coincident with V_{CC} supply voltage and cut off prior to or coincident with V_{CC} supply voltage.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Conditions	Values			Unit
				Min.	Typ.	Max.	
Input Leakage Current		$\|I_{LI}\|$	$V_{IN} = V_{CC} = 5.5V$			10	µA
Output Leakage Current		$\|I_{LO}\|$	$V_{OUT} = V_{CC} = 5.5V$			10	µA
V_{CC} Standby Current		I_{SB1}	$\overline{CE} = V_{IH}$			1.0	mA
V_{CC} Standby Current		I_{SB2}	$\overline{CE} = V_{CC} \pm 0.3V$			100	µA
V_{CC} Operation Current	100ns/120ns	I_{CC}	Cycle = min., I_{OUT} = 0mA			50	mA
	150ns					40	mA
V_{PP} Supply Current		I_{PP}	$V_{PP} = V_{CC} \pm 0.6V$			100	µA
Output High Level		V_{OH1}	I_{OH} = -400µA	2.4			V
Output High Level		V_{OH2}	I_{OH} = -100µA	V_{CC} -0.7			V
Output Low Level		V_{OL}	I_{OL} = 2.1mA			0.45	V

AC CHARACTERISTICS

(Recommended operating conditions unless other noted)

Parameter	Symbol	MBM27C1024A-10		MBM27C1024A-12		MBM27C1024A-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}		100		120		150	ns
$\overline{CE}$ to Output Delay Time	t_{CE}		100		120		150	ns
$\overline{OE}$ to Output Delay Time	t_{OE}		50		60		70	ns
$\overline{PGM}$ to Output Delay Time	t_{PGM}		50		60		70	ns
$\overline{CE}$ or $\overline{OE}$ to Output Float Delay (Note)	t_{DF}		50		50		60	ns
Address to Output Hold Time	t_{OH}	0		0		0		ns

Note: Output Float is defined as the point where data is no longer driven.

AC TEST Conditions

Input Pulse Levels:	0.45V to 2.4V
Input Rise/Fall Times:	≤20ns
Input Reference Levels:	0.8V to 2.0V
Output Reference Levels:	0.8V to 2.0V
Output Load:	1 TTL gate and CL = 100pF

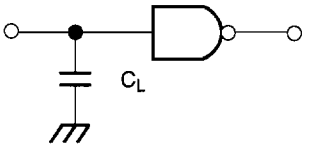
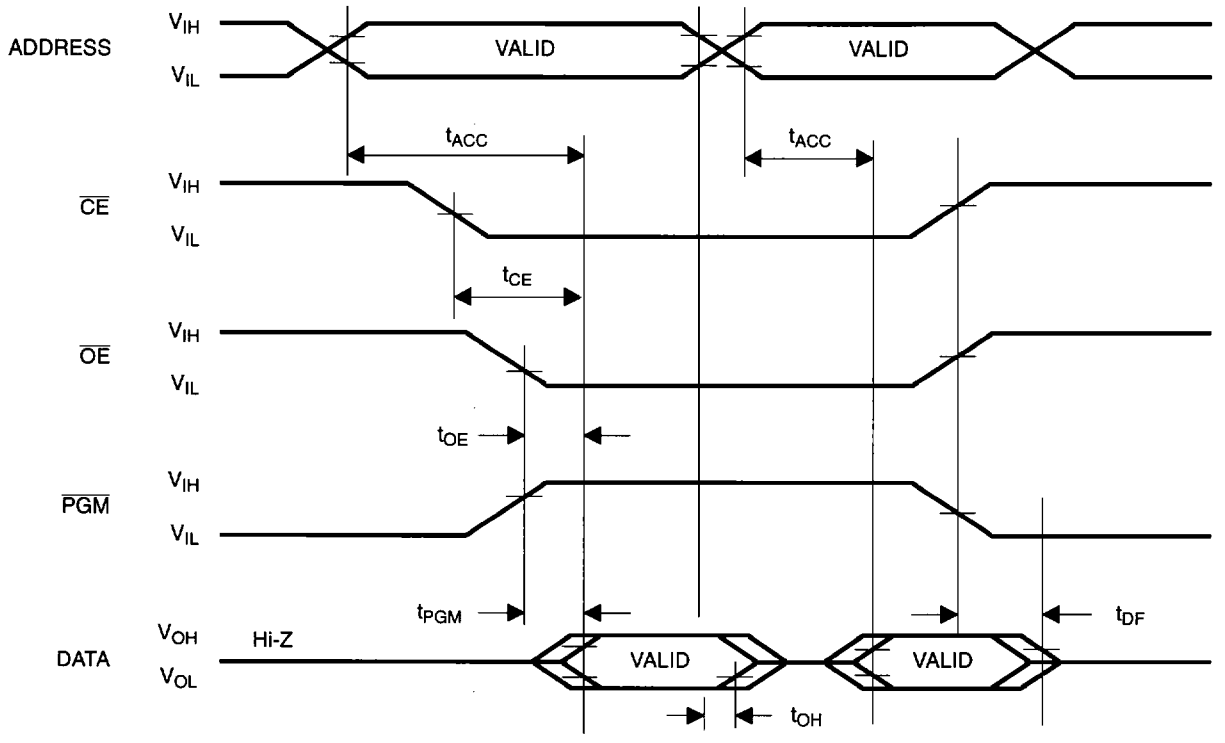


Figure 2. AC Test Conditions

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

READ WAVEFORM



PROGRAMMING/ERASING INFORMATION

PROGRAMMING

One-Word Programming. When +12.5V (±0.3) volts is applied to V_{PP}, +6 (±0.25) volts is applied to V_{CC}, $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ and $\overline{PGM} = V_{IH}$, the programming mode is initiated. Next, the proper address is input and the data pattern is applied to the input buffer (Figure 1). When both address and data are stable, a 0.5-millisecond negative pulse is applied to the $\overline{PGM}$ pin. Upon verification of written data an over pulse (three times the initial pulse width times the number of pulses used to accomplish a write) should be applied to complete the programming of one byte. Refer to the PROGRAMMING FLOWCHART that follows for step-by-step programming procedures.

Two-Word Programming. When compared to single-byte programming, the two-word programming method reduces the programming time by about 75% one quarter. Voltages applied to V_{PP} and V_{CC} are the same as those for single-byte programming; however, some logic levels differ; refer to "Two-Word Programming" in the Truth Table. In conjunction with the $\overline{OE}$ pin, address pins A_0 and A_1 are used to latch four bytes of data. When both address and data are stable, a 0.5 millisecond negative pulse is applied to the $\overline{PGM}$ pin. Upon verification of written data an over pulse (three times the initial pulse width times the number of pulses used to accomplish a write), should be applied to complete the programming of four bytes. Refer to the PROGRAMMING FLOWCHART for step-by-step programming procedures.

Caution

The width of one programming pulse must not exceed 40-milliseconds; thus, a continuous TTL low-level voltage should not be applied to the $\overline{PGM}$ pin. Also, a 0.1-microfarad capacitor must be connected between V_{PP} and ground to prevent excessive voltage transients. Neglecting either of these precautions may cause device failure.

Electronic Signature/Programming Algorithm. When the MBM27C1024A is shipped from the factory, all memory cells (1,048,576 bits) are set to the High state (logic 1). During the programming procedure, affected bit cells are set to the Low (logic 0) state.

The MBM27C1024A is programmed with a fast programming algorithm designed by Fujitsu called high speed programming. Manufacturer and device codes are electronically stored in each device; these codes can be read at the output port (D_0 to D_7) for the purpose of matching the device with the high speed programming algorithm. The Electronic Signature Code List is shown in the table preceding the ELECTRICAL CHARACTERISTICS.

ERASING

In order to clear all memory cells of programmed contents, the MBM27C1024A must be exposed to an ultraviolet light source. To completely erase the memory (restore all cells to a logic 1 state), a dosage of 10Wsec/cm^2 is required. The required exposure can be obtained by using a UV-lamp with a wavelength of 2537 Angstroms and with an intensity of 12mW/cm^2. Remove all filters from the lamp and clean the transparent lid of the MBM27C1024A with a non-abrasive cleaner. Hold the MBM27C1024A approximately one inch from the light source for 15 to 20 minutes. (Note: The MBM27C1024A and other similar devices can be erased by light sources with longer wavelengths: However, the erasing time is much greater. Nonetheless, exposure to florescents or sunlight will severely degrade and eventually erase the memory. When used in a lighted environment, it is recommended that the transparent window be covered with an opaque label.)

ELECTRONIC SIGNATURE CODE LIST

Definition	A_0	A_1	A_2 to A_8	A_9	A_{10} to A_{16}	D_0	D_1	D_2	D_2	D_4	D_5	D_6	D_7	D_8 to D_{15}	HEX
Manufacture	V_{IL}	V_{IL}	V_{IL}	12(±0.5)V	V_{IL}	0	0	1	0	0	0	0	0	0	#04
Device	V_{IH}	V_{IL}	V_{IL}	12(±0.5)V	V_{IL}	0	0	1	0	0	1	1	0	0	#64

PROGRAMMING INFORMATION

DC CHARACTERISTICS

(T_A = 25°C ± 5°C, V_{CC} *1 = 6V ± 0.25V, V_{PP} *2 = 12.5V ± 0.3V)

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Input Leakage Current	$\|I_{LI}\|$	V_{IN} = 6.25V/0V			10	µA
V_{PP} Supply Current (Single-Byte)	I_{PP1}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, $\overline{PGM}$ = V_{IL}			30	mA
V_{PP} Supply Current (Four-Byte)	I_{PP2}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IL}			50	mA
V_{PP} Supply Current	I_{PP3}	$\overline{PGM}$ = V_{IH}			5	mA
V_{PP} Supply Current	I_{PP4}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}			5	mA
V_{CC} Supply Current	I_{CC}				50	mA
Input Low Level	V_{IL}		-0.1		0.8	V
Input High Level	V_{IH}		2.0		V_{CC} +0.3	V
Output Low Level	V_{OL}	I_{OL} = 2.1mA			0.45	V
Output High Level	V_{OH}	I_{OH} = -400µA	2.4			V

NOTE: *1. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
*2. V_{PP} must not be 13.5 volts or more including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 12.5 volts. Also, during $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, V_{PP} must not be switched from V_C to V_{PP} volts or visa versa.

AC CHARACTERISTICS

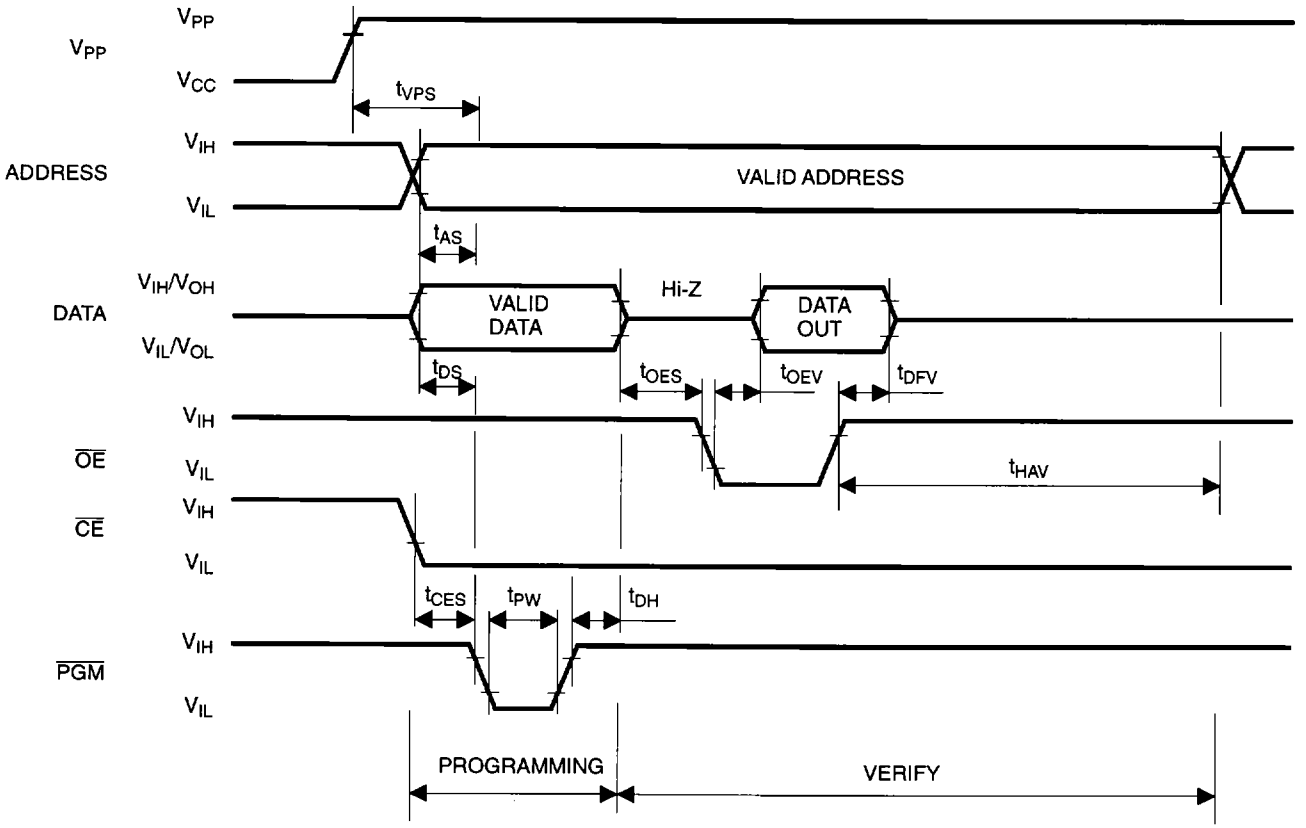
(T_A = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Address Setup Time	t_{AS}	0.5			µs
Address Hold Time	t_{AH}	0.5			µs
Data Setup Time	t_{DS}	0.5			µs
Data Hold Time	t_{DH}	0.5			µs
$\overline{OE}$ Hold Time ("H")	t_{OEH}	0.5			µs
Hold Time Before Programming	t_{HBP}	2			µs
Hold Time After Programming	t_{HAP}	2			µs
V_{PP} Setup Time	t_{VPS}	2			µs
Input Data Floating Setup Time	t_{DFS}	1			µs
Programming Pulse Width *1	t_{PW}	95	100	105	µs
Programming Pulse Width *2	t_{PW}	475	500	525	µs
Over Programming Pulse Width *2	t_{OPW}	1.4		39.4	ms
Over Programming Pulse Number *1	N	1		50	times
Over Programming Pulse Number *2	N	1		25	times
$\overline{CE}$ Setup Time	t_{CES}	2			µs
$\overline{OE}$ Setup Time	t_{OES}	2			µs
Address Access Time at Verify	t_{ACV}			500	ns
Output Disable to Data Out	t_{OEV}			500	ns
$\overline{OE}$ to Output Float	t_{DFV}			150	ns
Hold Time After Verify	t_{HAV}	0			µs

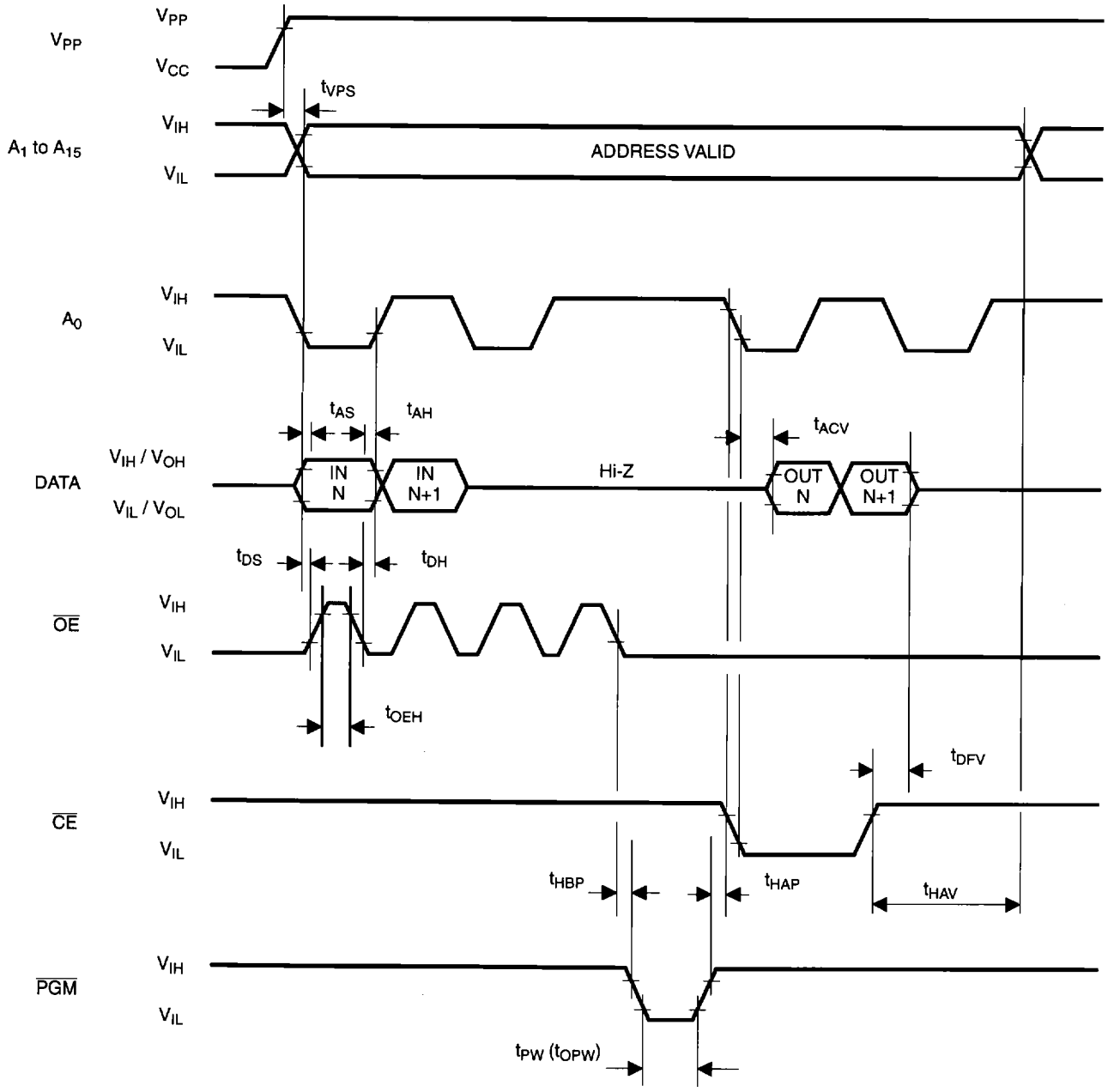
NOTES:

*1: Advanced Quick Programming
*2: Quick Programming

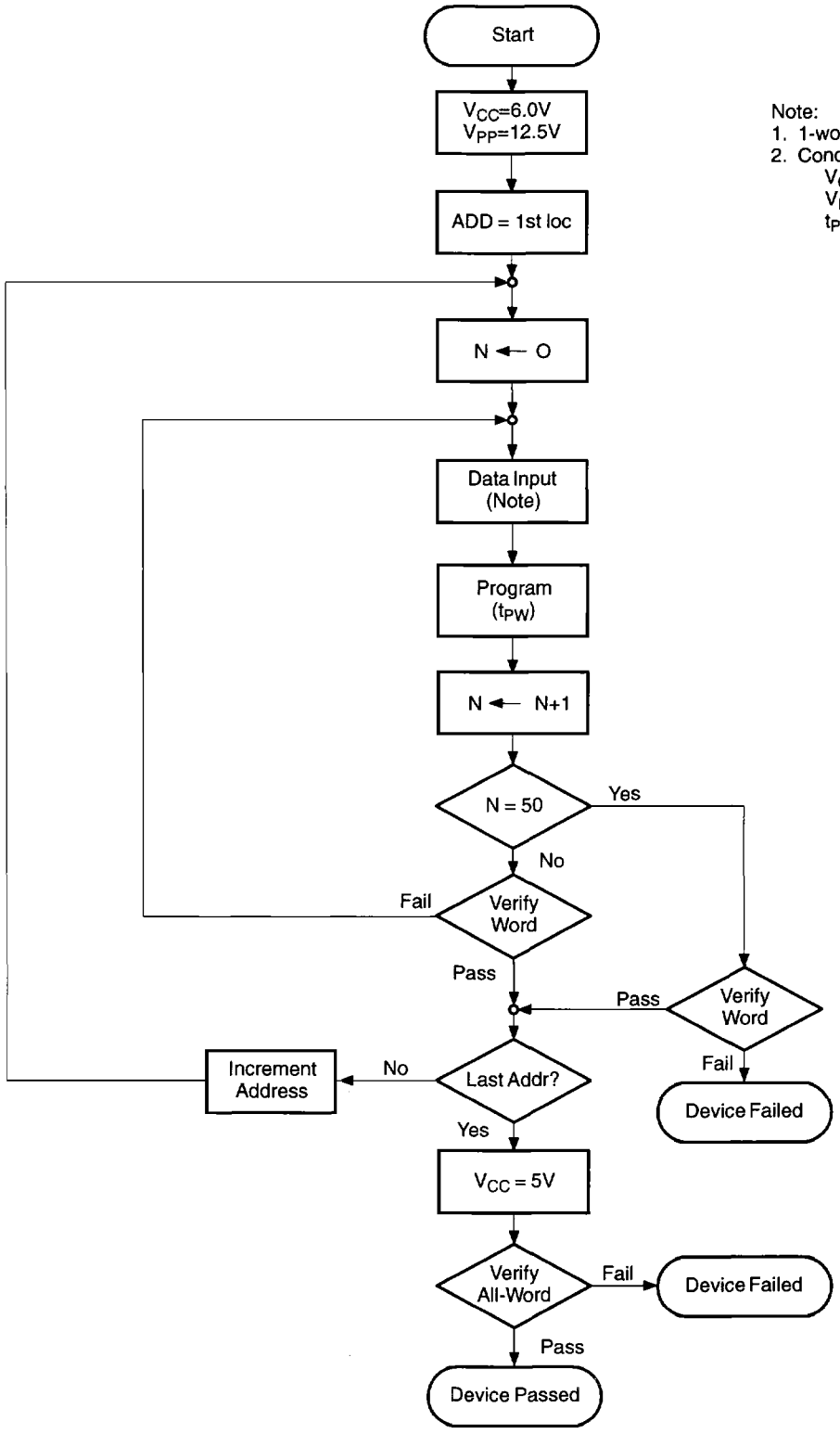
PROGRAMMING WAVEFORM (ONE-WORD)



PROGRAMMING WAVEFORM (TWO-WORD)

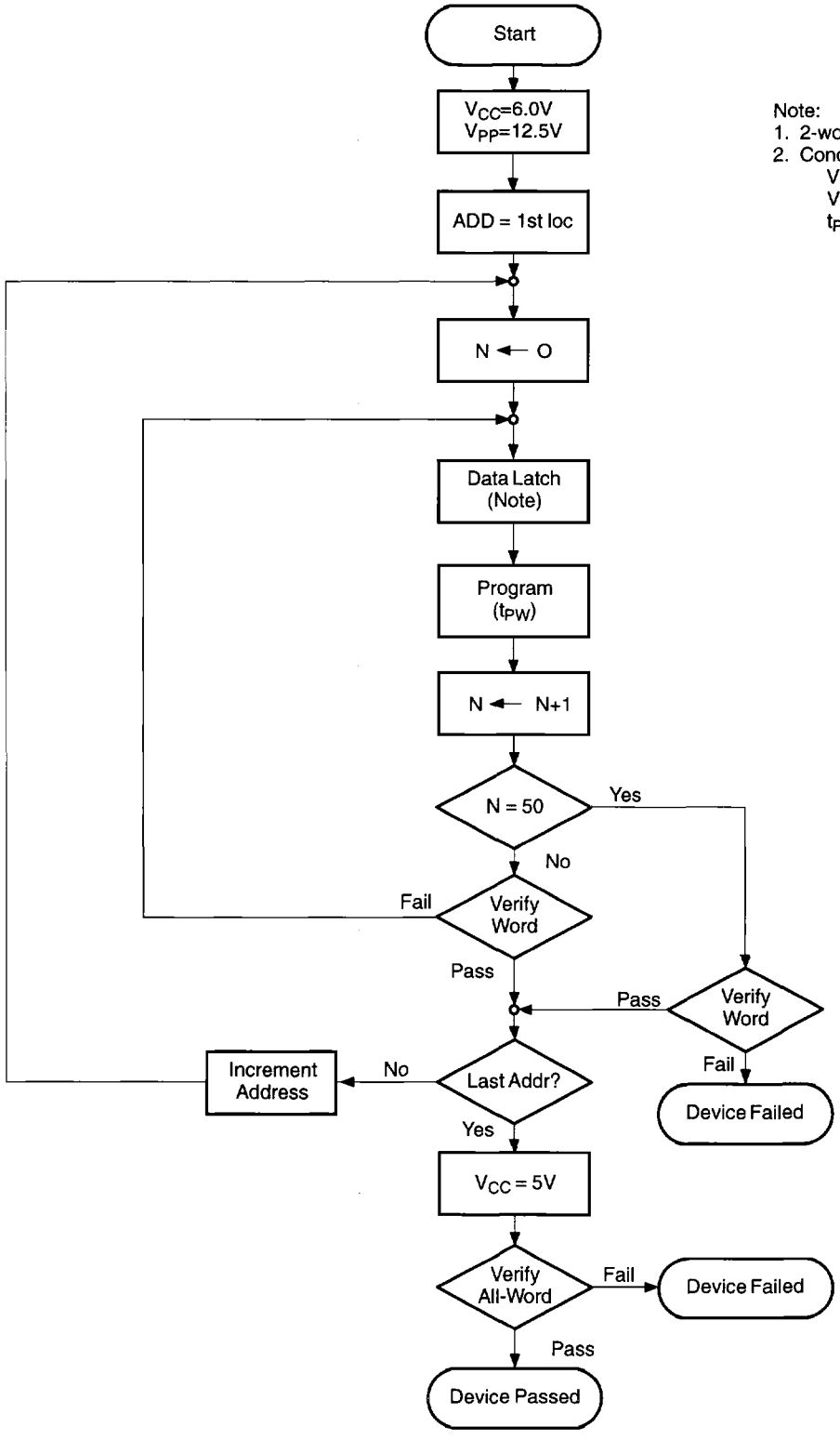


ONE-WORD PROGRAMMING FLOWCHART (ADVANCED QUICK PROGRAMMING)



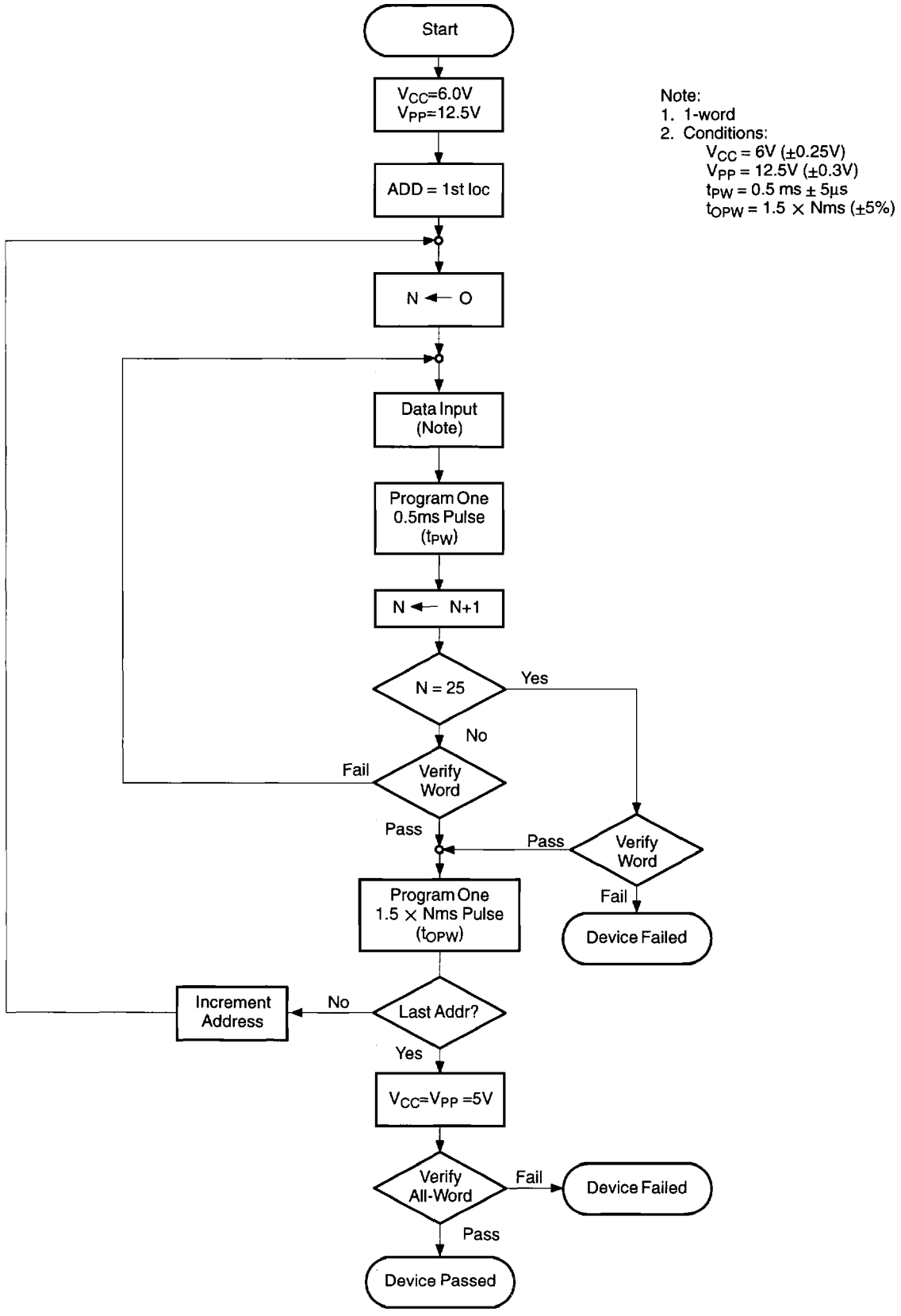
Note:
1. 1-word
2. Conditions:
   V_{CC} = 6V (±0.25V)
   V_{PP} = 12.5V (±0.3V)
   t_{PW} = 100 ± 5µs

TWO-WORD PROGRAMMING FLOWCHART (ADVANCED QUICK PROGRAMMING)



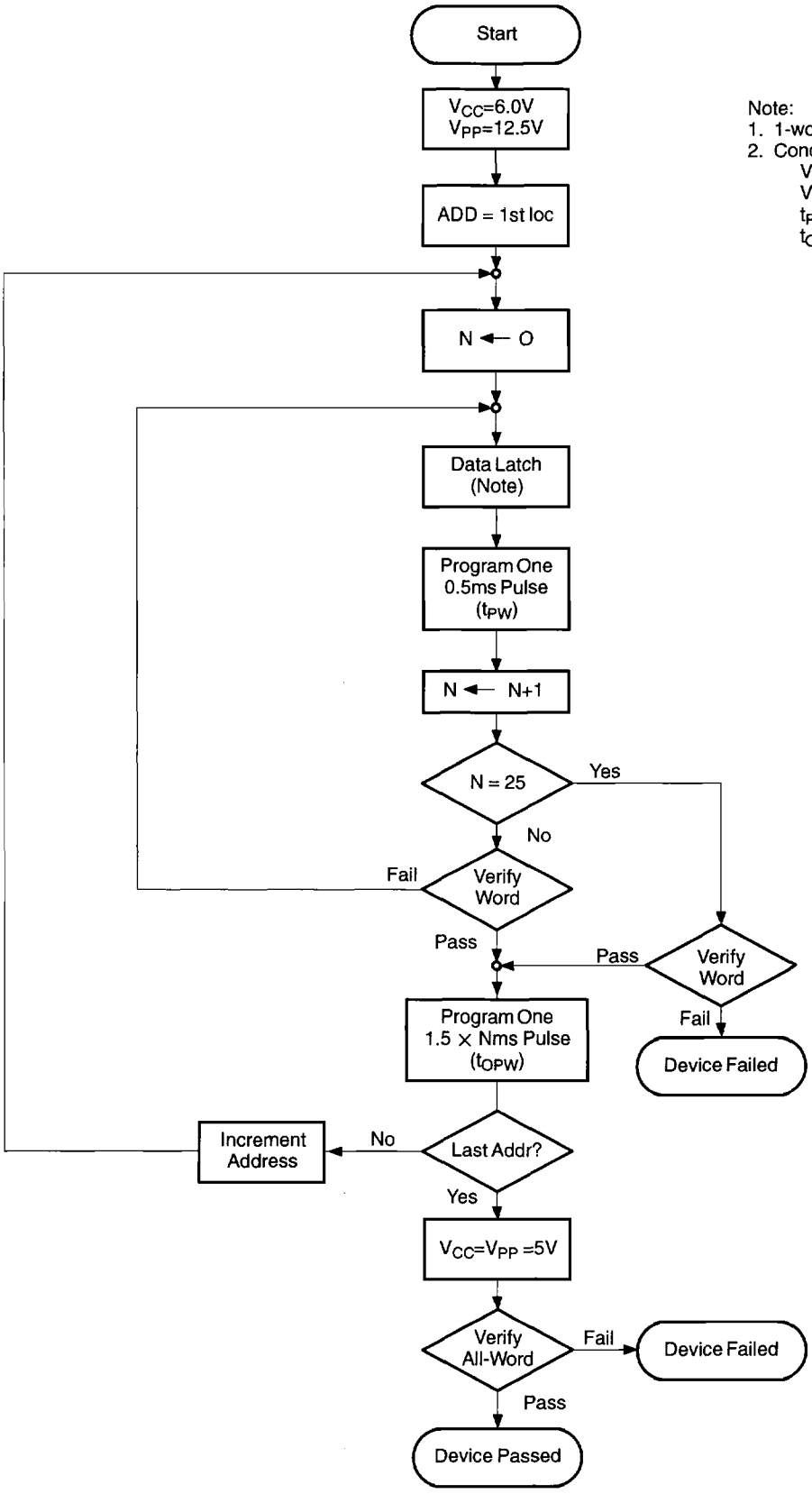
Note:
1. 2-word
2. Conditions:
   V_{CC} = 6V (±0.25V)
   V_{PP} = 12.5V (±0.3V)
   t_{PW} = 100 ± 5µs

ONE-WORD PROGRAMMING FLOWCHART (QUICK PROGRAMMING)



Note:
1. 1-word
2. Conditions:
   V_{CC} = 6V (±0.25V)
   V_{PP} = 12.5V (±0.3V)
   t_{PW} = 0.5 ms ± 5µs
   t_{OPW} = 1.5 × Nms (±5%)

TWO-WORD PROGRAMMING FLOWCHART (QUICK PROGRAMMING)

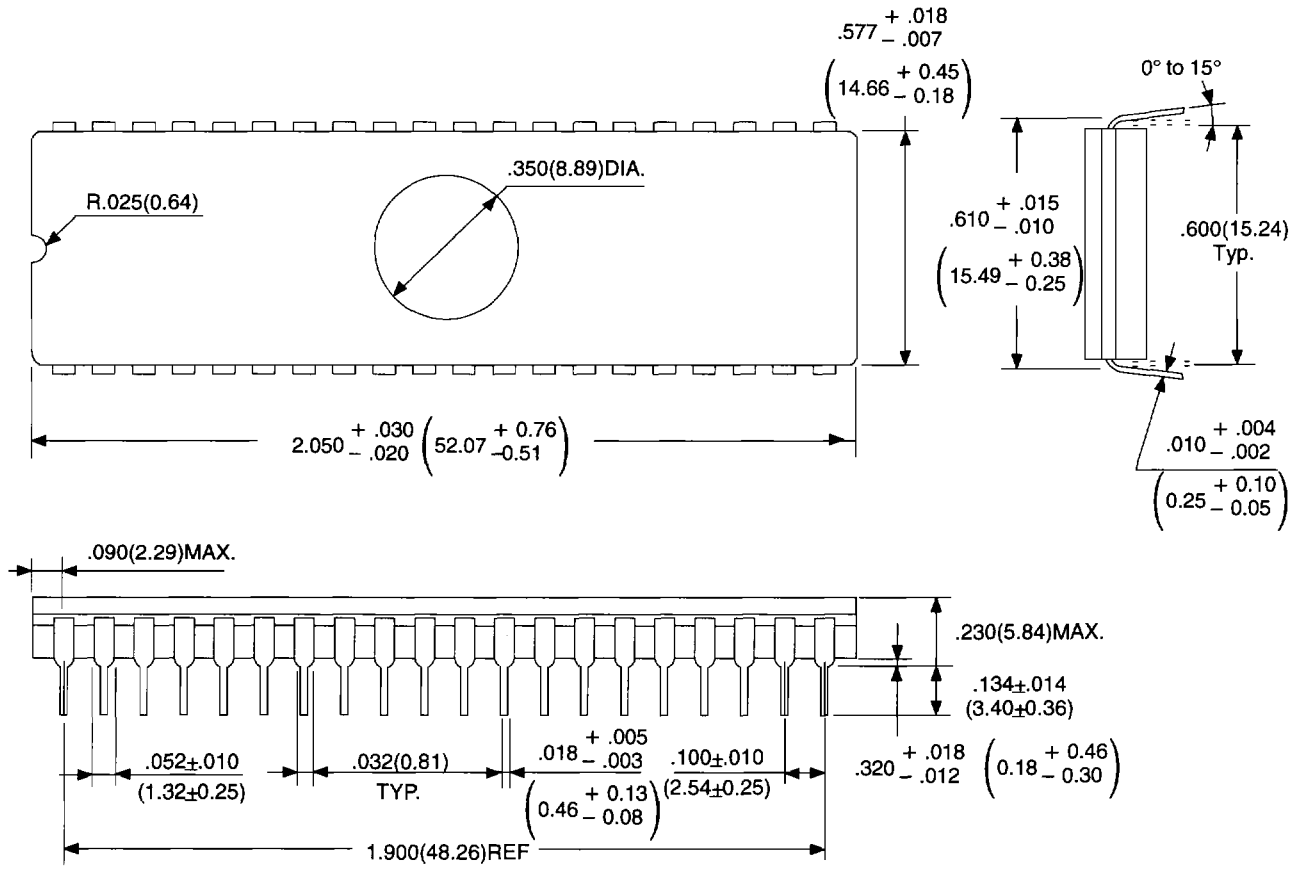


Note:
1. 1-word
2. Conditions:
   V_{CC} = 6V (±0.25V)
   V_{PP} = 12.5V (±0.3V)
   t_{PW} = 0.5 ms ± 25µs
   t_{OPW} = 1.5 × Nms (±5%)

PACKAGE DIMENSIONS

(Suffix: Z)

40-LEAD CERAMIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-40C-C02)



Dimensions in
inches (millimeters)

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