TC74HC190AP/AF
TC74HC191AP/AF

TC74HC190AP/AF BCD Up/Down Counter

TC74HC191AP/AF 4-Bit Binary Up/Down Counter

The TC74HC190A and TC74HC191A are a high speed CMOS 4-BIT UP/DOWN COUNTERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

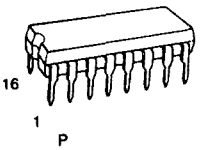
The TC74HC190 is BCD up/down counter and the TC74HC191A is 4-bit binary up/down counter.

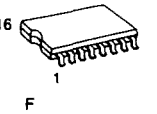
They have a asynchronous load input (LOAD) which is active low.

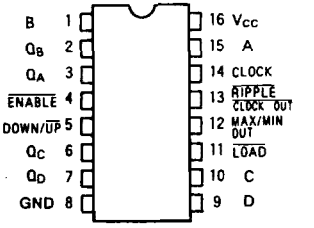
The direction of counting is determined by the level of DOWN/$\overline{UP}$. When D/$\overline{U}$ is low, the counter counts up; when D/U is high, it counts down. Counting occurs on the positive going transition of the clock input.

Enable input ($\overline{ENABLE}$) and two carry inputs ($\overline{RIPPLE\ CLOCK\ OUT}$, MAX/MIN) are provided to permit easy cascading of the counters, which facilitates easy implementation of N-bit counters without using external gates.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.





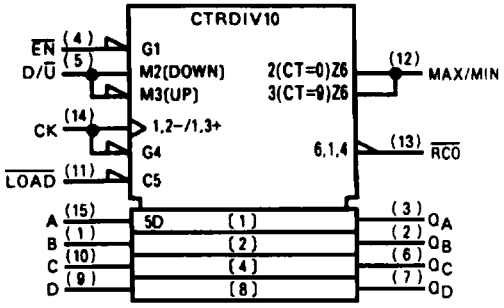


Pin Assignment

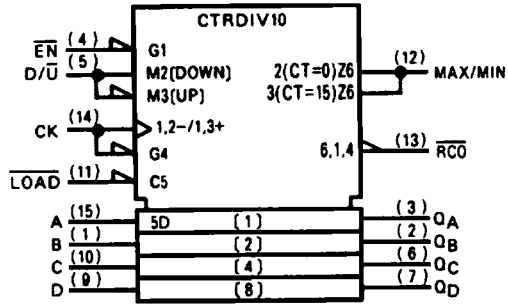
Features

- High Speed: f_{MAX} = 48MHz (Typ.) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28%V_{CC}(Min.)
- Output Drive Capability: 10 LSTTL Loads
- Symmetrical Output Impedance: $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays: $t_{pLH} = t_{pHL}$
- Wide Operating Voltage Range: V_{CC}(opr) = 2V ~ 6V
- Pin and Function Compatible with 74LS190/191

TC74HC190A



TC74HC191A

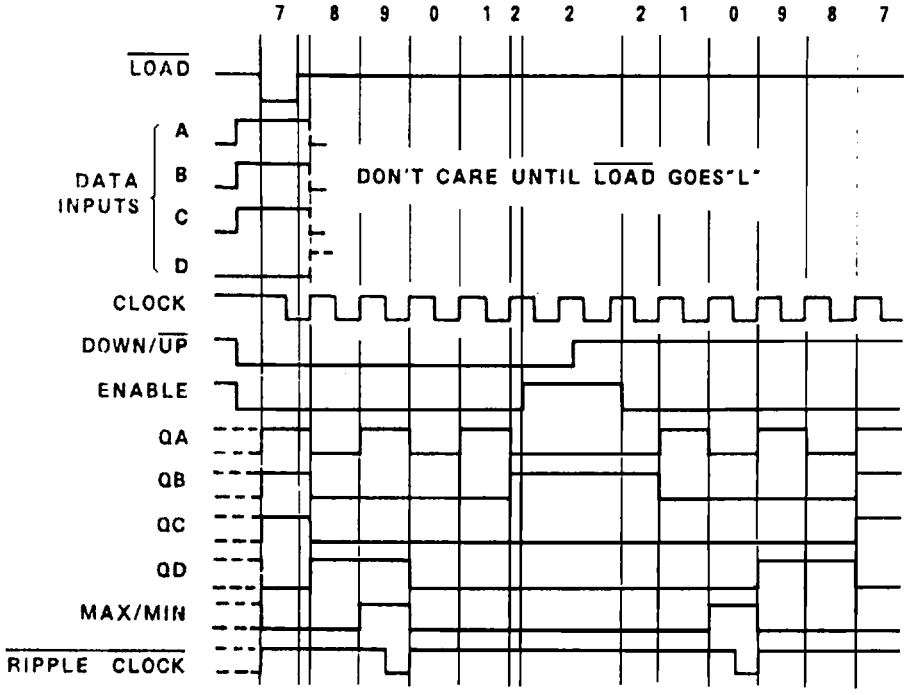


IEC Logic Symbol

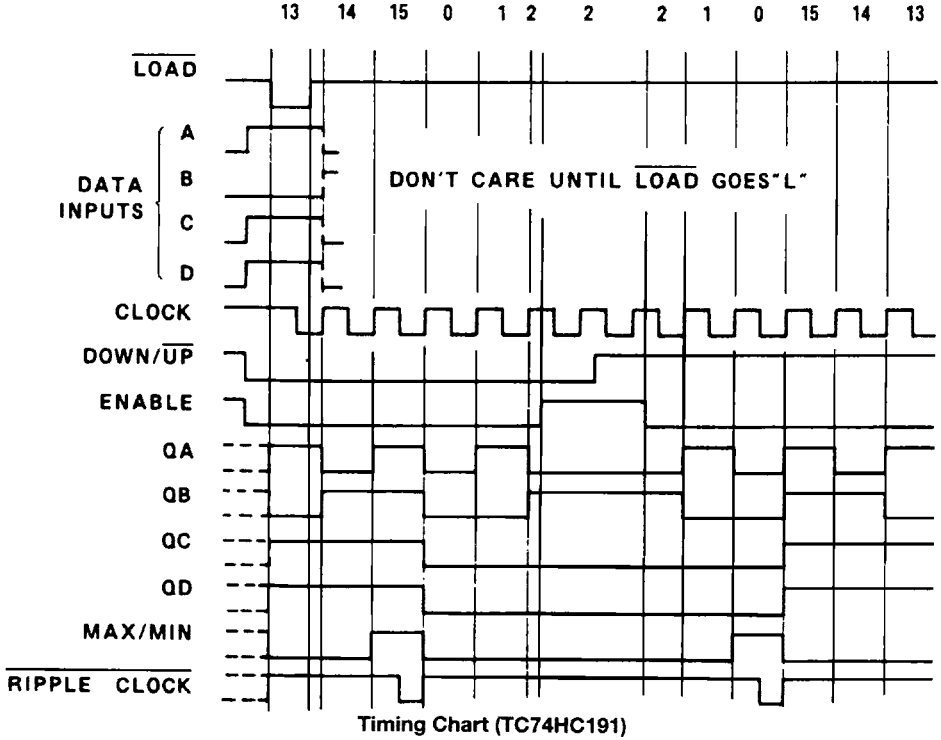
Truth Table

Inputs				Outputs				Function
LOAD	ENABLE	D/U	CLOCK	QA	QB	QC	QD	
L	X	X	X	a	b	c	d	Preset Data
H	L	L	⎍	Up Count				Up Count
H	L	H	⎍	Down Count				Down Count
H	H	X	⎍	No Change				No Count
H	X	X	⎏	No Change				No Count

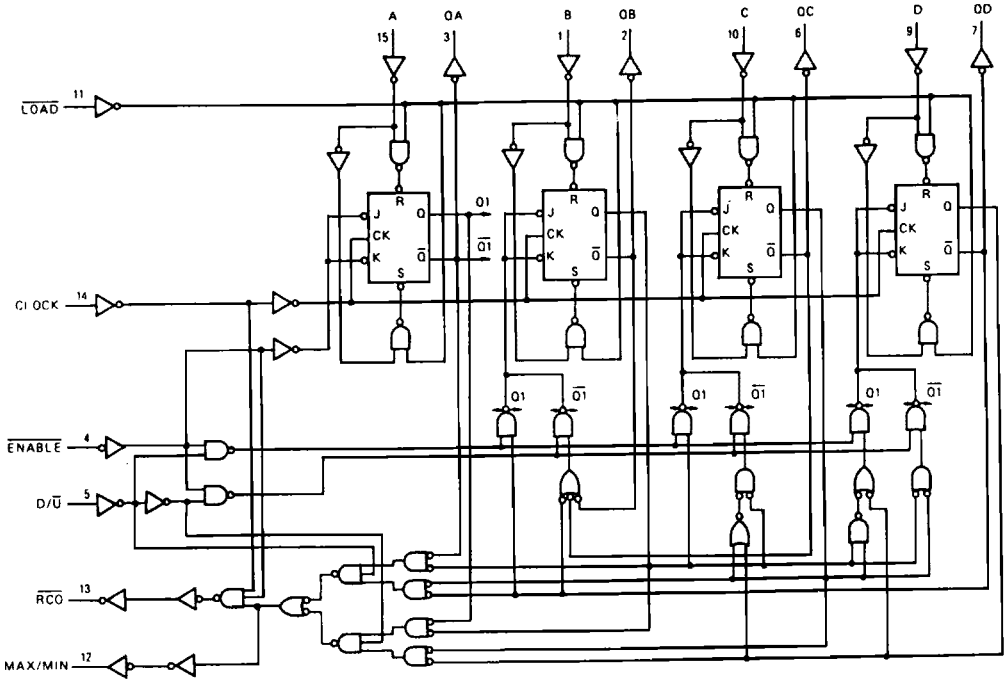
Note X: Don't Care
a ~ d: Inputs Level of A ~ D



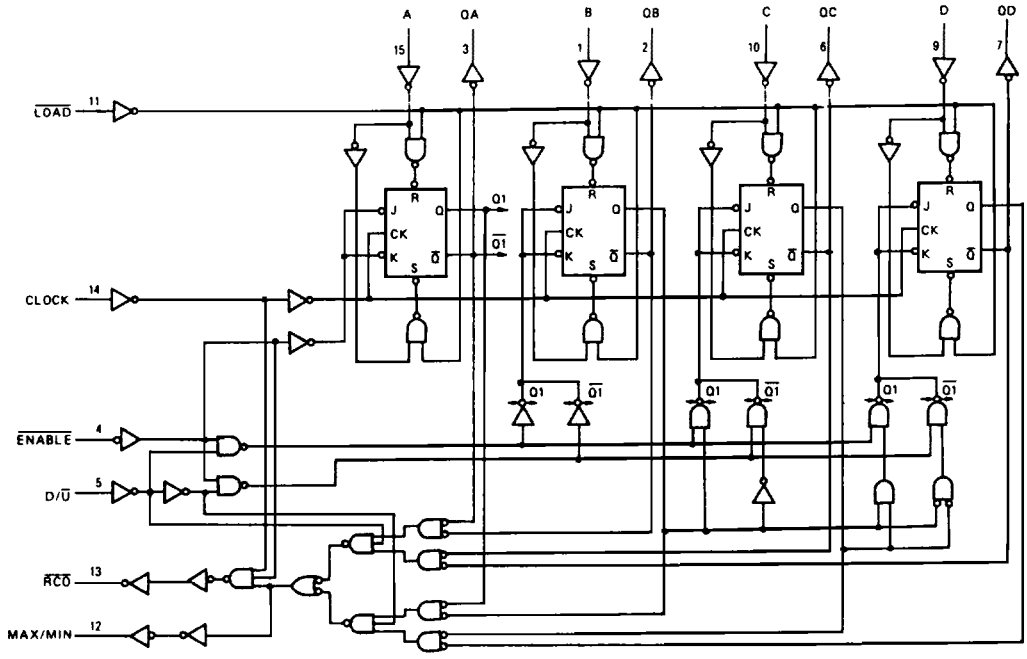
Timing Chart (TC74HC190A)



Timing Chart (TC74HC191)



Logic Diagram (TC74HC190A)



Logic Diagram (TC74HC191A)

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of Ta = -40°C ~ 65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C shall be applied until 300mW.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC} = 2.0V) 0 ~ 500(V_{CC} = 4.5V) 0 ~ 400(V_{CC} = 6.0V)	ns

DC Electrical Characteristics

Parameter	Symbol	Test Condition		Ta = 25°C			Ta = -40 ~ 85°C		Unit
			V_{CC}	Min	Typ.	Max.	Min.	Max.	
High-Level Input Voltage	V_{IH}	–	2.0	1.5	–	–	1.5	–	V
			4.5	3.15	–	–	3.15	–	
			6.0	4.2	–	–	4.2	–	
Low-Level Input Voltage	V_{IL}	–	2.0	–	–	0.5	–	0.5	V
			4.5	–	–	1.35	–	1.35	
			6.0	–	–	1.8	–	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	2.0	1.9	2.0	–	1.9	–	V
		I_{OH} = -20μA	4.5	4.4	4.5	–	4.4	–	
			6.0	5.9	6.0	–	5.9	–	
		I_{OH} = -4 mA	4.5	4.18	4.31	–	4.13	–	
		I_{OH} = -5.2mA	6.0	5.68	5.80	–	5.63	–	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	2.0	–	0.0	0.1	–	0.1	V
		I_{OL} = 20μA	4.5	–	0.0	0.1	–	0.1	
			6.0	–	0.0	0.1	–	0.1	
		I_{OL} = 4 mA	4.5	–	0.17	0.26	–	0.33	
		I_{OL} = 5.2mA	6.0	–	0.18	0.26	–	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND	6.0	–	–	±0.1	–	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND	6.0	–	–	4.0	–	40.0	

Timing Requirements (Input $t_r = t_f = 6ns$)

Parameter	Symbol	Test Condition		Ta = 25°C		Ta = -40 ~ 85°C	Unit
			V_{CC}	Typ.	Limit	Limit	
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$	–	2.0	–	100	125	ns
			4.5	–	20	25	
			6.0	–	17	21	
Minimum Pulse Width ($\overline{LOAD}$)	$t_{W(L)}$	–	2.0	–	75	95	
			4.5	–	15	19	
			6.0	–	13	16	
Minimum Setup Time (ENABLE, D/U)	t_s	–	2.0	–	150	190	
			4.5	–	30	38	
			6.0	–	26	33	
Minimum Setup Time (DATA-$\overline{LOAD}$)	t_s	–	2.0	–	50	65	
			4.5	–	10	13	
			6.0	–	9	11	
Minimum Hold Time (ENABLE, D/U)	t_h	–	2.0	–	0	0	
			4.5	–	0	0	
			6.0	–	0	0	
Minimum Hold Time (DATA-$\overline{LOAD}$)	t_h	–	2.0	–	0	0	
			4.5	–	0	0	
			6.0	–	0	0	
Minimum Removal Time	t_{rem}	–	2.0	–	50	65	
			4.5	–	10	13	
			6.0	–	9	11	
Clock Frequency	f	–	2.0	–	5	4	MHz
			4.5	–	25	20	
			6.0	–	29	24	

AC Electrical Characteristics ($C_L = 15pF$, $V_{CC} = 5V$, Ta = 25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Transition Time	t_{TLH} t_{THL}	–	–	4	8	ns
Propagation Delay Time (CLOCK-Q)	t_{pLH} t_{pHL}	–	–	18	31	
Propagation Delay Time (Clock-$\overline{RCO}$)	t_{pLH} t_{pHL}	–	–	10	20	
Propagation Delay Time (CLOCK-MAX/MIN)	t_{pLH} t_{pHL}	–	–	23	42	
Propagation Delay Time ($\overline{LOAD}$-Q)	t_{pLH} t_{pHL}	–	–	21	35	
Propagation Delay Time (DATA-Q)	t_{pLH} t_{pHL}	–	–	17	30	
Propagation Delay Time (ENABLE-$\overline{RCO}$)	t_{pLH} t_{pHL}	–	–	11	17	
Propagation Delay Time (D/$\overline{U}$-$\overline{RCO}$)	t_{pLH} t_{pHL}	–	–	17	31	
Propagation Delay Time (D/$\overline{U}$-MAX/MIN)	t_{pLH} t_{pHL}	–	–	15	27	
Maximum Clock Frequency	f_{MAX}	–	27	48	–	MHz

AC Electrical Characteristics (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Parameter	Symbol	Test Condition		Ta = 25°C			Ta = -40 ~ 85°C		Unit
			V_{CC}	Min.	Typ.	Max.	Min.	Max.	
Output Transition Time	t_{TLH} t_{THL}	–	2.0 4.5 6.0	– – –	30 8 7	75 15 13	– – –	95 19 16	ns
Propagation Delay Time (CLOCK-Q)	t_{pLH} t_{pHL}	–	2.0 4.5 6.0	– – –	88 22 19	180 36 31	– – –	225 45 38	
Propagation Delay Time (CLOCK-$\overline{RCO}$)	t_{pLH} t_{pHL}	–	2.0 4.5 6.0	– – –	52 13 11	120 24 20	– – –	150 30 26	
Propagation Delay Time (CLOCK-MAX/MIN)	t_{pLH} t_{pHL}	–	2.0 4.5 6.0	– – –	108 27 23	240 48 41	– – –	300 60 51	
Propagation Delay Time ($\overline{LOAD}$-Q)	t_{pLH} t_{pHL}	–	2.0 4.5 6.0	– – –	100 25 22	205 41 35	– – –	255 51 43	
Propagation Delay Time (DATA-Q)	t_{pLH} t_{pHL}	–	2.0 4.5 6.0	– – –	84 21 18	175 35 30	– – –	220 44 37	
Propagation Delay Time ($\overline{ENABLE}$-$\overline{RCO}$)	t_{pLH} t_{pHL}	–	2.0 4.5 6.0	– – –	56 14 12	105 21 18	– – –	130 26 22	
Propagation Delay Time (D/$\overline{U}$-$\overline{RCO}$)	t_{pLH} t_{pHL}	–	2.0 4.5 6.0	– – –	84 21 18	180 36 31	– – –	225 45 38	
Propagation Delay Time (D/$\overline{U}$-MAX/MIN)	t_{pLH} t_{pHL}	–	2.0 4.5 6.0	– – –	72 18 15	160 32 27	– – –	200 40 34	
Maximum Clock Frequency	t_{pLH} t_{pHL}	–	2.0 4.5 6.0	5 25 29	11 44 52	– – –	4 20 24	– – –	MHz
Input Capacitance	C_{IN}	–		–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)	TC74HC190A		–	104	–	–	–	
		TC74HC191A		–	101	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$I_{CC(opr)} = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}$