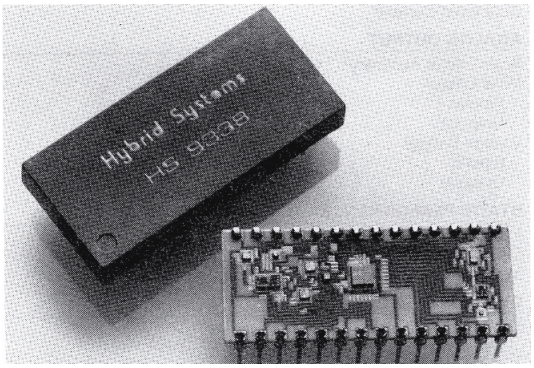
HS9338

Data Converter Line

Complete µP Compatible 12-Bit DAC

FEATURES

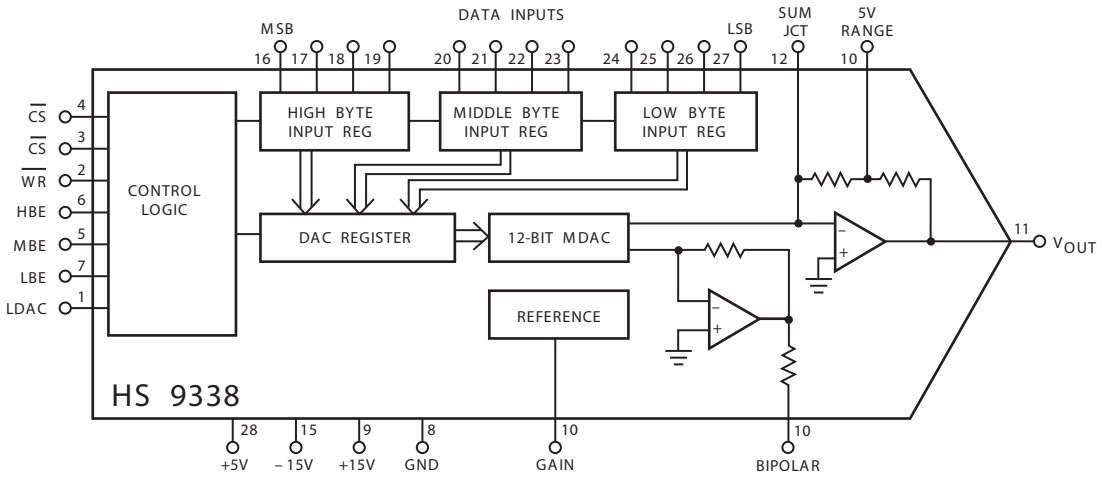
- Output ranges: 0 to +10V, ±10V.
- Coding: binary; offset binary
- Linearity: ±0.01%
- Settling time: 2.5 µS
- µP compatible
- 28-pin package
- CMOS, TTL compatible
- Double buffered inputs



DESCRIPTION

HS9338 is a µP-compatible, complete 12-bit double buffered digital-to-analog converter. To enhance application flexibility, the data input registers have been configured as 3 independent 4-bit bytes. This enables the user to directly interface to 4, 8, and 12-bit data buses. HS9338 comes complete with interface control logic. The three separate byte enable inputs latch data from the bus into the appropriate primary data latches. The LDAC input transfers data from the primary latches to the DAC register. In addition to these input functions are two chip select inputs and a read/write input allowing direct memory-map configurations. All input controls are static to allow hardwired configurations.

FUNCTIONAL DIAGRAM



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SPECIFICATIONS

(Typical @25°C unless otherwise noted. Power supply voltages: +15V. –15V. +5V, (±5%)

MODEL	HS 9338-2	HS9338-0
DIGITAL INPUT		
Resolution	12 Bit	
Unipolar Code	Binary	
Bipolar Code	Offset Binary	
Logic Compatibility[1]	CMOS. TTL	
Control Logic Inputs		
I_{IH} @V_{IH} = 2.4V	20µA	
I_{IL} @V_{IL} = 0.4V	–0.36mA	
Data Input Current[5]	±1µA	
ANALOG OUTPUT		
Scale Factor Accuracy[2]	±0.1% FSR	
Initial Offset[2]		
Bipolar	±0.1% FSR max	
Unipolar	± 0.05% FSR max	
Voltage Range[2]		
Bipolar	±10V.	
Unipolar	0 to +10V	
STATIC PERFORMANCE		
Integral Linearity[3]	±0.015% FSR max	±0.050% FSR max
Differential Linearity	±0.024% FSR max	±0.097% FSR max
Monotonicity	12 Bits	10 Bits
DYNAMIC PERFORMANCE		
Full Scale Transition		
Settling Time	5µS max	
	2.5µS max	
Full Scale Transition		
Slew Rate	10V/µS min	
Delay to Analog Output		
From Bits Input[4]	220nS	
From LDAC	220nS	
From CS4 or WE[4]	225nS	
STABILITY		
Scale Factor	20ppm FSR	
Integral Linearity	1 ppm FSR max	
Differential Linearity	1 ppm FSR max	
Offset Drift		
Bipolar	10ppm/°C	
Unipolar	5ppm/°C	
Monotonicity Temperature Range	0°C to +70°C	
±15V POWER SUPPLY		
+ 15V Supply Current	12mA	
-15V Supply Current	10mA	
PSRR	0.005% /%	
+ 5V POWER SUPPLY		
+ 5V Supply Current	24mA	
TEMPERATURE RANGE		
Operating	–55°Cto +125°C	
Storage	–65°Cto +155°C	

Continued on next page.

SPECIFICATION (Continued)

MECHANICAL

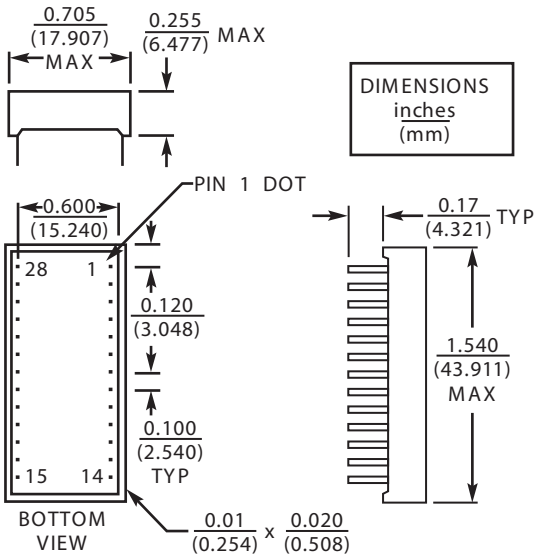
Case Style Ceramic

NOTES: 1. Control inputs are TTL and 5V CMOS only, data inputs are fully CMOS and TTL compatible. 2. See APPLICATION NOTES for adjustment procedures. 3 Specified as "Best Straight Line". 4. Operating the unit with the DAC Register transparent may result in output "glitches" due to logic skewing with the unit. 5. Digital Input Voltage must not exceed supply voltage or go below –0.5V."0" 0.8V, 2.4V "1" V_{DD}.

*Same as HS 9338-2

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below –0.5 volts.

PACKAGE OUTLINE



PIN DIAGRAM

PIN	FUNCTION
1	LOAC, LOADS OAC REGISTER AND CHANGES OUTPUT
2	WR, WRITE INPUT, ACTIVATES ALL CONTROLS
3	CS2, CHIP SELECT INPUT 2
4	CS1, CHIP SELECT INPUT 1
5	MBE, MIDDLE BYTE ENABLE. D4 TO D7
6	HBE, HIGH BYTE ENABLE. D8 TO D11
7	LBE, LOW BYTE ENABLE. D0 TO D3
8	GND, GROUND, ANALOG AND DIGITAL GROUND CONNECTED INTERNALLY
9	V_{EE}, –15V SUPPLY
10	N.C.
11	V_{OUT} DAC VOLTAGE OUTPUT
12	SUMJCT. SUMMING JUNCTION OF OUTPUT OPAMP
13	BIPOLAR. CONNECTED TO SUMJCT FOR BIPOLAR OUTPUT RANGE
14	GAIN. INPUT TO ADJUST FULL SCALE OUTPUT VOLTAGE
15	V_{EE}, -15V SUPPLY
16	D11, DATA INPUT, WEIGHT 2^{-1}. MSB
17	D10, DATA INPUT, WEIGHT 2^{-2}
18	09, DATA INPUT, WEIGHT 2^{-3}
19	08, DATA INPUT, WEIGHT 2^{-4}
20	D7, DATA INPUT, WEIGHT 2^{-5}
21	D6, DATA INPUT, WEIGHT 2^{-6}
22	D5, DATA INPUT, WEIGHT 2^{-7}
23	D4, DATA INPUT, WEIGHT 2^{-8}
24	D3, DATA INPUT, WEIGHT 2^{-9}
25	D2, DATA INPUT, WEIGHT 2^{-10}
26	D1, DATA INPUT, WEIGHT 2^{-11}
27	D0, DATA INPUT, WEIGHT 2^{-12}, LSB
28	V_{DD}, +5V SUPPLY, CONTROL LOGIC

ORDERING INFORMATION

MODEL	DESCRIPTION
HS 9338-2	µP DAC, 0.01% Linearity
HS 9338-	µP DAC, 0.05% Linearity