PRELIMINARY

CY7C1395
CY7C1395V25

2M x 36 PBSRAM with NoBL-Burst™ Architecture

Features

- **Pin-compatible to ZBT™ and NoBL™ devices**
- **Supports up to166-MHz bus operations with zero wait states**
  - **Data is transferred on every clock**
- **Internally self-timed output buffer control to eliminate the need to use asynchronous OE**
- **Fully registered (inputs and outputs) for pipelined operation**
- **Byte Write capability**
- **Common I/O architecture**
- **Single 2.5V or 3.3V power supply**
- **Fast clock-to-output times**
  - **3.5 ns (for 166-MHz device)**
  - **4.2 ns (for 133-MHz device)**
  - **5.0 ns (for 100-MHz device)**
- **Clock Enable ($\overline{CEN}$) pin to suspend operation**
- **Synchronous self-timed writes**
- **Available in 100 TQFP package**
- **119 BGA package is offered by opportunity basis (Check with Cypress sales and marketing)**
- **Burst Capability—linear or interleaved burst order**

Functional Description

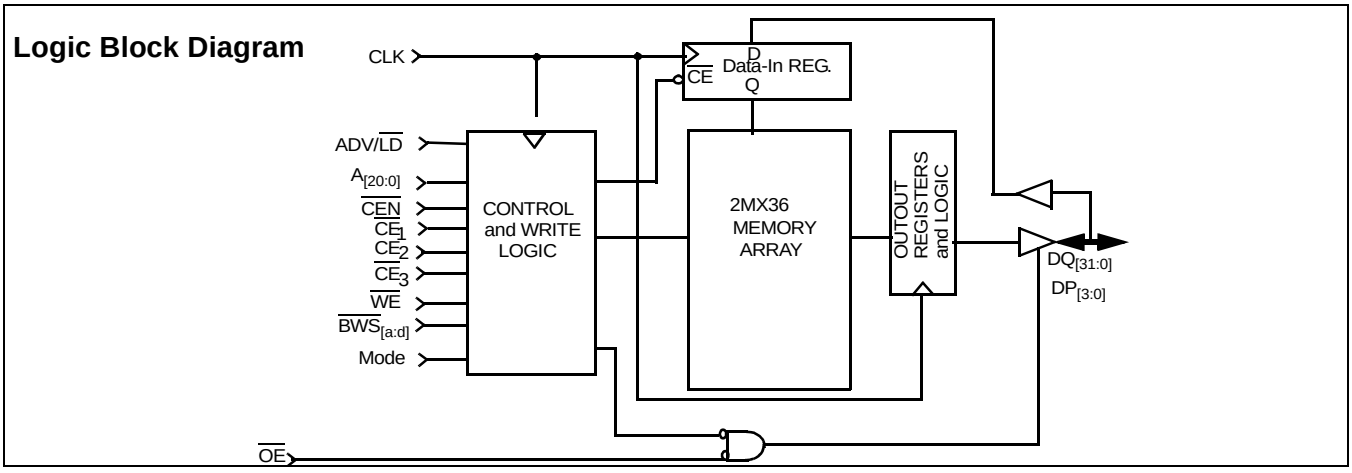
The CY7C1395V25 and CY7C1395 are 2.5V and 3.3V 2M × 36 synchronous pipelined burst SRAMs designed specifically to support unlimited true back-to-back Read/Write operations without the insertion of wait states. The CY7C1395V25 operates with a 2.5V power supply and the CY7C1395 operates with a 3.3V power supply. Both are equipped with the advanced No Bus Latency-Burst™ (NoBL-Burst™) logic required to enable consecutive Read/Write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data through the SRAM, especially in systems that require frequent Write/Read transitions.The CY7C1395V25 and CY7C1395 are pin-compatible with ZBT and NoBL devices.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. The clock input is qualified by the Clock Enable ($\overline{CEN}$) signal, which when deasserted suspends operation and extends the previous clock cycle. Maximum access delay from the clock rise is 3.5 ns (166-MHz device).

Write operations are controlled by the Byte Write Selects and a Write Enable ($\overline{WE}$) input. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output three-state control. In order to avoid bus contention, the output drivers are synchronously three-stated during the data portion of a write sequence.

Logic Block Diagram



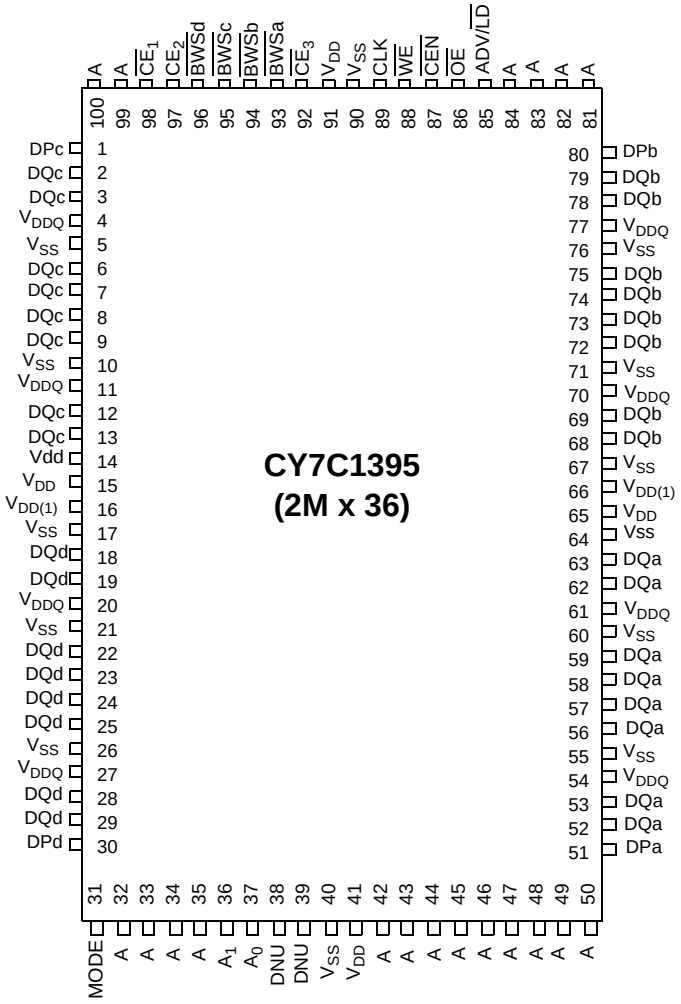
Selection Guide

	-166	-133	-100	Unit
Maximum Access Time	3.5	4.2	5.0	ns
Maximum Operating Current	220	200	175	mA
Maximum CMOS Standby Current	20	20	20	mA

Shaded area contains advanced information.

Pin Configurations

100-pin TQFP Package



Pin Configurations (continued)

119-ball Bump BGA
CY7C1395 (2M × 36) – 7 × 17 BGA

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	A	A	A	V_{DDQ}
B	NC	CE_2	A	ADV/$\overline{LD}$	A	$\overline{CE_3}$	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DPc	DQc	V_{SS}	NC	V_{SS}	DQb	DPb
E	DQc	DQc	V_{SS}	$\overline{CE_1}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{OE}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQb	$\overline{BWSc}$	A	$\overline{BWSb}$	DQb	DQb
H	DQc	DQc	V_{SS}	$\overline{WE}$	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CLK	V_{SS}	DQa	DQa
L	DQb	DQd	$\overline{BWSd}$	NC	$\overline{BWSa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{CEN}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	A1	V_{SS}	DQa	DQa
P	DPd	DQd	V_{SS}	A0	V_{SS}	DQa	DPa
R	NC	A	MODE	V_{DD}	Vdd	A	NC
T	NC	A	A	A	A	A	V_{SS}
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Pin Definitions (CY7C1395)

Name	I/O Type	Description
A0 A1 A(2:20)	Input-Synchronous	**Address inputs used to select one of the memory locations in the array**. Sampled at the rising edge of the CLK.
$\overline{BWSa}$ $\overline{BWSb}$ $\overline{BWSc}$ $\overline{BWSd}$	Input-Synchronous	**Byte Write Select Inputs, active LOW**. Enables or masks write data during active write cycles. Byte Writes must be valid two cycles before the write data. Sampled on the rising edge of CLK. $\overline{BWSa}$ controls DQa and DPa, $\overline{BWSb}$ controls DQb and DPb, $\overline{BWSc}$ controls DQc and DPc, $\overline{BWSd}$ controls DQd and DPd.
$\overline{WE}$	Input-Synchronous	**Write Enable Input, active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/$\overline{LD}$	Input-Synchronous	**Advance/Load Input used to advance the on-chip address counter or load a new address**. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access.
CLK	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.
$\overline{CE_1}$	Input-Synchronous	**Chip Enable 1 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE_3}$ to select/deselect the device.
CE_2	Input-Synchronous	**Chip Enable 2 Input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and $\overline{CE_3}$ to select/deselect the device.
$\overline{CE_3}$	Input-Synchronous	**Chip Enable 3 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and CE_2 to select/deselect the device.
$\overline{OE}$	Input-Asynchronous	**Output Enable, active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins. $\overline{OE}$ is masked once a write operation has been initiated, during the first clock when emerging from a deselected state and when the device has been deselected.

Pin Definitions (CY7C1395) (continued)

Name	I/O Type	Description
$\overline{CEN}$	Input-Synchronous	**Clock Enable Input, active LOW**. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Since deasserting $\overline{CEN}$ does not deselect the device, $\overline{CEN}$ can be used to extend the previous cycle when required.
DQa DQb DQc DQd	I/O-Synchronous	**Bidirectional Data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by $A_{[17:0]}$ during the initiation of the burst. The direction of the pins is controlled by $\overline{OE}$ and the internal control logic. When $\overline{OE}$ is asserted LOW, the pins can behave as outputs. When HIGH, DQa–DQd are placed in a three-state condition. The outputs are automatically three-stated once a write operation has been initiated, and during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
DPa DPb DPc DPd	I/O-Synchronous	**Bidirectional Data Parity I/O lines**. Functionally, these signals are identical to $DQ_{[31:0]}$. During write sequences, DPa is controlled by $\overline{BWSa}$, DPb is controlled by $\overline{BWSb}$, DPc is controlled by $\overline{BWSc}$, and DPd is controlled by $\overline{BWSd}$.
MODE	Input Strap Pin	**Mode Input**. Selects the burst order of the device. Tied HIGH selects the interleaved burst order. Pulled LOW selects the linear burst order. MODE should not change states during operation. When left floating MODE will default HIGH, to an interleaved burst order.
V_{DD}	Power Supply	**Power supply inputs to the core of the device**.
V_{DDQ}	I/O Power Supply	**Power supply for the I/O circuitry**.
V_{SS}	Ground	**Ground for the device**. Should be connected to ground of the system.
$V_{dd(1)}$	Input Static	**These pins have to be tied to a voltage level > Vih**. They need not be tied to Vdd.
NC	–	**No connect**. This pin is reserved ZZ function and is not connected to the die. May be tied high.
DNU	–	**Do Not Use pins**. These pins should be left floating or tied to V_{SS}.
TDO	JTAG output-Synchronous	**Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK.
TDI	JTAG input-Synchronous	**Serial data-in to the JTAG circuit**. Sampled on the rising edge of TCK.
TMS	JTAG input-Synchronous	**This pin controls the Test Access Port state machine**. Sampled on the rising edge of TCK.
TCK	JTAG input-Clock	**Clock input to the JTAG circuitry**.
NC	–	**No connects**.
NC(1)	–	**No connect, to be determined whether connected to V_{DD} or V_{SS}**. These pins will not affect the functionality of the product. These pins can be left not connected to the internal die.

Introduction

Functional Overview

The CY7C1395V25 and CY7C1395 are synchronous pipelined NoBL-Burst SRAMs designed specifically to eliminate wait states during Write/Read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the Clock Enable input signal ($\overline{CEN}$). If $\overline{CEN}$ is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with $\overline{CEN}$. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 3.5 ns (166-MHz device).

Accesses can be initiated by asserting all three Chip Enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) active at the rising edge of the clock. If Clock Enable ($\overline{CEN}$) is active LOW and ADV/$\overline{LD}$ is asserted LOW, the address presented to the device will be latched. The access can either be a read or write operation, depending on the status of the Write Enable ($\overline{WE}$). $\overline{BWS_{[x]}}$ can be used to conduct byte write operations.

Write operations are qualified by the Write Enable ($\overline{WE}$). All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) and an asynchronous Output Enable ($\overline{OE}$) simplify depth expansion. All operations (Reads, Writes, and Deselects) are pipelined. ADV/$\overline{LD}$ should be driven LOW once the device has been deselected in order to load a new address for the next operation.

Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are ALL asserted active, (3) the Write Enable input signal $\overline{WE}$ is deasserted HIGH, and (4) ADV/$\overline{LD}$ is asserted LOW. The address presented to the address inputs is latched into the Address Register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the rising edge of the next clock the requested data is allowed to propagate through the output register and onto the data bus within 3.5 ns (166-MHz device), provided $\overline{OE}$ is active LOW. After the first clock of the read access the output buffers are controlled by $\overline{OE}$ and the internal control logic. $\overline{OE}$ must be driven LOW in order for the device to drive out the requested data.

The NoBL-Burst architecture supports burst accesses only. Each Read access must be allowed to complete a burst sequence of four word. Each burst of four words is non-interruptible. Therefore, ADV/$\overline{LD}$ must be driven HIGH in order to increment the burst counter, throughout the entire burst sequence. Each Read access must be allowed to complete prior to the initiation of a new access (Read, Write or Deselect). Therefore, the input signals $\overline{CE_1}$, CE_2, $\overline{CE_3}$, $\overline{WE}$, and $\overline{BWS}$x will be ignored for the three clock rises ($\overline{CEN}$ active LOW) after the initiation of the access.

The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence (see burst sequence tables for details). Both burst counters will wrap-around when incremented sufficiently. If incremented sufficiently to wrap-around, the sequence of four read accesses must be allowed to be complete as if a new access was initiated. ADV/$\overline{LD}$ must be asserted LOW in order to load a new address into the SRAM. Consecutive read operations is supported such that data is latched out of the device on every clock rise. See timing diagrams for further details.

The type of access (Read, Write or Deselect) is established at the initiation of the burst. Therefore $\overline{CE_1}$, CE_2, $\overline{CE_3}$, $\overline{WE}$ and $\overline{BWS}$x are ignored during the burst portion of a Read access.

Deselecting the device is also pipelined (double cycle deselect). Therefore, when the SRAM is deselected at clock rise, its output will three-state following the next clock rise.

Write Accesses

Write access are initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are ALL asserted active, and (3) the write signal $\overline{WE}$ is asserted LOW. The address presented to the SRAM is loaded into the Address Register and the byte write signals are latched into the Control Logic block.

On the subsequent clock rise the data lines are automatically three-stated regardless of the state of the $\overline{OE}$ input signal. This allows the external logic to present the data on DQ and DP inputs. On the next clock rise the data presented to DQ and DP inputs (or a subset for byte write operations, see Write Cycle Description Table for details) is latched into the device.

The NoBL-Burst architecture supports burst accesses only. Each Write access must be allowed to complete a burst sequence of four words. Each burst of four is non-interruptible. Therefore, the input signals $\overline{CE_1}$, CE_2, $\overline{CE_3}$ and $\overline{WE}$ will be ignored for the three clock rises ($\overline{CEN}$ active LOW) after the initiation of the access. Consecutive Write operation is supported such that data is latched into the device on every clock rise.

The data written during the Write operation is controlled by $\overline{BWS_x}$ signals. Asserting the appropriate Byte Write Select ($\overline{BWS_x}$) input will selectively write to only the desired bytes. The $\overline{BWS_x}$ inputs are sampled two clocks prior to the actual data being latched into the device (see timing diagrams for details). Bytes not selected during a byte write operation will remain unaltered.

Deasserting all Byte Write Select inputs inactive HIGH will create a NOP/DUMMY Write. This is a Write cycle where no data is written into the device. Parts or all of a write sequence can consist of NOP/DUMMY Writes. The address counter is incremented during NOP/DUMMY Writes.

Deselecting the device is also pipelined (double cycle deselect). Therefore, when the SRAM is deselected at clock rise, the Write operations in progress are allowed to complete.

The type of access (Read, Write or Deselect) is established at the initiation of the burst. Therefore $\overline{CE_1}$, CE_2, $\overline{CE_3}$ and $\overline{WE}$ are ignored during the burst portion of a Write access.

A Synchronous self-timed write mechanism has been provided to simplify the write operations. Byte write capability has been included in order to greatly simplify Read/Modify/Write sequences, which can be reduced to simple byte write operations.

ADV/$\overline{LD}$ must be driven LOW in order to load the initial address, as described above. The sequence of the burst

counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and will wrap-around when incremented sufficiently. If incremented sufficiently to wraparound, the sequence of four read accesses must be allowed to be complete. If MODE is left floating, an interleaved burst order will be selected. MODE is a strap pin and should not change states during device operation.

Because the CY7C1395V25 and CY7C1395 are common I/O devices, data should not be driven into the device while the outputs are active. The Output Enable ($\overline{OE}$) can be deasserted HIGH before presenting data to the DQ and DP inputs. Doing so will three-state the output drivers. As a safety precaution, DQ and DP are automatically three-stated during the data portion of a write cycle, regardless of the state of $\overline{OE}$.

Extended Operations

The CY7C1395V25 and CY7C1395 devices contain the NoBL-Burst architecture. This architecture requires that one Burst Deselect sequence occur every 2,500 clock cycles (when running at 166-MHz clock frequency or 16 us, whichever comes first). Since the NoBL-Burst architecture operates on burst accesses, each Burst Deselect cycle must be allowed to complete the 4-cycle operation (see timing diagrams for details). After completing the Burst Deselect, the device can be accessed by a Burst Read or Burst Write operation. The deselect requirement includes extended periods when the device is deselected. During these periods, the device must be deselected once every 2,500 clock cycles or every 16 µs, whichever comes first.The number of cycles allowed between Burst Deselect operations will vary depending on the frequency of operation. As with Burst Read or Burst Write operations, ADV/$\overline{LD}$ must be asserted HIGH in order to complete the burst deselect cycle.

Cycle Description Truth Table[1]

Operation	Add. Used	$\overline{CE}$[1]	$\overline{CEN}$	$\overline{OE}$	ADV/$\overline{LD}$	$\overline{WE}$	$\overline{BWS_X}$	CLK
Deselected[2]	None	H	L	X	L	X	X	L-H
Continue Deselect[3]	None	X	L	X	H	X	X	L-H
Begin Burst Read[4]	External	L	L	L	L	H	X	L-H
Continue Burst Read	Internal	X	L	L	H	X	X	L-H
NOP/DUMMY Read Begin[5]	External	L	L	H	L	H	X	L-H
NOP/DUMMY Read Continue Burst[6]	Internal	X	L	H	H	X	X	L-H
Begin Write Burst[7, 12]	External	L	L	X	L	L	Valid	L-H
Continue Burst Write[8, 12]	Internal	X	L	X	H	X	Valid	L-H
NOP/DUMMY Write Begin[9, 12]	External	L	L	X	L	L	H	L-H
NOP/DUMMY Write Continue Burst[10, 12]	Internal	X	L	X	H	X	H	L-H
Suspend[11]	None	X	H		X	X	X	L-H

Interleaved Burst Sequence

First Address	Second Address	Third Address	Fourth Address
A[1:0]	A[1:0]	A[1:0]	A[1:0]
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Sequence

First Address	Second Address	Third Address	Fourth Address
A[1:0]	A[1:0]	A[1:0]	A[1:0]
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Notes:

1. X ="Don't Care", H = Logic HIGH, L = Logic LOW. $\overline{BWS_X}$ = 0 signifies at least one Byte Write Select is active, $\overline{BWS_X}$ = Valid signifies that the desired byte write selects are asserted, see Write Cycle Description table for details. $\overline{CE}$ is active LOW in this case and represents $\overline{CE_1}$, CE_2 and $\overline{CE_3}$. Any one of these can deselect the device. All three must be asserted active to select the device.
2. When deselected, pending transactions (Read or Write) are allowed to complete. Outputs are automatically three-stated following the next clock.
3. Deselected state previously entered.
4. Read access initiated and a burst is in progress. Addresses incremented internally in conjunction with the state of Mode input.
5. Read initiated, $\overline{OE}$ HIGH prevents data from being driven, thereby making the access a NOP/DUMMY Read.
6. $\overline{OE}$ HIGH prevents data from being driven, thereby making access a NOP/DUMMY Read Continue Burst.
7. Device will automatically three-state outputs during data portion of a Write sequence, regardless of the state of $\overline{OE}$.
8. Write Burst in progress.Addresses incremented internally in conjunction with the state of Mode input.
9. Write Burst initiated, $\overline{BWS}$x HIGH prevents data from being written, making the operation a NOP.
10. Write Burst in progress. $\overline{BWS}$x HIGH prevents data from being written, making the operation a NOP.
11. Clock ignored, all operations suspended.
12. Write is defined by $\overline{WE}$ and $\overline{BWS_X}$. See Write Cycle Description table for details.
13. The DQ and DP pins are controlled by the current cycle and the $\overline{OE}$ signal. Device will power-up deselected and the I/Os in a three-state condition, regardless of $\overline{OE}$.

Write Cycle Description[12]

Function (CY7C1395)	$\overline{WE}$	$\overline{BWS_d}$	$\overline{BWS_c}$	$\overline{BWS_b}$	$\overline{BWS_a}$
Read	1	X	X	X	X
Write - No bytes written	0	1	1	1	1
Write Byte 0 – (DQa and DPa)	0	1	1	1	0
Write Byte 1 – (DQb and DPb)	0	1	1	0	1
Write Bytes 1, 0	0	1	1	0	0
Write Byte 2 – (DQc and DPc)	0	1	0	1	1
Write Bytes 2, 0	0	1	0	1	0
Write Bytes 2, 1	0	1	0	0	1
Write Bytes 2, 1, 0	0	1	0	0	0
Write Byte 3 – (DQd and DPd)	0	0	1	1	1
Write Bytes 3, 0	0	0	1	1	0
Write Bytes 3, 1	0	0	1	0	1
Write Bytes 3, 1, 0	0	0	1	0	0
Write Bytes 3, 2	0	0	0	1	1
Write Bytes 3, 2, 0	0	0	0	1	0
Write Bytes 3, 2, 1	0	0	0	0	1
Write All Bytes	0	0	0	0	0

IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1395V25 and CY7C1395 incorporates a serial boundary scan Test Access Port (TAP) in the BGA package only. The TQFP package does not offer this functionality. This port operates in accordance with IEEE Standard 1149.1-1900, but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC-standard 2.5V I/O logic levels.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

Test Access Port (TAP) – Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the Most Significant Bit (MSB) on any register.

Test Data Out (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see TAP Controller State Diagram). The output changes on the falling edge of TCK. TDO is connected to the Least Significant Bit (LSB) of any register.

Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in the TAP Controller Block Diagram. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the CaptureIR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain states. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (VSS) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices. The CY7C1395 has a 72-bit configuration register.

The boundary scan register is loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the Input and Output ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Code table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load address, data, or control signals into the SRAM and cannot preload the Input or Output buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather it performs a capture of the Inputs and Output ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST (B41) is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in the TAP controller, and therefore this device is not compliant to the 1149.1 standard.

The TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the TAP controller is not fully 1149.1-compliant.

When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

Note that since the PRELOAD part of the command is not implemented, putting the TAP into the Update to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

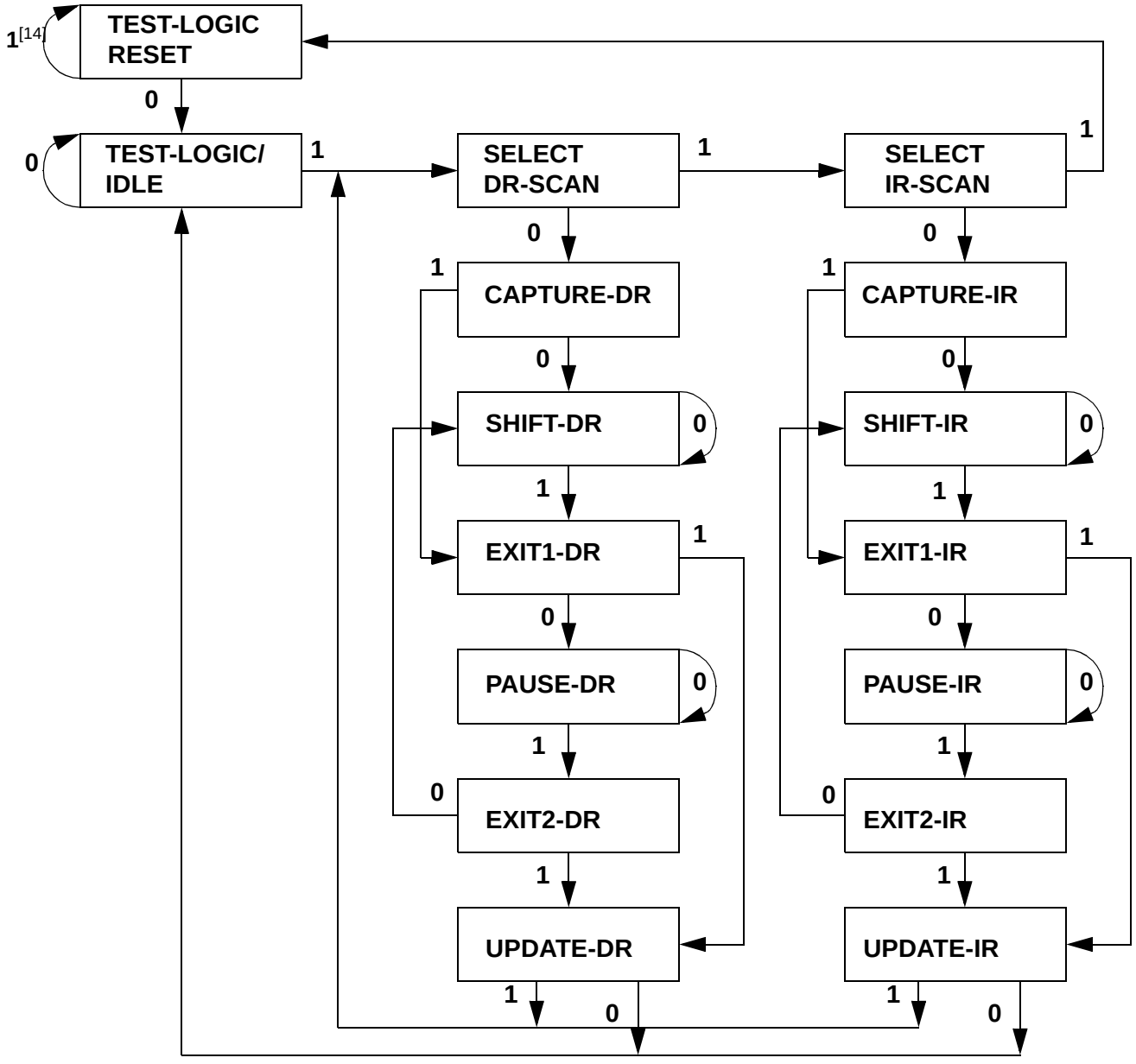
Bypass

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

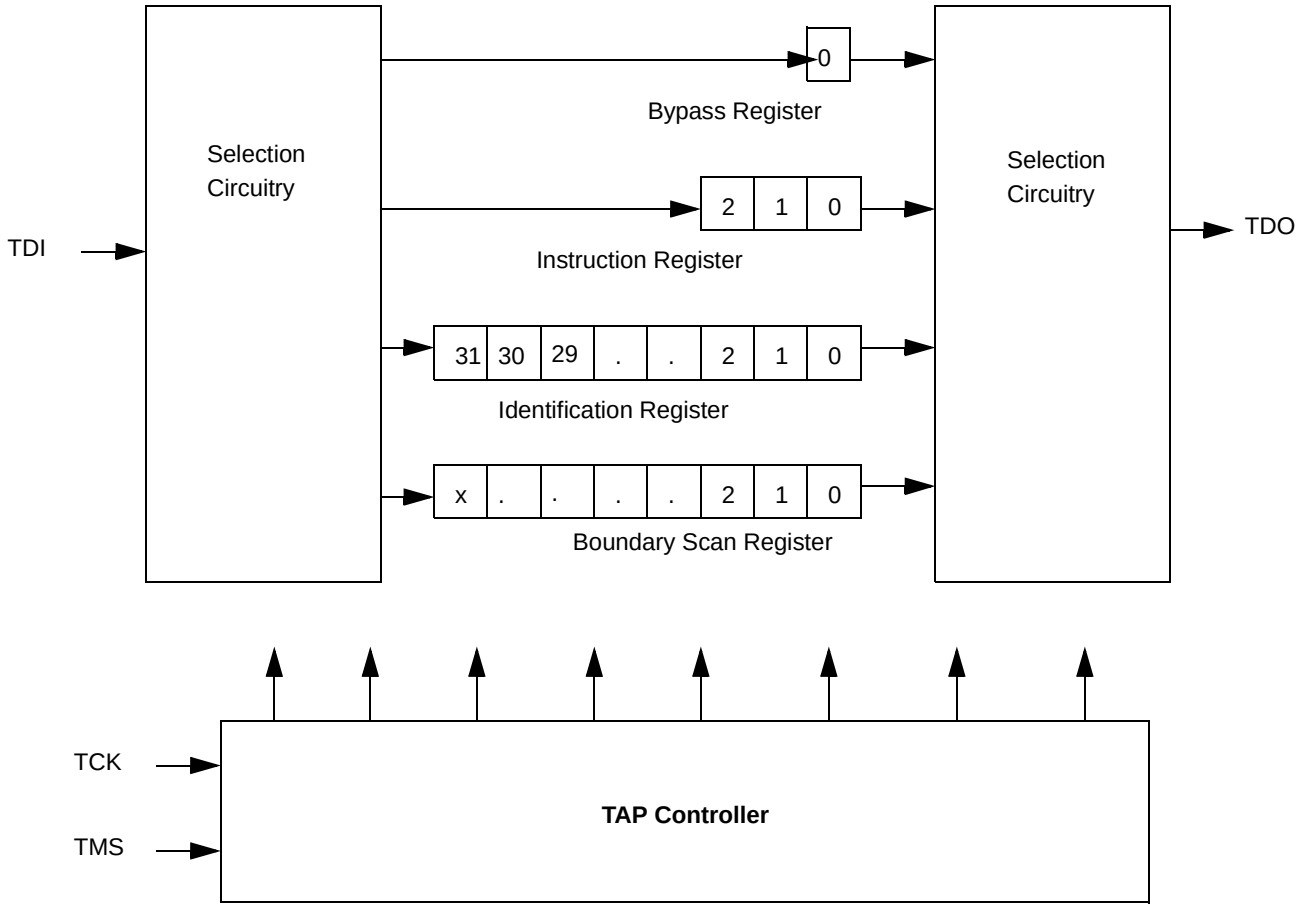
TAP Controller State Diagram



Note:

14. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Electrical Characteristics Over the Operating Range[15, 16]

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –2.0 mA	2.0		V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA	2.2		V
V_{OL1}	Output LOW Voltage	I_{OL} = 2.0 mA		0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA		0.2	V
V_{IH}	Input HIGH Voltage		1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.7	V
I_X	Input and Output Load Current	GND ≤ V_I ≤ V_{DDQ}	–5	5	µA

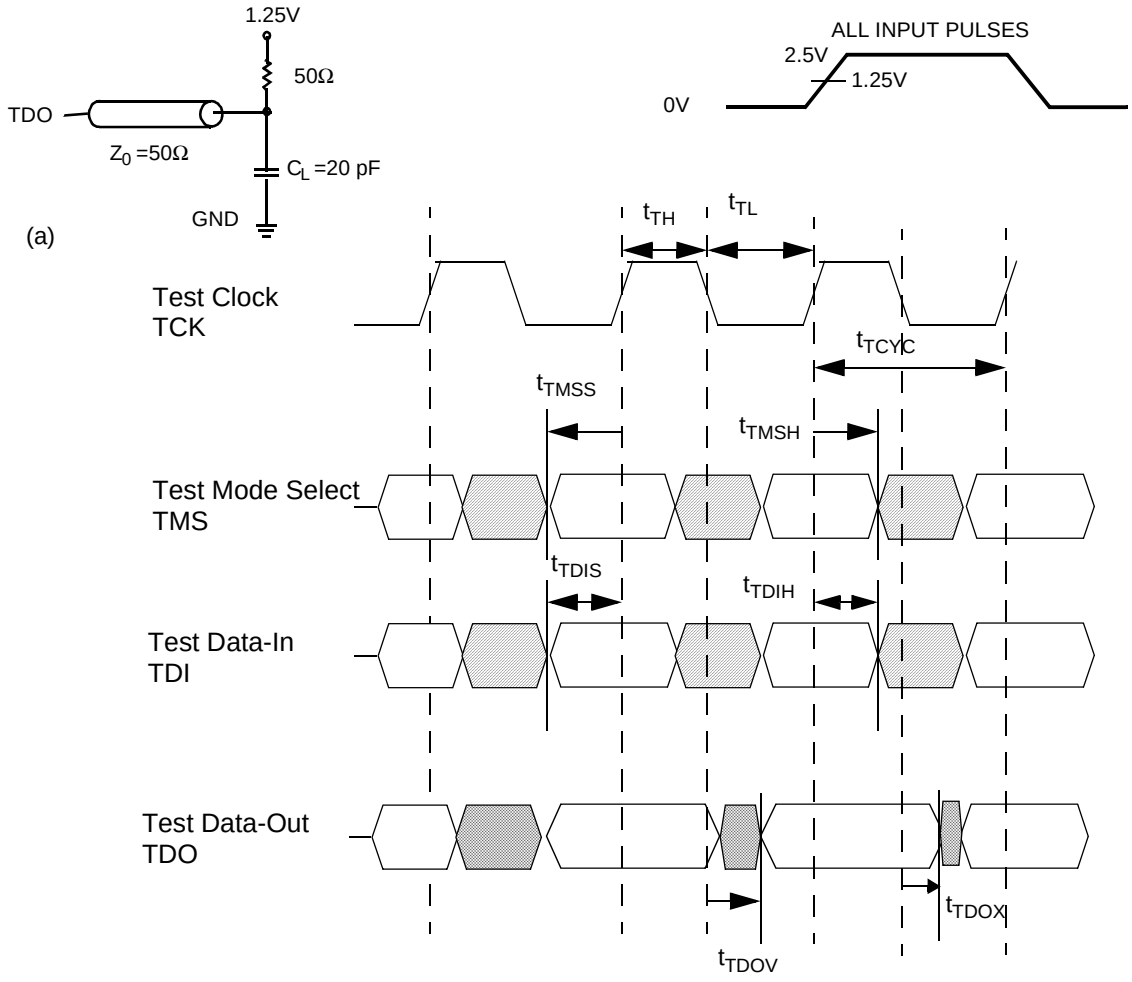
Notes:
15. All voltage referenced to ground.
16. Overshoot: $V_{IH}(AC) \leq V_{DD} + 0.7$ V for $t \leq t_{TCYC}/2$; undershoot: $V_{IL}(AC) \leq 0.5$V for $t \leq t_{TCYC}/2$; power-up: $V_{IH} < 2.6$V and $V_{DD} < 2.4$V and $V_{DDQ} < 1.4$V for t < 200 ms.

TAP AC Switching Characteristics Over the Operating Range[17, 18]

Parameter	Description	Min.	Max	Unit
t_{TCYC}	TCK Clock Cycle Time	100		ns
t_{TF}	TCK Clock Frequency		10	MHz
t_{TH}	TCK Clock HIGH	40		ns
t_{TL}	TCK Clock LOW	40		ns
Set-up Times				
t_{TMSS}	TMS Set-up to TCK Clock Rise	10		ns
t_{TDIS}	TDI Set-up to TCK Clock Rise	10		ns
t_{CS}	Capture Set-up to TCK Rise	10		ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	10		ns
t_{TDIH}	TDI Hold after Clock Rise	10		ns
t_{CH}	Capture Hold after clock rise	10		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid		20	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns

Notes:
17. t_{CS} and t_{CH} refer to the set-up and hold time requirements of latching data from the boundary scan register.
18. Test conditions are specified using the load in TAP AC test conditions. t_R/t_F = 1 ns.

TAP Timing and Test Conditions



Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:29)	TBD	Reserved for version number.
Voltage (28,24)	X,X	Defines Vdd voltage of SRAM - 0,0 (3.3V) and 0,1 (2.5V)
Reserved (27:25)	XXX	Reserved
Architecture (23,21)	001	Defines SRAM architecture (NoBL)
Memory Type (20:18)	011	Defines type of SRAM (pipelined burst 4)
Bus Width (17:15)	100	Defines width of the SRAM
Density (14:12)	100	Defines density of SRAM (72M)
Cypress JEDEC ID (11:1)	00000110100	Allows unique identification of SRAM vendor.
ID Register Presence (0)	1	Indicate the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	70

Identification Codes

Instruction	Code	Description
EXTEST	000	Captures the Input/Output ring contents. Places the boundary scan register between the TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1-compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the Input/Output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use. This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the Input/Output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1-compliant.
RESERVED	101	Do Not Use. This instruction is reserved for future use.
RESERVED	110	Do Not Use. This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

Boundary Scan Order

Bit #	Signal Name	BGA Pin Location	Bit #	Signal Name	BGA Pin Location
0	Mode	3R	35	A	5C
1	A	3A	36	A	6C
2	A	4A	37	A	3B
3	A	5A	38	ADV/$\overline{LD}$	4B
4	A	6A	39	$\overline{OE}$	4F
5	A1	4N	40	$\overline{CEN}$	4M
6	A0	4P	41	$\overline{WE}$	4H
7	A	2T	42	CLK	4K
8	A	3T	43	$\overline{CE_3}$	6B
9	A	4T	44	$\overline{BWS_a}$	5L
10	A	5T	45	$\overline{BWS_b}$	5G
11	A	6T	46	$\overline{BWS_c}$	3G
12	A	2R	47	$\overline{BWS_d}$	3L
13	A	6R	48	CE_2	2B
14	A	4G	49	$\overline{CE_1}$	4E
15	A	2C	50	A	5B
16	DQa	6P	51	A	2A
17	DPa	7P	52	DQc	1H
18	DQa	6N	53	DQc	2H
19	DQa	7N	54	DQc	1G

Boundary Scan Order

Bit #	Signal Name	BGA Pin Location	Bit #	Signal Name	BGA Pin Location
20	DQa	6M	55	DQc	2G
21	DQa	6L	56	DQc	2F
22	DQa	7L	57	DQc	1E
23	DQa	6K	58	DQc	2E
24	DQa	7K	59	DPc	1D
25	DQb	6H	60	DQc	2D
26	DQb	7H	61	DPd	1P
27	DQb	6G	62	DQd	2P
28	DQb	7G	63	DQd	1N
29	DQb	6F	64	DQd	2N
30	DQb	6E	65	DQd	2M
31	DQb	7E	66	DQd	1L
32	DQb	6D	67	DQd	2L
33	DPb	7D	68	DQd	1K
34	A	3C	69	DQd	2K

Maximum Ratings (CY7C1395V25)

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{DD} Relative to GND.....–0.5V to +3.6V

DC Voltage Applied to Outputs in High-Z State ..... –0.5V to V_{DDQ} + 0.5V

DC Input Voltage .....–0.5V to V_{DDQ} + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... >200 mA

Operating Range

Range	Ambient Temperature[19]	V_{DD}	V_{DDQ}
Com'l	0°C to +70°C	2.5V ± 5%	2.5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{DD}	Power Supply Voltage			2.375	2.625	V
V_{DDQ}	I/O Supply Voltage			2.375	2.625	V
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –1.0 mA[22]		2.0		V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 1.0 mA[22]			0.4	V
V_{IH}	Input HIGH Voltage[21]			1.7	V_{DD} + 0.3V	V
V_{IL}	Input LOW Voltage[20]			–0.3	0.7	V
I_X	Input Load Current	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE			–30	30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled		–5	5	µA
I_{DD}	V_{DD} Operating Supply	Read or write every four cycles, V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$[23]	6-ns cycle, 166 MHz		375	mA
			7.5-ns cycle, 133 MHz		300	mA
			10-ns cycle, 100 MHz		250	mA
I_{SB1}	Automatic CE Power-down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} f = f_{MAX} = $1/t_{CYC}$	6-ns cycle, 166 MHz		210	mA
			7.5-ns cycle, 133 MHz		170	mA
			10-ns cycle, 100 MHz		130	mA
I_{SB2}	Automatic CE Power-down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} − 0.3V, f = 0	All speed grades		25	mA
I_{SB3}	Automatic CE Power-down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, or V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} − 0.3V f = f_{MAX} = $1/t_{CYC}$	6-ns cycle, 166 MHz		210	mA
			7.5-ns cycle, 133 MHz		170	mA
			10-ns cycle, 100 MHz		130	mA
I_{SB4}	Automatic CE Power-down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = 0	All speed grades		25	mA

Shaded area contains advanced information.

19. T_A is the case temperature.
20. Minimum voltage equals –0.5V for pulse durations of less than tcyc/2.
21. Maximum voltage equals V_{DD} + 0.7V for pulse durations of less than $t_{CYC/2}$.
22. The load used for V_{OH} and V_{OL} testing is shown in figure (b) of the AC Test Conditions.
23. Icc is measured with 50% Reads and 50% Writes. So a read or a write command is issued every four cycles.

Maximum Ratings (CY7C1395)

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{DD} Relative to GND.....–0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State ..... –0.5V to V_{DDQ} + 0.5V

DC Input Voltage .....–0.5V to V_{DDQ} + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... >200 mA

Operating Range

Range	Ambient Temperature[19]	V_{DD}	V_{DDQ}
Com'l	0°C to +70°C	3.3V ± 5%	2.375V–3.465V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{DD}	Power Supply Voltage			3.135	3.465	V
V_{DDQ}	I/O Supply Voltage			2.375	3.465	V
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –1.0 mA[22]		2.4		V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 1.0 mA[22]			0.4	V
V_{IH}	Input HIGH Voltage[21]			2.0	V_{DD} + 0.3V	V
V_{IL}	Input LOW Voltage[20]			–0.3	0.8	V
I_X	Input Load Current	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE			–30	30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled		–5	5	µA
I_{DD}	V_{DD} Operating Supply	Read or write four cycles, V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$[23]	6-ns cycle, 166 MHz		375	mA
			7.5-ns cycle, 133 MHz		300	mA
			10-ns cycle, 100 MHz		250	mA
I_{SB1}	Automatic CE Power-down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} f = f_{MAX} = $1/t_{CYC}$	6-ns cycle, 166 MHz		210	mA
			7.5-ns cycle, 133 MHz		170	mA
			10-ns cycle, 100 MHz		130	mA
I_{SB2}	Automatic (B41) CE Power-down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} − 0.3V, f = 0	All speed grades		25	mA
I_{SB3}	Automatic CE Power-down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, or V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} − 0.3V f = f_{MAX} = $1/t_{CYC}$	6-ns cycle, 166 MHz		210	mA
			7.5-ns cycle, 133 MHz		170	mA
			10-ns cycle, 100 MHz		130	mA
I_{SB4}	Automatic CE Power-down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = 0	All speed grades		25	mA

Shaded area contains advanced information.

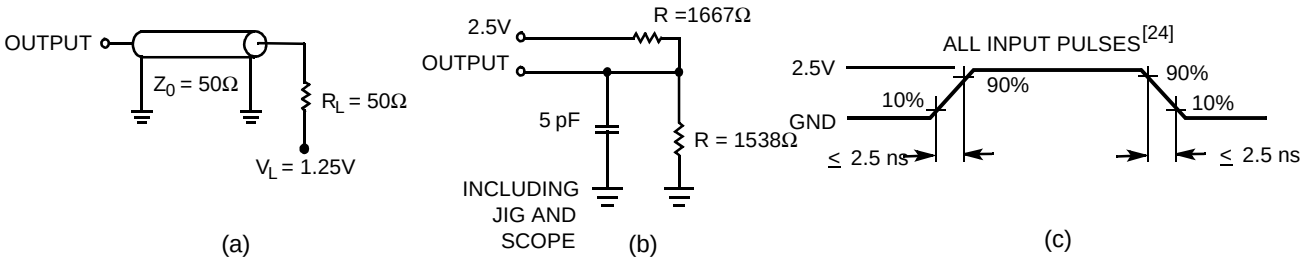
Capacitance[24]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = V_{DDQ} = 2.5V (CY7C1395V25), V_{DD} = V_{DDQ} = 3.3V (CY7C1395)	4	pF
C_{CLK}	Clock Input Capacitance		4	pF
$C_{I/O}$	Input/Output Capacitance		6	pF

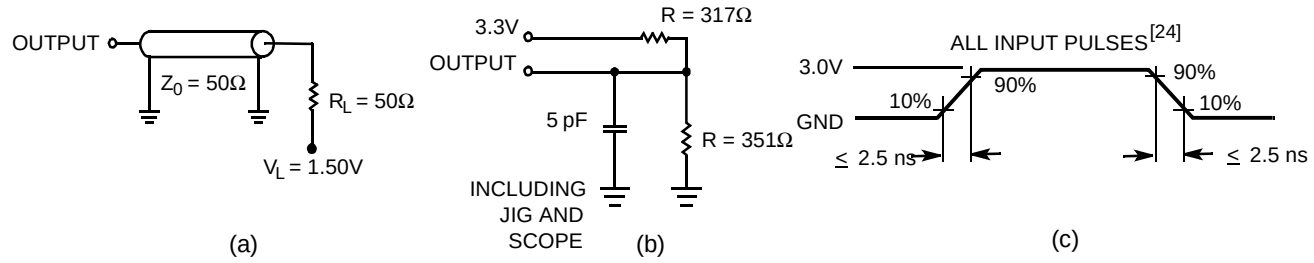
Note:

24. Tested initially and after any design or process change that may affect these parameters.

AC Test Loads and Waveforms (CY7C1395V25)



AC Test Loads and Waveforms (CY7C1395)



Thermal Resistance

Parameter	Description	Test Conditions	TQFP Typ.	PBGA Typ.	Unit	Notes
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit (B41) board	50	37	°C/W	24
Θ_{JC}	Thermal Resistance (Junction to Case)		10	10	°C/W	24

Switching Characteristics Over the Operating Range [25]

Parameter	Description	-166		-133		-100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Clock								
t_{CYC}	Clock Cycle Time	6		7.5		10.0		ns
F_{MAX}	Maximum Operating Frequency		166		133		100	MHz
t_{CH}	Clock HIGH[28]	2.3		2.8		3.2		ns
t_{CL}	Clock LOW[28]	2.3		2.8		3.2		ns
Output Times								
t_{CO}	Data Output Valid After CLK Rise[25]		3.5		4.2		5.0	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid[24, 26, 28]		3.5		4.2		5.0	ns
t_{DOH}	Data Output Hold After CLK Rise	1.5		1.5		1.5		ns
t_{CHZ}	Clock to High-Z[24, 25, 26, 27, 28]	1.5	3.5	1.5	3.5	1.5	3.5	ns
t_{CLZ}	Clock to Low-Z[24, 25, 26, 27, 28]	1.5		1.5		1.5		ns
t_{EOHZ}	$\overline{OE}$ HIGH to Output High-Z[25, 26, 27, 28]		3.3		4.0		4.8	ns
t_{EOLZ}	$\overline{OE}$ LOW to Output Low-Z[25, 26, 27, 28]	0		0		0		ns

Notes:

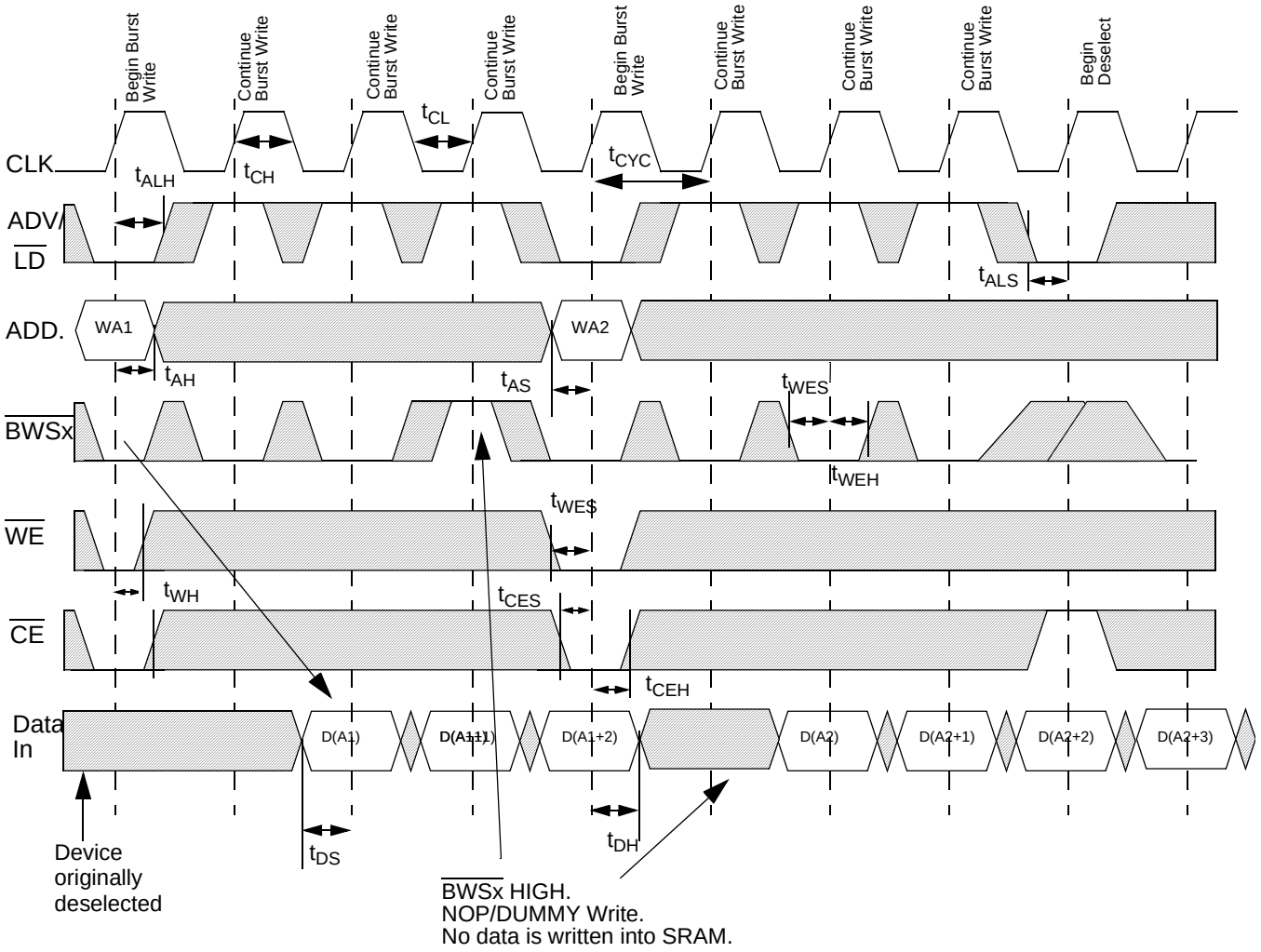
25. AC test conditions assume signal transition time of 2.5 ns or less, timing reference levels, input pulse levels and output loading shown in (a) of AC Test Loads. For –166 speed grade, t_{CO} applies to operation at t_{CYC} >= 7ns. This parameter must be derated by 1.0 ns at F_{MAX}=166 MHz.
26. t_{CHZ}, t_{CLZ}, t_{OEV}, t_{EOLZ}, and t_{EOHZ} are specified with A/C test conditions shown in (a) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
27. At any given voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
28. This parameter is sampled and not 100% tested.

Switching Characteristics Over the Operating Range (continued)[25]

Parameter	Description	-166		-133		-100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Set-up Times								
t_{AS}	Address Set-up Before CLK Rise	2.0		2.0		2.0		ns
t_{DS}	Data Input Set-up Before CLK Rise	2.0		2.0		2.0		ns
t_{CENS}	$\overline{CEN}$ Set-up Before CLK Rise	2.0		2.0		2.0		ns
t_{WES}	$\overline{WE}$, $\overline{BWS_x}$ Set-up Before CLK Rise	2.0		2.0		2.0		ns
t_{ALS}	ADV/$\overline{LD}$ Set-up Before CLK Rise	2.0		2.0		2.0		ns
t_{CES}	Chip Select Set-up	2.0		2.0		2.0		ns
Hold Times								
t_{AH}	Address Hold After CLK Rise	0.5		0.5		0.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CENH}	$\overline{CEN}$ Hold After CLK Rise	0.5		0.5		0.5		ns
t_{WEH}	$\overline{WE}$, $\overline{BW_x}$ Hold After CLK Rise	0.5		0.5		0.5		ns
t_{ALH}	ADV/$\overline{LD}$ Hold after CLK Rise	0.5		0.5		0.5		ns
t_{CEH}	Chip Select Hold After CLK Rise	0.5		0.5		0.5		ns

Switching Waveforms

Burst Write Sequences

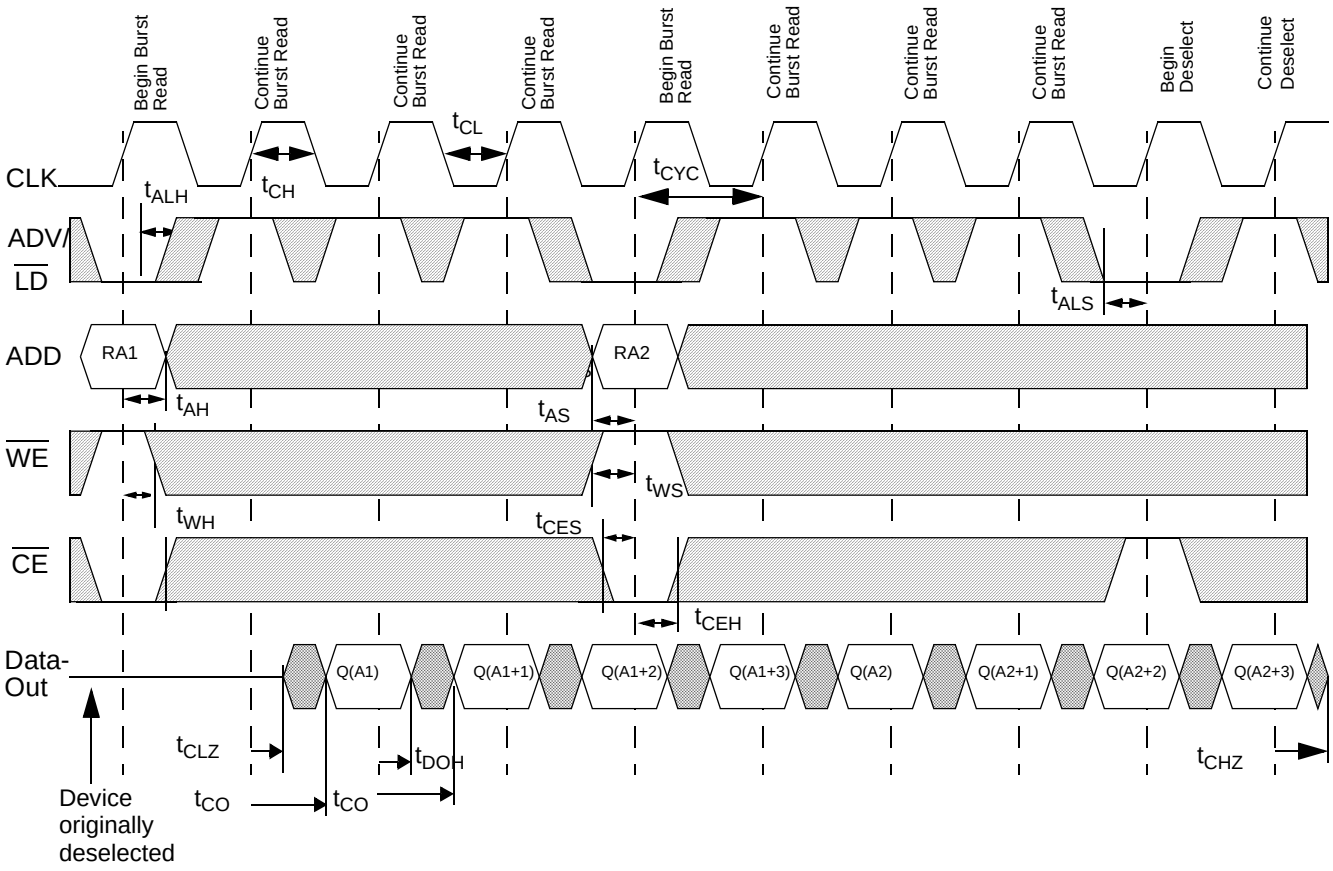


The combination of $\overline{WE}$ and $\overline{BWS}_x$ (x = a, b c, d) defines a write cycle (see Write Cycle Definition table). $\overline{CE}$ is the combination of $\overline{CE}_1$, CE_2, and $\overline{CE}_3$. All chip enables need to be active in order to select the device. Any chip enable can deselect the device. RAx stands for Read Address X, WA stands for Write Address X, Dx stands for Data-in for location X, Qx stands for Data-out for location X. $\overline{CEN}$ held LOW. During burst writes, byte writes can be conducted by asserting the appropriate $\overline{BWS}_x$ input signals. Burst order determined by the state of the MODE input. $\overline{CEN}$ held LOW. $\overline{OE}$ held LOW.

= DON'T CARE = UNDEFINED

Switching Waveforms (continued)

Burst Read Sequences

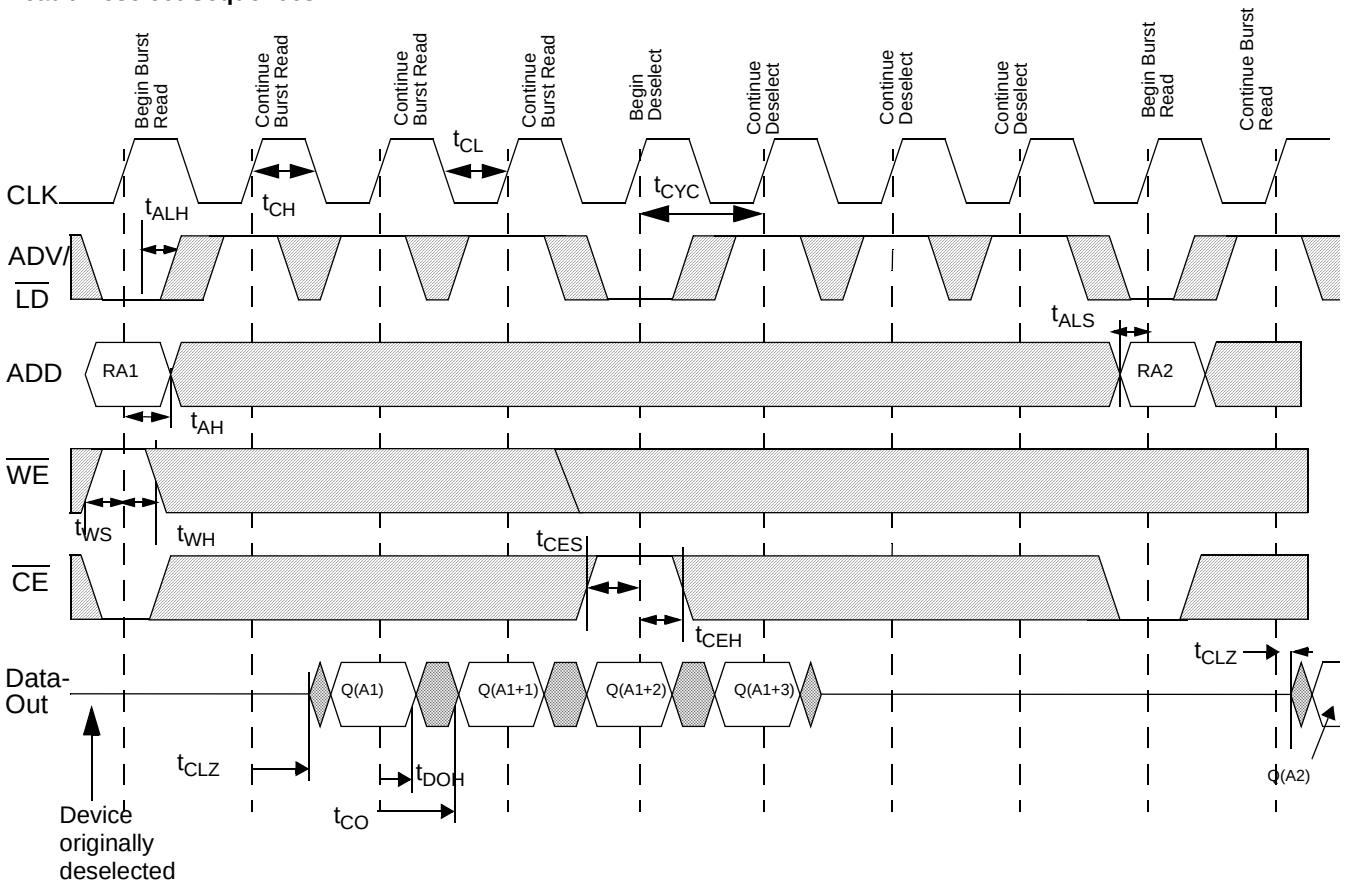


The combination of $\overline{WE}$ and $\overline{BWS}_x$ defines a write cycle (see Write Cycle Definition table). $\overline{CE}$ is the combination of $\overline{CE}_1$, CE_2, and $\overline{CE}_3$. All chip enables need to be active in order to select the device. Any chip enable can deselect the device. RAx stands for Read Address X, WA stands for Write Address X, Dx stands for Data-in for location X, Qx stands for Data-out for location X. $\overline{CEN}$ held LOW. During burst writes, byte writes can be conducted by asserting the appropriate $\overline{BWS}_x$ input signals. Burst order determined by the state of the MODE input. $\overline{CEN}$ held LOW. $\overline{OE}$ held LOW.

= DON'T CARE = UNDEFINED

Switching Waveforms (continued)

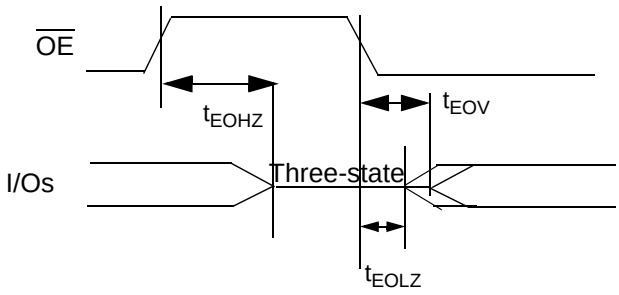
Read / Deselect Sequences



The combination of $\overline{WE}$ and $\overline{BWS_x}$ defines a write cycle (see Write Cycle Definition table). $\overline{CE}$ is the combination of $\overline{CE_1}$, CE_2, and $\overline{CE_3}$. All chip enables need to be active in order to select the device. Any chip enable can deselect the device. RAx stands for Read Address X, WA stands for Write Address X, Dx stands for Data-in for location X, Qx stands for Data-out for location X. $\overline{CEN}$ held LOW. During burst writes, byte writes can be conducted by asserting the appropriate $\overline{BWS_x}$ input signals. Burst order determined by the state of the MODE input. $\overline{CEN}$ held LOW. $\overline{OE}$ held LOW.

= DON'T CARE = UNDEFINED

$\overline{OE}$ Timing



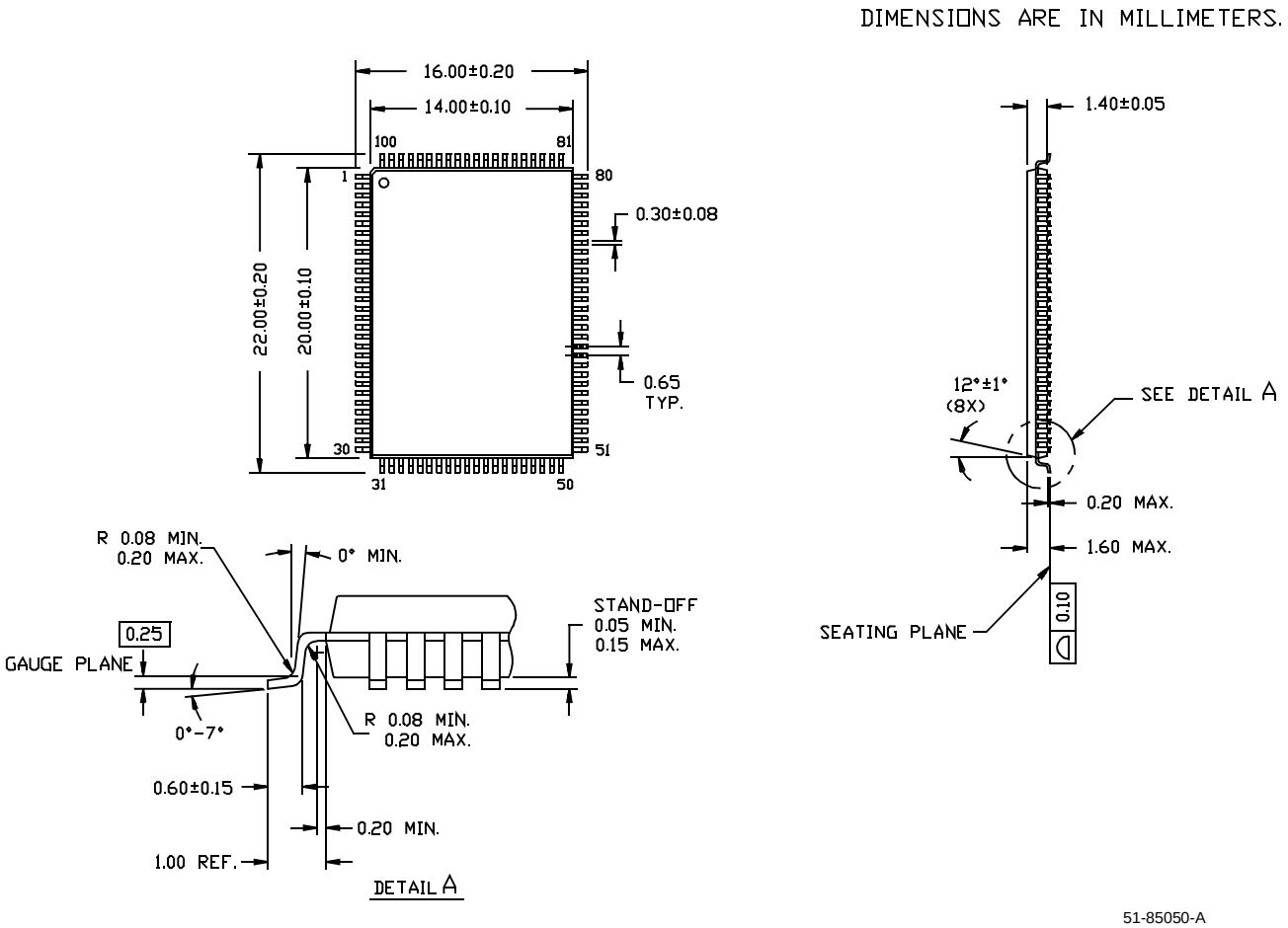
Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
166	CY7C1395V25-166AC CY7C1395-166AC	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	Commercial
	CY7C1395V25-166BGC CY7C1395-166BGC	BG119	14 x 22 BGA	
133	CY7C1395V25-133AC CY7C1395-133AC	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	
	CY7C1395V25-133BGC CY7C1395-133BGC	BG119	14 x 22 BGA	
100	CY7C1395V25-100AC CY7C1395-100AC	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	
	CY7C1395V25-100BGC CY7C1395-100BGC	BG119	14 x 22 BGA	

Shaded area contains advanced information.

Package Diagrams

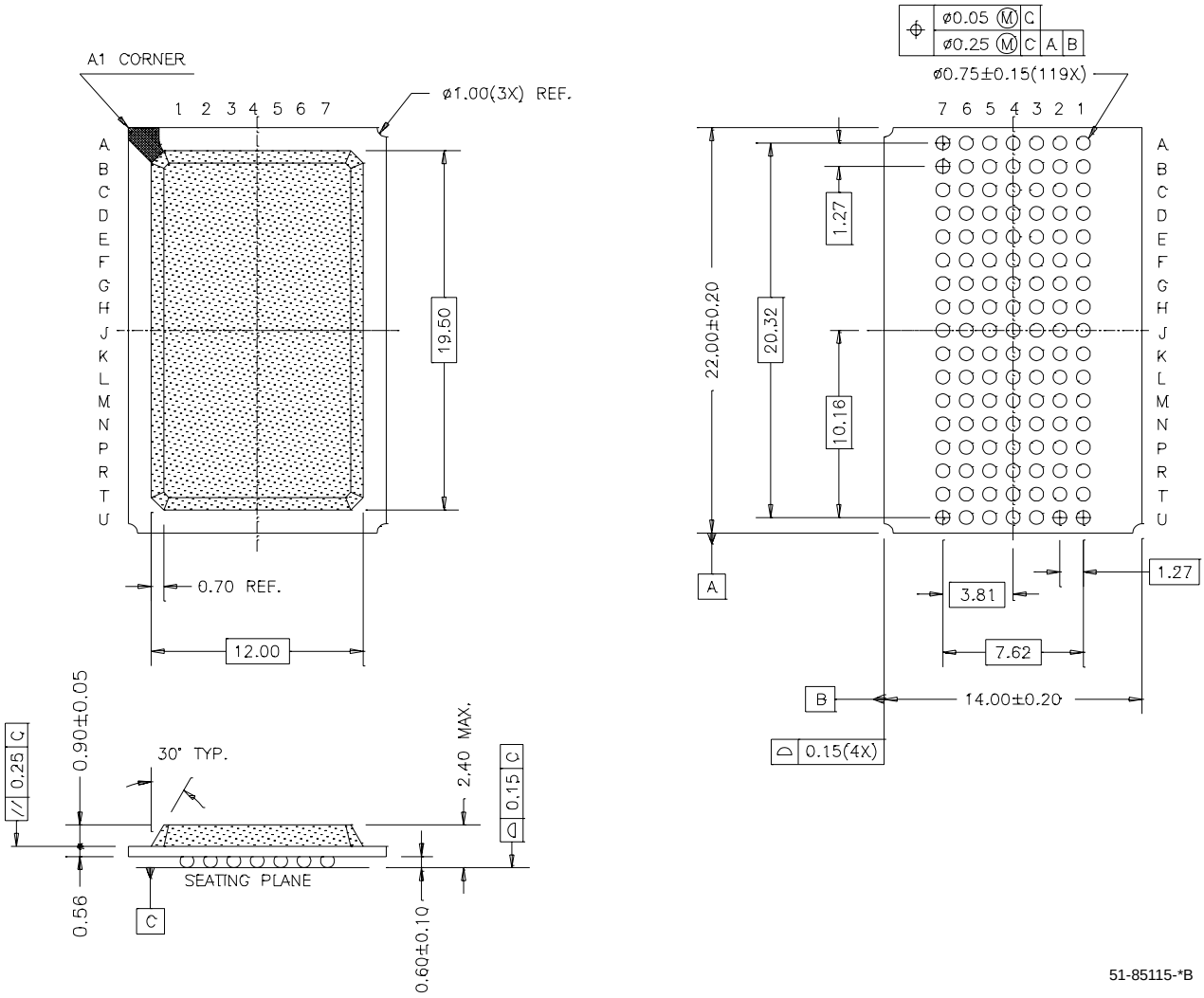
100-pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101



51-85050-A

Package Diagrams (continued)

119-lead PBGA (14 x 22 x 2.4 mm) BG119



51-85115-*B

Document History Page

Document Title: CY7C1395/CY7C1395V25 2M x 36 PBSRAM with NoBL-Burst™ Architecture Document Number: 38-05183				
REV.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110887	10/10/01	SKX	New Data Sheet
*A	124091	02/20/03	CJM	Updated 166 MHz as Advanced Information Updated 119 BGA package pin R7 and T7 Changed operating and standby current for all speeds bin Updated note 24 to include the constraints for 166 MHz speed bin Changed set-up time for -166, from 1.5 ns to 2.0 ns Updated Ordering Information