mosaic

Mosaic Semiconductor Inc.

128Kx 32 FLASH Module

PUMA 2F4001-12/15/20

Issue 1.1 :November 1993

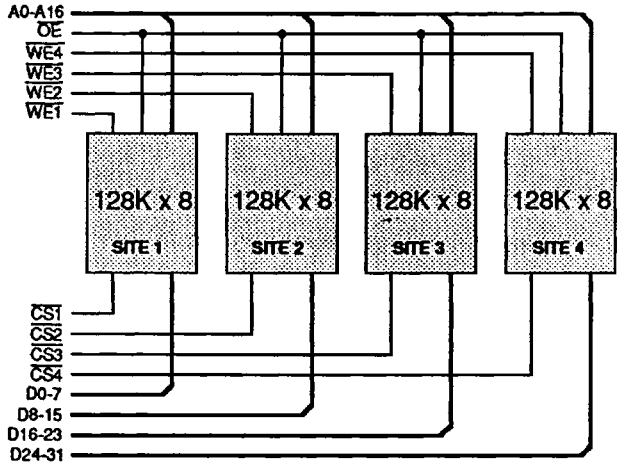
ADVANCE PRODUCT INFORMATION

4,194,304 bit CMOS FLASH Memory

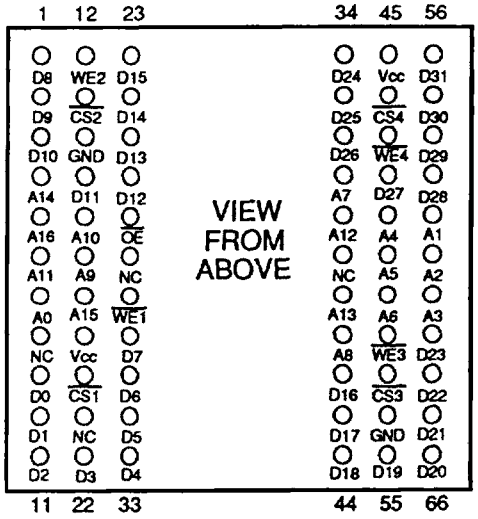
Features

Access Times of 120 /150 /200
User Configurable as 8 / 16 / 32 bit wide output.
Operating Power 275 / 550 / 1100 mW (max).
Low Power Standby 6.6 mW (max).
Five-Volt-Only Reprogramming
Page Write (128 Bytes)
Hardware and Software Data Protection.
$\overline{\text{DATA}}$ Polling and Toggle Bit Functions.
Endurance of 10^3 Cycles
Data Retention 10 years.
Module Components May be Processed to MIL-STD-883 Method 5004.

Block Diagram



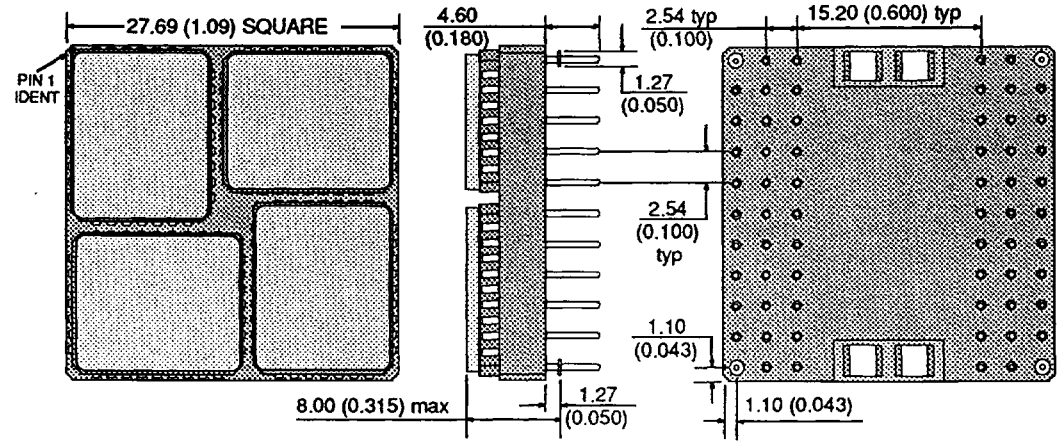
Pin Definition



Pin Functions

A0-16	Address Inputs
D0-31	Data Inputs/Outputs
$\overline{\text{CS1-4}}$	Chip Select
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE1-4}}$	Write Enable
NC	No Connect
V_{cc}	Power (+5V)
GND	Ground

Package Details Dimensions in mm (inches).



MOSCS087

Absolute Maximum Ratings (1)

Operating Temperature	T_{OPR}	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Input voltages (including N.C. pins) with Respect to GND	V_{IN}	-0.6 to 6.25	V
Output voltages with respect to GND	V_{OUT}	-0.6 to V_{CC}+0.6	V

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

		min	*typ*	*max*	
DC Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-	-	0.8	V
Input High Voltage	V_{IH}	2.0	-	-	V
Operating Temp Range	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (I Suffix)
	T_{AM}	-55	-	125	°C (**M, MB** Suffix)

DC Electrical Characteristics (T_A=-55°C to +125°C, V_{CC}=5V ± 10%)

Parameter		*Symbol*	*Test Condition*	*min*	*max*	*Unit*
Input Leakage Current	A0~A15, $\overline{OE}$	I_{LI1}	V_{IN} = GND to V_{CC}	-	40	µA
	$\overline{WE1\sim4}$, $\overline{CS1\sim4}$	I_{LI2}	V_{IN} = GND to V_{CC}	-	10	µA
Output Leakage Current	8 bit	I_{LO}	V_{IN} = GND to V_{CC}, $\overline{CS}^{(1)}$=V_{IH}	-	10	µA
Operating Supply Current	32 bit	I_{CC32}	$\overline{CS}^{(1)}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}, I_{OUT}=0mA, f=5MHz	-	200	mA
	16 bit	I_{CC16}	As above	-	106	mA
	8 bit	I_{CC8}	As above	-	59	mA
Standby Supply Current	TTL levels	I_{SB1}	$\overline{CS}^{(1)}$ = V_{IH}, I_{VO} = 0mA, Other Inputs = V_{IH}	-	12	mA
	CMOS levels	I_{SB2}	$\overline{CS}^{(1)}$ = V_{CC}-0.3V, I_{VO} = 0mA, Other Inputs = V_{CC}	-	1.2	mA
Output Low Voltage		V_{OL}	I_{OL} = 2.1mA.	-	0.45	V
Output High Voltage		V_{OH1}	I_{OH} = -400µA.	2.4	-	V
Output High Voltage CMOS		V_{OH2}	I_{OH} = -100µA.	4.2	-	V

Notes (1) $\overline{CS}$ above are accessed through $\overline{CS1\text{-}4}$. These inputs must be operated simultaneously for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.

Capacitance (T_A=25°C, f=1MHz) Note: These parameters are calculated, not measured.

Parameter		*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance	A0~A15, $\overline{OE}$	C_{IN1}	V_{IN}=0V	16	24	pF
	$\overline{WE1\sim4}$, $\overline{CS1\sim4}$	C_{IN2}	V_{IN}=0V	4	6	pF
Output Capacitance	32 bit	C_{OUT32}	V_{OUT}=0V	8	12	pF

AC Test Conditions

* Input pulse levels: 0.45V to 2.4V
* Input rise and fall times: ≤20ns
* Input and Output timing reference levels: 1.5V
* V_{cc}=5V±10%
* Module tested in 32 bit mode.

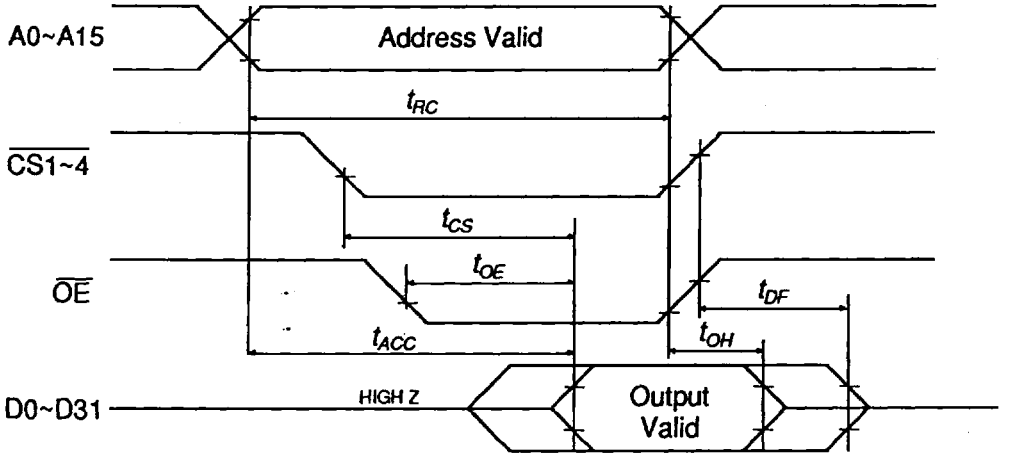
AC READ CHARACTERISTICS

Read Cycle

		-12		-15		-20		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*Unit*
Read Cycle Time	t_{RC}	120	-	150	-	200	-	ns
Address to Output Delay	t_{ACC}	-	120	-	150	-	200	ns
$\overline{CS}$ to Output Delay	t_{CS}	-	120	-	150	-	200	ns
$\overline{OE}$ to Output Delay	t_{OE}	0	50	0	70	0	80	ns
$\overline{CS}$ or $\overline{OE}$ to Output Float (1,2)	t_{DF}	0	40	0	50	0	55	ns
Output Hold from $\overline{OE}$, $\overline{CS}$ or Address, (whichever occured first)	t_{OH}	0	-	0	-	0	-	ns

Notes: (1) t_{DF} is specified from $\overline{OE}$ or $\overline{CS1\sim4}$ whichever occurs first (C_L = 5pF).
(2) This parameter is only sampled and is not 100% tested.

Read Cycle Timing Waveform

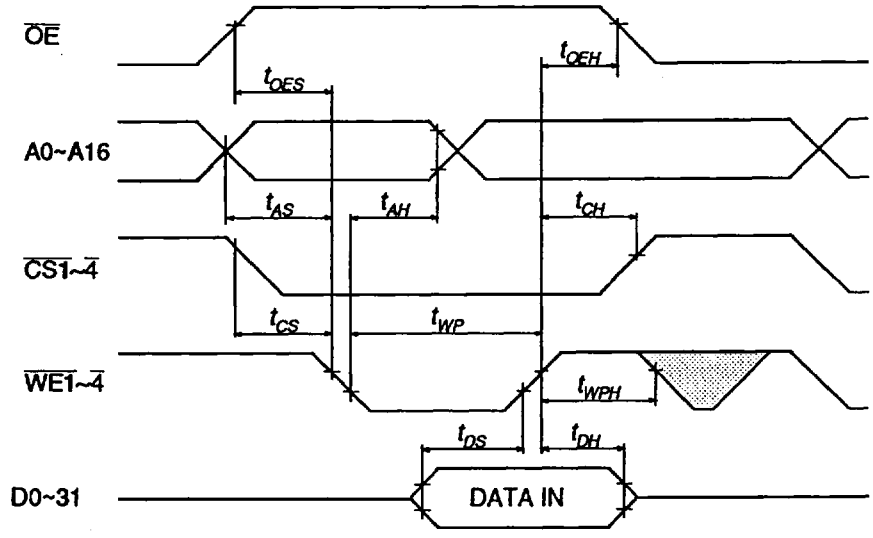


AC WRITE CHARACTERISTICS

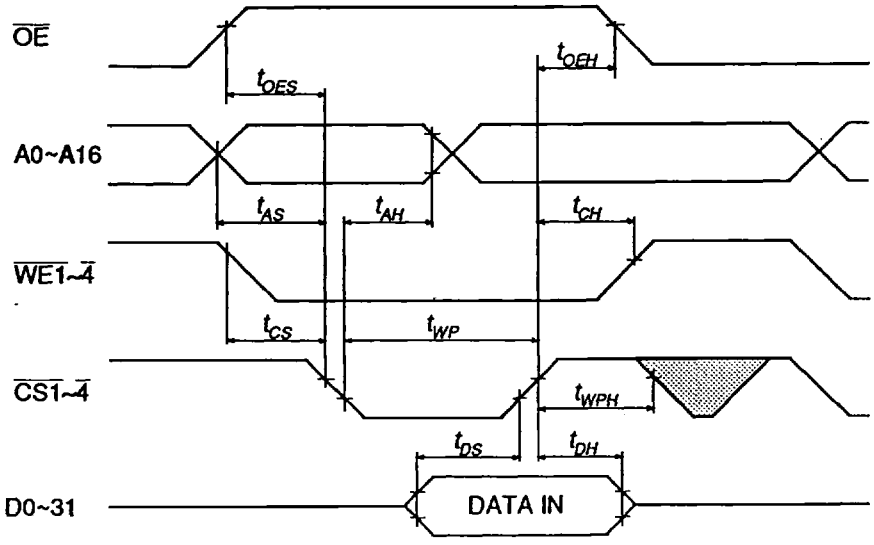
Write Cycle

Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Address Set-up Time	t_{AS}	0	-	-	ns
$\overline{OE}$ Set-up Time	t_{OES}	0	-	-	ns
Address Hold Time	t_{AH}	50	-	-	ns
Chip Select Set-up Time	t_{CS}	0	-	-	ns
Chip Select Hold Time	t_{CH}	0	-	-	ns
Write Pulse Width ($\overline{WE}$ or $\overline{CS}$)	t_{WP}	150	-	-	ns
Data Set-up Time	t_{DS}	50	-	-	ns
Data, $\overline{OE}$ Hold Time	t_{DH}, t_{OEH}	0	-	-	ns
Write Cycle Time	t_{WC}	-	-	10	ms

AC Write Waveform - $\overline{WE}$ Controlled



AC Write Waveform - $\overline{CS}$ Controlled

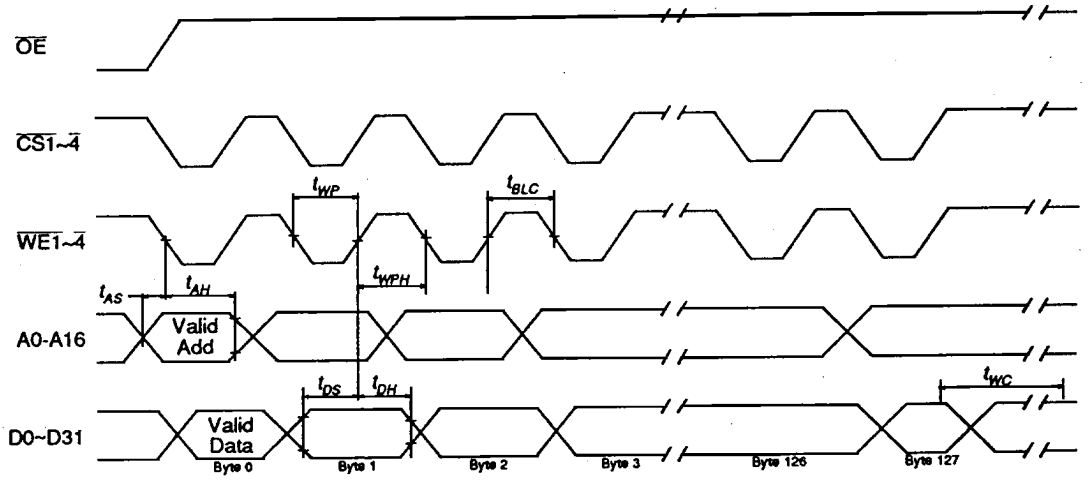


PAGE MODE WRITE CHARACTERISTICS

Write Cycle

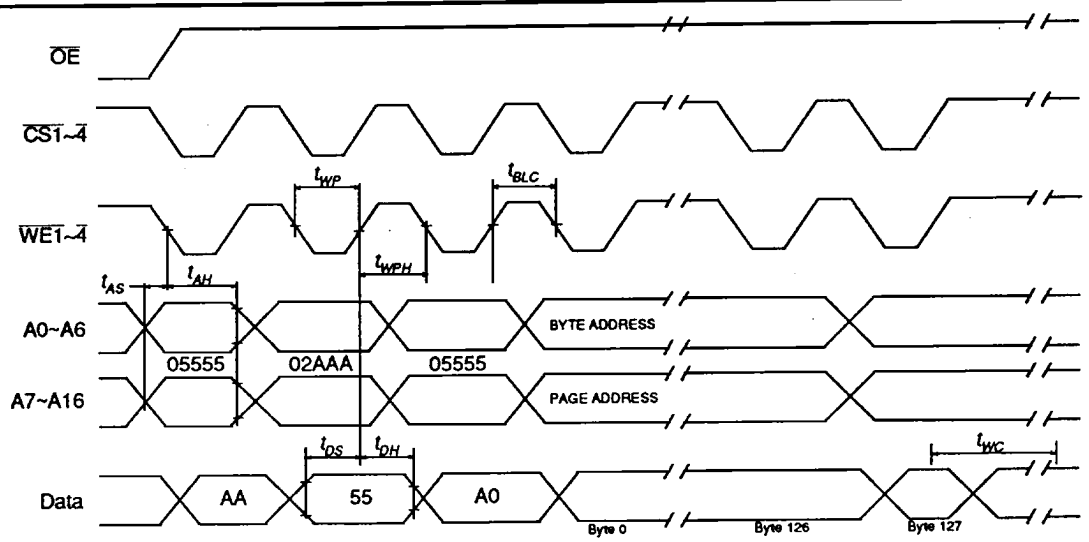
Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Write Cycle Time	t_{WC}	-	-	10	ms
Address Set-up Time	t_{AS}	10	-	-	ns
Address Hold Time	t_{AH}	50	-	-	ns
Data Set-up Time	t_{DS}	50	-	-	ns
Data Hold Time	t_{DH}	10	-	-	ns
Write Pulse Width	t_{WP}	150	-	-	ns
Byte Load Cycle Time	t_{BLC}	-	-	150	µs
Write Pulse Width High	t_{WPH}	100	-	-	ns

Page Mode Write Waveform



Note: A7 through A16 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CS}$). $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CS}$ are both low.

Software Protected Write Waveform



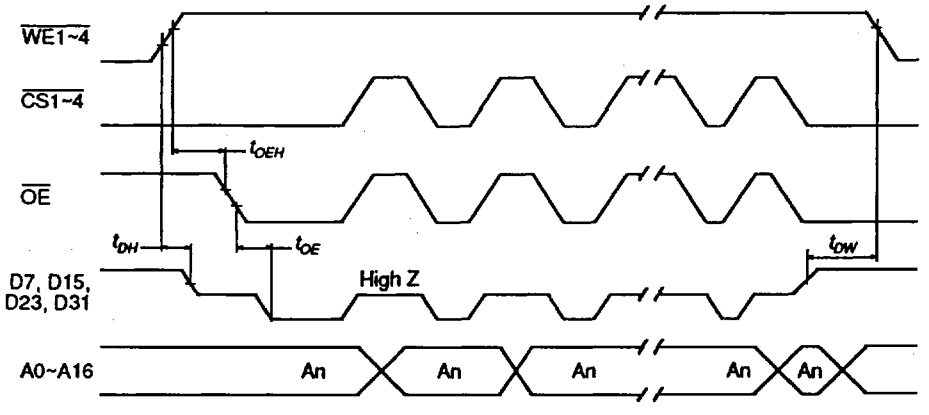
Notes: (1) A7 through A16 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CS}$). $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CS}$ are both low.

(2) The example above is for the PUMA 2F4001 module operating in 8 bit mode.

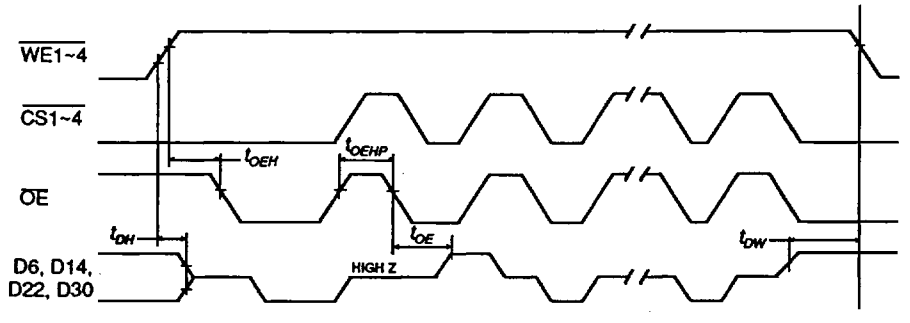
$\overline{\text{DATA}}$ Polling and Toggle Bit Characteristics

Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Data Hold Time	t_{DH}	10	-	-	ns
Output Enable Hold Time	t_{OEH}	10	-	-	ns
Output Enable to Output Delay	t_{OE}	-	-	100	ns
Output Enable High Pulse	t_{OEHP}	150	-	-	ns
Delay to next Write	t_{DW}	0	-	-	µs

$\overline{\text{DATA}}$ Polling Waveform

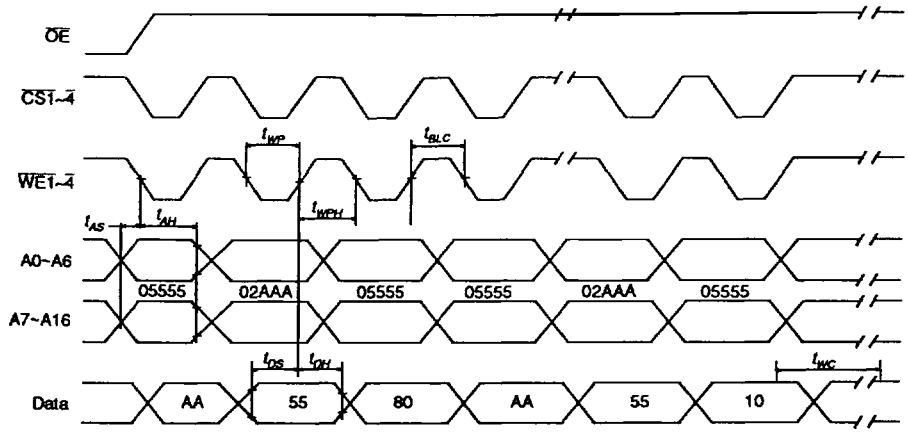


Toggle Bit Waveform

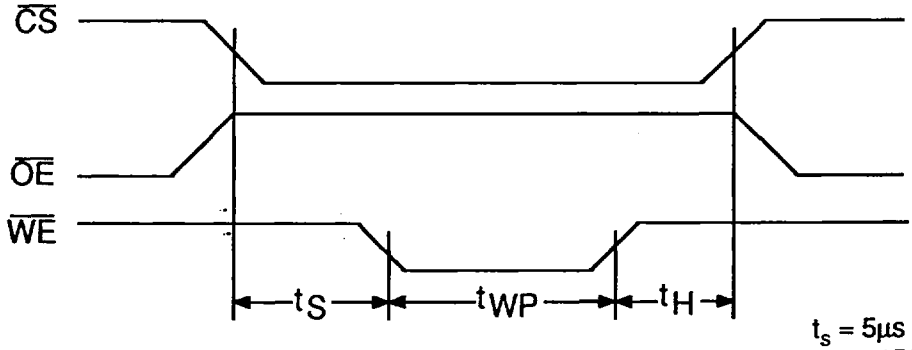


Notes : (1) Toggling either $\overline{\text{OE}}$ or $\overline{\text{CE}}$ or both $\overline{\text{OE}}$ and $\overline{\text{CE}}$ will operate toggle bit
(2) Beginning and ending state of D6,D14,D22,D30 may vary.
(3) Any address location may be used but the address should not vary.

Chip Erase Cycle Waveform



High Voltage Chip Erase



t_S = 5µs (min)
t_{WP} = 150 ns (min)
t_H = 20 ms (min)
V_H = 12.0V±0.5V

DEVICE OPERATION

In the following, $\overline{CS}$ refers to $\overline{CS1}$~4 and $\overline{WE}$ to $\overline{WE1}$~4.

Read

The PUMA 2F4001 is accessed in the same way as a static RAM, with the data stored at the memory location determined by the address pins being placed on the output pins when $\overline{CS}$ and $\overline{OE}$ are low, and $\overline{WE}$ are high. Whenever $\overline{CS}$ or $\overline{OE}$ are high, the outputs are in the OFF or high impedance state.

Programming

The device is reprogrammed on a sector basis.Byte loads are used to enter the 128 bytes of a sector to be programmed or the software codes for data protection. A byte load is performed by ap plying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$.
If a byte of data within a sector is to be changed, data for the entire sector must be loaded into the device. Any byte that is not loaded during the programming of its sector will be erased to read FFh.
During a reprogram cycle, the address locations and 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the sector and then program the latched data using an internal control timer. The end of a program cycle can be detected by DATA polling of I/O7. Once the end of a program cycle has been detected, a new access for a read or program can begin .

DATA Polling

In order to detect the end of a Write Cycle, two methods are provided. During a Write operation (Byte or Page) an attempt to read the last byte written will result in the complement of the written data appearing on D7 (or D15, D23 or D31, depending on the device selected). Once the Write Cycle is complete, true data appears on the outputs and the next Write Cycle may begin. Using this method of indicating the end of a Write can effectively reduce the total write timeby 50%.

Toggle Bit

In addition to DATA polling, another method is provided to determine the end of a Write Cycle. During a write operation successive attempts to read data will result in D6 (or D14, D22 or D30, depending on the device selected) toggling between 1 and 0. Once a write is complete, this toggling will stop and valid data will be read as normal, allowing the next write cycle to be performed. This can eliminate the software housekeeping chore of saving and fetching the last address and data written in order to implement DATA polling. This can be especially helpful in an array composed of multiple PUMA 2F4001 modules that are frequently updated.

Data Protection

Both hardware and software protection is provided as described below.

Four types of hardware protection give high security against accidental writes:

(a) If $V_{cc} \leq 3.8V$, Write is inhibited
(b) $\overline{OE}$ low, $\overline{CS}$ or $\overline{WE}$ high inhibits inadvertent Write Cycles during power-on and power-off. Write Cycle timing specifications must be observed concurrently.
(c) Pulses of less than 15ns on $\overline{WE}$ do not initiate a Write Cycle.

Software controlled data protection, once enabled by the user, means that a software algorithm must be used before any write can be performed. To enable this feature the algorithm opposite is followed, and must be reused for each subsequent write operation. Once set the data protection remains operational until it is disabled by the using the second algorithm opposite; power transitions will not reset this feature.

Operating Modes

The table below shows the logic inputs required to control the operating modes of each Device on the PUMA 2F4001.

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	*Outputs*
Read	0	0	1	Data Out
Write (1)	0	1	0	Data In
Standby	1	X	X	High Z
Write Inhibit	X	X	1	
Write Inhibit	X	0	X	
Output Disable	X	1	X	High Z

$1 = V_{IH}$ $0 = V_{IL}$ X = Don't care
Note: (1) Refer to AC Programming Waveforms

Software Data Protection

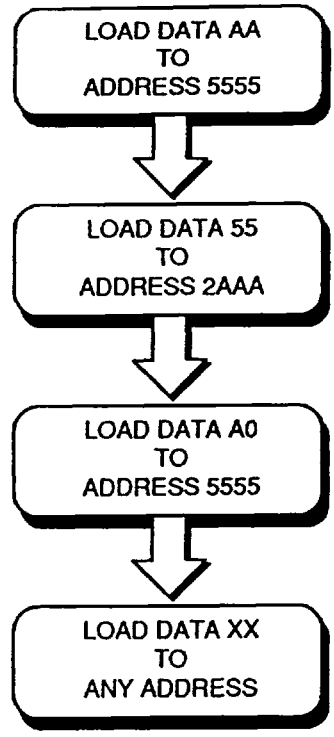
The algorithms below describe the process by which an individual 128K x 8 device on the PUMA may be software write protected and unprotected. Thus, these algorithms apply to the PUMA operating in 8 bit mode; if 16 or 32 bit modes are being used, then the relevant data would be placed on the 16 or 32 bit buses as two or four 8 bit bytes respectively e.g. 5555_H and 55555555_H. In the case of 16 bit mode, this process would be repeated twice with the appropriate devices selected.

The PUMA 2F4001 is shipped with data Protection **NOT ENABLED.** In this mode data should be protected during power-up and power-down operations through the use of external circuits.

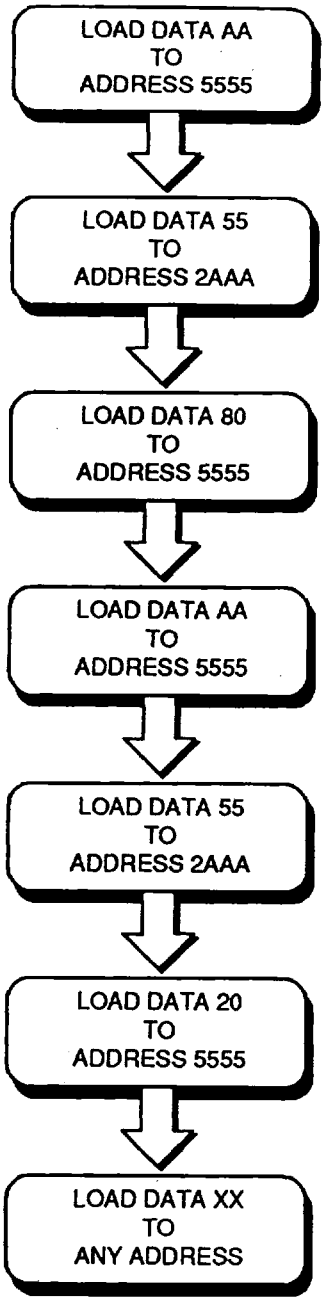
Once data protection has been enabled it is set for the life of the device unless the reset algorithm is followed. In protected mode write operations to the device(s) on the PUMA must be preceeded by a series of three write operations to three specific locations, after which 1 to 128 bytes of data may be written. Once the page load cycle is complete, the device(s) return to the data protected state.

NOTE: Once initiated, the sequence of write operations to Enable and Disable Write Protect should not be interrupted.

Enable Algorithm



Disable Algorithm(1)



Notes:

(1) Data Format I/O7-I/O0 (Hex);
Address Format: A14-A0 (Hex).
Once initiated, this sequence of write operations should not be interrupted.

(2) Enable Write Protect state will be initiated at end of write even if no other data is loaded.

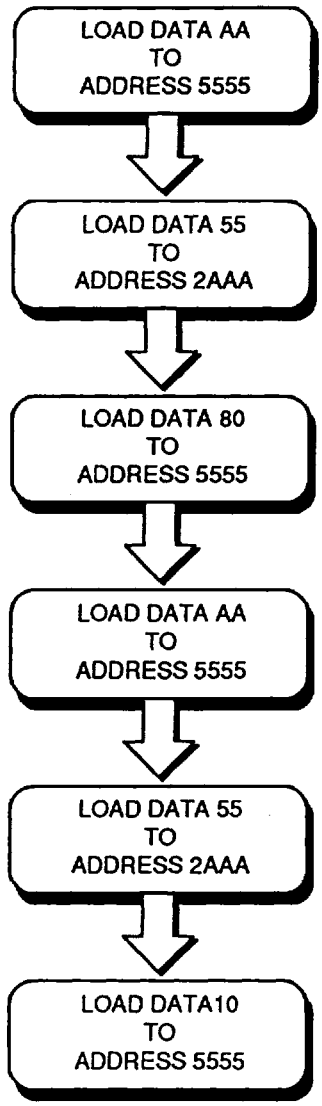
(3) Disable Write Protect state will be initiated at end of write period even if no other data is loaded.

(4) 1 to 128 bytes of data may be loaded.

Chip Erase

The Puma 2F4001 offers a chip erase function in which the entire device can be erased by a six byte algorithm. Once this code has been entered, the device will set each byte to a high state erasing any stored data. The device will also internally time this operation so that no external clocks are needed.
The PUMA 2F4001 can also be completely erased by setting the entire device to a high state. This is accomplished by first placing $\overline{OE}$ at 12 volts with $\overline{CE}$ low and $\overline{WE}$ high: when $\overline{WE}$ is pulsed low for a minimum of 20 ms, the contents of the entire device will be erased.

Chip Erase Algorithm



Ordering Information

PUMA 2F4001MB-20

Speed	12	= 120 ns
	15	= 150 ns
	20	= 200 ns
Temp. range/screening	Blank	= Commercial Temperature
	I	= Industrial Temperature
	M	= Military Temperature
	MB	= Processed to MIL-STD-883C Method 5004, non compliant.
Organization	4001	= 128K x 32, user configurable as 256K x 16 and 512K x 8
Memory Type	F	= FLASH MEMORY
Package	PUMA 2	= 66 pin Ceramic PGA

The policy of the company is one of continuous development and while the information presented in this data sheet is believed to be accurate, no liability is assumed for any data contained within. The company reserves the right to make changes without notice at any time.

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