FEDL7603_7603B-03
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OKI Semiconductor

MSM7603/7603B

Echo Canceler

GENERAL DESCRIPTION

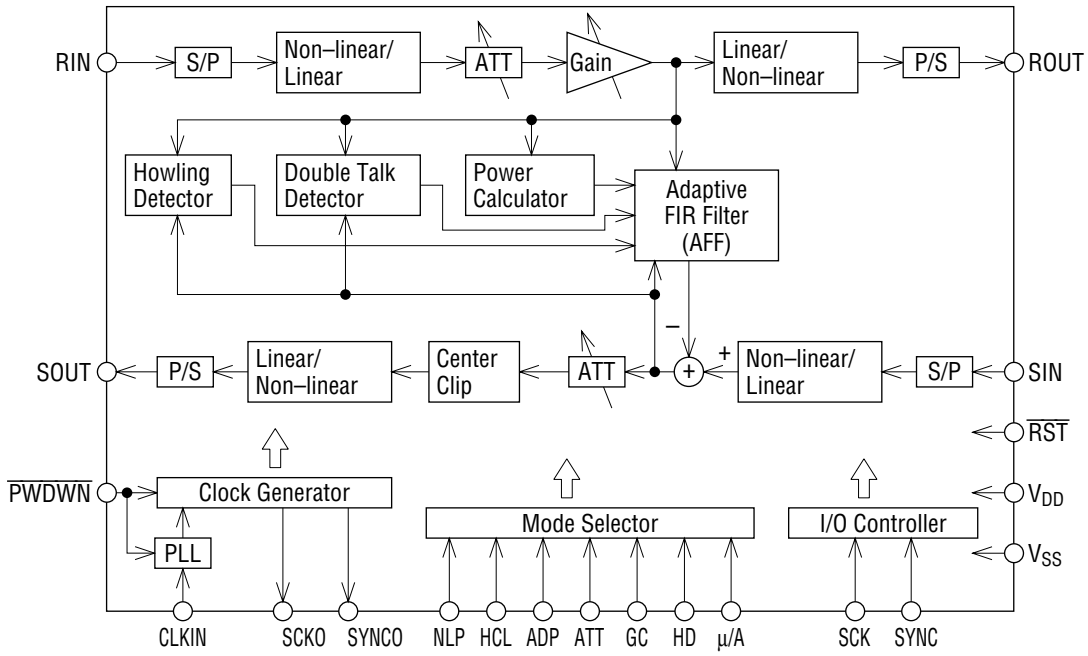
The MSM7603/7603B is an improved version of the MSM7602 with basically the same configuration, and offers twice the cancelable echo delay time of the MSM7602.
The MSM7603B I/O interface allows switching between μ-law PCM and A-law PCM.
The MSM7603/7603B is a low-power CMOS IC device for canceling echo (in an acoustic system or telephone line) generated in a speech path.
Echo is canceled, in digital signal processing, by estimating the echo path and generating a pseudo echo signal.
When used as an acoustic echo canceler, the device can cancel the acoustic echo, between the loud speaker and the microphone, which occur during hands free communication such as on a cellular phone or a conference system phone.
When used as a line echo canceler, the device can cancel the line echo which returns due to impedance mismatching in a hybrid.
In addition, a quality conversation is made possible by controlling the level and by preventing howling through a howling detector, double talk detector, attenuation function and a gain control function, and by controlling the low level noise by means of a center clipping function.
The use of a single chip codec, such as the MSM7704 (3 V) and MSM7533 (5 V), allows an economic and efficient echo canceler to be configured.

FEATURES

- Can handle both acoustic and telephone line echoes.
- Switchable between μ-law PCM and A-law PCM interfaces. (MSM7603B)
- Cancelable echo delay time:
  MSM7603B-003 ..... 55 ms (max.)
- Echo attenuation : 30 dB (typ.)
- Clock frequency : 19.2 MHz
  17.5 MHz to 20 MHz (when internal sync signal not used)
- Power supply voltage : 2.7 V to 5.5 V
- Package:
  28-pin plastic SSOP (SSOP28-P-485-0.65-K) (Product name : MSM7603-003GS-K)
  (Product name : MSM7603B-003GS-K)

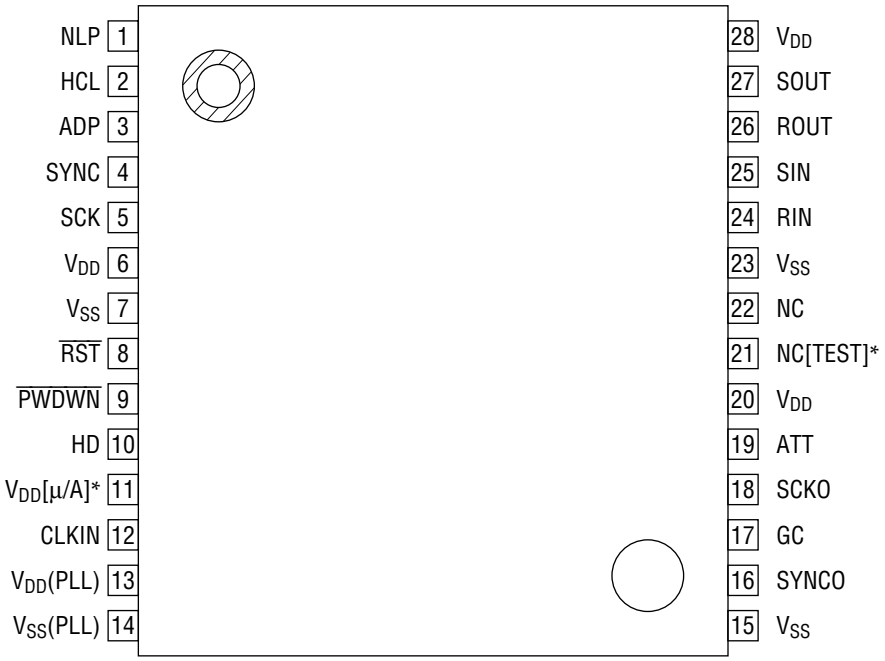
BLOCK DIAGRAM

MSM7603/7603B



* For MSM7603B only

PIN CONFIGURATION (TOP VIEW)



NC : No connect pin

28-Pin Plastic SSOP

* Pins shown in brackets apply to MSM7603B.

PIN DESCRIPTIONS

Pin	Symbol	Type	Description
1	NLP	I	This is the control pin for the center clipping function to force the SOUT output to a minimum value when the SOUT signal is below –54 dBm0. Effective for reducing low-level noise. "H": Center clip ON "L": Center clip OFF
2	HCL	I	This is the through mode control pin. When this pin is in the through mode the RIN and SIN data are output to ROUT and SOUT. At the same time, the coefficient of the adaptive FIR filter is cleared. "H": Through mode "L": Normal mode (echo canceler operates)
3	ADP	I	This is the AFF coefficient control pin which stops updating the adaptive FIR filter (AFF) coefficient and sets it to a fixed value, when the pin is configured to be the coefficient fix mode. Used when holding the AFF coefficient which has been once converged. "H": Coefficient fix mode "L": Normal mode (coefficient update)
4	SYNC	I	This is the input pin for the sync signal for transmit/receive serial data. This pin uses the external SYNC or SYNCO. Inputs the PCM codec transmit/receive sync signal (8 kHz).
5	SCK	I	This is the clock input pin for transmit/receive serial data. It uses the external SCK or the SCKO. Input the PCM codec transmit/receive clock (64 to 2048 kHz).
8	$\overline{RST}$	I	This is the input pin for the reset signal. "L": Reset mode "H": Normal operation mode Due to initialization, input signals are disabled for 100 μs after reset (after $\overline{RST}$ is returned from "L" to "H"). Input the basic clock during the reset. Output pins during the reset are in the following sates : High impedance: SOUT, ROUT Not affected: SYNCO, SCKO After the power is turned on, initialize the LSI's internal registers by your execution of H→L sequence 1μs later than the master clock starts normal oscilation. This LSI starts a normal operation by releasing this pin to H after the H→L sequence above. Here, this pin must stay L for 1μs or longer.

PIN DESCRIPTIONS (Continued)

Pin	Symbol	Type	Description
9	$\overline{\text{PWDWN}}$	I	This is the power-down mode control pin for power down operation "L": Power-down mode "H": Normal operation mode During power-down mode, all input pins are disabled and output pins are in the following states : High impedance : SOUT, ROUT "L": SYNCO, SCKO Reset after the power-down mode is released.
10	HD	I	This pin controls the howling detect function that detects and cancels a howling generated during hands-free talking for acoustic system. This function is used to cancel acoustic echoes. "L": Howling detector ON "H": Howling detector OFF
11	(μ/A)	I	Used for MSM7603B only. This is the input pin for μ-law PCM/A-law PCM interface select signal. "L": A-law PCM interface "H": μ-law PCM interface For MSM7603, apply V_{DD}.
12	CLKIN	I	This is the input pin for external input for the basic clock. Input the basic clock (17.5 to 20 MHz). When the internal sync signal (SYNCO, SCKO) is used, input the basic clock of 19.2 MHz.
13	V_{DD} (PLL)	I	This is the power supply pin for the PLL circuit used for the basic clock. Insert a 0.1 μF capacitor with excellent high frequency characteristics between V_{DD} (PLL) and V_{SS} (PLL).
14	V_{SS} (PLL)	I	This is the ground pin for the PLL circuit used for the basic clock.
16	SYNCO	O	This is the output pin for the 8 kHz sync signal for the PCM codec. Connect to the SYNC pin and the PCM codec transmit/receive sync pin. Leave open if using an external SYNC.

PIN DESCRIPTIONS (Continued)

Pin	Symbol	Type	Description
17	GC	I	This is the pin for the input signal by which the gain controller for the RIN input is controlled. The pin also controls RIN input level and prevents howling. The gain controller adjusts the RIN input level when it is –20 dBm0 or above. RIN input levels from –20 to –11.5 dBm0 will be suppressed to –20 dBm0 in the attenuation range from 0 to 8.5 dB. RIN input levels above –11.5 dBm0 will always be attenuated by 8.5 dB. "H": Gain control ON "L": Gain control OFF "H" is recommended for performing echo cancellation.
18	SCKO	O	This is the output pin for the transmit clock signal (256 kHz) for the PCM codec. Connect to the SCK pin and the PCM codec transmit/receive clock pin. Leave open when using an external SCK.
19	ATT	I	This is the control pin for the ATT function which prevents howling by attenuators (ATT) for the RIN input and SOUT output. If there is input only to RIN, then the ATT for the SOUT output is activated. If there is no input to SIN or there is input to both SIN and RIN, then the ATT for the RIN input is activated. Either the ATT for the RIN output or the ATT for the SOUT is always activated in all cases, and the attenuation of ATT is 6 dB. "H": ATT OFF "L": ATT ON "L" is recommended for performing echo cancellation.
21	(TEST)	O	This pin is for MSM7603B only and not used. Should be left open. In MSM7603 it is an NC pin.
24	RIN	I	This is the receive serial data input pin. Input the PCM signal synchronized to SYNC and SCK. Data is read at the falling edge of SCK.
25	SIN	I	This is the transmit serial data input pin. Input the PCM signal synchronized to SYNC and SCK. Data is read at the falling edge of SCK.
26	ROUT	O	This is the output pin for receive serial data. Outputs the PCM signal synchronized to SYNC and SCK. This pin is in high impedance state during the absence of data output.
27	SOUT	O	This is the output pin for transmit serial data. Outputs the PCM signal synchronized to SYNC and SCK. This pin is in high impedance state during the absence of data output.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to + 7	V
Input Voltage	V_{IN}		–0.3 to V_{DD} + 0.3	V
Power Dissipation	P_D		1	W
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{DD} = 2.7 V to 3.6 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	—	2.7	3.3	3.6	V
Power Supply Voltage	V_{SS}	—	—	0	—	V
High Level Input Voltage	V_{IH}	—	2.0	—	V_{DD}	V
Low Level Input Voltage	V_{IL}	—	0	—	0.5	V
Operating Temperature	Ta	—	–40	+25	+85	°C

(V_{DD} = 4.5 V to 5.5 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	—	4.5	5	5.5	V
Power Supply Voltage	V_{SS}	—	—	0	—	V
High Level Input Voltage	V_{IH}	—	2.4	—	V_{DD}	V
Low Level Input Voltage	V_{IL}	—	0	—	0.8	V
Operating Temperature	Ta	—	–40	+25	+85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 2.7 V to 3.6 V, Ta = –40°C to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High Level Output Voltage	V_{OH}	I_{OH} = 40 µA	2.2	—	V_{DD}	V
Low Level Output Voltage	V_{OL}	I_{OL} = 1.6 mA	0	—	0.4	V
High Level Input Current	I_{IH}	$V_{IH} = V_{DD}$	—	0.1	1	µA
Low Level Input Current	I_{IL}	$V_{IL} = V_{SS}$	–1	–0.1	—	µA
High Level Output Leakage Current	I_{OZH}	$V_{OH} = V_{DD}$	—	0.1	1	µA
Low Level Output Leakage Current	I_{OZL}	$V_{OL} = V_{SS}$	–1	–0.1	—	µA
Power Supply Current (Operating)	I_{DDO}	—	—	30	50	mA
Power Supply Current (Standby)	I_{DDS}	$\overline{PWDWN}$ = "L"	—	0.5	1	mA
Input Capacitance	C_I	—	—	—	15	pF
Output Load Capacitance	C_{LOAD}	—	—	—	20	pF

(V_{DD} = 4.5 V to 5.5 V, Ta = –40°C to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High Level Output Voltage	V_{OH}	I_{OH} = 40 µA	4.2	—	V_{DD}	V
Low Level Output Voltage	V_{OL}	I_{OL} = 1.6 mA	0	—	0.4	V
High Level Input Current	I_{IH}	$V_{IH} = V_{DD}$	—	0.1	10	µA
Low Level Input Current	I_{IL}	$V_{IL} = V_{SS}$	–10	–0.1	—	µA
High Level Output Leakage Current	I_{OZH}	$V_{OH} = V_{DD}$	—	0.1	10	µA
Low Level Output Leakage Current	I_{OZL}	$V_{OL} = V_{SS}$	–10	–0.1	—	µA
Power Supply Current (Operating)	I_{DDO}	—	—	40	70	mA
Power Supply Current (Standby)	I_{DDS}	$\overline{PWDWN}$ = "L"	—	0.5	1	mA
Input Capacitance	C_I	—	—	—	15	pF
Output Load Capacitance	C_{LOAD}	—	—	—	20	pF

Echo Canceler Characteristics (Refer to Characteristics Diagram)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Echo Attenuation	L_{RES}	R_{IN} = –10 dBm0 (5 kHz band white noise) E. R. L. (echo return loss) = 6 dB T_D = 50 ms ATT, GC, NLP: OFF	—	30	—	dB
Cancelable Echo Delay Time	T_D	R_{IN} = –10 dBm0 (5 kHz band white noise) E. R. L. = 6 dB ATT, GC, NLP: OFF	—	—	55	ms

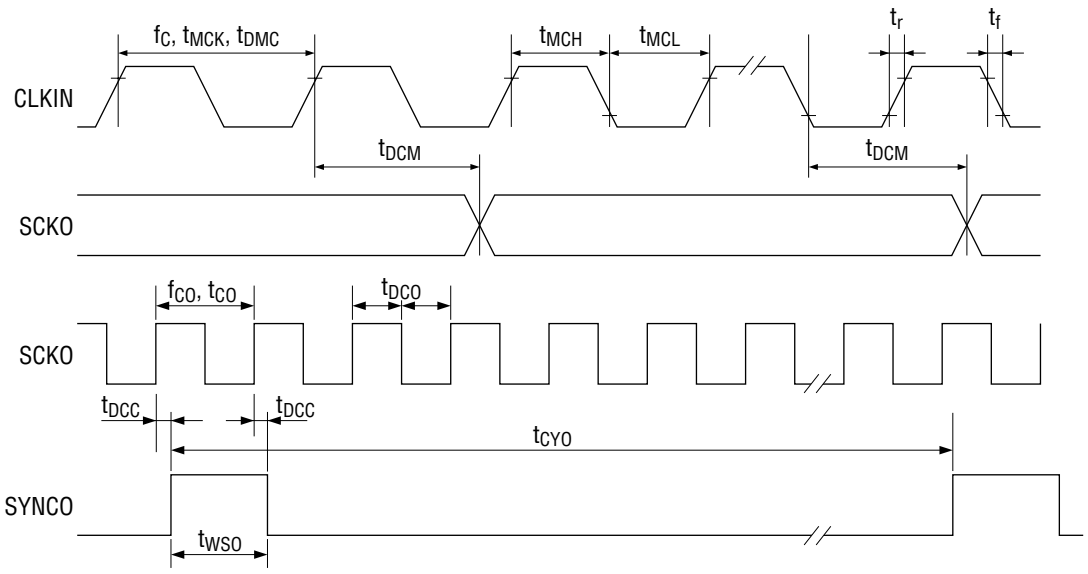
AC Characteristics

(Ta = –40°C to +85°C)

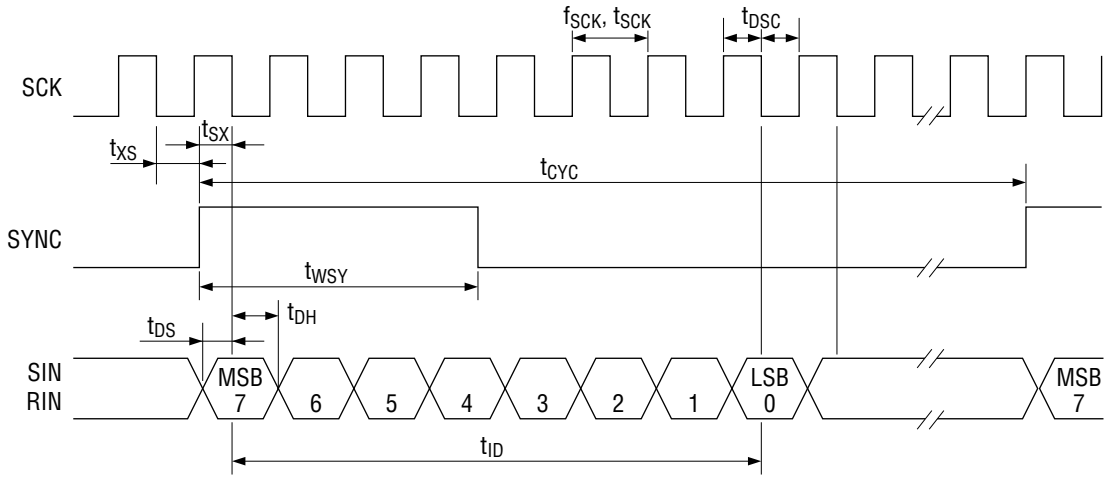
Parameter	Symbol	V_{DD} = 2.7 V to 3.6 V			V_{DD} = 4.5 V to 5.5 V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	f_C	—	19.2	—	—	19.2	—	MHz
When Internal Sync Signal is not used		17.5	—	20.0	17.5	—	20.0	
Clock Cycle Time	t_{MCK}	—	52.08	—	—	52.08	—	ns
When Internal Sync Signal is not used		50.0	—	57.14	50.0	—	57.14	
Clock Duty Ratio	t_{DMC}	40	—	60	40	—	60	ns
Clock "H" Level Pulse Width f_C = 19.2 MHz	t_{MCH}	20.8	—	31.3	20.8	—	31.3	ns
Clock "L" Level Pulse Width f_C = 19.2 MHz	t_{MCL}	20.8	—	31.3	20.8	—	31.3	ns
Clock Rise Time	t_r	—	—	5	—	—	5	ns
Clock Fall Time	t_f	—	—	5	—	—	5	ns
Sync Clock Output Time	t_{DCM}	—	—	40	—	—	40	ns
Internal Sync Clock Frequency	f_{CO}	—	256	—	—	256	—	kHz
Internal Sync Clock Output Cycle Time	t_{CO}	—	3.9	—	—	3.9	—	µs
Internal Sync Clock Duty Ratio	t_{DCO}	—	50	—	—	50	—	%
Internal Sync Signal Output Delay Time	t_{DCC}	—	—	5	—	—	5	ns
Internal Sync Signal Period	t_{CYO}	—	125	—	—	125	—	µs
Internal Sync Signal Output Width	t_{WSO}	—	t_{CO}	—	—	t_{CO}	—	µs
Transmit/Receive Sync Clock Frequency	f_{SCK}	64	—	2048	64	—	2048	kHz
Transmit/Receive Sync Clock Cycle Time	t_{SCK}	0.488	—	15.6	0.488	—	15.6	µs
Transmit/Receive Sync Clock Duty Ratio	t_{DSC}	40	50	60	40	50	60	%
Transmit/Receive Sync Signal Period	t_{CYC}	123	125	—	123	125	—	µs
Sync Timing	t_{XS}	45	—	—	45	—	—	ns
	t_{SX}	45	—	—	45	—	—	ns
Sync Signal Width	t_{WSY}	t_{SCK}	—	t_{CYC}-t_{SCK}	t_{SCK}	—	t_{CYC}-t_{SCK}	µs
Receive Signal Setup Time	t_{DS}	45	—	—	45	—	—	ns
Receive Signal Hold Time	t_{DH}	45	—	—	45	—	—	ns
Receive Data Input Time	t_{ID}	—	$7t_{SCK}$	—	—	$7t_{SCK}$	—	µs
Serial Output Delay Time	t_{SD}	—	—	90	—	—	90	ns
	t_{XD}	—	—	90	—	—	90	ns
Reset Signal Input Width	t_{WR}	1	—	—	1	—	—	µs
Reset Start Time	t_{DRS}	5	—	—	5	—	—	ns
Reset End Time	t_{DRE}	—	—	52	—	—	52	ns
Processing Operation Start Time	t_{DIT}	100	—	—	100	—	—	µs
Power Down Start Time	t_{DPS}	—	—	111	—	—	111	ns
Power Down End Time	t_{DPE}	—	—	15	—	—	15	ns
Reset Pulse Width Immediately after Power Down	t_{WPR}	10	—	—	10	—	—	ns
Control Pin Setup Time ($\overline{RST}$)	t_{DSR}	20	—	—	20	—	—	ns
Control Pin Hold Time ($\overline{RST}$)	t_{DHR}	20	—	—	20	—	—	ns
Control Pin Setup Time	t_{DTS}	0	—	—	0	—	—	ns
Control Pin Hold Time	t_{DTH}	160	—	—	160	—	—	ns

TIMING DIAGRAM

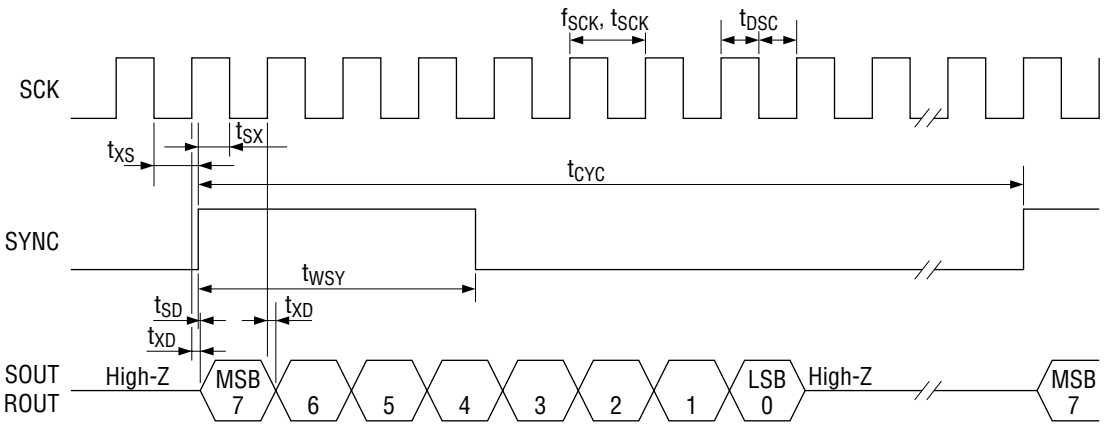
Clock Timing



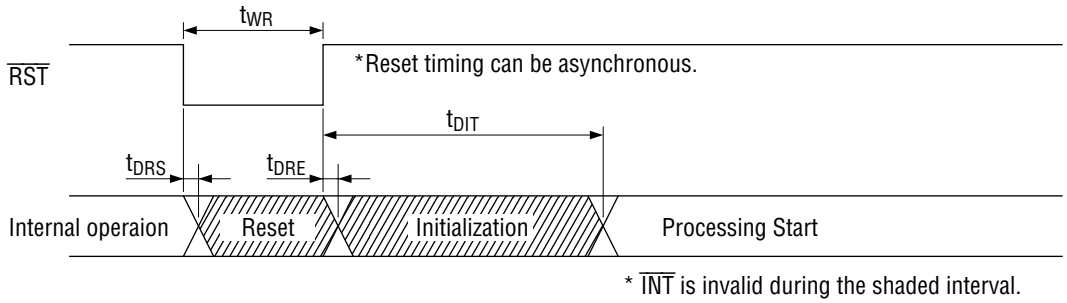
Serial Input Timing



Serial Output Timing

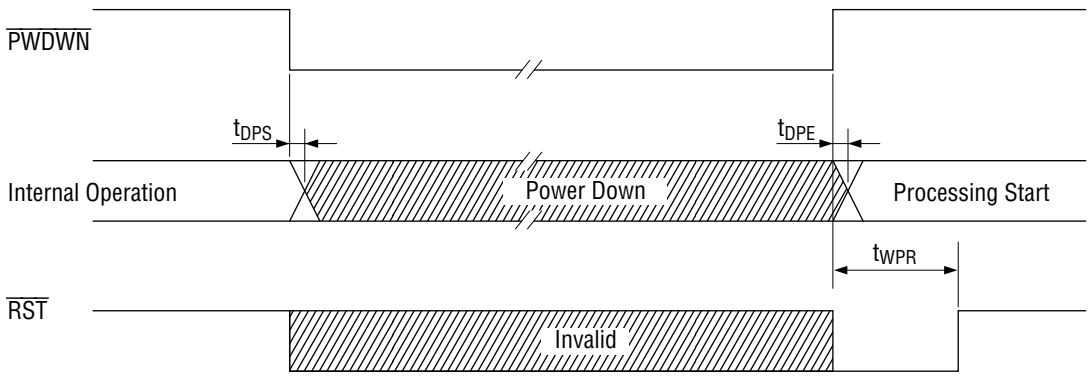


Operation Timing After Reset

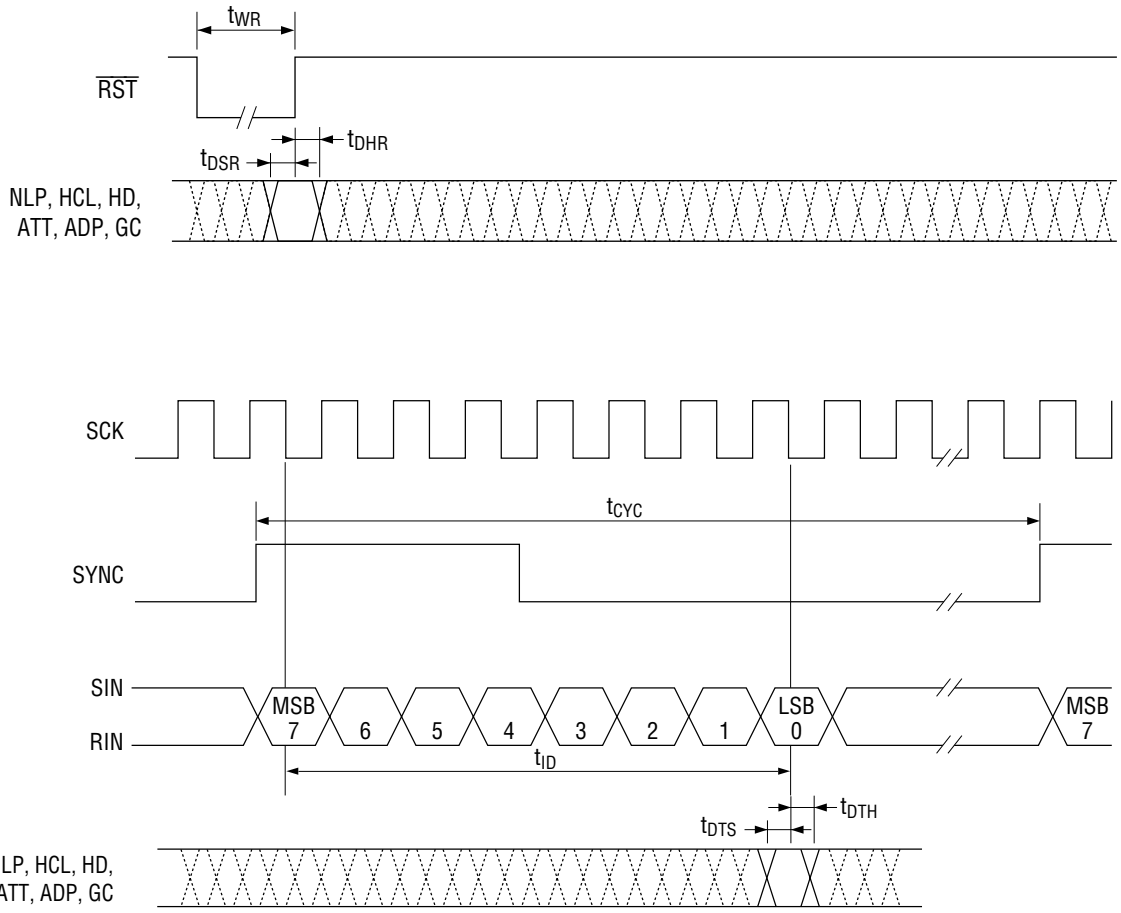


* $\overline{INT}$ is invalid during the shaded interval.

Power Down Timing



Control Pin Load-in Timing

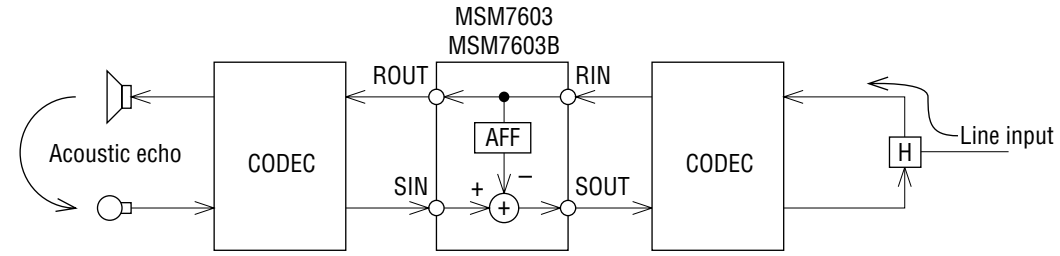


HOW TO USE THE MSM7603/7603B

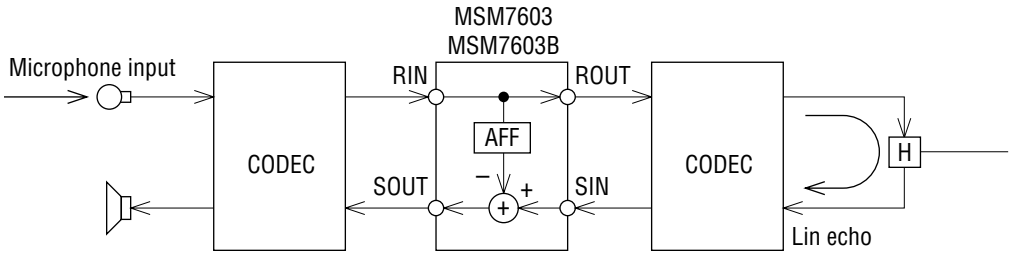
The MSM7603/7603B cancels, based on the RIN signal, the echo which returns to SIN. Connect the base signal to the R side and the echo-generated signal to the S side.

Connection Methods According to Echoes

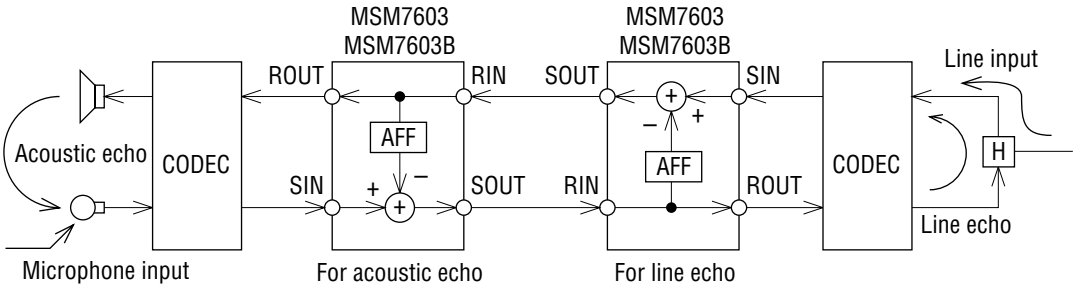
Example 1: Canceling acoustic echo (to handle acoustic echo from line input)



Example 2: Canceling line echo (to handle line echo from microphone input)

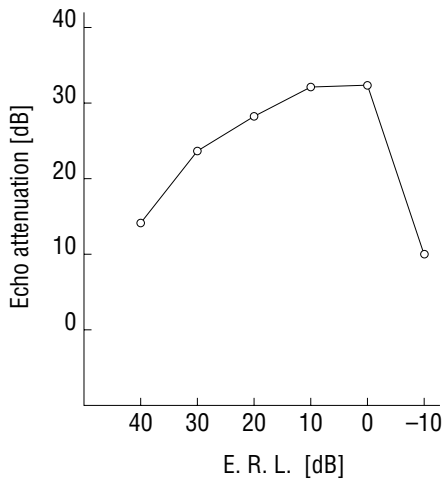


Example 3: Canceling of both acoustic and line echo
(to handle both acoustic echo from line input and line echo from microphone input)



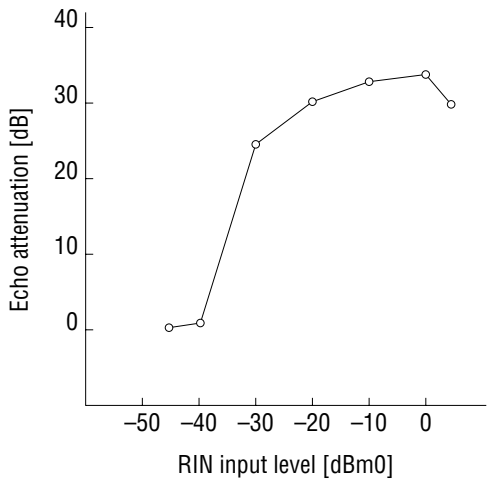
ECHO CANCELER CHARACTERISTICS DIAGRAM
(for μ-law and A-law, and for reference only)

E. R. L. vs. echo attenuation



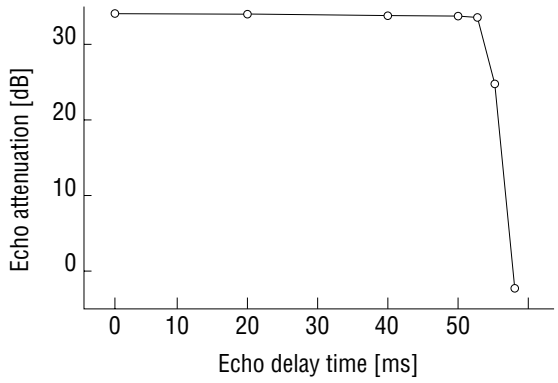
Measurement Conditions :
RIN input = –10 dBm0 5 kHz band white noise
Echo delay time T_D = 50 ms
ATT, GC, NLP = OFF
Power supply voltage 5 V

RIN input level vs. echo attenuation



Measurement Conditions :
RIN input: 5 kHz band white noise
Echo delay time T_D = 50 ms
E.R.L. = 6 dB
ATT, GC, NLP = OFF
Power supply voltage 5 V

Echo delay time vs. echo attenuation



Measurement Conditions :
RIN input = –10 dBm
5 kHz band white noise

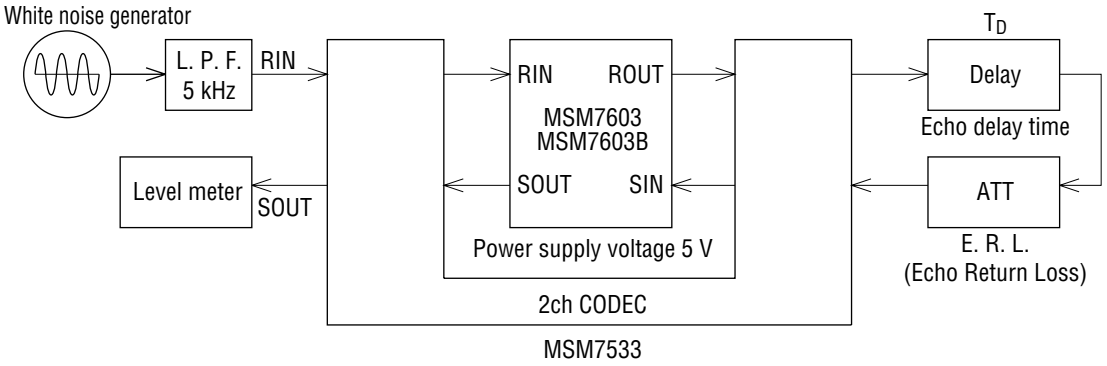
E.R.L. = 6 dB
ATT, GC, NLP = OFF
Power supply voltage 5 V

Note: Above characteristics are for the MSM7533 (V_{DD} 5 V, μ-law CODEC interface). For the MSM7704 (V_{DD} 3 V, μ-law interface) the characteristics are basically the same except for input and output levels. Refer to the PCM CODEC data sheet.

MSM7533 (for both transmit and receive)
0 dBm0 = 0.85 Vrms = 0.8 dBm (600 Ω)

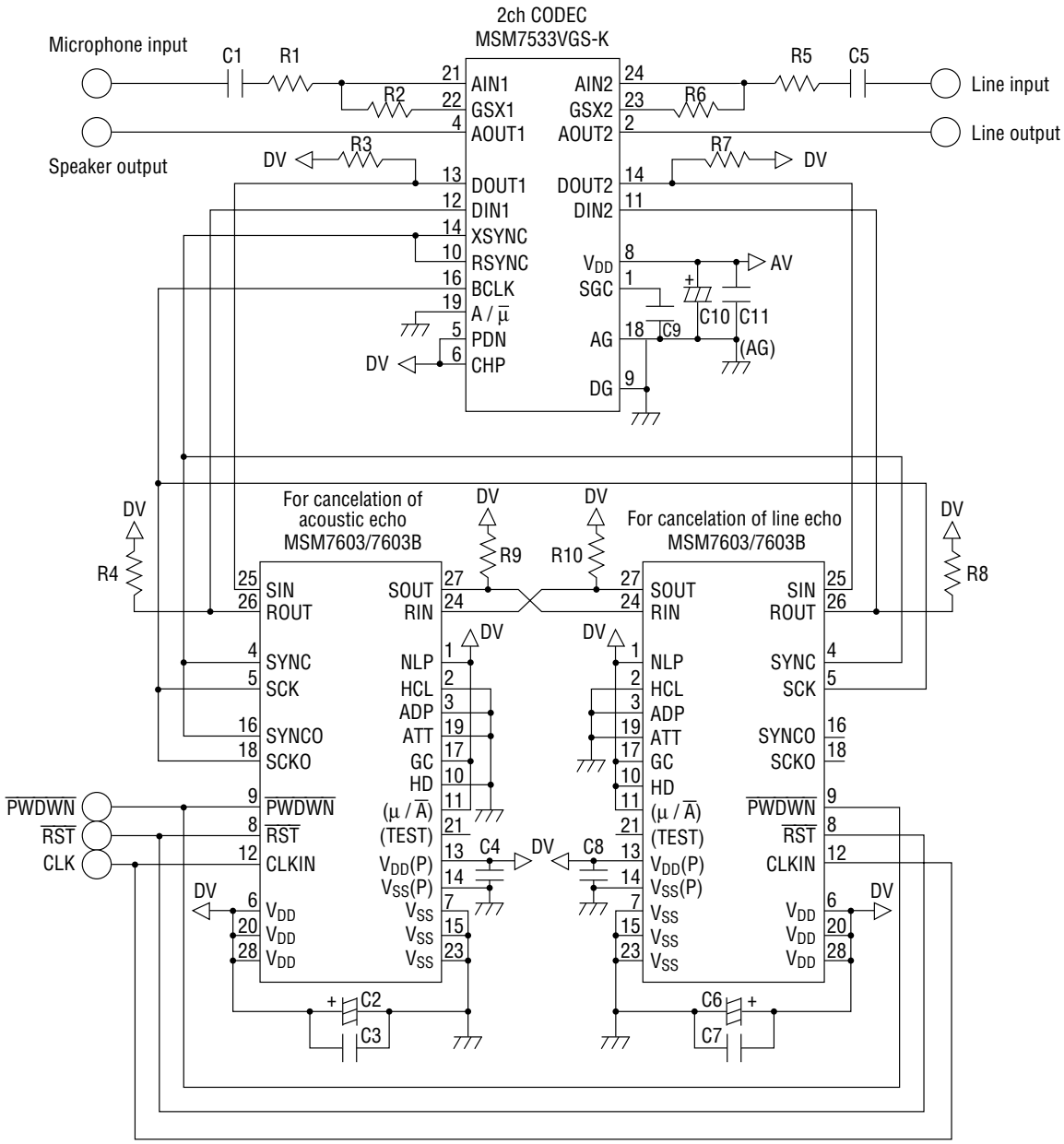
MSM7704 (for transmit side)
0 dBm0 = 0.35 Vrms = –6.9 dBm (600 Ω)
(for receive side)
0 dBm0 = 0.5 Vrms = –3.8 dBm (600 Ω)

Measurement System Block Diagram



APPLICATION CIRCUIT

Bidirectional Connection Example



R1=20 kΩ
R2=20 kΩ
R3=2.2 kΩ
R4=10 kΩ
R9=10 kΩ

C1=1 μF
C2=10 μF
C3=0.1 μF
C4=0.1 μF

R5=20 kΩ
R6=20 kΩ
R7=2.2 kΩ
R8=10 kΩ
R10=10 kΩ

C5=1 μF
C6=10 μF
C7=0.1 μF
C8=0.1 μF
C9=0.1 μF
C10=10 μF
C11=0.1 μF

Use the MSM7704-01GS-VK as a PCM CODEC when V_{DD} 3 V is used.
The MSM7533 is pin compatible with the MSM7704.

NOTES ON USE

1. Set echo return loss (ERL) to be attenuated. If the echo return loss is set to be amplified, the echo cannot be eliminated.
   Refer to the characteristics diagram for E. R. L. vs. echo attenuation quantity.

2. Set the level of the analog input so that the PCM codec does not overflow.

3. The recommended input level is –10 to –20 dBm0. Refer to the characteristics diagram for the RIN input level vs. echo attenuation quantity.

4. Applying the tone signal to this echo canceler for long duration may decrease echo attenuation.
   When used with the HD pin "L" (howling detector ON), this echo canceler may operate faultily if, while a signal is input to the RIN pin, a tone signal with a higher level than the signal being input to RIN is input to the SIN pin.
   A signal should therefore be input either to the RIN pin or to the SIN pin. If, however, the tone signal is input to the SIN pin while a signal is input to the RIN pin, the ADP, HD, or HCL pin must be set to "H".

5. For changes in the echo path (retransmit, circuit switching during transmission, and so on), convergence may be difficult.
   Perform a reset to make it converge.
   If the state of the echo path changes after a reset, convergence may again be difficult. In cases such as a change in the echo path, perform a reset each time.

6. When turning the power ON, set the $\overline{\text{PWDWN}}$ pin to "1" and input the basic clock simultaneously with power ON.
   If the device is put into power down mode immediately after power ON, be sure to input 10 or more clocks of the basic clock before setting to the power down mode.

7. After power ON, be sure to reset the device.

8. After the power down mode is released (when $\overline{\text{PWDWN}}$ pin is changed to a "1" from a "0"), be sure to reset the device.

9. If this canceler is used to cancel acoustic echoes, an echo attenuation may be less than 30 dB.

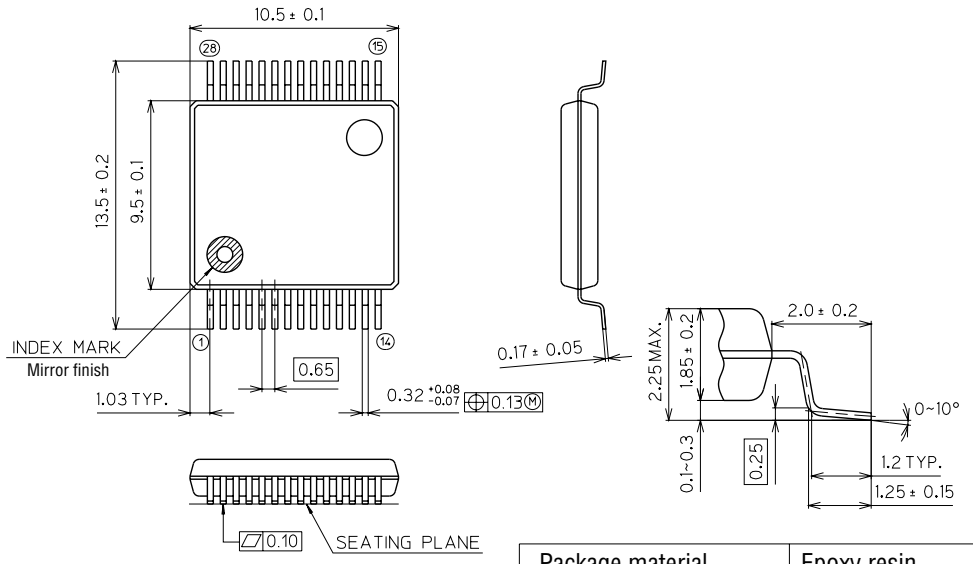
EXPLANATION OF TERMS

Attenuating Function :	This function prevents howling and controls the noise level with the attenuator for the RIN input and SOUT output. Refer to the explanation of pins (ATT pin).
Echo Attenuation :	If there is talking (input only to RIN) in the path of a rising echo arises, the echo attenuation refers to the difference in the echo return loss (canceled amount) when the echo canceler is not used and when it is used. Echo attenuation = (SOUT level during through mode operation) – (SOUT level during echo canceler operation) [dB]
Echo Delay Time :	This is the time from when the signal is output from ROUT until it returns to SIN as an echo.
Acoustic Echo :	When using a hands-free phone, for example, the signal output from the speaker echoes and is input again to the microphone. The return signal is referred to as acoustic echo.
Telephone Line Echo :	This is a signal which is delayed midway in a telephone line and returns as an echo, due to reasons such as a hybrid impedance mismatch.
Gain Control Function :	This function prevents howling and controls the sound level by with a gain controller for the RIN input. Refer to the explanation of pins (GC pin).
Center Clipping Function :	This function forces the SOUT output to a minimum value when the signal is below –54 dBm0. Refer to the explanation of pins (NLP pin).
Double Talk Detection :	Double talk refers to a state in which the SIN and RIN signals are input simultaneously. In a double talk state, a signal other than the echo signal which is to be canceled can be input to the SIN input, resulting in malfunction. The double talk detector prevents such malfunction of the canceler.
Howling Detection :	This is the oscillating state caused by the acoustic coupling between the loud speaker and the microphone during hands-free talking. Howling not only interferes with talking, but can also cause malfunction of the echo canceler. The howling detector prevents such malfunction and howling.
Echo Return Loss (ERL) :	When the signal output from ROUT returns to SIN as an echo, ERL refers to how much loss there is in the signal level during ROUT. ERL = (ROUT level) – (SIN level of the ROUT signal which returns as an echo) [dB] If ERL is positive (ROUT > SIN), acts as an attenuator. If ERL is negative (ROUT < SIN), acts as an amplifier.
PHS :	Personal Handyphone System

PACKAGE DIMENSIONS

(Unit : mm)

SSOP28-P-485-0.65-K



Oki Electric Industry Co., Ltd.

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5 μm)
Package weight (g)	0.39 TYP.
Rev. No./Last Revised	3/Dec. 5, 1996

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL7603_7603B-02	Nov. 2001	–	–	Final edition 2
FEDL7603_7603B-03	Jun. 1, 2005	10	10	Revised Max. values of “Sync Timing” and “Sync Signal Width” in the Table in the “AC Characteristics” Section.

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1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

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