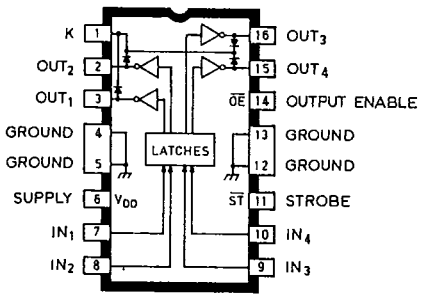
5831

T-52-13-25

BiMOS II 4-BIT LATCHED DRIVER



Dwg. PP-025

ABSOLUTE MAXIMUM RATINGS at $T_J \le +150°C$

Output Voltage, V_{CE} . . . . . **50 V**
Output Voltage, $V_{CE(sus)}$ . . . . . **45 V***
Output Current, I_{OUT} (peak) . . . . . **1.2 A**
(continuous) . . . . . **1.0 A**
Logic Supply Voltage, V_{DD} . . . . . **7.0 V**
CMOS Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

*For inductive load applications: The sum of the load supply voltage and the clamping voltage.

Output current may be limited by duty cycle, number of drivers operating, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified maximum current rating or a junction temperature of 150°C.

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Combining CMOS logic circuitry and bipolar power drivers, the UCN5831B is a 4-bit latched driver capable of providing an interface capability beyond the reach of standard logic buffers and power driver arrays. Although primarily designed for use with 2-phase unipolar stepper motors, this device can also be used to drive relays, low-voltage multiplexed LED displays, or incandescent lamps within its peak output current rating.

The CMOS inputs cause minimum loading and are compatible with most microprocessor/LSI-based systems. An active-low OUTPUT ENABLE can be used to disable all outputs without affecting the logic inputs or the state of the latches. Use with TTL may require input pull-up resistors to ensure an input logic high. BiMOS latches will typically operate at better than a 4.4 MHz rate.

The bipolar power outputs are open-collector 50 V saturated (non-Darlington) drivers. A sustaining voltage rating of 45 V, and internal clamp diodes, are provided for use with inductive loads. The four outputs can simultaneously sink load currents of almost 800 mA, continuously and without additional heat sinking, over the full operating temperature range. The outputs may be paralleled for increased load current capability. A similar device, featuring Darlington power driver outputs, is the UCN5830B.

The UCN5831B is supplied in a 16-pin plastic dual in-line batwing package with a copper lead frame that maximizes the device's power-handling capabilities.

FEATURES

- Low Output Saturation Voltage
- 50 V Minimum Output Breakdown
- 45 V Minimum Sustaining Voltage
- 1.2 A Peak Output Current
- Internal High-Current Clamp Diodes
- Low-Power CMOS Latches
- Output Enable and Strobe Functions

Always order by complete part number: **UCN5831B** .

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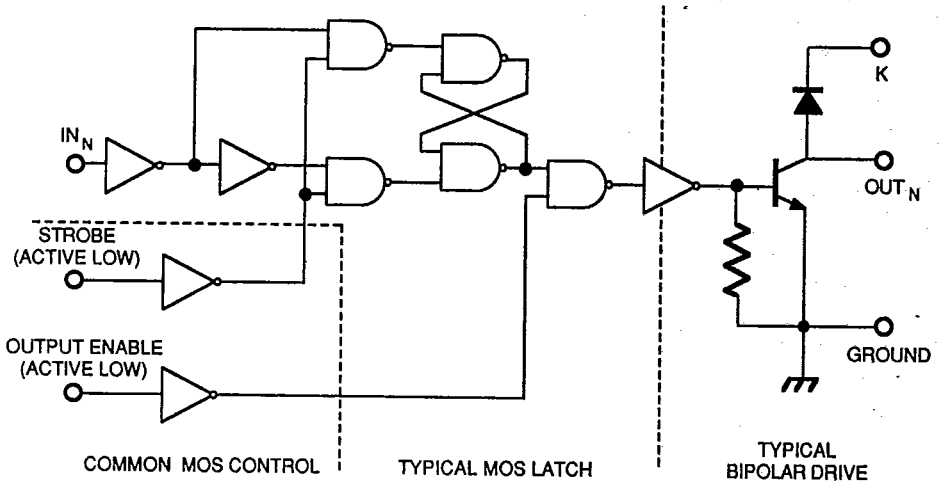
FUNCTIONAL BLOCK DIAGRAM

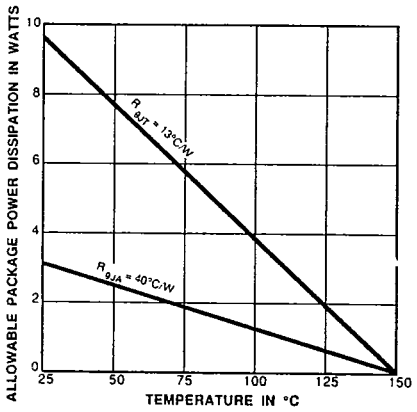


Dwg. FP-012

TRUTH TABLE

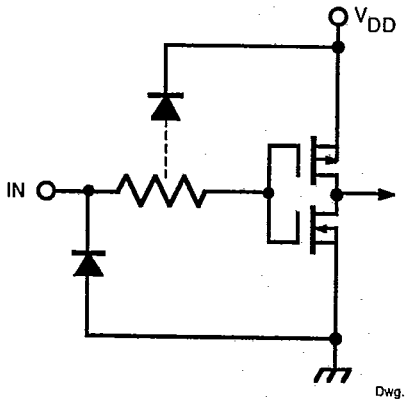
IN_N	STROBE	OUTPUT ENABLE	OUT_N
X	1	0	Prior State
0	0	0	Off
1	0	0	On
X	X	1	Off

X = irrelevant



Dwg. GP-004-1

TYPICAL INPUT CIRCUIT



Dwg. EP-010-1

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T-52-13-25

ELECTRICAL CHARACTERISTICS at T_A = +25°C, $T_J \leq$ +150°C, V_{DD} = 5 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_C = 50 V	–	1.0	100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	I_C = 300 mA	–	0.25	0.4	V
		I_C = 625 mA	–	0.35	0.5	V
		I_C = 800 mA	–	0.45	0.6	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_C = 625 mA, L = 400 mH	45	–	–	V
Clamp Diode Leakage Current	I_R	V_R = 50 V	–	1.0	100	µA
Clamp Diode Forward Voltage	V_F	I_F = 625 mA	–	1.0	1.2	V
		I_F = 800 mA	–	1.1	1.3	V
Logic Input Voltage	$V_{IN(1)}$		3.5	–	5.3	V
	$V_{IN(0)}$		-0.3	–	0.8	V
Logic Input Current	$I_{IN(1)}$	$V_{IN} = V_{DD}$	–	50	500	nA
	$I_{IN(0)}$	V_{IN} = 0.8 V	–	-50	-500	nA
Logic Supply Current	I_{DD}	All Outputs OFF	–	–	100	µA
		One Output ON	–	24	30	mA

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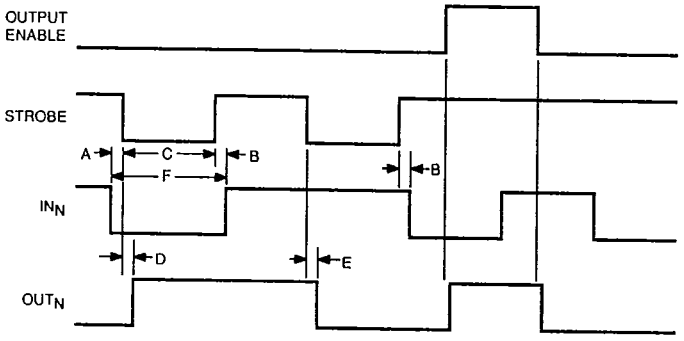


Dwg. WP-009

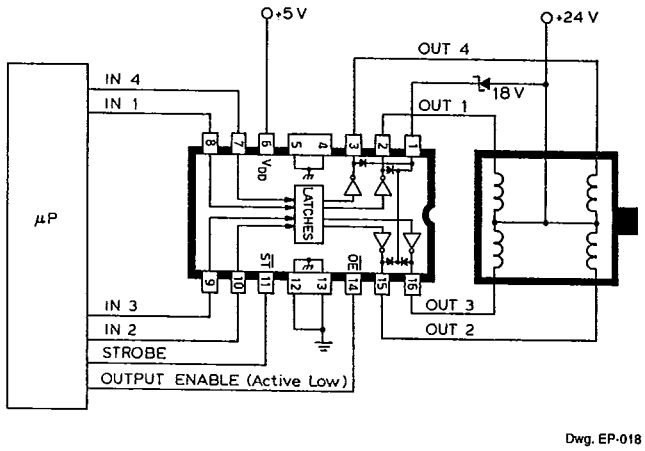
Data present at an input is transferred to its respective latch when STROBE is low. The latches will continue to accept new data as long as STROBE is held low. In applications where the latches are bypassed (STROBE tied low), the outputs will follow the data unless the OUTPUT ENABLE is high during data entry.

When OUTPUT ENABLE is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches. With OUTPUT ENABLE low, the outputs are controlled by the state of the latches.

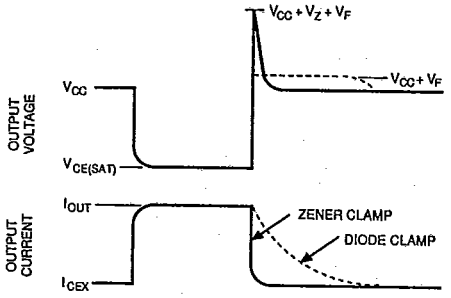
TIMING CONDITIONS
Logic Levels are V_{DD} and Ground

A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time) . . . . . **50 ns**
B. Minimum Data Active Time After Strobe Enabled (Data Hold Time) . . . . . **50 ns**
C. Minimum Strobe Pulse Width . . . . . **125 ns**
D. Typical Time Between Strobe Activation and Output Turn-OFF Transition (Resistive Load) . . . . . **500 ns**
E. Typical Time Between Strobe Activation and Output Turn-ON Transition (Resistive Load) . . . . . **100 ns**
F. Minimum Data Pulse Width . . . . . **225 ns**

TYPICAL APPLICATION
UNIPOLAR STEPPER-MOTOR DRIVE



Dwg. EP-018



Dwg. WP-001

A typical application is shown driving a unipolar stepper-motor. A Zener diode is used to increase the flyback voltage. This gives a much faster inductive load turn-OFF current decay. The maximum Zener voltage plus the load supply voltage plus the internal diode forward voltage must not exceed the device's rated sustaining voltage.