

CFI2370A DMA Controller

DESCRIPTION: CFI2370A is compatible in functionality with the Intel 8237A 4-channel programmable DMA controller. Performance is improved much over that of the standard part. I/Os can be made compatible to the standard part, as shown in the diagram on page 5 of 6. Note that the DB70_CN output is used to gate the output of the data lines. All other signals are compatible to the standard part. For functional information, see the Intel data sheet.

INPUTS (LOADING IN TRANSISTOR PAIRS):

RESET(1.5), CSN(2), READY(5), CLOCK(9.5),
 DREQ0(1), DREQ1(1), DREQ2(1), DREQ3(1),
 HLDA(10), DB7I(4), DB6I(4), DB5I(4),
 DB4I(4), DB3I(4), DB2I(4), DB1I(4),
 DB0I(4), IORN_I(1), IOWN_I(1), EOPN_I(1),
 A3I(3), A2I(3), A1I(3), A0I(1.5)

OUTPUTS (DRIVE IN (#P, #N)):

AEN(4,2), ADSTB(2,2), MEMRN(2,2), MEMWN(2,2),
 IORN_O(2,2), IOWN_O(2,2), EOPN_O(2,1), DACK0(2,2),
 DACK1(2,2), DACK2(2,2), DACK3(2,2), HRQ(2,2), A7(4,2),
 A6(4,2), A5(4,2), A4(4,2), A3O(4,2), A2O(4,2),
 A1O(4,2), A0O(4,2), DB7O_CN(2,2), DB7O(2,2),
 DB6O(2,2), DB5O(2,2), DB4O(2,2), DB3O(2,2),
 DB2O(2,2), DB1O(2,2), DB0O(2,2)

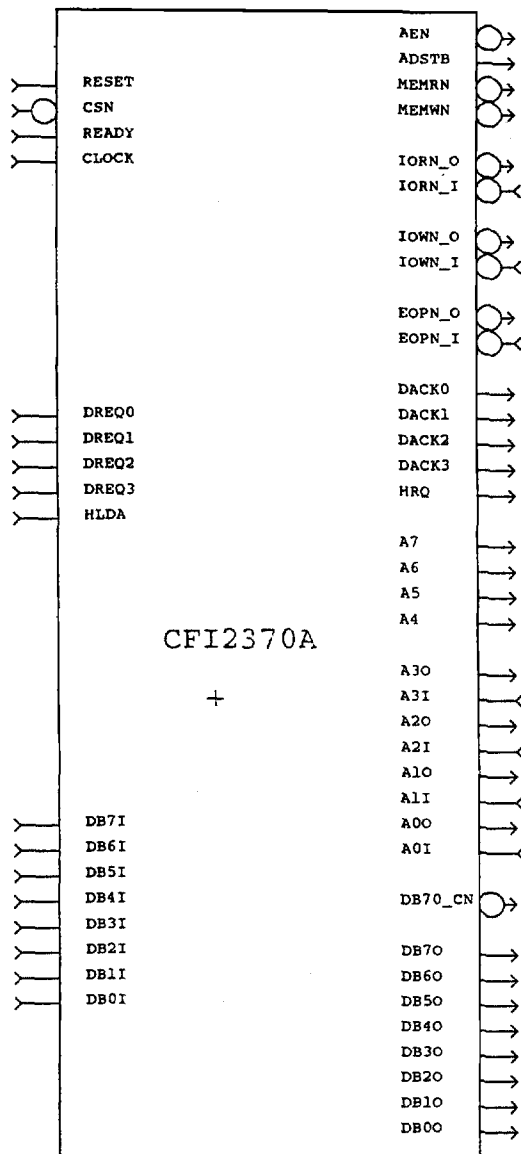
Z(AEN, ADSTB, MEMRN, MEMWN, IORN_O, IOWN_O, EOPN_O,
 DACK0, DACK1, DACK2, DACK3, HRQ, A7, A6, A5, A4, A3O,
 A2O, A1O, A0O, DB7O_CN, DB7O, DB6O, DB5O, DB4O, DB3O,
 DB2O, DB1O, DB0O)

=CFI2370A (RESET, CSN, READY, CLOCK, DREQ0, DREQ1,
 DREQ2, DREQ3, HLDA, DB7I, DB6I, DB5I, DB4I, DB3I, DB2I,
 DB1I, DB0I, IORN_I, IOWN_I, EOPN_I, A3I, A2I, A1I, A0I)\$

GATE COUNT:

ARRAY GATE USAGE = 3605
 ARRAY AREA USAGE = 3620

LOGIC SYMBOL:



CFI2370A

AC CHARACTERISTICS

DMA(MASTER) MODE

SYMBOL	PARAMETER	CFI2370A	
		MIN.	MAX.
TAEL	AEN HIGH FROM CLK LOW(S1) DELAY TIME		35
TAET	AEN LOW FROM CLK HIGH(S1) DELAY TIME		35
TAHR	ADR FROM READN HIGH HOLD TIME	TCY	
TAHW	ADR FROM WRITEN HIGH HOLD TIME	TCY	
TAK	DACK VALID FROM CLK LOW DELAY TIME		35
	EOPN HIGH FROM CLK HIGH DELAY TIME		35
	EOPN LOW FROM CLK HIGH DELAY TIME		35
TASM	ADR STABLE FROM CLK HIGH		35
TASS	DB TO ADSTB LOW SETUP TIME	TCY	
TCH	CLOCK HIGH TIME(TRANSITIONS<10 NS)	35	
TCL	CLOCK LOW TIME(TRANSITION<10 NS)	35	
TCY	CLK CYCLE TIME	70	
TDCL	CLK HIGH TO READN OR WRITEN LOW DELAY		35
TDCTR	READN HIGH FROM CLK HIGH(S4) DELAY TIME		35
TDCTW	WRITEN HIGH FROM CLK HIGH(S4) DELAY TIME		35
TDQ1 TDQ2	HRQ VALID FROM CLK HIGH DELAY TIME		35 35
TEPS	EOPN LOW FROM CLK LOW SETUP TIME	60	
TEPW	EOPN PULSE WIDTH	200	
TFAAB	ADR FLOAT TO ACTIVE DELAY FROM CLK HIGH		35
TFAC	READN OR WRITEN ACTIVE FROM CLK HIGH		35
TFADB	DB FLOAT TO ACTIVE DELAY FROM CLK HIGH		35
THS	HLDA VALID TO CLK HIGH SETUP TIME	20	
TIDH	INPUT DATA FROM MEMRN HIGH HOLD TIME	0	
TIDS	INPUT DATA TO MEMRN HIGH SETUP TIME	100	
TODH	OUTPUT DATA FROM MEMWN HIGH TIME	20	
TODV	OUTPUT DATA VALID TO MEMWN HIGH	TCY	
TQS	DREQ TO CLK LOW(S1, S4) SETUP TIME	0	
TRH	CLK TO READY LOW HOLD TIME	20	
TRS	READY TO CLK LOW SETUP TIME	.5TCY	
TSTL	ADSTB HIGH FROM CLK HIGH DELAY TIME		35
TSTT	ADSTB LOW FROM CLK HIGH DELAY TIME		35

*ALL UNITS ARE IN NS & APE TYPICAL(10K TECHNOLOGY)

CFI2370A

AC CHARACTERISTICS

PERIPHERAL(SLAVE) MODE

SYMBOL	PARAMETER	CFI2370A	
		MIN.	MAX.
TAR	ADR VALID OR CSN LOW TO READN LOW	20	
TAW	ADR VALID TO WRITEN HIGH SETUP TIME	35	
TCW	CS LOW TO WRITEN HIGH SETUP TIME	35	
TDW	DATA VALID TO WRITEN HIGH SETUP TIME	35	
TRA	ADR OR CS HOLD FROM READN HIGH	0	
TRDE	DATA ACCESS FROM READN LOW		70
TRDF	DB FLOAT DELAY FROM READN HIGH	10	70
TRSTD	POWER SUPPLY HIGH OR RESET LOW SETUP TIME	500	
TRSTS	RESET TO FIRST IOWRN	2TCY	
TRSTW	RESET PULSE WIDTH	300	
TRW	READN WIDTH	70	
TWA	ADR FROM WRITEN HIGH HOLD TIME	20	
TWC	CS HIGH FROM WRITEN HIGH HOLD TIME	20	
TWD	DATA FROM WRITEN HIGH HOLD TIME	30	
TWS	WRITE WIDTH	70	

*ALL UNITS ARE IN NS & ARE TYPICAL(10K TECHNOLOGY)

