SYNCHRONOUS SRAM MODULE

32K x 64 SRAM

256KB, 3.3V, FLOW-THROUGH SYNCHRONOUS BURST, SECONDARY CACHE MODULES

FEATURES

- 160-lead, dual-in-line memory module (DIMM)
- Fast access times: 9, 10, 11 and 12ns
- Fast $\overline{OE}$ access times: 5 and 6ns
- Single +3.3V ±5% power supply
- 5V-tolerant common data I/O
- Individual BYTE WRITE control
- Clock controlled and registered inputs
- Internally self-timed WRITE cycle
- Burst control options (interleaved T2 or linear burst T1)
- Low capacitive bus loading
- High 30pF output drive capability at rated access time

OPTIONS — MARKING

- Timing
  - 9ns access/15ns cycle — -9
  - 10ns access/15ns cycle — -10
  - 11ns access/15ns cycle — -11
  - 12ns access/20ns cycle — -12
- Burst sequence
  - Linear Burst — T1
  - 486/Pentium™ Burst — T2
- Packages
  - 160-lead DIMM (gold) — G
- Low power (optional) — P
- 2V data retention, low power (optional) — L

VALID PART NUMBERS

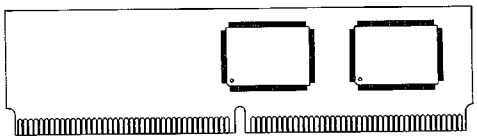
PART NUMBER	DESCRIPTION
MT2LSYT3264T1G-xx	32K x 64, Linear Burst
MT2LSYT3264T1G-xx P	32K x 64, Linear Burst, Low Power
MT2LSYT3264T1G-xx L	32K x 64, Linear Burst, 2V Data Retention, Low Power
MT2LSYT3264T2G-xx	32K x 64, Interleaved Burst
MT2LSYT3264T2G-xx P	32K x 64, Interleaved Burst, Low Power
MT2LSYT3264T2G-xx L	32K x 64, Interleaved Burst, 2V Data Retention, Low Power

GENERAL DESCRIPTION

The Micron SyncBurst™ SRAM module family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using an advanced CMOS process.

PIN ASSIGNMENT (Front View)

160-Lead DIMM
(SD-1)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	41	Vss	81	Vss	121	Vss
2	DQ62	42	DQ10	82	DQ63	122	DQ11
3	Vcc	43	Vcc	83	RSVD	123	RSVD
4	DQ60	44	DQ8	84	DQ61	124	DQ9
5	Vcc	45	NC	85	RSVD	125	NC
6	DQ58	46	Vcc	86	DQ59	126	RSVD
7	DQ56	47	DQ6	87	DQ57	127	DQ7
8	Vss	48	DQ4	88	Vss	128	DQ5
9	NC	49	DQ2	89	NC	129	DQ3
10	DQ54	50	DQ0	90	DQ55	130	DQ1
11	DQ52	51	Vss	91	DQ53	131	Vss
12	DQ50	52	A0A	92	DQ51	132	A0B
13	Vss	53	A1A	93	Vss	133	A1B
14	DQ48	54	A2A	94	DQ49	134	A2B
15	DQ46	55	A3A	95	DQ47	135	A3B
16	DQ44	56	A5	96	DQ45	136	A4
17	DQ42	57	Vss	97	DQ43	137	Vss
18	Vss	58	A7	98	Vss	138	A6
19	DQ40	59	A9	99	DQ41	139	A8
20	NC	60	A11	100	NC	140	A10
21	DQ38	61	A13	101	DQ39	141	A12
22	DQ36	62	NC	102	DQ37	142	A14
23	DQ34	63	Vss	103	DQ35	143	Vss
24	Vss	64	PD0	104	Vss	144	NC
25	DQ32	65	Vss	105	DQ33	145	Vss
26	DQ30	66	RSVD	106	DQ31	146	CLK
27	DQ28	67	RSVD	107	DQ29	147	RSVD
28	DQ26	68	Vss	108	DQ27	148	Vss
29	DQ24	69	$\overline{BW6}$	109	DQ25	149	$\overline{BW7}$
30	Vss	70	$\overline{BW4}$	110	Vss	150	$\overline{BW5}$
31	NC	71	$\overline{BW2}$	111	NC	151	$\overline{BW3}$
32	DQ22	72	$\overline{BW0}$	112	DQ23	152	$\overline{BW1}$
33	DQ20	73	Vss	113	DQ21	153	Vss
34	Vcc	74	$\overline{ADSC0}$	114	RSVD	154	$\overline{ADSC1}$
35	DQ18	75	$\overline{CE0}$	115	DQ19	155	$\overline{CE1}$
36	Vss	76	$\overline{ADV0}$	116	Vss	156	$\overline{ADV1}$
37	DQ16	77	$\overline{OE0}$	117	DQ17	157	$\overline{OE1}$
38	Vcc	78	Vcc	118	RSVD	158	RSVD
39	DQ14	79	$\overline{ADSP0}$	119	DQ15	159	$\overline{ADSP1}$
40	DQ12	80	Vss	120	DQ13	160	Vss

GENERAL DESCRIPTION (continued)

The MT2LSYT3264T1/T2 module integrates two 32K x 32 synchronous SRAMs. All synchronous inputs pass through registers controlled by positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, data inputs, active LOW chip enables ($\overline{CE0}$-1), burst control inputs ($\overline{ADSC0}$-1, $\overline{ADSP0}$-1, $\overline{ADV0}$-1) and byte write enables ($\overline{BW0}$-7).

Asynchronous inputs include the output enables ($\overline{OE0}$-1) and the clock (CLK). The data-out (Q), enabled by $\overline{OE}$, is also asynchronous. WRITE cycles can be from one to eight bytes wide as controlled by the byte write enables.

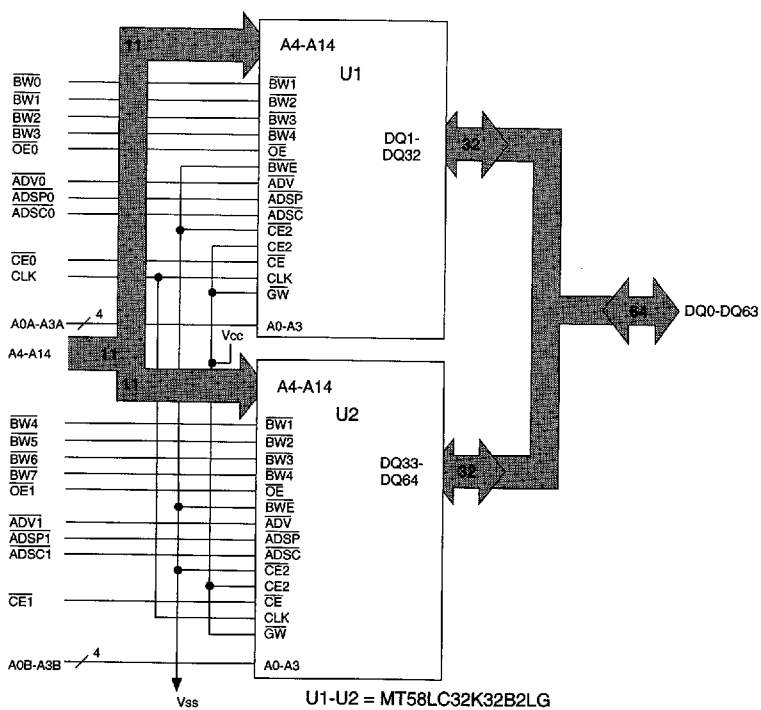
Burst operation can be initiated with either address status processor ($\overline{ADSP0}$-1) or address status controller ($\overline{ADSC0}$-1) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pins ($\overline{ADV0}$-1).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. $\overline{BW0}$ controls DQ0-DQ7, $\overline{BW1}$ controls DQ8-DQ15, $\overline{BW2}$ controls DQ16-DQ23, $\overline{BW3}$ controls DQ24-DQ31 and so forth.

The "L" version of this module has a data retention option which is useful for battery backup mode of operation. Although the part is not guaranteed to operate functionally below Vcc MIN (3.1V), it will retain data with a minimum of power dissipation.

The module operates from a +3.3V power supply and all inputs and outputs are TTL-compatible and 5V tolerant. This module is ideally suited to Pentium systems and those systems which benefit from a very wide data bus.

FUNCTIONAL BLOCK DIAGRAM
256KB
(32K x 64)



NOTE: 1. The Functional Block Diagram illustrates simplified module operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

PIN DESCRIPTIONS

MODULE PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
56, 58-61, 136, 138-142	A4-A14	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
69-72, 149-152	$\overline{BW0}$-7	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A BYTE WRITE enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW0}$ controls DQ0-DQ7. $\overline{BW1}$ controls DQ8-DQ15. $\overline{BW2}$ controls DQ16-DQ23. $\overline{BW3}$ controls DQ24-DQ31, and so forth. Data I/O are tristated if any of these eight inputs are LOW.
146	CLK	Input	Clock: This signal latches the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
75, 155	$\overline{CE0}$-$\overline{CE1}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
52-55, 132-135	A0A-A3A, A0B-A3B	Input	Synchronous Address Input: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. These lower order address signals are provided for the two data banks to simplify the interface to many cache controllers.
77, 157	$\overline{OE0}$-$\overline{OE1}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
76, 156	$\overline{ADV0}$-$\overline{ADV1}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
79, 159	$\overline{ADSP0}$-$\overline{ADSP1}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be latched. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$. $\overline{ADSP}$ is ignored if $\overline{CE}$ is HIGH.
74, 154	$\overline{ADSC0}$-$\overline{ADSC1}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst and causes a new external address to be latched. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive.
66, 83, 85, 114, 118, 123, 126, 147, 158	RSVD	-	No Connect: These pins are reserved.

PIN DESCRIPTIONS (continued)

MODULE PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
2, 4, 6-7, 10-12, 14, 16-17, 19, 21-23, 25-29, 32-33, 35, 37, 39-40, 42, 44, 47-50, 82, 84, 86-87, 90-92, 94-97, 99, 101-103, 105-109, 112-113, 115, 117, 119-120, 122, 124, 127-130	DQ0-DQ63	Input/ Output	SRAM Data I/O: Byte 1 is DQ0-DQ7; Byte 2 is DQ8-DQ15; Byte 3 is DQ16-DQ23; Byte 4 is DQ24-DQ31 and so forth. Input data must meet setup and hold times around the rising edge of CLK.
3, 5, 34, 38, 43, 46, 78	Vcc	Supply	Power Supply: +3.3V ±5%
1, 8, 13, 18, 24, 30, 36, 41, 51, 57, 63, 68, 73, 80, 81, 88, 93, 98, 104, 110, 116, 121, 131, 137, 143, 148, 153, 160	Vss	Supply	Ground: GND

INTERLEAVED BURST ADDRESS TABLE (MT2LSYT3264T2)

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

LINEAR BURST ADDRESS TABLE (MT2LSYT3264T1)

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

PRESENCE-DETECT TABLE

DENSITY	PD0 (PIN #64)
• 256KB	NC
512KB	Vss

TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{CE}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ0-63
Deselected Cycle, Power-down	None	H	X	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	H	H	L	X	L-H	D

NOTE:
1. X means "don't care." H means logic HIGH. L means logic LOW. $\overline{WRITE}$=L means any one or more byte write enable signals ($\overline{BW0}$, $\overline{BW1}$, $\overline{BW2}$, etc.) are LOW. $\overline{WRITE}$=H means all byte write enable signals are HIGH.
2. $\overline{BW0}$ enables writes to Byte 1 (DQ0-DQ7). $\overline{BW1}$ enables writes to Byte 2 (DQ8-DQ15). $\overline{BW2}$ enables writes to Byte 3 (DQ16-DQ23). $\overline{BW3}$ enables writes to Byte 4 (DQ24-DQ31) and so forth.
3. All inputs except $\overline{OE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to Vss ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6V
Storage Temperature (plastic) ..... -55°C to +125°C
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(V_{CC} = +3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage			V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage			V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	$\overline{BW0}$-7	I_{LI1}	-1	1	µA	
		A4-A15	I_{LI2}	-4	4	µA	
		All other inputs	I_{LI3}	-2	2	µA	
Output Leakage Current	Output(s) Disabled, 0V ≤ V_{OUT} ≤ V_{CC}		I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		V	1, 11, 16
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	V	1, 11
Supply Voltage			V_{CC}	3.135	3.465	V	1

DESCRIPTION	CONDITIONS	SYM	VER	TYP	MAX -9	MAX -10	MAX -11	MAX -12	UNITS	NOTES
Power Supply Current: Operating	Device selected; V_{CC} = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ ^tKC MIN; outputs open	I_{CC1}	ALL	360	540	540	540	450	mA	3, 12, 13
Power Supply Current: Idle	Device selected; V_{CC} = MAX; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≥ V_{IH}; all inputs ≤ Vss +0.2 or ≥ V_{CC} -0.2; cycle time ≥ ^tKC MIN	I_{CC2}	ALL	56	100	100	100	90	mA	12, 13
CMOS Standby	Device deselected; V_{CC} = MAX; all inputs ≤ Vss +0.2 or ≥ V_{CC} -0.2; all inputs static; CLK frequency = 0	I_{SB1}	STD	1.0	10	10	10	10	mA	12, 13
			P	0.4	4	4	4	4	mA	
TTL Standby	Device deselected; V_{CC} = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; CLK frequency = 0	I_{SB2}	STD	30	50	50	50	50	mA	12, 13
			P	16	36	36	36	36	mA	
Clock Running	Device deselected; V_{CC} = MAX; all inputs ≤ Vss +0.2 or ≥ V_{CC} -0.2; CLK cycle time ≥ ^tKC MIN	I_{SB3}	ALL	60	100	100	100	90	mA	12, 13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance: A4-A14, CLK	T_A = 25°C; f = 1 MHz	C_{I1}	8	9	pF	4
Input Capacitance: $\overline{ADSP0}$-1 or $\overline{ADV0}$-1, $\overline{ADSC0}$-1	Vcc = 3.3V	C_{I2}	4	5	pF	4
Input Capacitance: $\overline{BW0}$-7, $\overline{OE0}$-1, $\overline{CE0}$-1, A0A-A3A, A0B-A3B		C_{I3}	4	5	pF	4
Input/Output Capacitance: DQ0-63		C_O	8	10	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (Vcc = +3.3V ±5%)

DESCRIPTION	SYM	-9		-10		-11		-12		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock											
Clock cycle time	^tKC	15		15		15		20		ns	
Clock HIGH time	^tKH	4		5		5		6		ns	
Clock LOW time	^tKL	4		5		5		6		ns	
Output Times											
Clock to output valid	^tKQ		9		10		11		12	ns	
Clock to output invalid	^tKQX	3		3		3		3		ns	
Clock to output in Low-Z	^tKQLZ	4		4		4		5		ns	4, 6, 7
Clock to output in High-Z	^tKQHZ		5		5		5		6	ns	4, 6, 7
$\overline{OE}$ to output valid	^tOEQ		5		5		5		6	ns	9
$\overline{OE}$ to output in Low-Z	^tOELZ	0		0		0		0		ns	4, 6, 7
$\overline{OE}$ to output in High-Z	^tOEHZ		5		5		5		6	ns	4, 6, 7
Setup Times											
Address	^tAS	2.5		2.5		2.5		3		ns	8, 10
Address Status ($\overline{ADSC0}$-1, $\overline{ADSP0}$-1)	^tADSS	2.5		3		3		3		ns	8, 10
Address Advance ($\overline{ADV0}$-1)	^tAAS	2.5		3		3		3		ns	8, 10
Byte Write Enables ($\overline{BW0}$-7)	^tWS	2.5		3		3		3		ns	8, 10
Data-in	^tDS	2.5		3		3		3		ns	8, 10
Chip Enable ($\overline{CE0}$-1)	^tCES	2.5		3		3		3		ns	8, 10
Hold Times											
Address	^tAH	0.5		0.5		0.5		0.5		ns	8, 10
Address Status ($\overline{ADSC0}$-1, $\overline{ADSP0}$-1)	^tADSH	0.5		0.5		0.5		0.5		ns	8, 10
Address Advance ($\overline{ADV0}$-1)	^tAAH	0.5		0.5		0.5		0.5		ns	8, 10
Byte Write Enables ($\overline{BW0}$-7)	^tWH	0.5		0.5		0.5		0.5		ns	8, 10
Data-in	^tDH	0.5		0.5		0.5		0.5		ns	8, 10
Chip Enable ($\overline{CE0}$-1)	^tCEH	0.5		0.5		0.5		0.5		ns	8, 10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	2.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

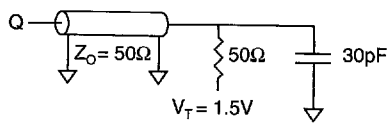


Fig. 1 OUTPUT LOAD EQUIVALENT

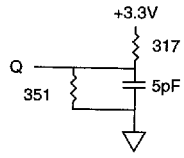


Fig. 2 OUTPUT LOAD EQUIVALENT

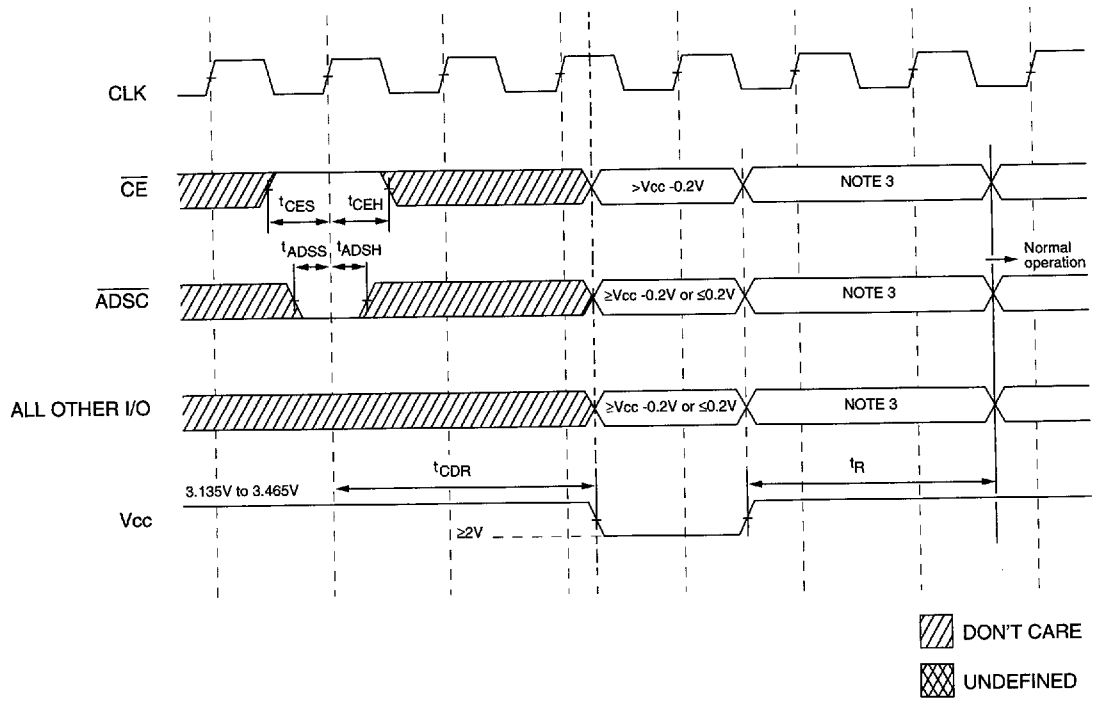
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$.
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tKC/2$.
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.135V$ for $t \leq 200ms$.
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$ and ${}^tOEHZ$ is less than ${}^tOELZ$.
8. A READ cycle is defined by byte write enables all HIGH or $\overline{ADSP}$ LOW for the required setup and hold times. A WRITE cycle is defined by at least one byte write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times.
9. $\overline{OE}$ is a "don't care" when a byte write enable is sampled LOW.
10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.
11. The load used for V_{OH}, V_{OL} testing is shown in Fig. 2. AC load current is higher than the shown DC values.
12. "Device deselected" means device is in POWER-DOWN mode as defined in the truth table. "Device selected" means device is active (not in POWER-DOWN mode).
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
14. Typical values are measured at 25°C.
15. The device must have a deselect cycle applied at least one clock cycle before data retention mode is entered.
16. DQs are guaranteed to meet V_{OH} MIN for up to 10ms after outputs become static.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

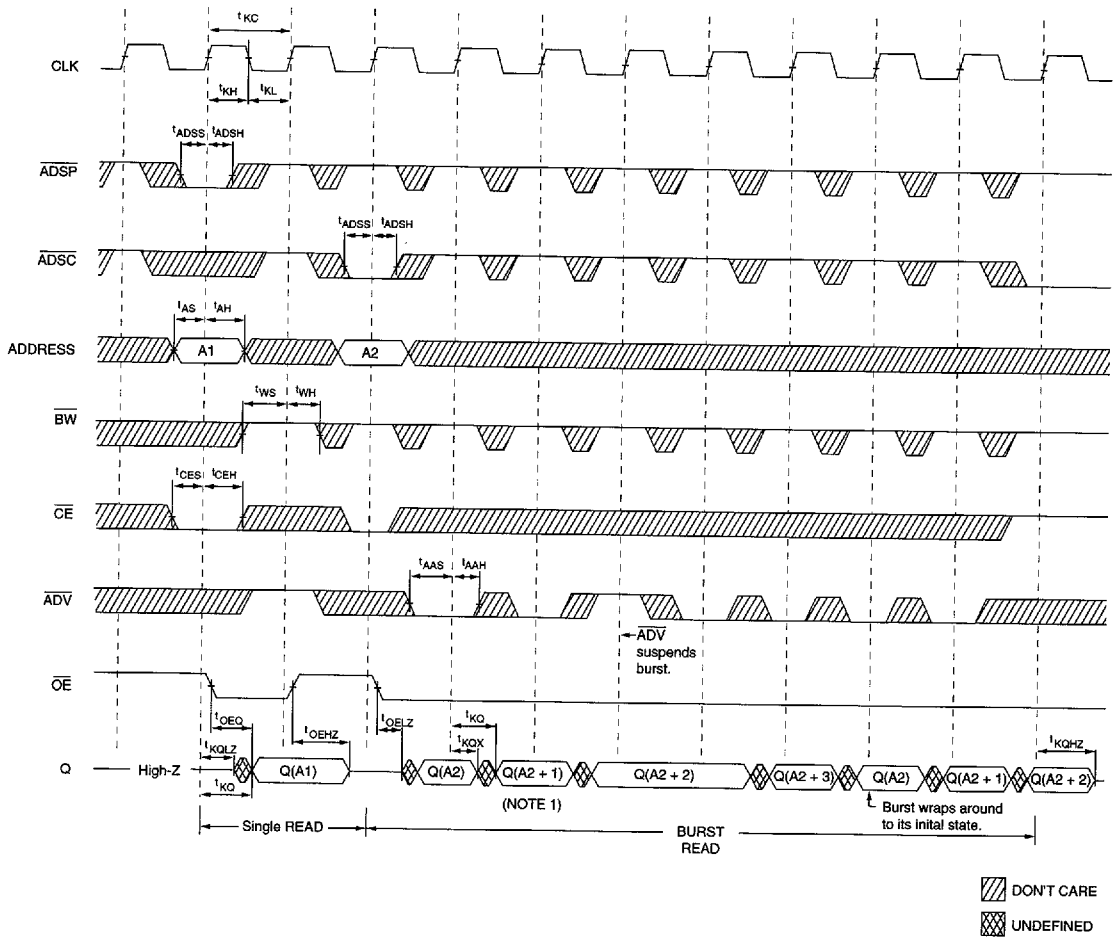
DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2		V	
Data Retention Current	$\overline{CE}$, $\overline{CE2}$ ≥ (Vcc -0.2V), CE2 ≤ 0.2V V_{IN} ≥ (Vcc -0.2V) or ≤ 0.2V Vcc = 2V	I_{CCDR}		TBD	µA	14
Chip Deselect to Data Retention Time		^tCDR	^tKC		ns	4, 15
Operation Recovery Time		^tR		^tKC	ns	4

LOW Vcc DATA RETENTION WAVEFORM



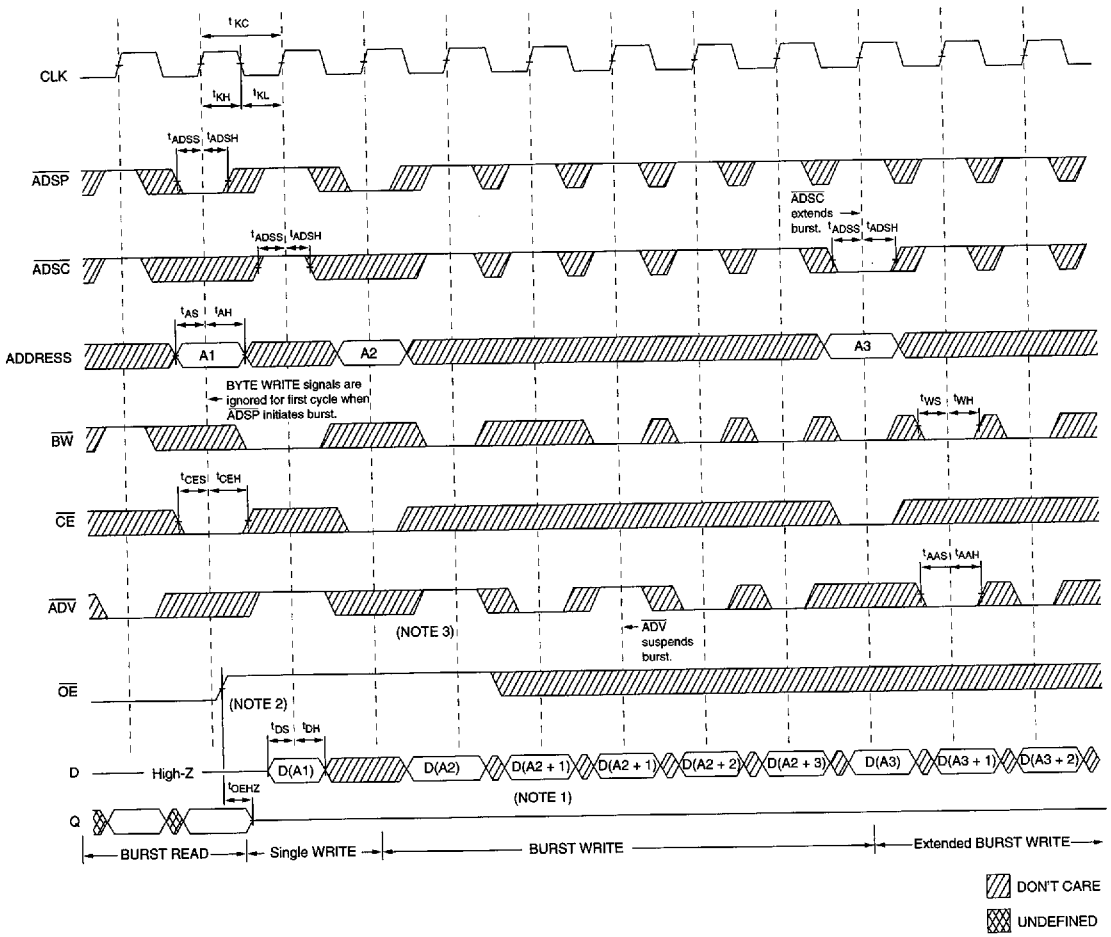
NOTE:
1. All inputs must be ≥ Vcc -0.2V or ≤ 0.2V to guarantee I_{CCDR} in data retention mode. If inputs are between these levels or left floating, I_{CCDR} may be exceeded.
2. Only one of the available deselect cycle sequences is shown above ($\overline{CE}$ = HIGH, $\overline{ADSC}$ = LOW). Any of the other deselect cycle sequences may also be used.
3. The device control signals should be in a deselect state between the rising edge of Vcc and until ^tR is met.
4. All inputs must be ≤ Vcc +2V while the device is in data retention mode.

READ TIMING



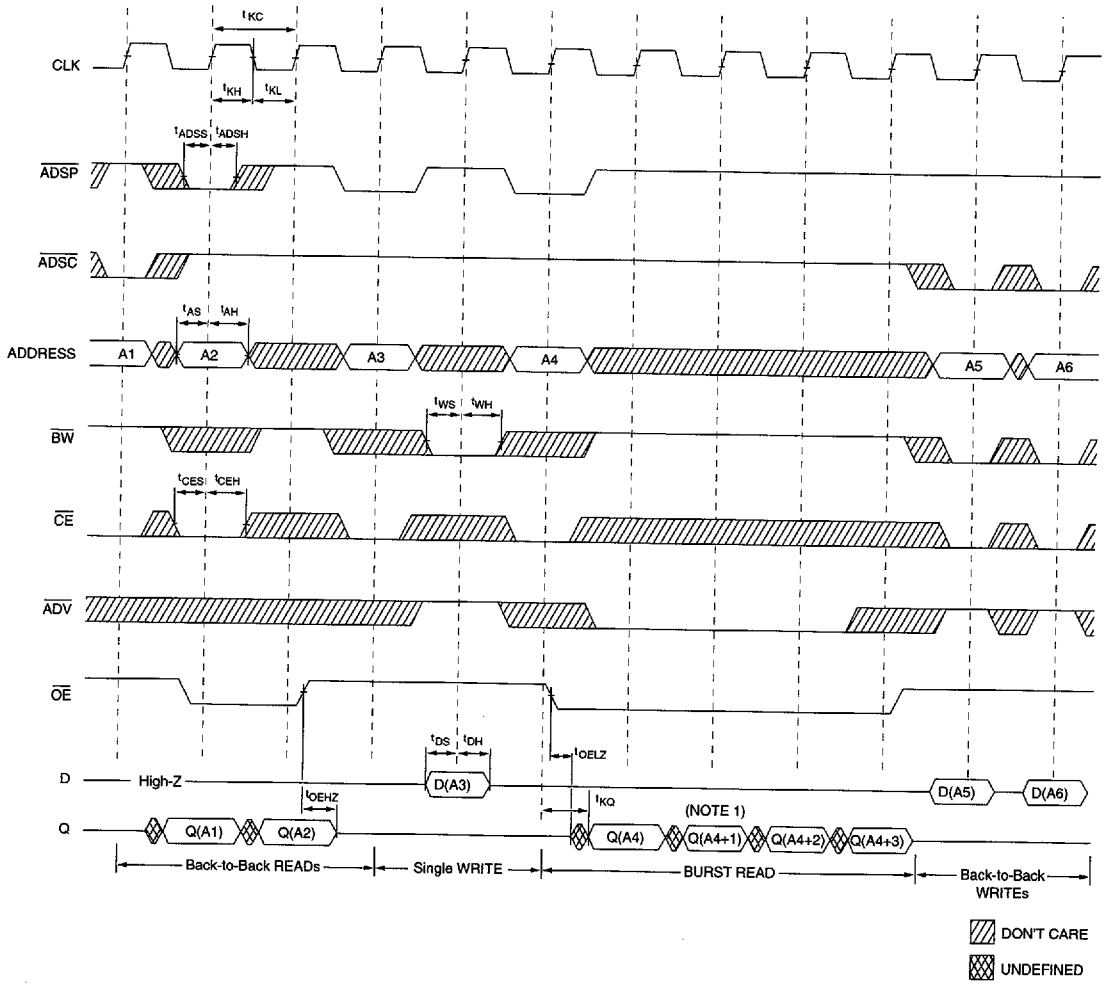
NOTE: 1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. Timing is shown assuming that the device was not enabled before entering into this sequence. $\overline{OE}$ does not cause Q to be driven until after the following clock rising edge.

WRITE TIMING



NOTE:
1. D(A2) refers to input for address A2. D(A2+1) refers to input for the next internal burst address following A2.
2. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
3. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.

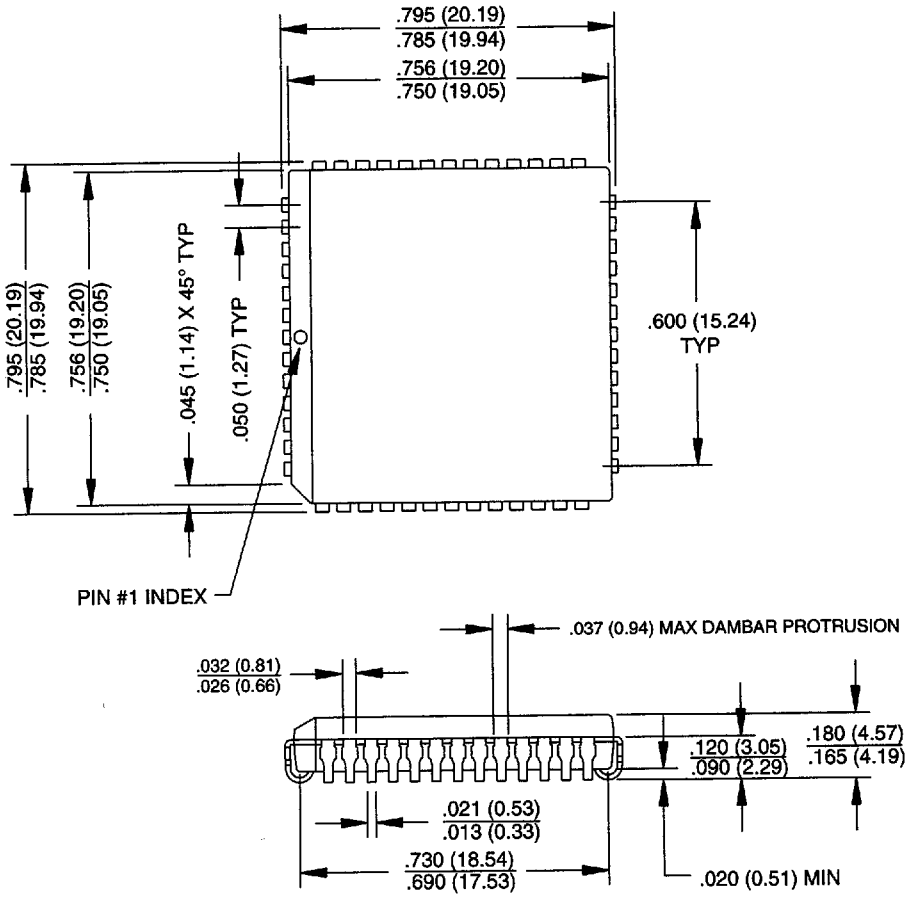
READ/WRITE TIMING



NOTE:
1. Q(A4) refers to output from address A4. Q(A4+1) refers to output from the next internal burst address following A4.
2. The data bus (Q) remains in High-Z following a WRITE cycle unless an $\overline{\text{ADSP}}$, $\overline{\text{ADSC}}$ or $\overline{\text{ADV}}$ cycle is performed.
3. Back-to-back READs may be controlled by either $\overline{\text{ADSC}}$ or $\overline{\text{ADSP}}$.

52-PIN PLCC

SA-1



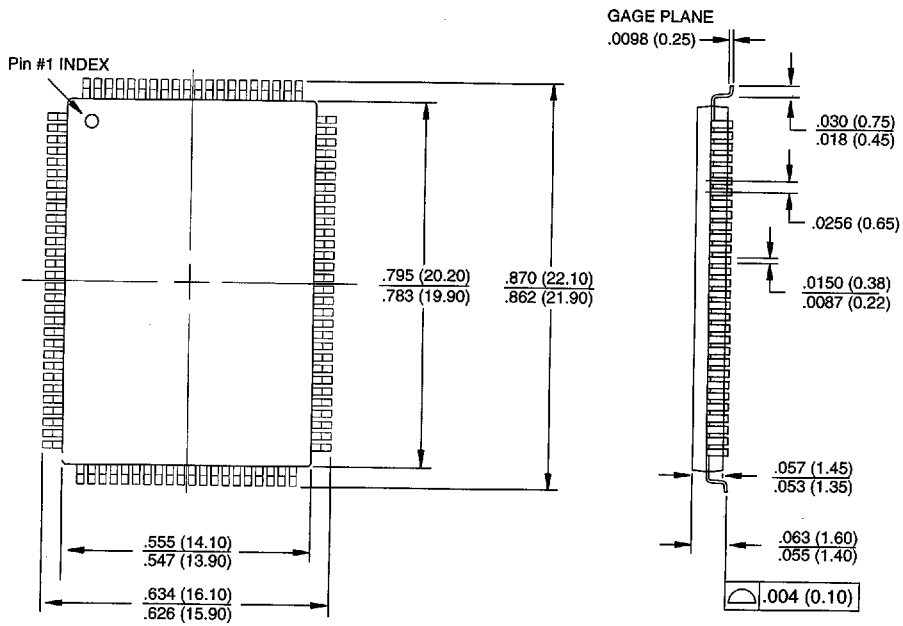
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

PACKAGE INFORMATION

100-PIN TQFP

SB-1



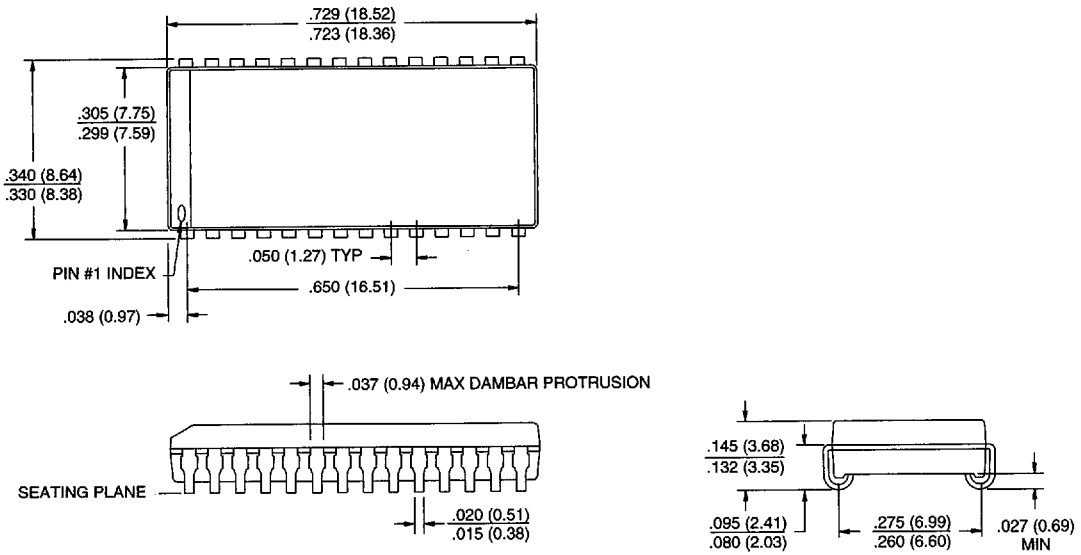
PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

28-PIN PLASTIC SOJ

SC-1

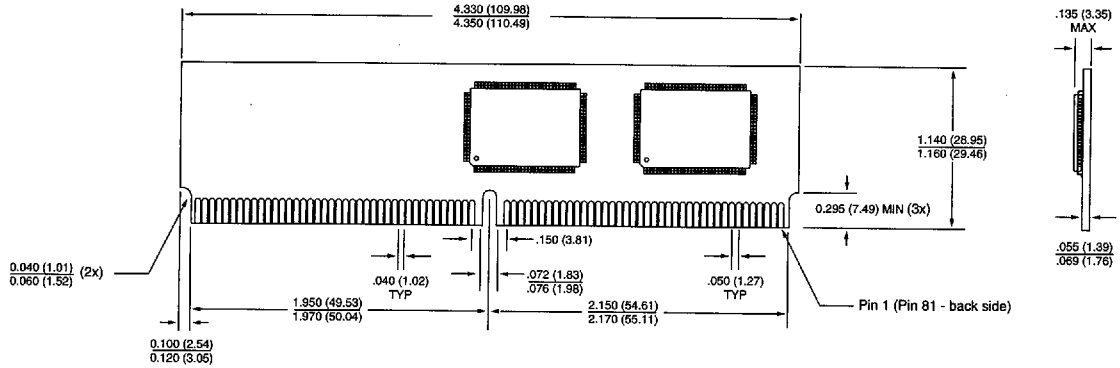


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

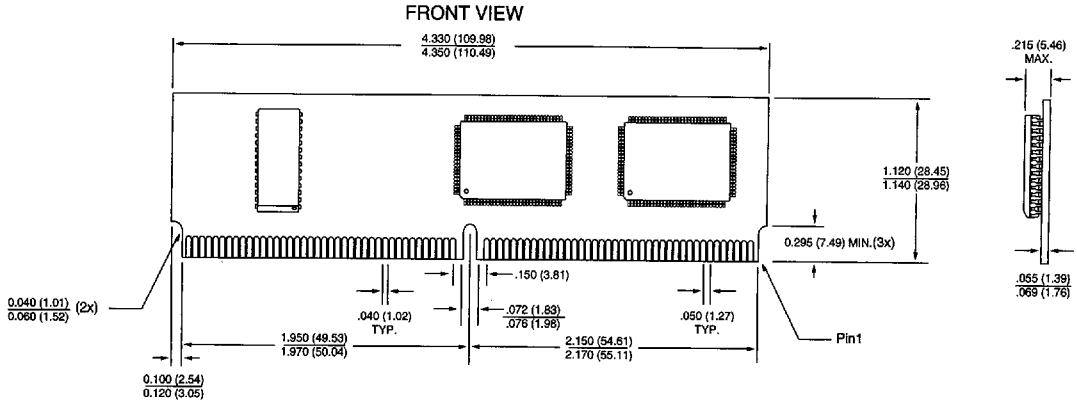
160-PIN MODULE DIMM

SD-1



160-PIN MODULE DIMM

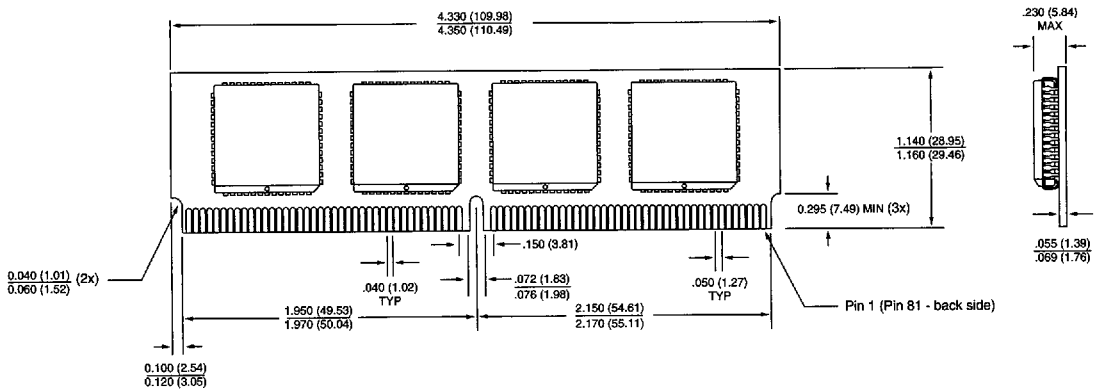
SD-2



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

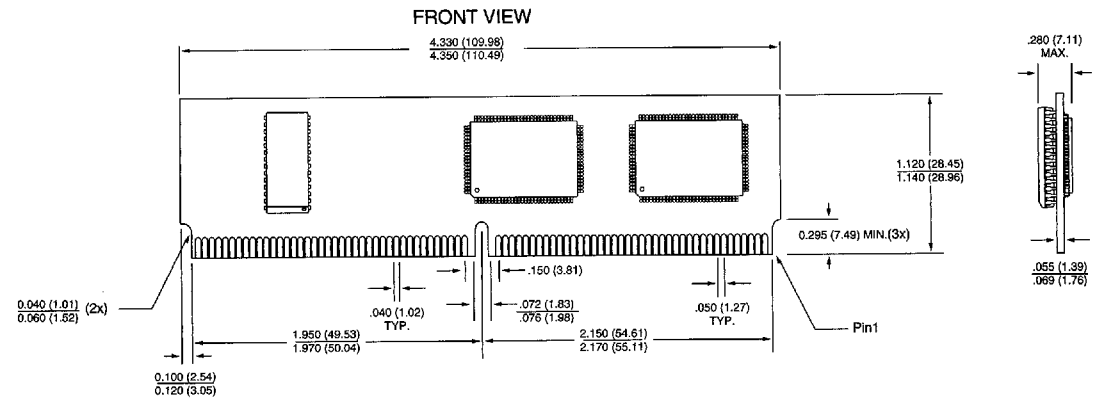
160-PIN MODULE DIMM

SD-3



160-PIN MODULE DIMM

SD-4



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

PACKAGE INFORMATION