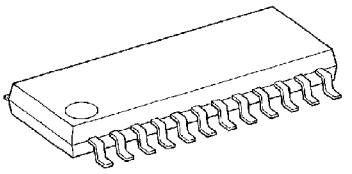
TOSHIBA INTELLIGENT POWER DEVICE SILICON MONOLITHIC BIPOLAR LINEAR INTEGRATED CIRCUIT

TPD7000F

4-CHANNEL LOW-SIDE POWER MOS FET DRIVER

TPD7000F is a power MOS FET driver for low-side switching. This 4-channel driver with a built-in circuit is used to monitor the voltage between the MOS FET drain and source for each channel and to output the state of the power MOS FET.



SSOP24-P-300-1.00B

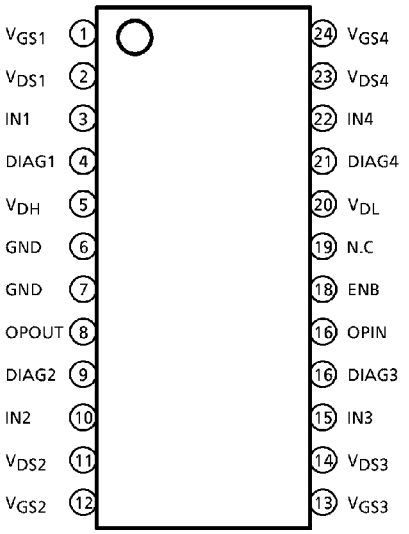
Weight : 0.29g (Typ.)

FEATURES

- Low-side N-channel power MOS FET driver (input capacitance: 15nF Max).
- Incorporates a power MOS FET overcurrent protection function.
- Incorporates induction load energy clamping function.
- INHIBIT option using enable input, open collector output.
- 24-pin SSOP

PIN ASSIGNMENT

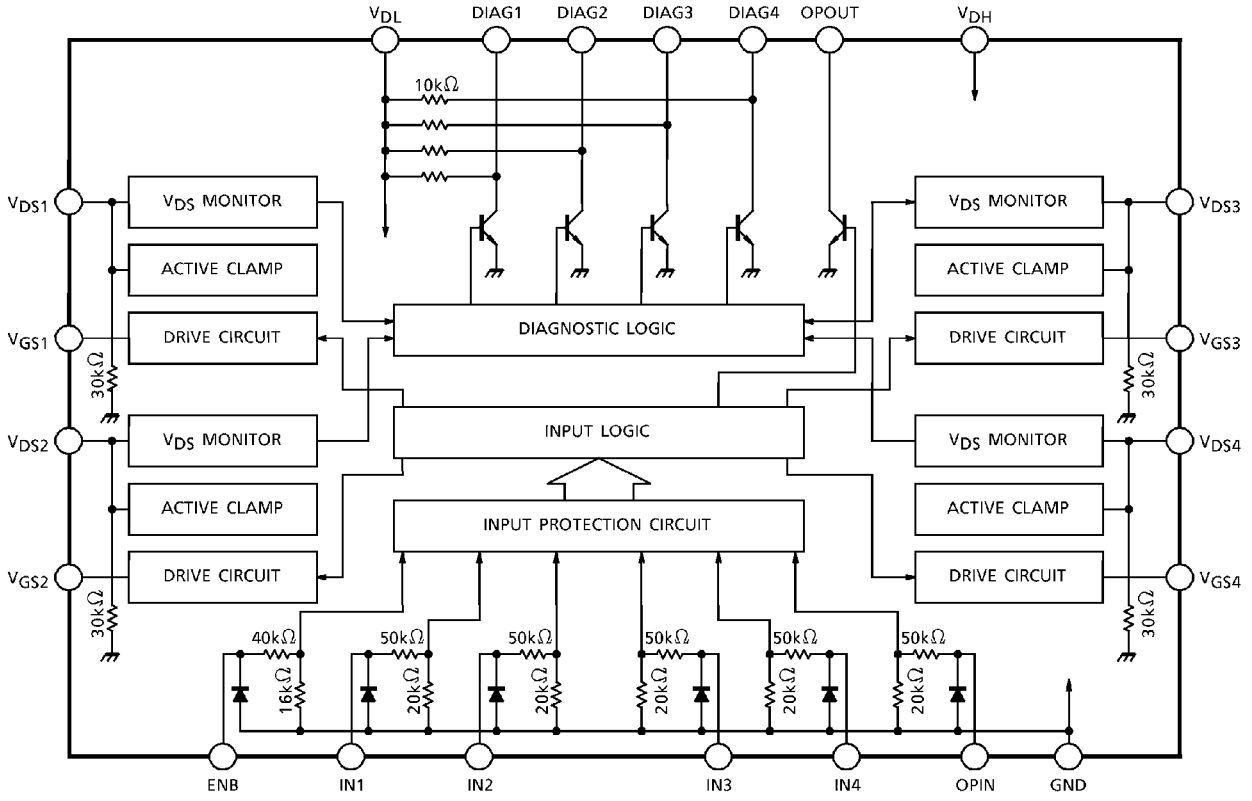
(TOP VIEW)



(Note) That this product is sensitive to static electricity.

961001EBA2

BLOCK DIAGRAM

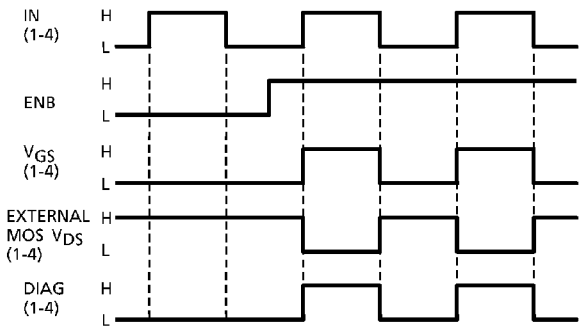


PIN DESCRIPTION

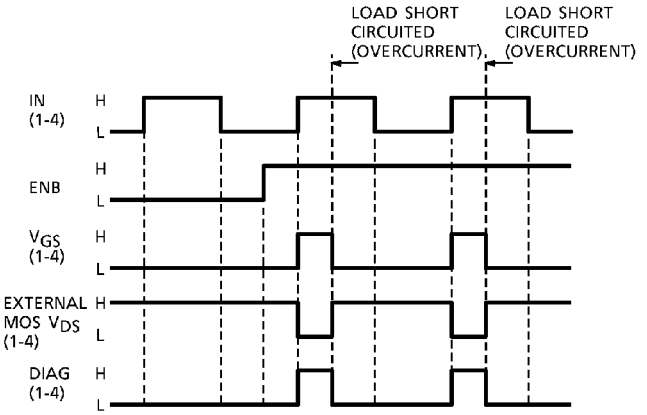
PIN No.	SYMBOL	FUNCTION
1, 12, 13, 24	V_{GS1}, V_{GS2}, V_{GS3}, V_{GS4}	Power MOS FET gate drive pins. The power MOS FET is charged by a 1mA (Typ.) constant current. The gate voltage is clamped at 14V (Typ.) as gate protection. At overcurrent, to protect the MOS FET, these pins are shut down and latched. The next input signal releases the latch.
2, 11, 14, 23	V_{DS1}, V_{DS2}, V_{DS3}, V_{DS4}	Voltage monitor pins for monitoring the voltage between the power MOS FET drain and source. These monitor the state of the power MOS FET and output DIAG.
3, 10, 15, 22	IN1, IN2, IN3, IN4	Input pins. Even if the input is open, pull-down resistors prevent output from accidentally being turned on.
4, 9, 16, 21	DIAG1, DIAG2, DIAG3, DIAG4	Diagnosis output pins. These pins monitor the V_{DS} pin voltage. When the V_{DS} pin voltage rises above the V_{DS} detection voltage, the DIAG pins output a low signal; when the voltage drops below the V_{DS} detection voltage, the pins output a high signal.
5	V_{DH}	Power MOS FET gate drive power pin.
6, 7	GND	Ground pins.
8	OPOUT	OPTION function output pin. NPN open collector.
17	OPIN	OPTION function input pin.
18	ENB	Enable pin. When ENB = low, the INHIBIT function operates and the MOS FET enters standby mode regardless of the input signal.
19	N.C	—
20	V_{DL}	Power pin for control circuit.

TIMING CHART

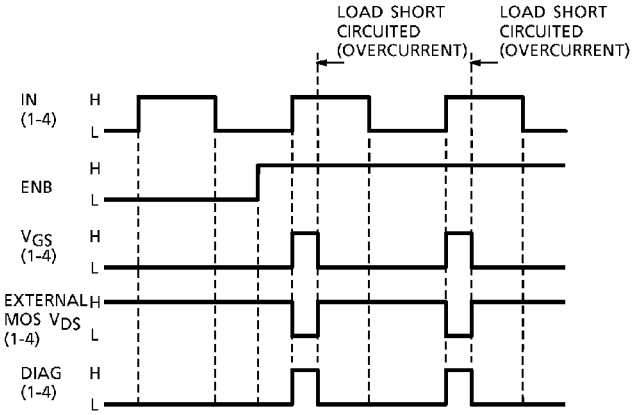
* Normal mode



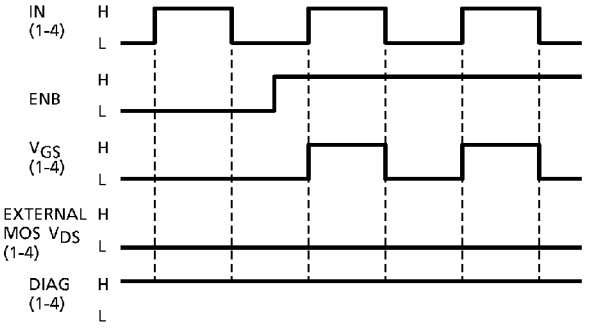
* Overcurrent mode



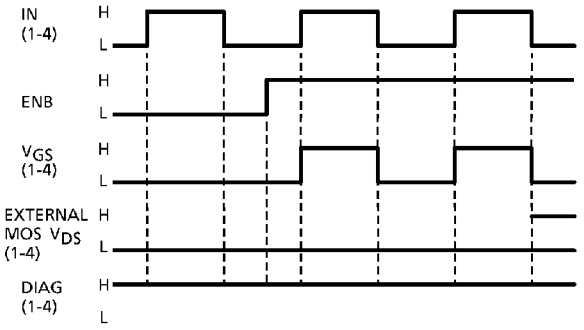
* Load short circuited mode
(short circuited to battery)



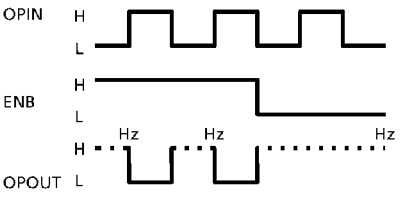
* Load open mode



* Short circuit between external power
MOS drain and source



* Optional driver operation



*Hz : High impedance

TRUTH TABLE

MODE	IN	ENB	V_{DS}	DIAG
Normal	L	H	H	L
	H		L	H
	L	L	H	L
	H		H	L
Overcurrent	L	H	H	L
	H		H	L
	L	L	H	L
	H		H	L
Load short circuit	L	H	H	L
	H		H	L
	L	L	H	L
	H		H	L
Power MOS short circuit	L	H	L	H
	H		L	H
	L	L	L	H
	H		L	H
Load open	L	H	L	H
	H		L	H
	L	L	L	H
	H		L	H

OPIN	ENB	OPOUT
L	H	Hz
H	H	L
L	L	Hz
H	L	Hz

*OPOUT is an NPN open collector.
*Hz : High impedance
*ENB is active high.
*DIAG monitors V_{DS} regardless of IN or ENB.

OPERATION

(1) When normal

① At external power MOS on

When 3.5V or more is applied to the IN and ENB pins, the V_{GS} pin goes high and a 1mA (Typ.) constant current drives the power MOS gate.
A V_{GS} mask circuit is built in to prevent erroneous detection of overcurrent in the transient area before the power MOS comes sufficiently on from off state. This circuit is set so that overcurrent is not erroneously detected before the V_{GS} rises to 6.5V (Typ.).
DIAG outputs a voltage that is the inverse of the V_{DS} state. The power MOS and its load state can be checked by monitoring the input voltage and the DIAG output.

② External power MOS off

When the input voltage of IN or ENB falls to 1.5V or below, the V_{GS} pin goes low, the external power MOS gate is discharged, and the MOS FET turns off.
The ENB pin has priority over the IN pin. When ENB is low, the V_{GS} pin does not go on even if a high level input voltage is applied to IN.

(2) At Overcurrent

If the V_{DS} pin voltage (the voltage between the power MOS drain and source) is around 0.7V or above (V_{DS} typical detection voltage) while high level input voltage is applied to the IN and ENB pins, overcurrent to the external power MOS is detected and the V_{GS} output is instantly shut down and latched. Setting the input voltage back to low level releases the latch.
When the voltage reaches the V_{DS} detection voltage or above, DIAG outputs low level.

(3) At load open

As a pull-down resistor is connected to the V_{DS} pin, when the load is open the V_{DS} pin is always low and high level is output to DIAG.

(4) OPTION function

The OPTION function is controlled by two input pins: OPIN and ENB. ENB has priority over OPIN. When high level voltage is input to OPIN or ENB, the OPOUT pin goes low. This function can be used as a pre-driver for lamps and mechanical relays.

(5) At V_{DL} low voltage

TPD7000F incorporates a low-voltage lock circuit for locking the V_{GS} and DIAG outputs when V_{DL} falls. This circuit is designed to operate around $V_{DL} = 2.8V$ (Typ.) or lower. When the circuit is in operation, ENB is locked at low level to cut off the V_{GS} output.

MAXIMUM RATINGS (Ta = 25°C)

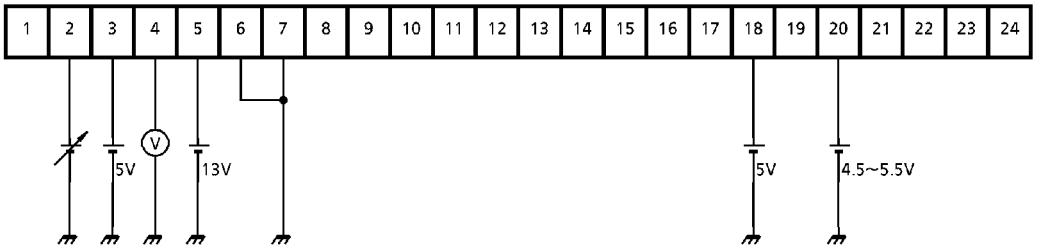
CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage	DC	V_{DH} (1)	25	V
	Pulse	V_{DH} (2)	30 (1 s)	
Supply Voltage		V_{DL}	10	V
Output Voltage		VOPOUT	10	V
Input Voltage		V_{IN}	−0.5~7	V
Output Current		IOPOUT	20	mA
Power Dissipation	Ta = 25°C	P_D	0.5	W
Operating Temperature		T_{opr}	−40~110	°C
Junction Temperature		Tj	150	°C
Storage Temperature		T_{stg}	−55~150	°C

ELECTRICAL CHARACTERISTICS (T_j = −40~110°C, V_{DH} = 13V, V_{DL} = 5 ± 0.5V)

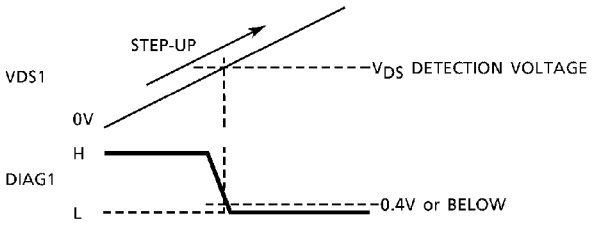
CHARACTERISTIC		SYMBOL	PIN NAME	TEST CONDITION	MIN	TYP.	MAX	UNIT
Operating Voltage		V_{DH}	V_{DH}	—	8	13	18	V
		V_{DL}	V_{DL}	—	4.5	5	5.5	
Current Dissipation		I_{DH}	V_{DH}	V_{IN} = 0V, V_{DH} = 13V, Output off	—	2	5	mA
		I_{DL}	V_{DL}	V_{IN} = 0V, V_{DL} = 5V, Output off	—	8	12	
Input Voltage		V_{IL}	IN / ENB / OPIN	When output off	—	—	1.5	V
		V_{IH}		When output on	3.5	—	—	
Input Crrent		I_{IL}	IN / ENB / OPIN	V_{IN} = 0V	—	—	1	μA
		I_{IH}		V_{IN} = 5V	—	100	200	
High-level Output Voltage 1		V_{OH1}	V_{GS}	V_{IN} = 5V, I_O = 0A, V_{DH} < 14V	—	—	V_{DH}	V
High-level Output Voltage 2		V_{OH2}	V_{GS}	V_{IN} = 5V, I_O = 0A, V_{DH} ≧ 14V	12	—	15	V
Low-level Output Voltage		V_{OL}	V_{GS}	V_{IN} = 0V, I_O = 0A	—	—	0.5	V
V_{DS} Detection Voltage		V_{DS}	V_{DS}	—	—	0.7	—	V
Diagnosis Resistance		RDIAG	DIAG	—	—	10	—	kΩ
Diagnosis Output Voltage	"L" Level	VDIAG	DIAG	V_{DL} = 5V	—	—	0.4	V
Diagnosis Off Current	"H" Level	IDIAG	DIAG	VDIAG = 5V	—	—	10	μA
Optional Output Voltage		V_{OPL}	OPOUT	I_{OP} = 10mA	—	—	0.4	V
Optional Off Current		I_{OPH}	OPOUT	VOPOUT = 5V	—	—	10	μA
Zener Voltage Between Drain and Gates		VCLAMP	V_{DS}	I_{DS} = 5mA, VCLAMP = V_{DS} − V_{GS}	30	35	40	V
Switching Time	When On	t_{PLH}	V_{GS}	C = 3000pF (Capacitance between V_{GS} and GND)	—	—	100	μs
	When Off	t_{PHL}			—	—	100	

ELECTRICAL CHARACTERISTICS TEST CIRCUIT

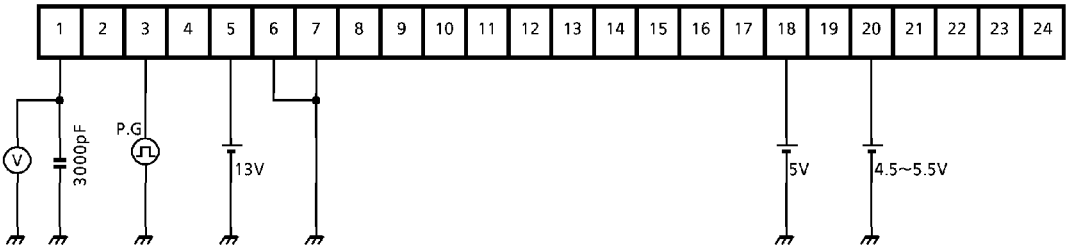
(1) V_{DS} detection voltage (V_{DS}) (The following circuit measures channel 1)



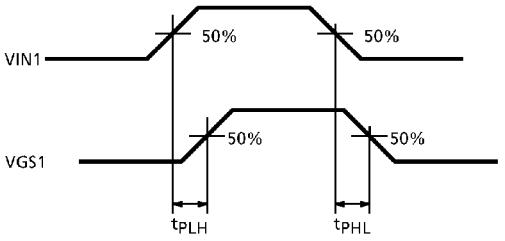
MEASURED WAVEFORM



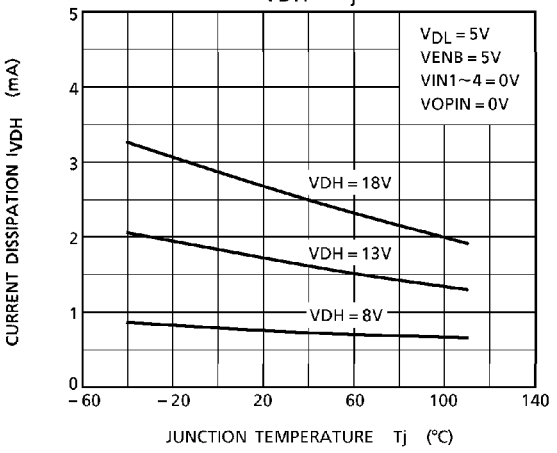
(2) Switching time (t_{PLH}, t_{PHL}) (The following circuit measures channel 1)



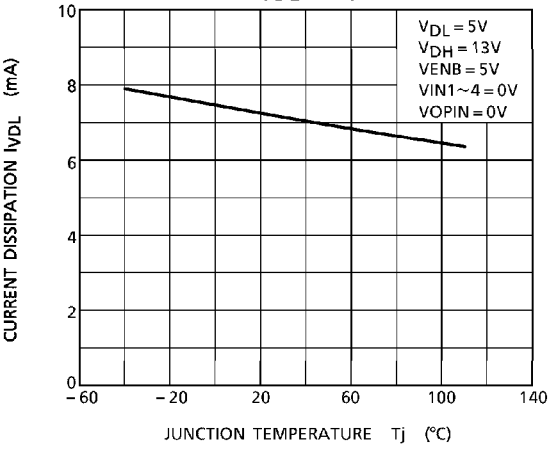
MEASURED WAVEFORM



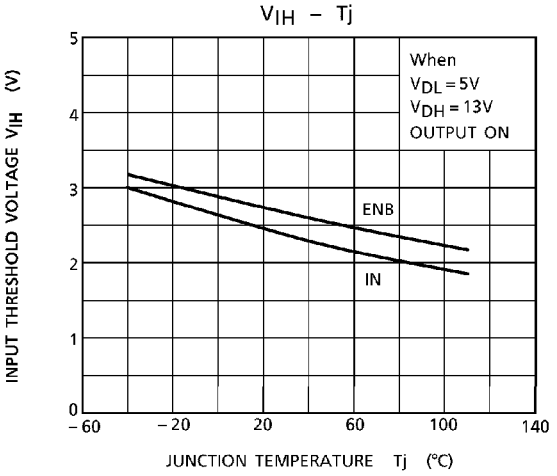
I_{VDH} – Tj



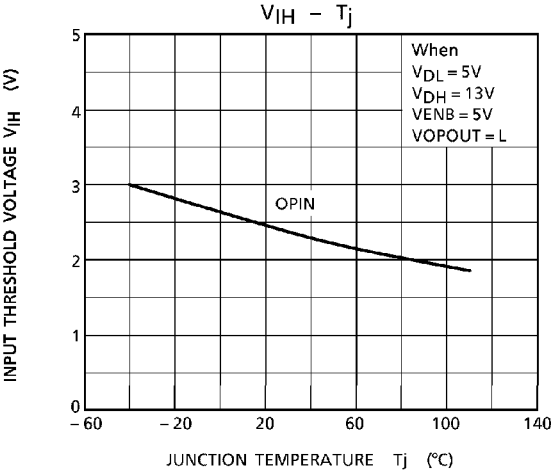
I_{VDL} – Tj



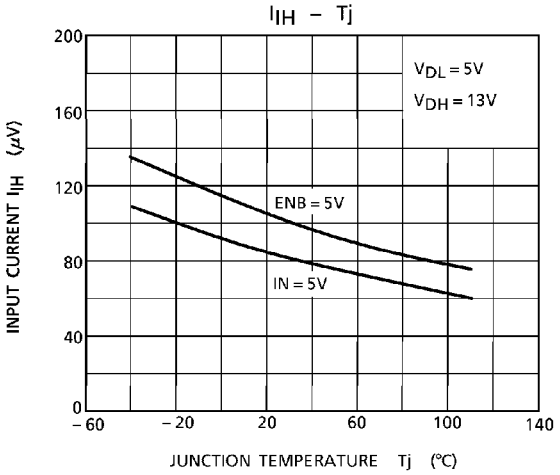
V_{IH} – Tj



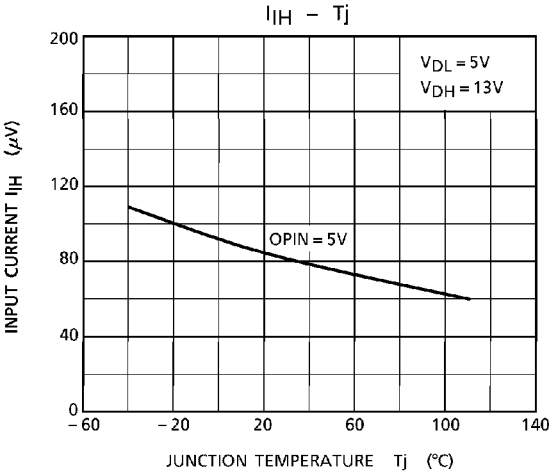
V_{IH} – Tj



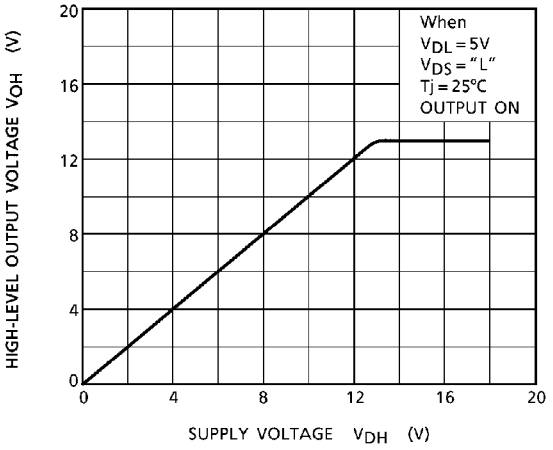
I_{IH} – Tj



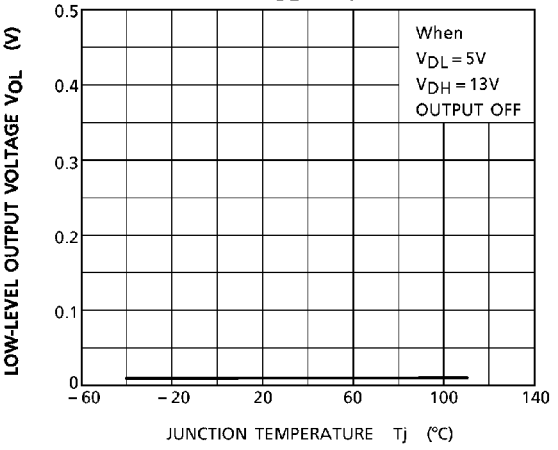
I_{IH} – Tj



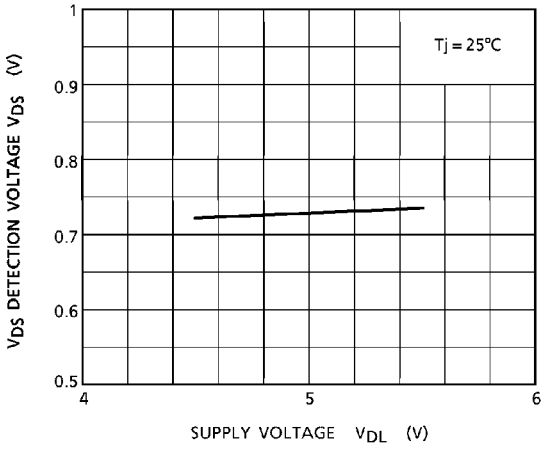
V_{OH} – V_{DH}



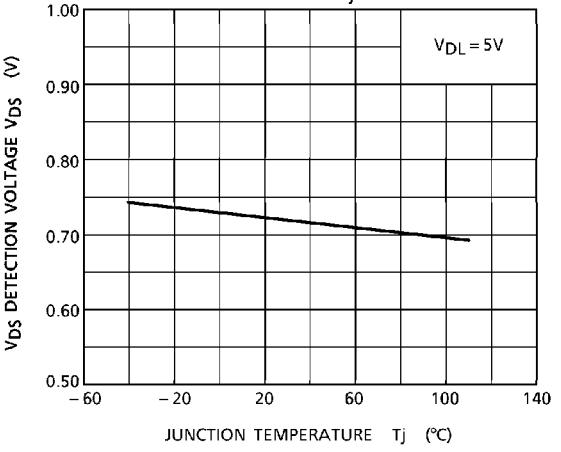
V_{OL} – Tj



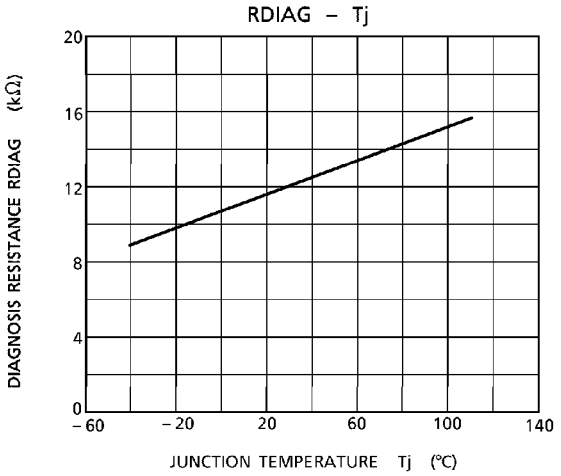
V_{DS} – V_{DL}



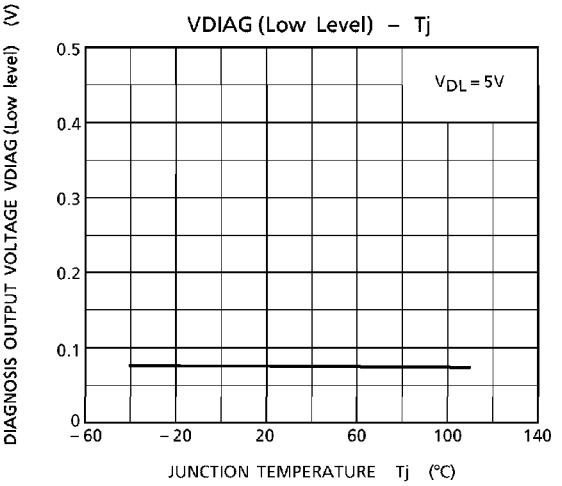
V_{DS} – Tj



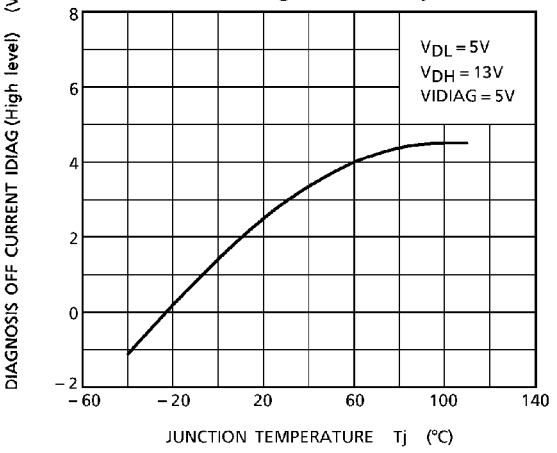
RDIAG – Tj



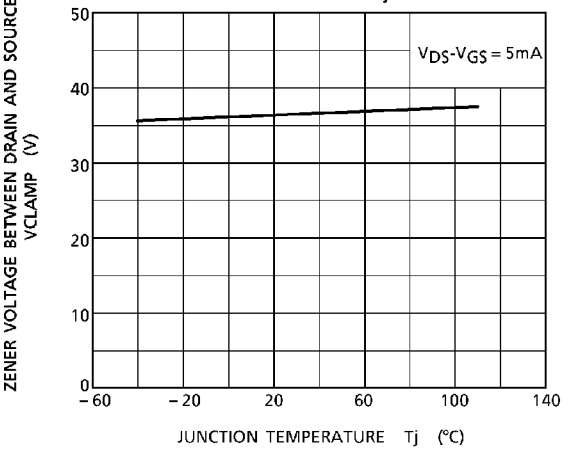
VDIAG (Low Level) – Tj



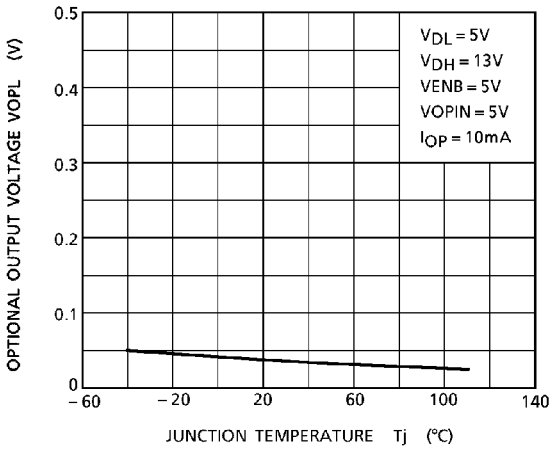
IDIAG (High Level) – Tj



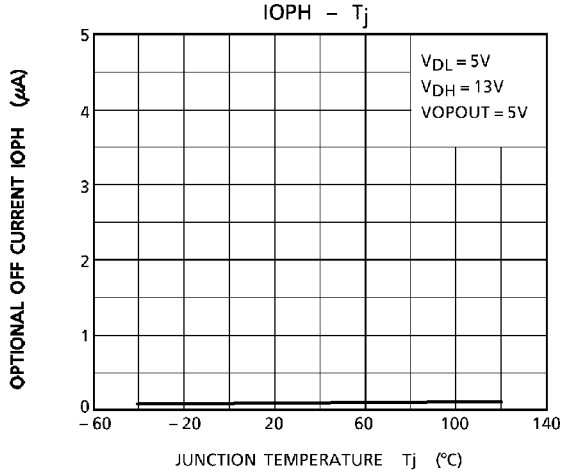
VCLAMP – Tj



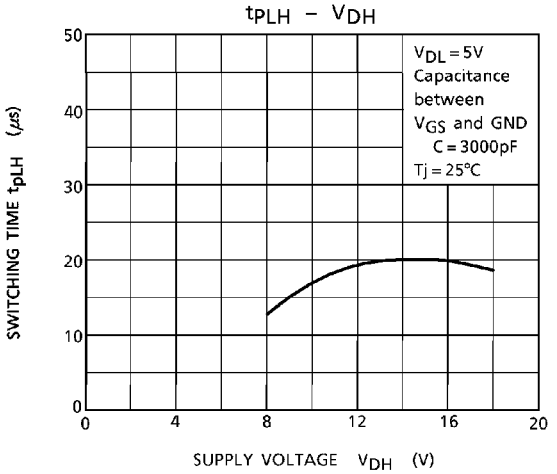
VOPL – Tj



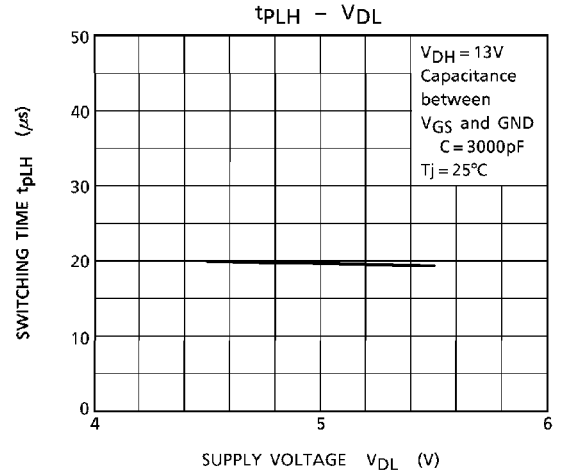
IOPH – Tj



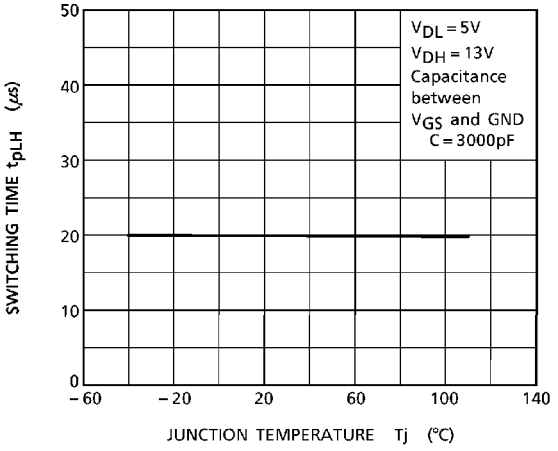
tPLH – VDH



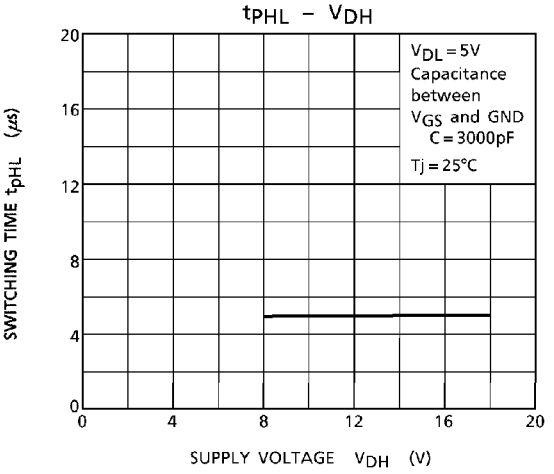
tPLH – VDL



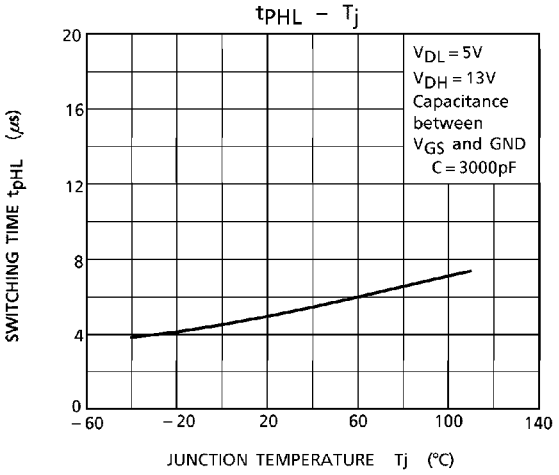
t_{PLH} – Tj



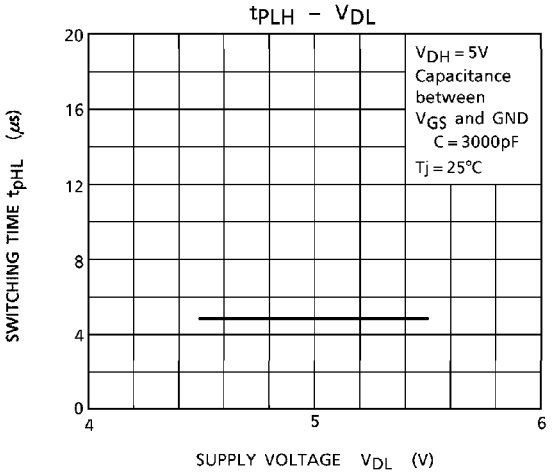
t_{PHL} – V_{DH}



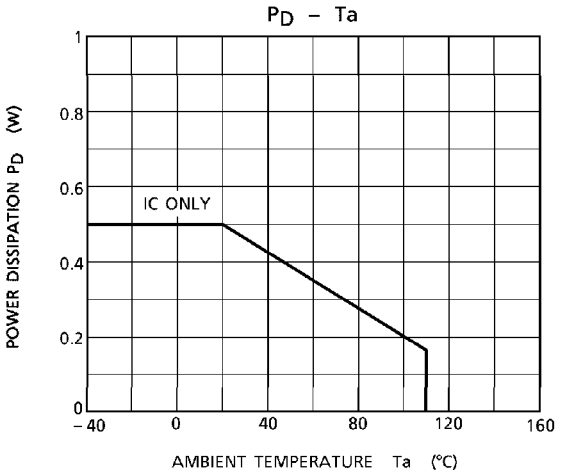
t_{PHL} – T_j



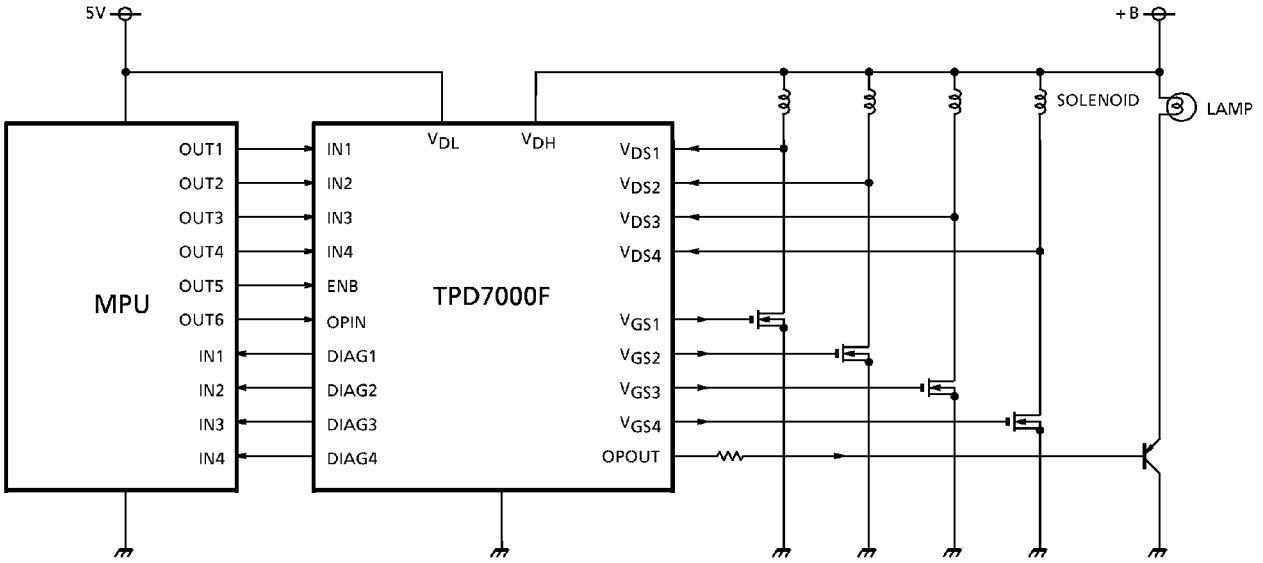
t_{PLH} – V_{DL}



P_D – Ta



APPLICATION CIRCUIT EXAMPLE



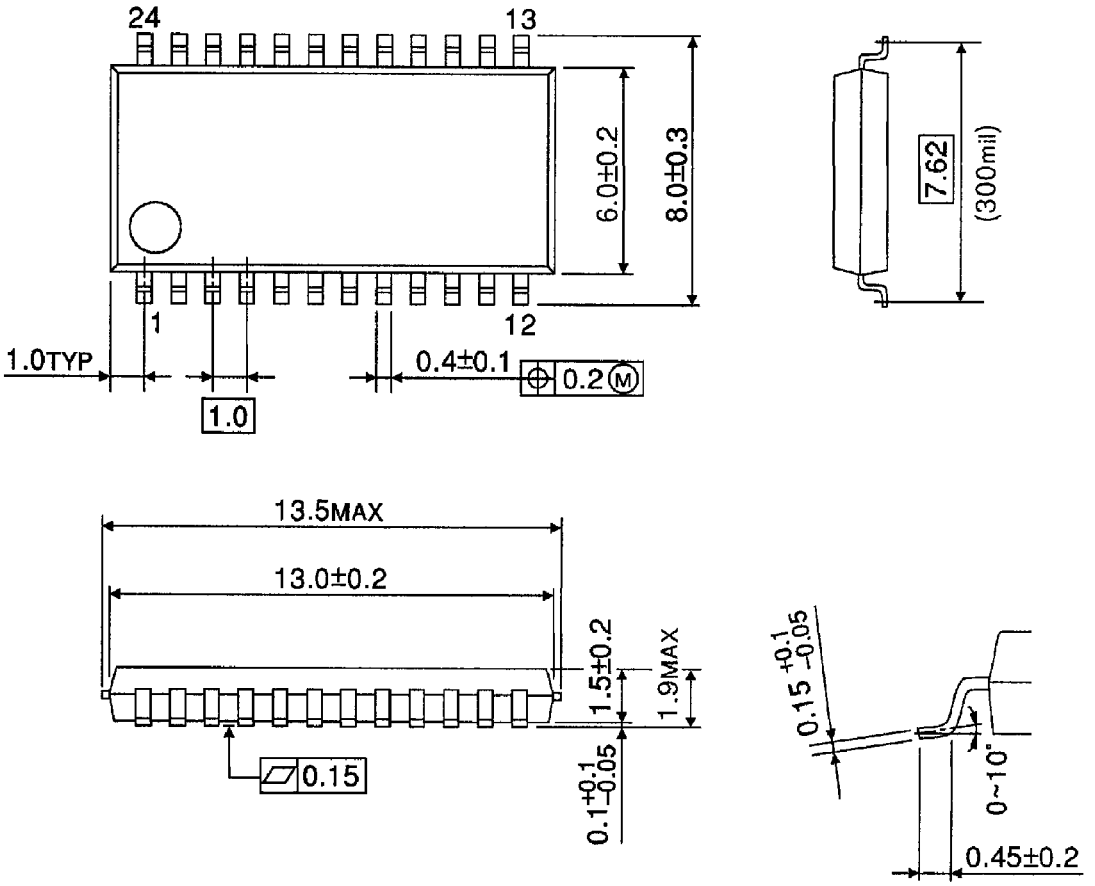
PRECAUTIONS CONCERNING MOISTURE-PROOF PACKAGING

Mount the device within 48 hours of removing it from the moisture-proof packaging in an environment of 30°C max, RH60% Max. As chips delivered in embossed taping cannot be baked, after removing the moisture-proof packaging be sure that mounting is performed within the allowable conditions.

OUTLINE DRAWING

SSOP24-P-300-1.00B

Unit : mm



Weight : 0.29g (Typ.)