FEATURES

- Four-Wide 2901 ALUs Plus Carry Look-Ahead Logic and Full 16-bit Data Paths
- High Speed, Low Power CMOS Technology
- Fast Clock Period:
  35 ns Commercial, 45 ns Military
- DESC SMD No. 5962-89517
- Available 100% Screened to MIL-STD-883, Class B
- Pin and Functionally Equivalent to AMD Am29C101 and Cypress CY7C9101
- Package Styles Available:
  - 64-pin Sidebraze, Hermetic DIP
  - 68-pin Ceramic Pin Grid Array

DESCRIPTION

The **L29C101** is a high-performance, expandable, 16-bit Arithmetic Logic Unit slice manufactured using CMOS technology. Completely code compatible with its 4-bit predecessors, the part can be used to implement the arithmetic section of central processors or many types of programmable controllers.

The microinstruction set of the L29C101 is straightforward, yet versatile enough so that the part can be used to emulate the ALU operations of most digital computers.

The L29C101 is comprised of functions equivalent to four 2901 bit-slice ALUs plus the 2902 carry look-ahead logic, all in a single 64-pin device.

Included are a 16-word by 16-bit dual-port register file, a 16-bit 8-function ALU, 16-bit shifters, and all the necessary decoding and control logic.

All status, shift linkage, and carry functions are cascadable to allow construction of architectures wider than 16-bits if desired. Expanded

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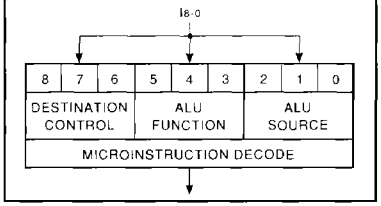
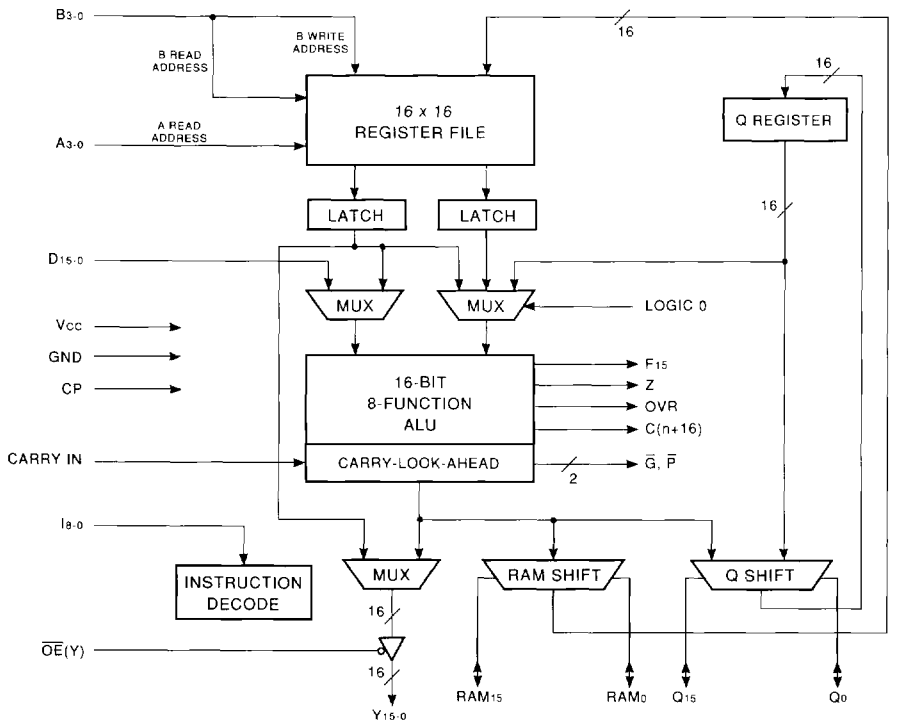
L29C101 Instruction Decoding



L29C101 Block Diagram



designs can take advantage of full carry-look-ahead for improved performance.

The L29C101 is fully pin and function compatible with the Am29C101. The L29C101 is available in High-Rel versions that are fully compliant with MIL-STD-883, Class B.

L29C101 ARCHITECTURE

A typical execution cycle for the L29C101 consists of reading two operands simultaneously from the two-port register file, performing an ALU operation on these operands, and returning the result to the register file. This entire operation can be completed in a single clock cycle, providing high performance and simple microcode. Optionally, the ALU operands may be sourced by the external data port, an auxiliary register denoted the Quotient or "Q" register, or forced to zero under instruction control. Also, the data returned to the register file and the Q register may be shifted one bit in either direction to aid multiplication and division operations.

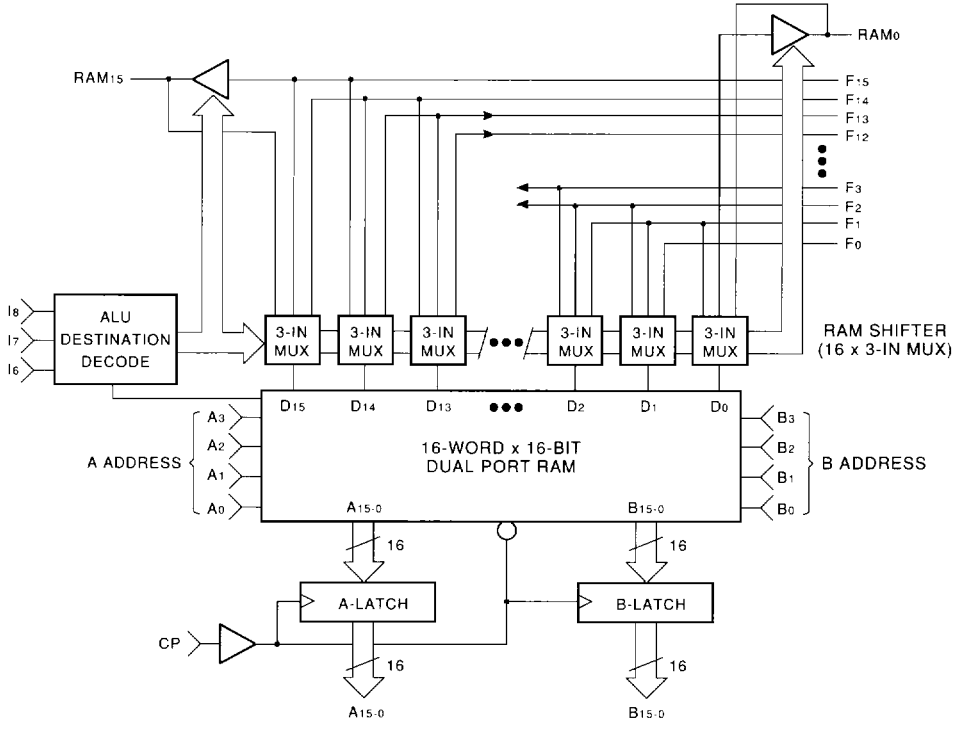
REGISTER FILE

The two-port register file has a capacity of 16 words of 16 bits each. The A-port address, A_{3-0}, specifies the register to be read from the A-port, and the B-port address, B_{3-0}, specifies the register to the read from the B-port. Both A and B addresses may be the same, in which case identical data will appear at both A and B ports. In addition, the B-port address can specify a register location for writing. Data from the locations indicated by the A and B addresses are read from the register file during the low period of the clock. The data is applied to two latches which are transparent during the clock low period, and hold their state during the clock high period. The purpose of these latches is to hold the A and B ALU operands constant while a computation result is written back to the register file at the B address. This allows for a read-modify-write cycle, which is useful in applications such as accumulation. Under control of the Result Destination Field (I_{8-6}), data to be written to the register file is stored into the register addressed by the B field on the rising edge of the clock.

ALU CONTROL

The ALU is capable of performing eight operations. These functions are described in Table 2. The control inputs, I_{5-3}, select one of three arith-

FIGURE 1. REGISTER FILE



metic or five logical operations to be performed on the input operands. The integral carry-look-ahead circuitry across all 16 ALU bits is functionally equivalent to the 2902 carry-look-ahead unit and provides significant speed advantages.

In the arithmetic mode, the ALU result is also a function of the Carry-In input. When executing ALU Add or Subtract instructions, setting the C(n) input to '1' causes the addition of '1' to the result. Thus for two's complement operations, C(n) of the least significant slice would be set to zero for addition, and to '1' for subtraction. This is because the L29C101 ALU naturally implements one's complement subtraction, that is, a bitwise complement of one of the operands. In order to achieve a two's complement result, a '1' must be added in the least significant position. This is accomplished by using C(n). PASS and Negate operations are also available by combining arithmetic instructions (Add, Subtract) with any of the operand source options which set one operand to zero. Tables 5 and 6 show the detailed ALU logic and arithmetic functions and the operands selected. Table 5 includes ALU function selection.

OPERAND SOURCE CONTROL

As shown in the figure below, each of the ALU operands is supplied by a multiplexer, which allows significant flexibility in the selection of the operand source. The two 16-bit ALU inputs are denoted R and S. The R operand may be sourced by the A read port of the register file, from the D input pins, or may be forced to zero. The S operand may be sourced by the B read port of the register file, the A read port (when the R operand is D or zero), the Q register, or forced to zero. Control of the operand selection multiplexers is encoded into control field I_{2-0}, as described in Table 1.

RESULT DESTINATION CONTROL

The instruction field, I_{8-6}, is encoded to control the routing of the ALU result field, denoted F, and the Q register contents. The encoding is defined in Table 3. Under instruction control, the ALU result can be stored in the register file, the Q register, or both. A No Operation capability is also provided during which the result is not stored in either location. This field also controls the value presented at the Y_{15-0} outputs. These outputs generally reflect the ALU result F, but for one of the instruction decodes, the outputs are

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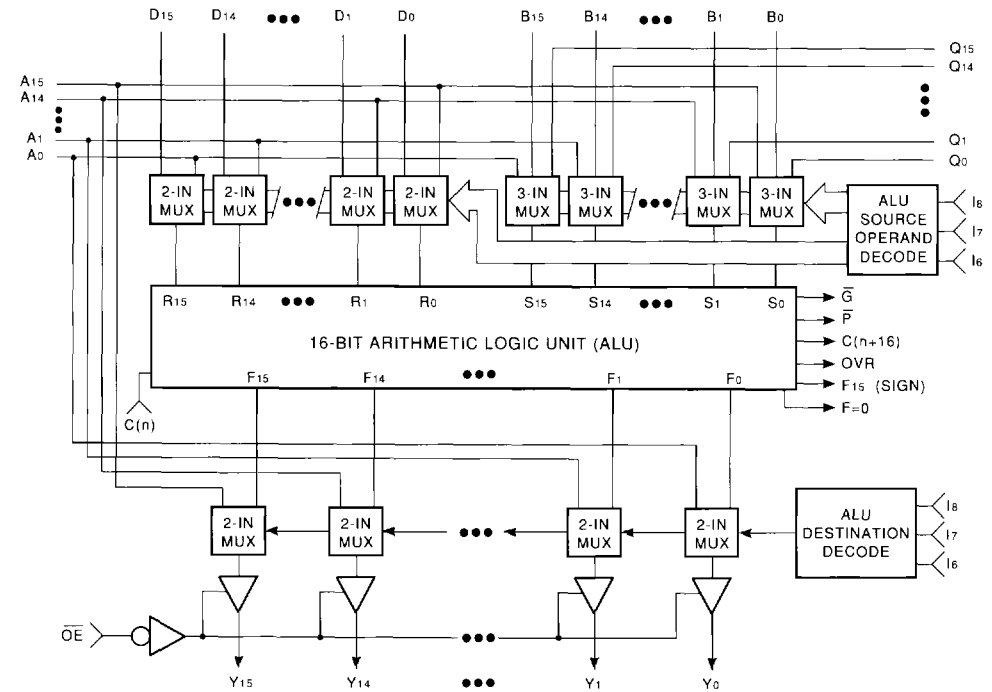
FIGURE 2. ALU



driven by the A port value read from the register file. This provides the capability to read data from the register file while simultaneously performing an ALU operation. This is useful in applications such as postincrement address generation.

In addition to destination control, up or down shifting of both the register file and Q register load values are controlled by the I8-6 field. Each can be up or down shifted one position prior to storing in the destination register. The RAM0 or Q0 pins output the least significant bit of the value being stored for downshifts, and accept the bit to be stored in the least signficant position for upshifts. Similarly, the RAM15 or Q15 pins output the most significant bit for upshifts, and accept the bit to be stored in the most significant position for downshifts. Table 3 gives the various shift actions and data destinations controlled by the I8-6 inputs.

Q REGISTER

The Q register is intended primarily for use as a separate working register for multiplication and division routines but it also serves as an accumulator or for temporary storage. The Q register is loaded via a multiplexer, which allows either up or downshift of the Q register contents, or an unshifted load of the Q register with the ALU result.

STATUS OUTPUTS

The $\overline{G}$ and $\overline{P}$ outputs are low-true Carry-Generate and Carry-Propagate signals. They are used in conjunction with an external carry-look-ahead generator when cascading L29C101 slices beyond 32 bits. The C(n+16) is the Carry-Out signal, which can be directly connected to the C(n) input of another L29C101 to implement a 32-bit system. The OVR output indicates two's complement overflow for addition and subtraction. The logical definitions of the $\overline{G}$, $\overline{P}$, C(n+16), and OVR signals are given in Table 7.

The MSB of the ALU result (F15) is provided so that the sign bit may be examined easily. The Z output is used for zero detection and is high when all of the F output bits are low. It is an open drain output which may be wire OR'ed across multiple slices.

FIGURE 3. Q REGISTER

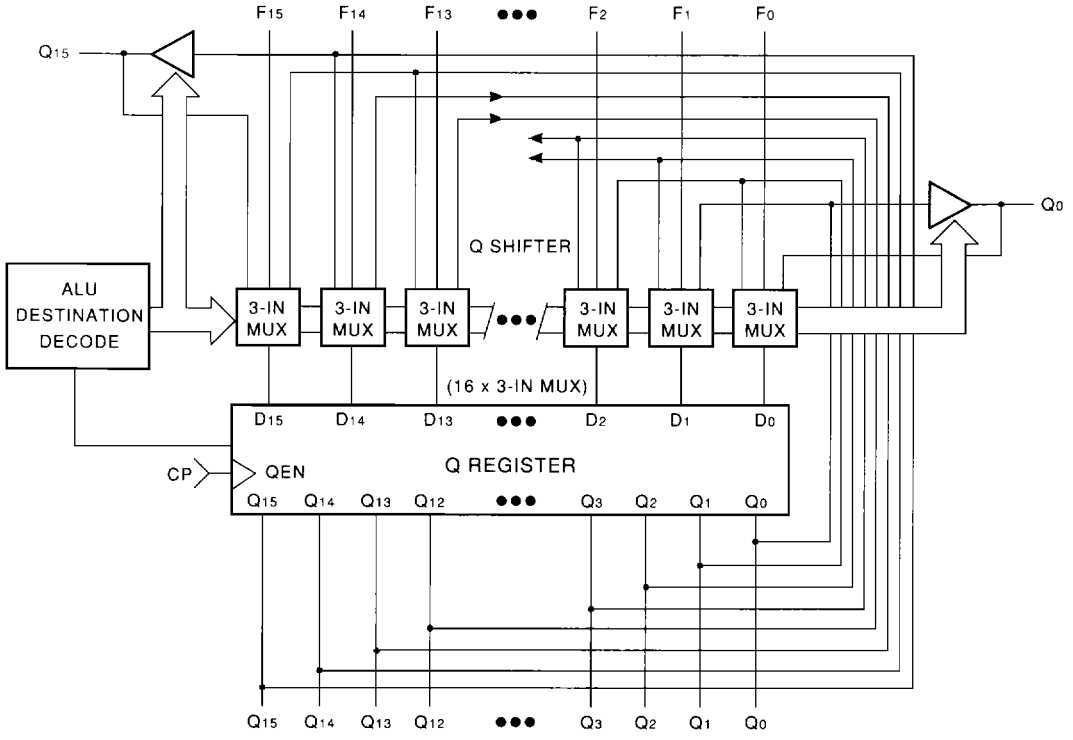


TABLE 1. ALU SOURCE OPERAND CONTROL

Mnemonic	Micro Code I2	I1	I0	Octal Code	ALU Source Operands R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	O	Q
ZB	L	H	H	3	O	B
ZA	H	L	L	4	O	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	O

TABLE 2. ALU FUNCTION CONTROL

Mnemonic	Micro Code I5	I4	I3	Octal Code	ALU Function	Symbol
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S – R
SUBS	L	H	L	2	R Minus S	R – S
OR	L	H	H	3	R OR S	
AND	H	L	L	4	R AND S	
NOTRS	H	L	H	5	$\overline{R}$ AND S	
EXOR	H	H	L	6	R EX-OR S	
EXNOR	H	H	H	7	R EX-NOR S	

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TABLE 3. ALU DESTINATION CONTROL

Mnemonic	Micro Code I8	I7	I6	Octal Code	RAM Function Shift	Load	Q-Reg. Function Shift	Load	Y Output	RAM Shifter RAM0	RAM15	Q Shifter Q0	Q15
QREG	L	L	L	0	X	None	None	F → Q	F	X	X	X	X
NOP	L	L	H	1	X	None	X	None	F	X	X	X	X
RAMA	L	H	L	2	None	F → B	X	None	A	X	X	X	X
RAMF	L	H	H	3	None	F → B	X	None	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F0	IN15	Q0	IN15
RAMD	H	L	H	5	DOWN	F/2 → B	X	None	F	F0	IN15	Q0	X
RAMQU	H	H	L	6	UP	2F → B	UP	2Q → Q	F	IN0	F15	IN0	Q15
RAMU	H	H	H	7	UP	2F → B	X	None	F	IN0	F15	X	Q15

TABLE 4. SOURCE OPERAND AND ALU FUNCTION MATRIX

Octal I5-3	I2-0 → / ALU Function	0	1	2	3	4	5	6	7
		ALU Source							
		A, Q	A, B	O, Q	O, B	O, A	D, A	D, Q	D, O
0	C(n) = L R plus S	A + Q	A + B	Q	B	A	D + A	D + Q	D
	C(n) = H	A + Q + 1	A + B + 1	Q + 1	B + 1	A + 1	D + A + 1	D + Q + 1	D + 1
1	C(n) = L S minus R	Q – A – 1	B – A – 1	Q – 1	B – 1	A – 1	A – D – 1	Q – D – 1	– D – 1
	C(n) = H	Q – A	B – A	Q	B	A	A – D	Q – D	– D
2	C(n) = L R minus S	A – Q – 1	A – B – 1	– Q – 1	– B – 1	– A – 1	D – A – 1	D – Q – 1	D – 1
	C(n) = H	A – Q	A – B	– Q	– B	– A	D – A	D – Q	D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	$\overline{A}$ ∧ Q	0	0	0	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	A ∧ B	Q	B	A	D ∧ A	D ∧ Q	0
6	R EX-OR S	A ∀ Q	A ∀ B	Q	B	A	D ∀ A	D ∀ Q	D
7	R EX-NOR S	$\overline{A \forall Q}$	$\overline{A \forall B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \forall A}$	$\overline{D \forall Q}$	$\overline{D}$

TABLE 5. ALU LOGIC MODE FUNCTIONS

Octal I_{5-3}, I_{2-0}	Group	Function
40	AND	$A \wedge Q$
41		$A \wedge B$
45		$D \wedge A$
46		$D \wedge Q$
30	OR	$A \vee Q$
31		$A \vee B$
35		$D \vee A$
36		$D \vee A$
60	EX – OR	$A \forall Q$
61		$A \forall B$
65		$D \forall A$
66		$D \forall Q$
70	EX – NOR	$\overline{A \forall Q}$
71		$\overline{A \forall B}$
75		$\overline{D \forall A}$
76		$\overline{D \forall Q}$
72	INVERT	$\overline{Q}$
73		$\overline{R}$
74		$\overline{A}$
77		$\overline{D}$
62	PASS	Q
63		B
64		A
67		D
32	PASS	Q
33		B
34		A
37		D
42	ZERO	0
43		0
44		0
47		0
50	MASK	$\overline{A} \wedge Q$
51		$\overline{A} \wedge B$
55		$\overline{D} \wedge A$
56		$\overline{D} \wedge Q$

TABLE 6. ALU ARITHMETIC MODE FUNCTIONS

Octal I_{5-3}, I_{2-0}	C(n) = 0 (Low)		C(n) = 1 (High)	
	Group	Function	Group	Function
00	ADD	A + Q	ADD Plus One	A + Q + 1
01		A + B		A + B + 1
05		D + A		D + A + 1
06		D + Q		D + Q + 1
02	PASS	Q	Increment	Q + 1
03		B		B + 1
04		A		A + 1
07		D		D + 1
12	Decrement	Q – 1	PASS	Q
13		B – 1		B
14		A – 1		A
27		D – 1		D
22	1's Comp.	– Q –1	2's Comp. (Negate)	– Q
23		– B – 1		– B
24		– A – 1		– A
17		– D – 1		– D
10	Subtract (1's Comp.)	Q – A –1	Subtract (2's Comp.)	Q – A
11		B – A – 1		B – A
15		A – D – 1		A – D
16		Q – D – 1		Q – D
20		A – Q –1		A – Q
21		A – B – 1		A – B
25		D – A – 1		D – A
26		D – Q – 1		D – Q

TABLE 7. LOGIC FUNCTIONS FOR CARRY AND OVERFLOW CONDITIONS

I_{5-3}	Function	P	G	C (n+16)	OVR
0	R + S	$\overline{P_0 \cdot P_1 \cdots P_{15}}$	$\overline{G_{15} + P_{15} G_{14} + P_{15} P_{14} G_{13} + \cdots}$	C_{16}	$C_{16} \forall C_{15}$
1	S – R	Same as R + S equations, but substitute $\overline{Ri}$ for Ri in definitions			
2	R – S	Same as R + S equations, but substitute $\overline{Si}$ for Si in definitions			
3	$R \vee S$	HIGH	HIGH	LOW	LOW
4	$R \wedge S$				
5	$R \wedge S$				
6	$\overline{R} \forall S$				
7	$\overline{R \forall S}$				

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

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OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		15	30	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			5.0	mA

SWITCHING CHARACTERISTICS — COMMERCIAL OPERATING RANGE (0°C to +70°C) *Note 9 (ns)*

OUTPUT ENABLE/DISABLE TIMES *(Note 11)*

Device	Input	Output	tENA	tDIS
L29C101-35	$\overline{OE}$	Y	20	17

CYCLE TIME AND CLOCK CHARACTERISTICS

Read – Modify – Write Cycle (from selection of A, B registers to end of cycle)	35 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	30 MHz
Minimum Clock LOW Time	15 ns
Minimum Clock HIGH Time	20 ns

COMBINATIONAL PROPAGATION DELAYS *(Note 13)*

From Input \ To Output	Y	F15	C (n16)	$\overline{G}$, $\overline{P}$	F = 0	OVR	RAM0 RAM15	Q0 Q15
A,B Address	46	43	35	37	49	41	40	—
D	34	34	27	27	40	29	33	—
C(n)	27	24	20	—	28	23	28	—
I0, I1, I2	40	40	33	30	42	32	35	—
I3, I4, I5	41	38	32	28	40	36	38	—
I6, I7, I8	20	—	—	—	—	—	26	26
A bypass ALU (I = 2XX)	26	—	—	—	—	—	—	—
Clock	38	34	30	30	36	32	34	25

SETUP AND HOLD TIMES RELATIVE TO CLOCK INPUT *(Note 13)*

Input	Setup Time Before H → L	Hold Time After H → L	Setup Time Before L → H	Hold Time After L → H
A,B Source Address (Notes 15, 16)	24	3	35	—
B Destination Address (Note 14)	24	Do Not Change		0
D	—	—	26	0
C(n)	—	—	16	0
I0, I1, I2	—	—	30	0
I3, I4, I5	—	—	31	0
I6, I7, I8 (Note 14)	10	Do Not Change		0
RAM0, RAM15, Q0, Q15	—	—	12	0

SWITCHING CHARACTERISTICS — MILITARY OPERATING RANGE (-55°C to +125°C) *Note 9 (ns)*

OUTPUT ENABLE/DISABLE TIMES *(Note 11)*

Device	Input	Output	tENA	tDIS
L29C101-45	$\overline{OE}$	Y	23	20

CYCLE TIME AND CLOCK CHARACTERISTICS

Read – Modify – Write Cycle (from selection of A, B registers to end of cycle)	45ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	25 MHz
Minimum Clock LOW Time	20 ns
Minimum Clock HIGH Time	20 ns

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COMBINATIONAL PROPAGATION DELAYS *(Note 13)*

From Input \ To Output	Y	F_{15}	C (n16)	$\overline{G}$, $\overline{P}$	F = 0	OVR	RAM_0 RAM_{15}	Q_0 Q_{15}
A,B Address	52	50	40	38	48	46	43	—
D	37	36	30	32	40	32	35	—
C(n)	30	28	24	—	29	27	30	—
I_0, I_1, I_2	44	43	36	34	46	38	41	—
I_3, I_4, I_5	47	44	35	35	45	44	45	—
I_6, I_7, I_8	22	—	—	—	—	—	30	30
A bypass ALU (I = 2XX)	27	—	—	—	—	—	—	—
Clock	44	39	32	32	40	36	34	28

SETUP AND HOLD TIMES RELATIVE TO CLOCK INPUT *(Note 13)*

Input	Setup Time Before H → L	Hold Time After H → L	Setup Time Before L → H	Hold Time After L → H
A,B Source Address (Notes 15, 16)	22	3	40	—
B Destination Address (Note 14)	22	Do Not Change		0
D	—	—	30	0
C(n)	—	—	20	0
I_0, I_1, I_2	—	—	37	0
I_3, I_4, I_5	—	—	36	0
I_6, I_7, I_8 (Note 14)	10	Do Not Change		0
RAM_0, RAM_{15}, Q_0, Q_{15}	—	—	12	0

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

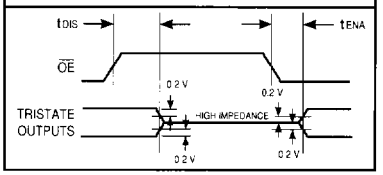
13. A dash indicates a propagation delay or setup time constraint that does not exist.

14. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change."

15. Source addresses must be stable prior to the clock H→L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.

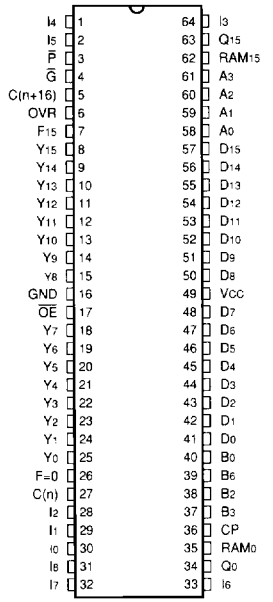
16. The setup time prior to the clock L→H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→H transition, regardless of when the clock H→L transition occurs.

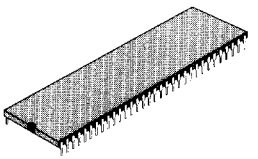
FIGURE 4. THRESHOLD LEVELS



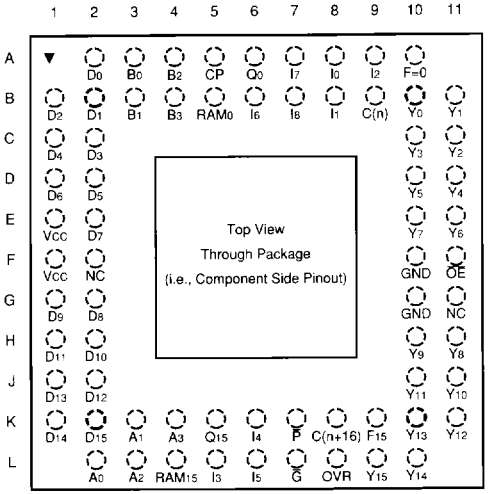
ORDERING INFORMATION

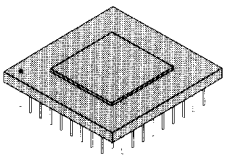
64-pin





68-pin





Speed	Sidebraze Hermetic DIP (D6)	Ceramic Pin Grid Array (G1)
	0°C to +70°C — COMMERCIAL SCREENING	
35 ns	L29C101DC35	L29C101GC35
	–55°C to +125°C — COMMERCIAL SCREENING	
45 ns	L29C101DM45	L29C101GM45
	–55°C to +125°C — MIL-STD-883 COMPLIANT	
45 ns	L29C101DMB45	L29C101GMB45