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Advance Information

17C724

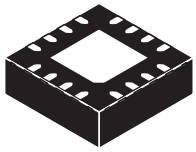
0.4 A Dual H-Bridge Motor Driver IC

0.4 A DUAL H-BRIDGE MOTOR DRIVER IC

The 17C724 is a compact monolithic dual channel H-Bridge power IC, ideal for portable electronic applications containing bipolar stepper motors or brush DC motors such as those used in camera lenses and shutters.

The 17C724 can operate efficiently with supply voltages from 2.7 V to 5.5 V and can provide continuous motor drive currents of 0.4 A with low $R_{DS(ON)}$ of 1.0 Ω. It is easily interfaced to low-cost MCUs via parallel 3.0 V- or 5.0 V-compatible logic and has built-in shoot-through current protection circuit and undervoltage detector to avoid malfunction.

The 17C724 has four output control modes: Forward, Reverse, Brake, and Tri-State (High Impedance). The H-bridge outputs are designed to be independently PWM'ed at up to 200 kHz for speed/torque and current control.



EP (Pb-FREE) SUFFIX
CASE 1524-01
16-LEAD QFN

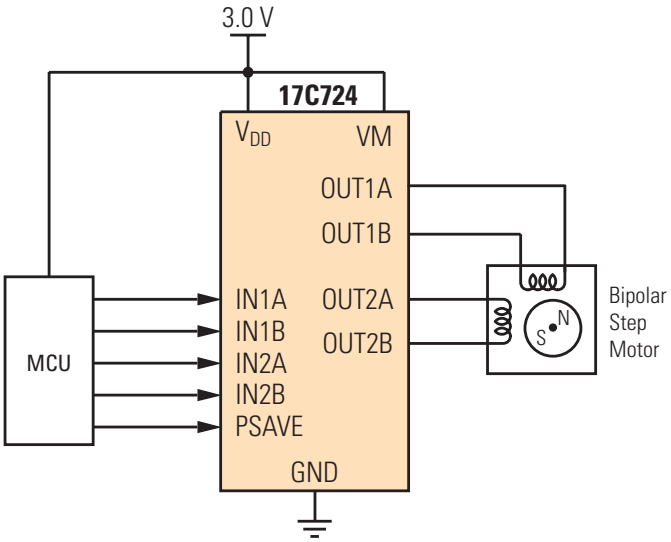
Features

- Manufactured in SMOS7 Process Technology
- Built-In 2-Channel H-Bridge Driver
- Provides 4 Driving Modes (Forward, Reverse, Break, High Impedance)
- Direct Interface to MCU
- Low ON-Resistance, $R_{DS(ON)}$ = 1.0 Ω (Typical)
- Dual Channel Parallel Drive, $R_{DS(ON)}$ = 0.5 Ω (Typical)
- Output Current Driver (IDR) is 400 mA (Continuous)
- Low Power Consumption
- Built-In Shoot-Through Current Prevention Circuit
- Built-In Low-Voltage Shutdown Circuit
- PWM Control Frequency 200 kHz (Max)
- Very Compact Size, Comes in 16-Terminal QFN Package (3x3 mm Terminal Pitch: 0.5 mm)
- Pb-Free Packaging Designated by Suffix Code EP

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
PPC17C724EP/R2	-20°C to 85°C	16 QFN

17C724 Simplified Application Diagram



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Specifications and information herein are subject to change without notice.

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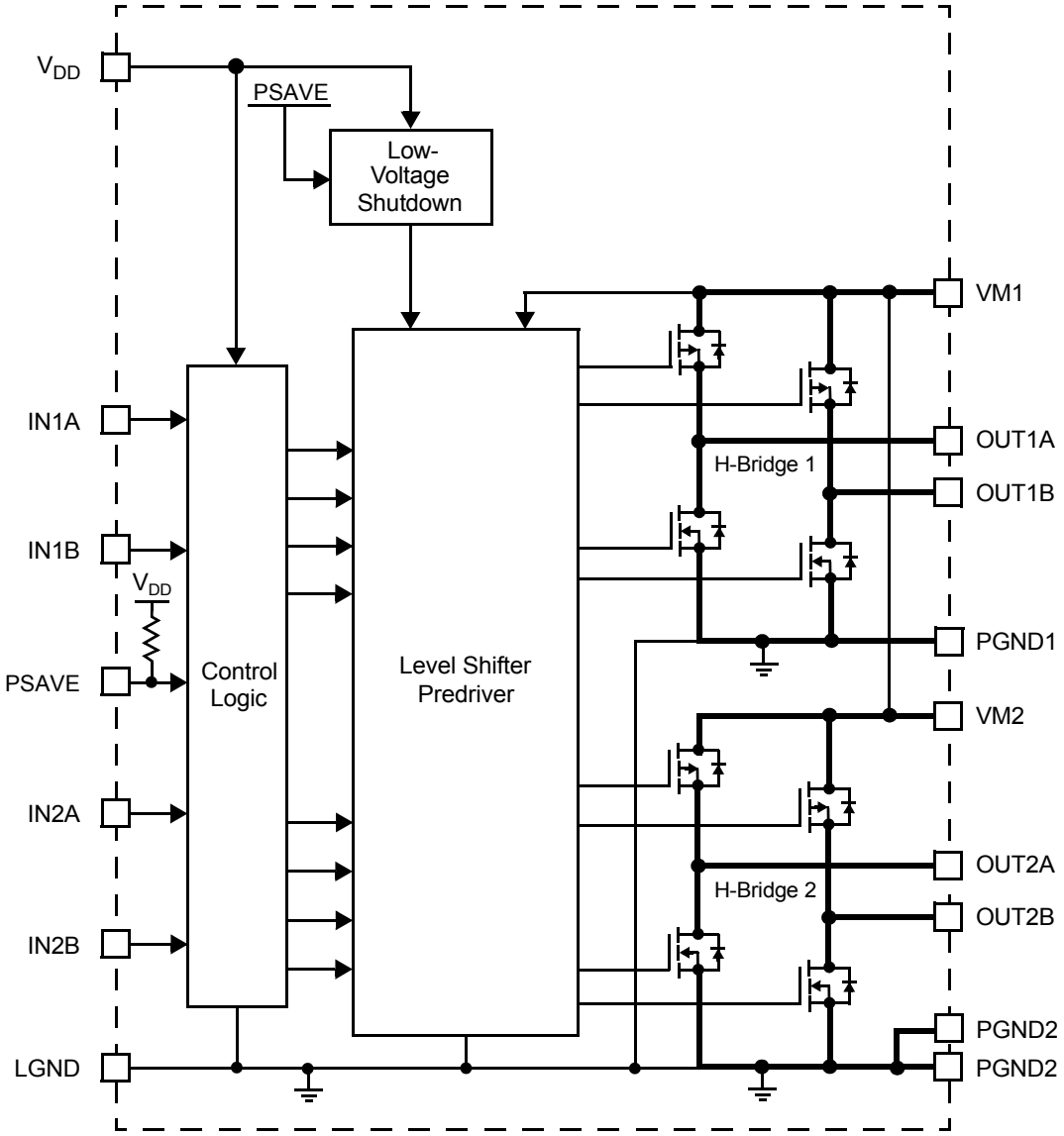
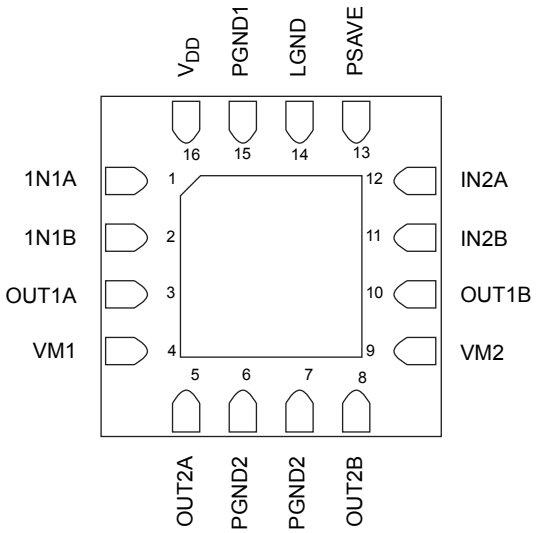


Figure 1. 17C724 Simplified Internal Block Diagram

Transparent Top View of Package



TERMINAL DEFINITIONS

A functional description of each terminal can be found in the System/Application Information section beginning on page 8.

Terminal	Terminal Name	Formal Name	Definition
1	IN1A	Logic Input Control 1A	Logic input control of OUT1A (refer to Table 1, Truth Table, page 7).
2	IN1B	Logic Input Control 1B	Logic input control of OUT1B (refer to Table 1, Truth Table, page 7).
3	OUT1A	H-Bridge Output 1A	Output A of H-Bridge channel 1.
4	VM1	Motor Driver Power Supply 1	Positive power source connection for H-Bridge 1 (Motor Driver Power Supply) (Note 1).
5	OUT2A	H-Bridge Output 2A	Output A of H-Bridge channel 2.
6, 7	PGND2	Power Ground 2	High-current power ground 2 (Note 2).
8	OUT2B	H-Bridge Output 2B	Output B of H-Bridge channel 2.
9	VM2	Motor Driver Power Supply 2	Positive power source connection for H-Bridge 2 (Motor Driver Power Supply) (Note 1).
10	OUT1B	H-Bridge Output 1B	Output B of H-Bridge channel 1.
11	IN2B	Logic Input Control 2B	Logic input control of OUT2B (refer to Table 1, Truth Table, page 7).
12	IN2A	Logic Input Control 2A	Logic input control of OUT2A (refer to Table 1, Truth Table, page 7).
13	PSAVE	Input Enable Control	Logic input enable control of H-Bridges to save power.
14	LGND	Logic Ground	Low-current logic signal ground (Note 2).
15	PGND1	Power Ground 1	High-current power ground 1 (Note 2).
16	V_{DD}	Logic Circuit Power Supply	Positive power source connection for logic circuit.

Notes
1. VM1 and VM2 are internally connected.
2. LGND, PGND1, and PGND2 are internally connected.

MAXIMUM RATINGS

All voltages are with respect to ground at T_A = 25°C unless otherwise noted. Exceeding these voltages may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
Power Supply Voltage (Motor Driver) Normal Operation (Steady-State) Transient Conditions (Note 3)	 $V_{M(SS)}$ $V_{M(PK)}$	 -0.3 to 6.0 -0.3 to 6.5	V
Logic Supply Voltage	V_{DD}	6.0	V
Input Terminal Voltage	V_{IN}	-0.3 to V_{DD} + 0.3	V
Driver Output Current (Continuous) (Note 4)	I_O	400	mA
Driver Output Current (Peak) (Note 5)	I_{OPK}	800	mA
ESD Voltage Human Body Model (Note 6) Machine Model (Note 7)	 V_{ESD1} V_{ESD2}	 ±2000 ±200	V
Storage Temperature	T_{STG}	-40 to 150	°C
Operating Ambient Temperature	T_A	-20 to 85	°C
Operating Junction Temperature	T_J	-20 to 150	°C
Terminal Soldering Temperature (Note 8)	T_{SOLDER}	260	°C
Thermal Resistance (Junction-to-Ambient) Single-Layer PCB Mounting (Note 9) Multi-Layer PCB (2S2P) Mounting (Note 10)	 $R_{\theta JA}$ $R_{\theta JMA}$	 169 47	°C/W

Notes

3. Transient condition within 500 ms.
4. Continuous output current must not be exceeded and at operating junction temperature below 150°C.
5. Peak time is for 10 ms pulse width at 200 ms intervals.
6. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP}=100 pF, R_{ZAP}=1500 Ω).
7. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP}=200 pF, R_{ZAP}=0 Ω).
8. Terminal soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
9. For cases using SEMI G38-87, JEDEC JESD51-2, JESD51-3, JESD51-5, single layer PCB mounting without thermal vias.
10. For cases using SEMI JEDEC JESD51-6, JESD51-5, JESD51-7, 2S2P PCB mounting with 4 thermal vias.

STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions T_A = 25°C, V_{DD} = V_M = 3.0 V unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Supply Voltage Range					V
Motor Driver Supply Voltage	V_M	2.7	3.0	5.5	
Logic Supply Voltage	V_{DD}	2.7	3.0	5.5	
Standby Power Supply Current (Note 11)					μA
V_M = 3.0 V	$I_{V_{MSTBY}}$	–	–	1.0	
V_{DD} = 3.0 V	$I_{V_{DDSTBY}}$	–	–	1.0	
Operating Power Supply Current (Note 12)	I_C				μA
V_{DD} = 3.0 V		–	40	100	
Logic Input Function					
High-Level Input Voltage	V_{IH}	V_{DD} 0.7	–	–	V
Low-Level Input Voltage	V_{IL}	–	–	V_{DD} 0.3	V
High-Level Input Current	I_{IH}	–	–	1.0	μA
Low-Level Input Current	I_{IL}	-1.0	–	–	μA
PSAVE Terminal Low Level Input Current (Note 13)	I_{IL}	–	-30	-60	μA
Driver Output ON Resistance (Note 14)	$R_{DS(ON)}$	–	1.0	1.5	Ω
Low-Voltage Shutdown Detection Voltage (Note 15)	V_{DD}DET	1.5	2.0	2.5	V

Notes

11. Power SAVE mode.
12. I_C is the sum of the current of V_{DD} monitor block “Low Voltage Detection Module” and the PSAVE pull-up resistor at f_{IN} = 200 kHz.
13. V_{DD} = 3.0 V.
14. I_O = 375 mA. $R_{DS(ON)}$ = R_{SOURCE} + R_{SINK}. R_L = 6.8 Ω.
15. Detection voltage is defined as when the output becomes high impedance after V_{DD} voltage falls and when V_M = 5.5 V.

DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions T_A = 25°C, V_{DD} = V_M = 3.0 V, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT					
Pulse Input Frequency	f_{IN}	–	–	200	kHz
Input Pulse Rise Time (Note 16)	t_R	–	–	1.0 (Note 17)	μs
Input Pulse Fall Time (Note 18)	t_F	–	–	1.0 (Note 17)	μs
OUTPUT					
Output Propagation Delay Time (Note 19)					μs
Turn-ON Time	t_{PLH}	–	0.2	0.5	
Turn-OFF Time	t_{PHL}	–	0.1	0.5	
Low-Voltage Detection Time	$t_{V_{DD}DET}$	–	0.02	1.0	ms

Notes

16. Time is defined between 10% and 90%.
17. That is, the input waveform slope must be steeper than this.
18. Time is defined between 90% and 10%.
19. R_L = 6.8 Ω. Slew time, rise time, and fall times are between 10% and 90% of output low and high levels with respect to the 50% level of the input.

Timing Diagrams

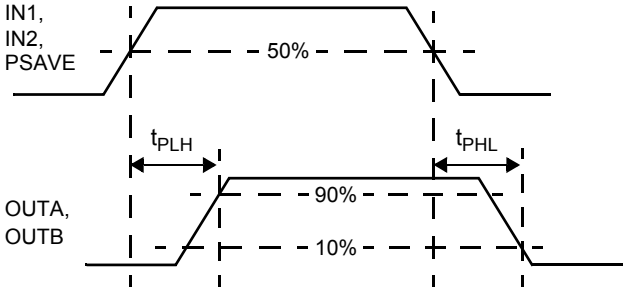


Figure 2. t_{PLH} and t_{PHL} Timing

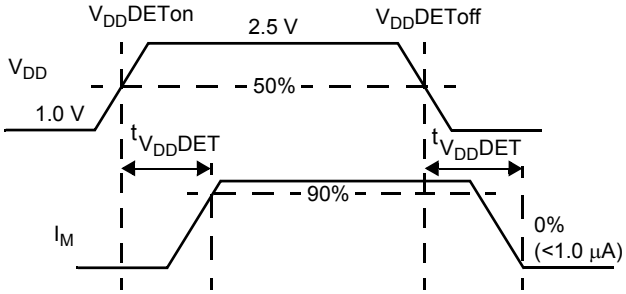


Figure 3. Low-Voltage Detection Timing

Table 1. Truth Table

INPUT			OUTPUT		V_{DD}DET (Note 21)
PSAVE (Note 20)	**IN1A IN2A**	**IN1B IN2B**	**OUT1A OUT2A**	**OUT1B OUT2B**	
L	L	L	L	L	Enabled
L	H	L	H	L	Enabled
L	L	H	L	H	Enabled
L	H	H	Z	Z	Enabled
H	X	X	Z	Z	Disabled

H : High
L : Low
Z : High impedance
X : Don't care

Notes
20. Terminal 13 (PSAVE) is pulled up by an internal resistor.
21. When V_{DD} is lower than V_{DD}DET while V_M is applied, output becomes "Z" (high impedance); however, when PSAVE = "H", the low-voltage shutdown detection circuit is disabled.

SYSTEM/APPLICATION INFORMATION

INTRODUCTION

The 17C724 is a monolithic dual H-Bridge that is ideal in portable electronic applications to control bipolar step motors and brush DC motors such as those used in camera lens and shutters. The 17C724 can operate efficiently with supply voltages as low as 2.7 V to as high as 5.5 V, and provide continuous motor drive currents of 0.4 A while handling peak currents up to 0.8 A. It is easily interfaced to low-cost MCUs via parallel 3.0 V- or 5.0 V-compatible logic. The device can be pulse width modulated (PWM'ed) at up to 200 kHz.

The 17C724 can drive two motors simultaneously (see Figure 4, page 9), or it can drive one bipolar step motor as shown in the simplified application diagram on page 1. Dual channel parallel drive is also possible if higher current drive is desired (0.8 A). Two-motor operation is accomplished by hooking one motor between OUT1A and OUT1B, and the other motor between OUT2A and OUT2B.

This IC has a built-in shoot-through current protection circuit and undervoltage detector to avoid malfunction. It also allows for power-conserving Sleep mode by the setting of the PSAVE terminal (refer to Table 1, Truth Table, page 7).

The device features four operating modes: Forward, Reverse, Brake, and Tri-Stated (High Impedance).

FUNCTIONAL TERMINAL DESCRIPTION

V_{DD}

The V_{DD} terminal carries the power source connection to the control (logic) circuit, and its input range is between 2.7 V to 5.5 V (3.0 V and 5.0 V compatible). V_{DD} has an undervoltage threshold. If the supply voltage to V_{DD} drops below 2.0 V (typical), then all the output of H-Bridges (OUT1A, OUT1B, OUT2A, OUT2B) will become open (high impedance = Z). When the supply voltage returns to a level that is above the threshold voltage the H-Bridge outputs automatically resume normal operation according to the established condition of the input terminals.

IN1A, IN1B, IN2A, and IN2B

These logic input terminals control each H-Bridge output. For example, IN1A logic HIGH = OUT1A HIGH; likewise, IN1B logic HIGH = OUT1B HIGH. If both A and B inputs are HIGH, then both A and B outputs are Z (refer to Table 1, Truth Table, page 7).

PSAVE

The PSAVE input controls the functioning of the power output stages (the H-Bridges). When it is set logic LOW, the output stages are enabled and the H-Bridges function normally. When it is set logic HIGH, the output stages are disabled and all the outputs are opened (high impedance). In this mode, the built-in low-voltage detection circuit is disabled.

OUT1A, OUT1B, OUT2A, and OUT2B

These terminals are the outputs of the power MOSFET H-Bridges. OUT1 is from H-Bridge Channel 1, and OUT2 from H-Bridge Channel 2. These terminals will typically connect to an external load (step motor or brush DC motors).

VM1 and VM2

VM1 and VM2 carries the main supply voltage and current into the power sections (the H-Bridges) of the IC. Both of these terminals are connected internally but they must be connected together on the printed circuit board with as short as possible traces. The input range is 2.7 V to 5.5 V.

PGND1 and PGND2

These two are the power ground terminals that connect to the power ground of the H-Bridges. The power grounds are for higher current handling capability from loads and they must be connected together on the PCB.

LGND

LGND is the logic ground terminal and its current handling level is lower than the PGND.

APPLICATIONS

Figure 4 shows a typical application for the 17C724.

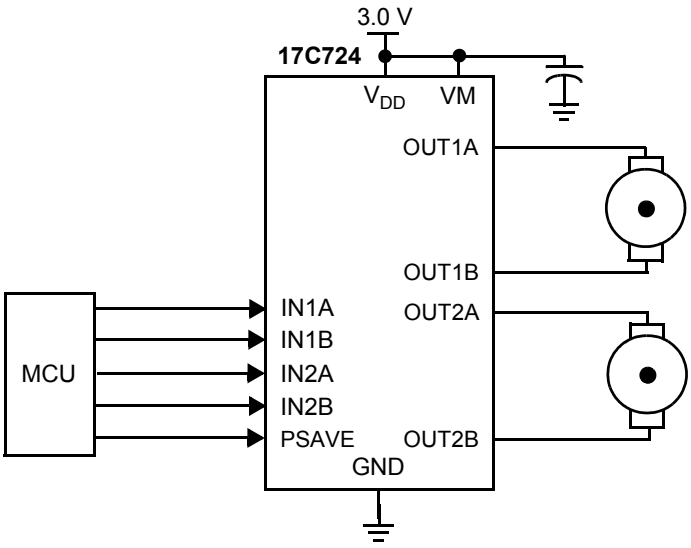


Figure 4. 17C724 Typical Application Diagram

CEMF Snubbing Techniques

Care must be taken to protect the IC from potentially damaging CEMF spikes induced when commutating currents in inductive loads. Typical practice is to provide snubbing of voltage transients by placing a zener or capacitor at the supply terminal (VM) (see Figure 5).

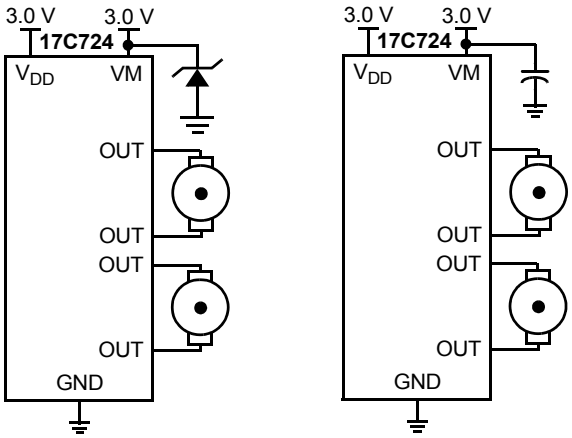


Figure 5. CEMF Snubbing Techniques

PCB Layout

When designing the printed circuit board (PCB), connect sufficient capacitance between power supply and ground terminals to ensure proper filtering from transients. For all high-current paths, use wide copper traces and shortest possible distance.

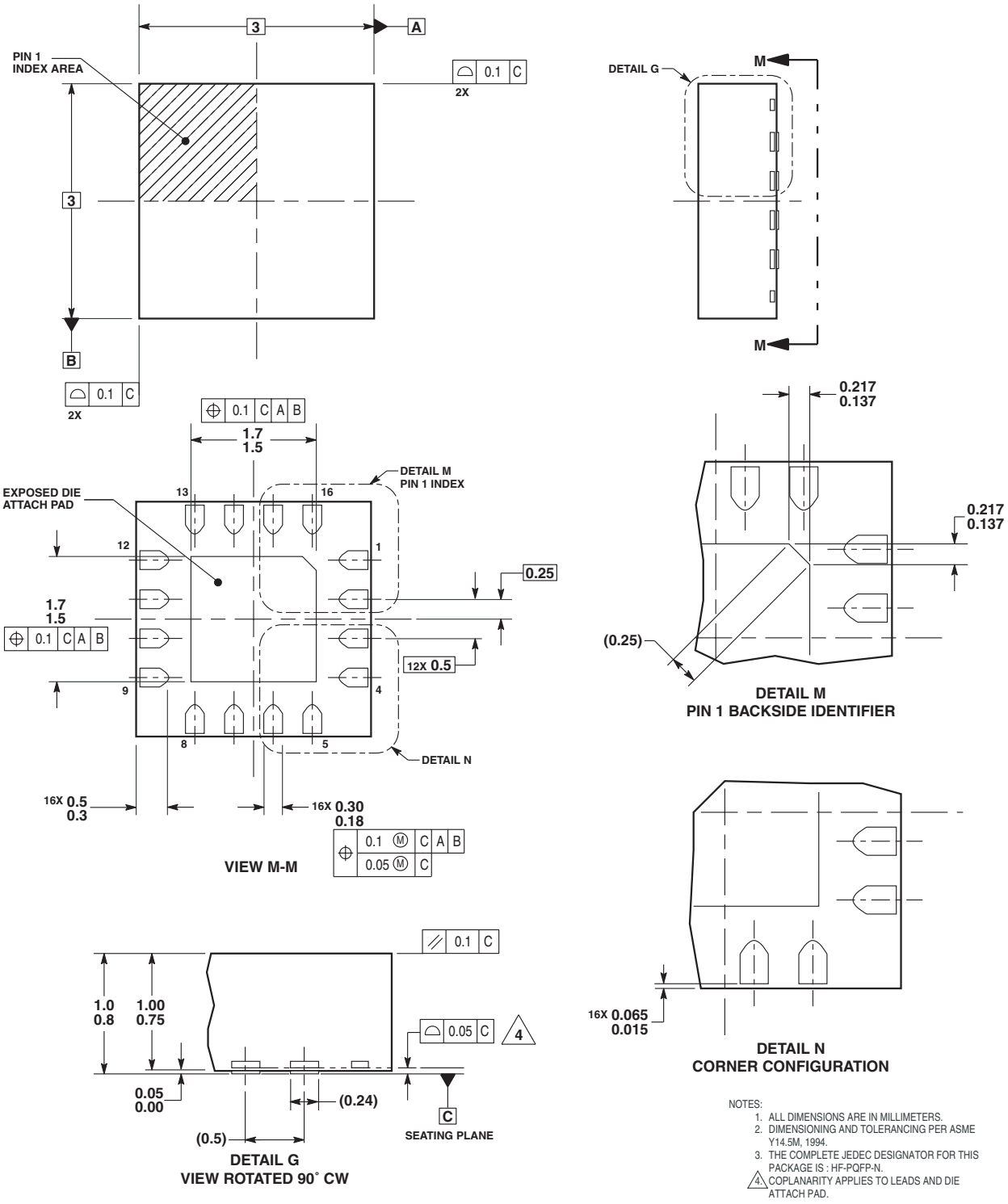
Application Notes

Although VM1 and VM2 are connected internally, they must be connected externally to attain sufficient power distribution.

Take precautions to guard against electrostatic discharge when handling the device, especially when mounting and demounting the device to a PCB.

PACKAGE DIMENSIONS

EP (Pb-FREE) SUFFIX
16-LEAD QFN
NON-LEADED PACKAGE
CASE 1524-01
ISSUE O



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