EPL20F series

CMOS ELECTRICALLY PROGRAMMABLE LOGIC

EPL20F is a programmable logic array of AND-(fixed) OR-register configuration (I/O delay time: 15 ns).

The user can program the device simply by writing to the EPROM cell assigned on the array. This shortens the development period greatly and simplifies circuit correction.

■ FEATURES

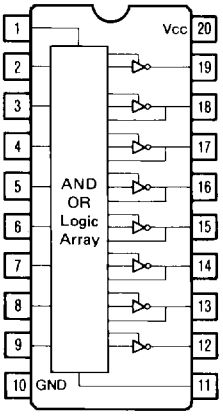
- Low power consumption and high reliability based on CMOS-EPROM process
- Ceramic package products can be erased with ultraviolet light.
- 66 product terms
- Replaceable with general-purpose logic
- Output polarity programmed for each pin
- Asynchronous programmable reset
- Data copy prevention
- I/O propagation delay time : 15 ns (max.)
- Package : 20-pin 300 mil Plastic DIP
  20-pin 300 mil CERDIP (with window)
  20-pin PLCC
  20-pin SOP

■ EPL20F Series

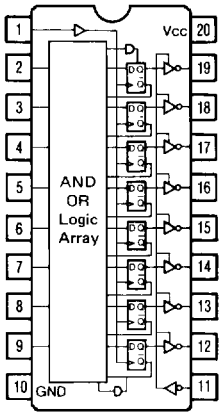
Package	Molded DIP	CERDIP (with window)	PLCC	SOP
EPL20F series	EPL16P8FP EPL16RP8FP EPL16RP6FP EPL16RP4FP	EPL16P8FD EPL16RP8FD EPL16RP6FD EPL16RP4FD	EPL16P8FJ EPL16RP8FJ EPL16RP6FJ EPL16RP4FJ	EPL16P8FS EPL16RP8FS EPL16RP6FS EPL16RP4FS

■ PIN CONFIGURATION

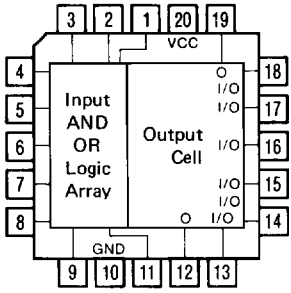
EPL16P8FP
EPL16P8FD
EPL16P8FS



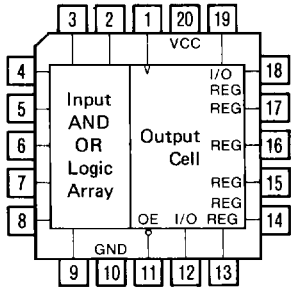
EPL16RP8FP
EPL16RP8FD
EPL16RP8FS



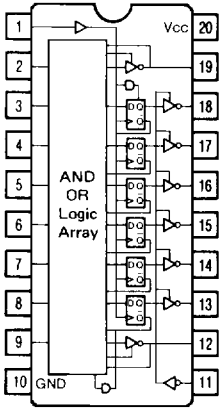
EPL16P8FJ



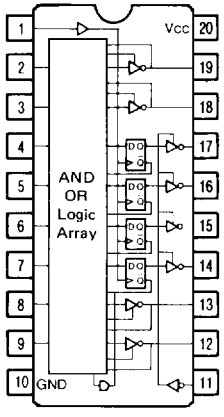
EPL16RP6FJ



EPL16RP6FP
EPL16RP6FD
EPL16RP6FS



EPL16RP4FP
EPL16RP4FD
EPL16RP4FS



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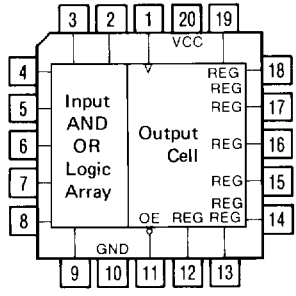
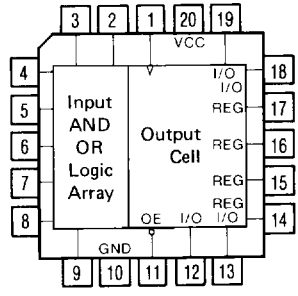


EPL16RP4FJ



■ PIN DISCRIPTION

Pin No.	Pin Name	Function	
	Logic Mode	Logic Mode	
1	CLK/I1		Clock
2	I2		
3	I3	Input	
4	I4		
5	I5		
6	I6		
7	I7		
8	I8		
9	I9		
10	GND	GND	
11	$\overline{OE}$/I10	Output Enable/Input	
12	I/01		
13	I/02		
14	I/03		
15	I/04	Input/Output	
16	I/05		
17	I/06		
18	I/07		
19	I/08		
20	Vcc	Vcc	

■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Rating	Unit
Vcc	Vcc Power Supply	With respect to GND	-0.3 ~ 7.0	V
Vpp	Vpp Power Supply		-0.3 ~ 14.5	V
Vi	Input Voltage		-0.3 ~ Vcc+0.3	V
Vo	Output Voltage		-0.3 ~ Vcc+0.3	V
Pd	Max. Power Consumption	Ta=25°C	0.8	W
Topr	Operating Ambient Temperature		0 ~ 70	°C
Tstg	Storage Temperature		-40 ~ 125	°C

■ RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Power Supply	4.75	5.0	5.25	V
V_{IH}	"H" Input Voltage	2.0		Vcc+0.3	V
V_{IL}	"L" Input Voltage	-0.3		0.8	V

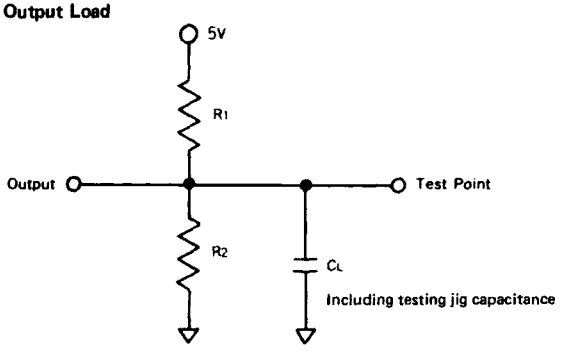
■ DC CHARACTERISTICS (Ta=0~70°C, Vcc=5V±5%)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{IN}=0V~Vcc	-10		10	μA
I_{LO}	Output Leakage Current for OFF state	Vo =0V~Vcc	-10		10	μA
V_{IL}	"L" Input Voltage		-0.3		0.8	V
V_{IH}	"H" Input Voltage		2.0		Vcc+0.3	V
V_{OL}	"L" Output Voltage	Vcc=MIN, I_{OL}=24mA			0.5	V
V_{OH}	"H" Output Voltage	Vcc=MIN, I_{OH}=-3.2mA	2.4			V
Icc1	Power Supply Current (Standby)	Vcc=MAX, V_{IN}=GND or Vcc, f=0Hz			60	mA
Icc2	Power Supply Current (Operation)	Vcc=MAX, V_{IN}=GND or Vcc, f=15MHz			70	mA

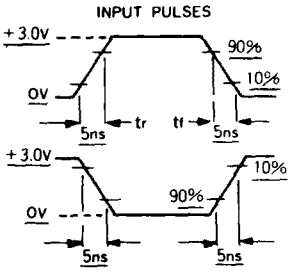
■ AC CHARACTERISTICS

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
	Clock	Parameters					
t_{PD}		Input or I/O input to non-registered output				15	ns
t_{PIX}		Input or I/O input to output disable				15	ns
t_{PIZ}		Input or I/O input to output enable				15	ns
t_{PXZ}		$\overline{OE}$ (pin 11) to output disable	C_L=50pF			15	ns
t_{PZX}		$\overline{OE}$ (pin 11) to output enable	R1=200Ω			15	ns
t_{SU}	External Clock	Input or I/O input setup time	R2=390Ω	12			ns
t_H		Input or I/O input hold time		0			ns
t_{CLK}		Clock to output delay				12	ns
t_{FPD}	CLK (1 pin)	Clock to non-registered output from registered feed back				24	ns
t_W		Clock width		10			ns
t_{RST}		Input or I/O input to asynchronous reset				15	ns
t_P1		Minimum clock period (t_{SU} + t_{CLK})				24	ns
f1		Maximum frequency ($1/t_P1$)		41.6			MHz
t_{PON}		Power On Reset Time		45			μs

● **Output Load**

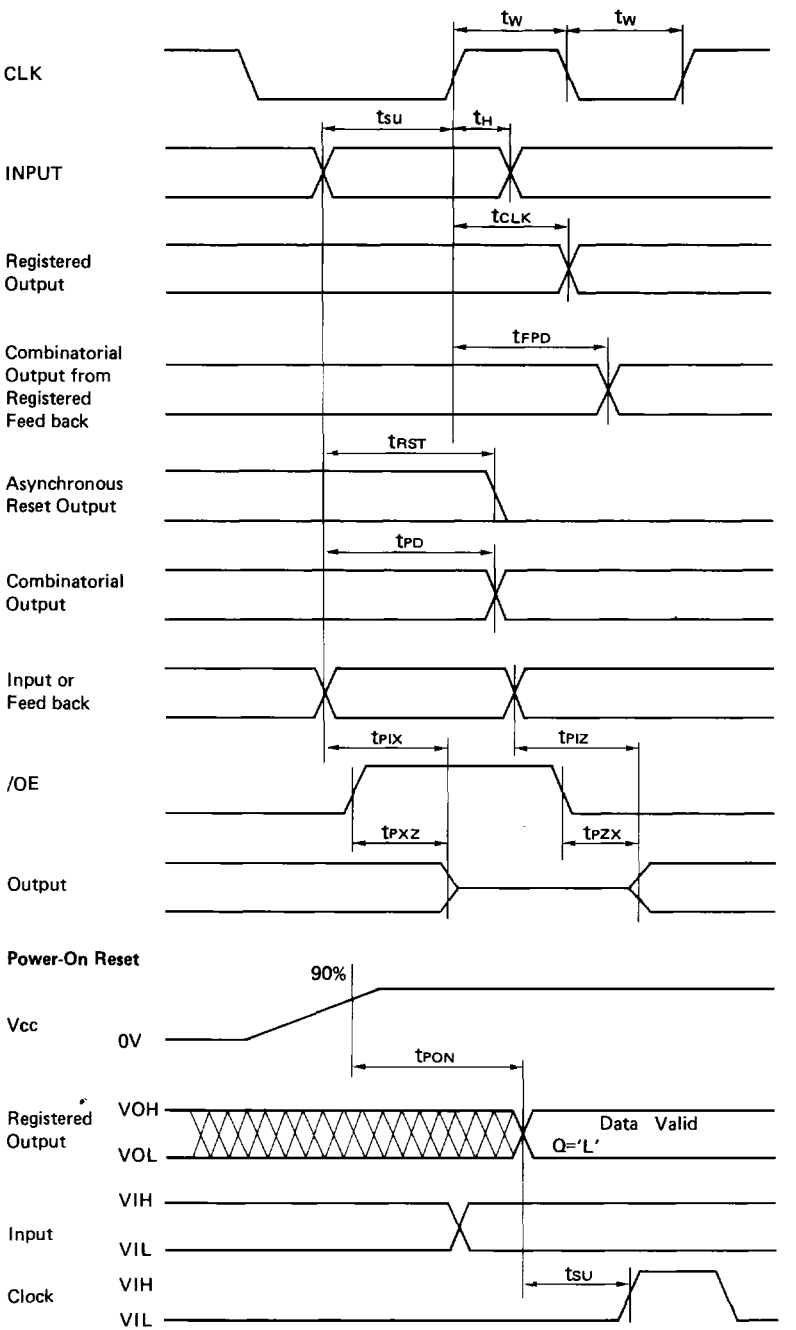


● **Input Waveform**



Note) AC characteristics are measured at voltage of 1.5V on both input and output.

■ TIMING CHART



■ DESCRIPTION

- **Logic Function** (logic mode)

EPL20F is an erasable, writable logic array that uses CMOS EPROM and has 32 input terms and 66 product terms.

All I/O pins perform normal logical operation at the TTL level. Register usage and output polarities can be selected by using the I/O macro cell.

All crosspoints on the AND array (crosspoints of product terms and input terms) have an EPROM cell connection. Upon initial delivery, all crosspoints are connected.

As illustrated in Fig.1, if both positive input (I) and negative input ($\overline{I}$) are not written to, the AND output (P1) is inactive. If both positive input (I) and negative input ($\overline{I}$) are written to, the AND output (P2) is logically "Don't Care".

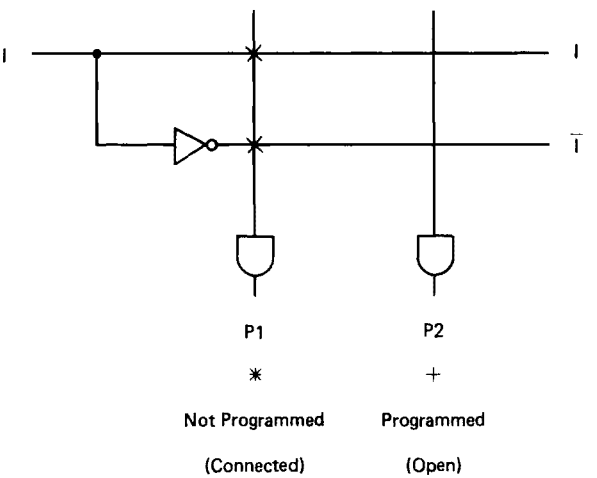


Fig. 1

- **Option Bit**

  (a) Polarity Bit

  Polarity can be selected for each output pin (pins 12 to 19). By default, the polarity is Active Low. Programming the polarity bit makes the polarity Active High.

  (b) Power Control Bit

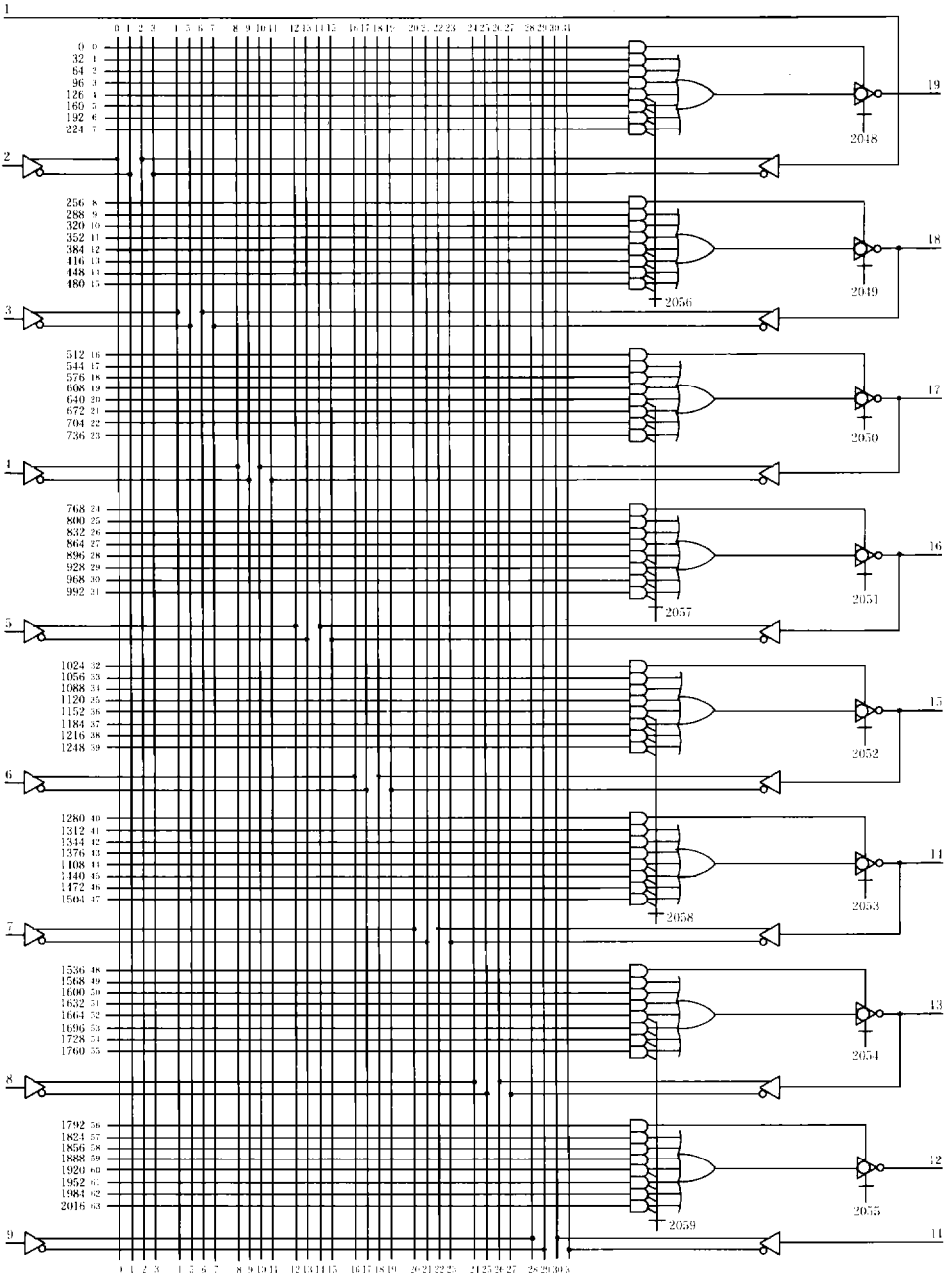
  EPL20F has eight product terms per output.
  Four product terms are controlled by the power control bit.
  By default, four product terms operate per output. Programming the power control bit allows eight product terms to operate.
  Thus, disabling unnecessary product terms reduces power consumption. The power control bit is controlled for two pins simultaneously (pins 19 and 18, 17 and 16, 15 and 14, and 13 and 12).

  (c) Security Bit

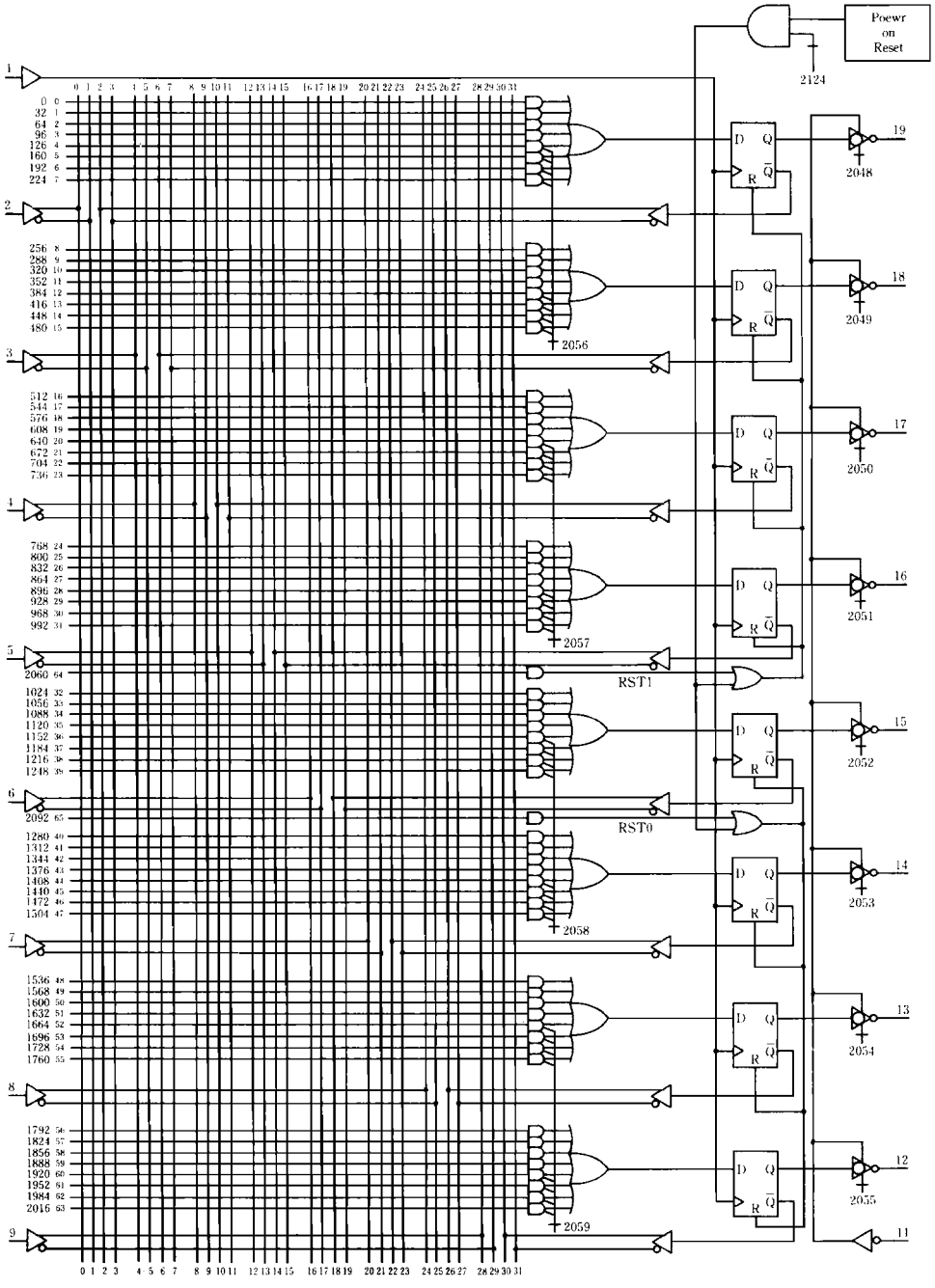
  This function inhibits reading (verifying) the programmed contents.
  Programming the security bit inhibits verification.

■ LOGIC DIAGRAM

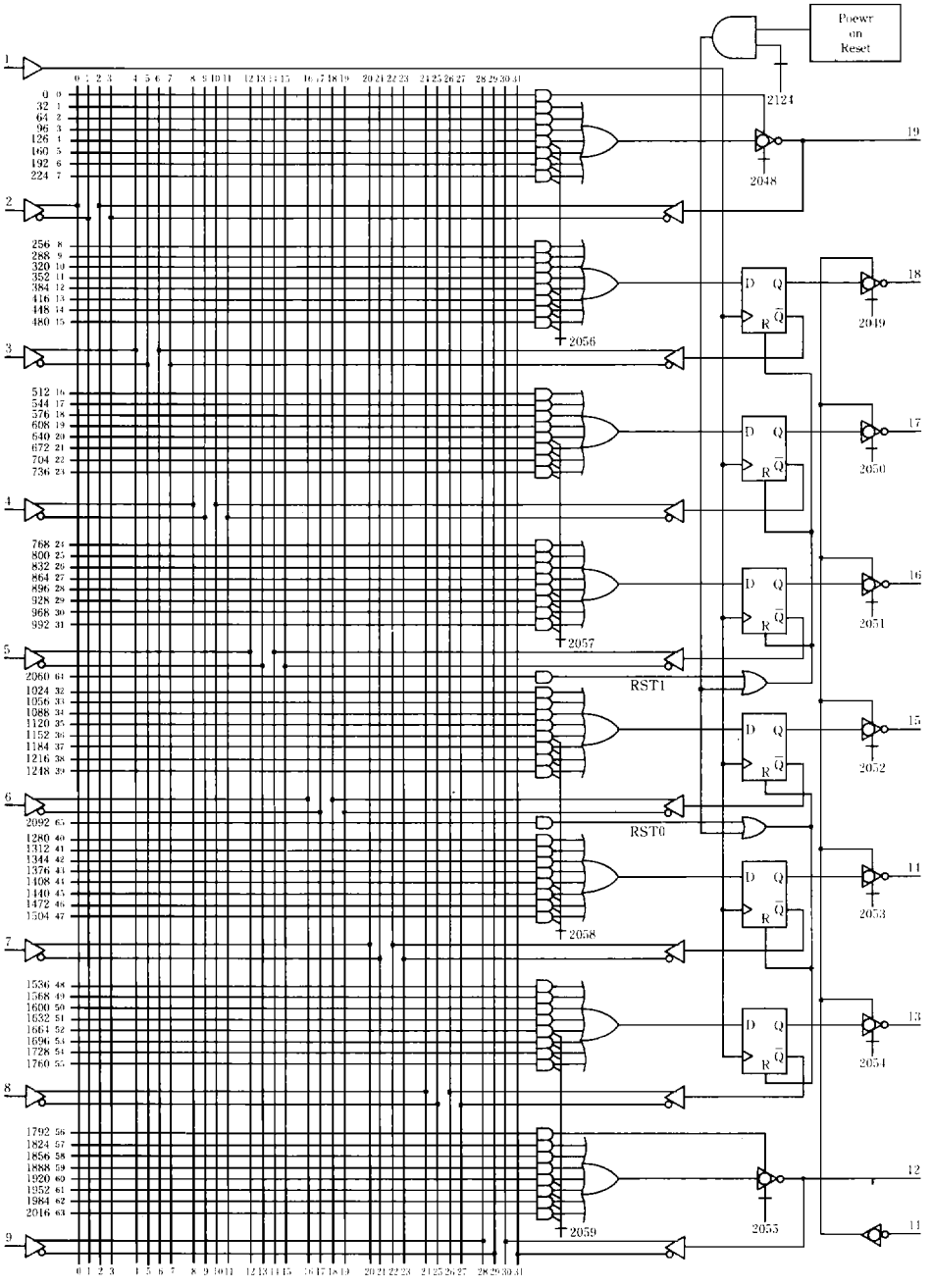
●EPL16P8F



●EPL16RP8F


Poewr on Reset
2124
2048
2049
2050
2051
2052
2053
2054
2055
2056
2057
2058
2059
2060
2092
RST1
RST0
D
Q
R

●EPL16RP6F


Poewr on Reset
2124
2048
2056
2057
2058
2059
2055
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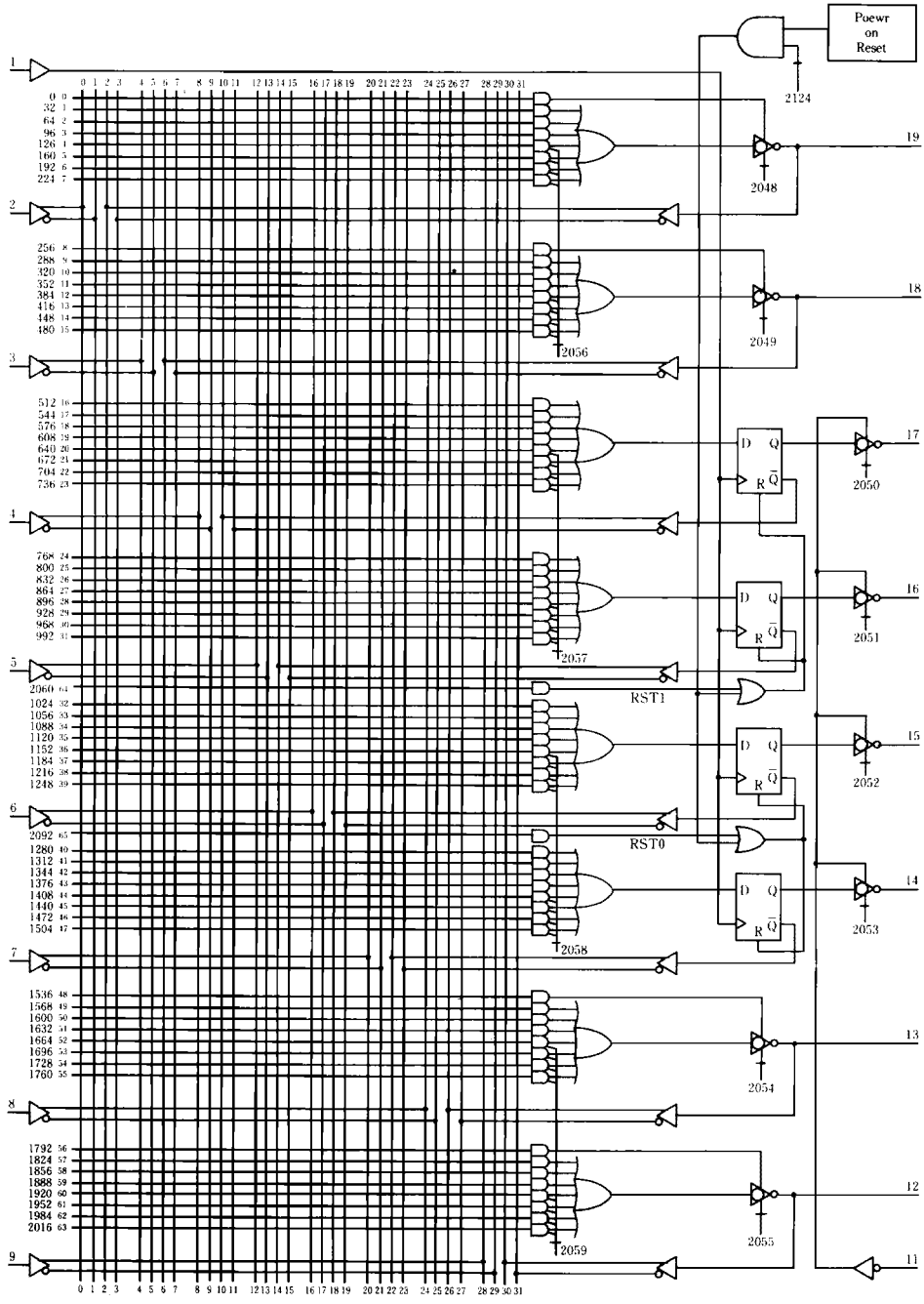
2050
2051
2052
2053
2054
RST1
RST0
D
Q
R

●EPL16RP4F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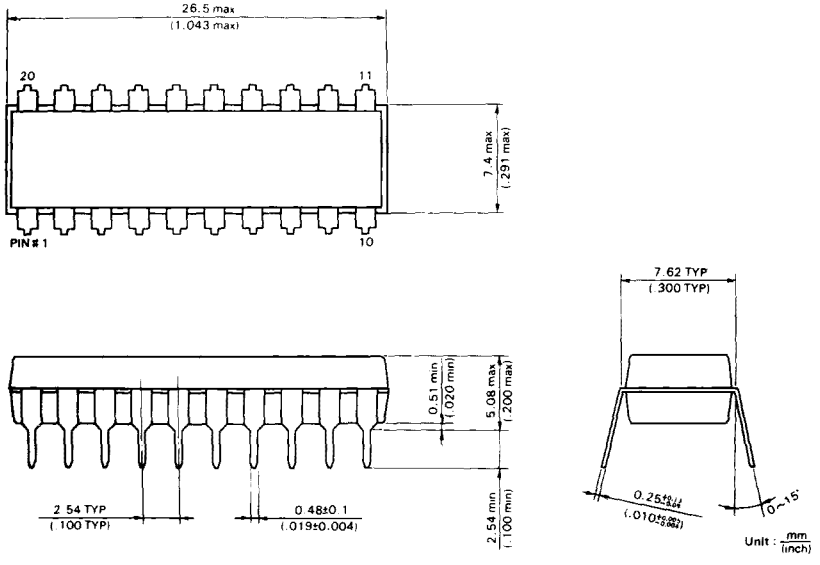
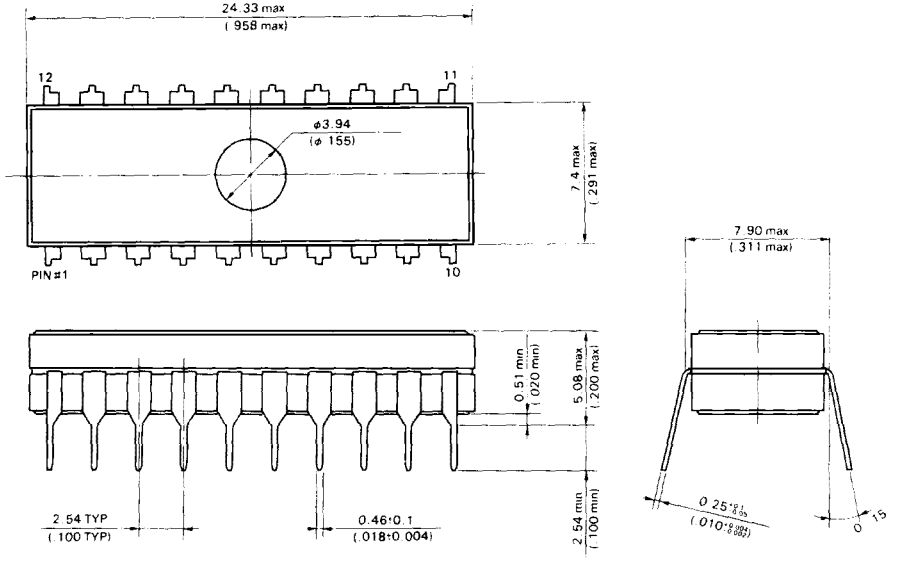
2059
2055
19
18
17
16
15
14
13
12
11
D
Q
R

■ PACKAGE DIMENSION (Unit : mm/inch)

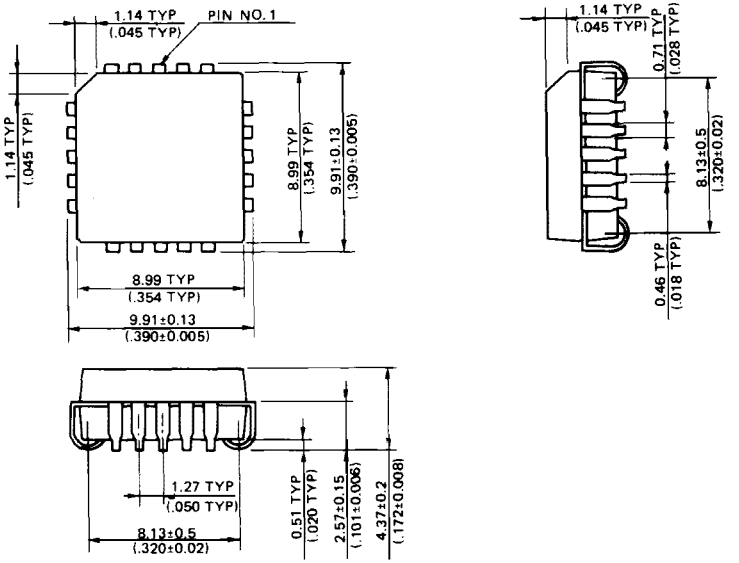
●EPL16P8FP、EPL16RP8FP、EPL16RP6FP、EPL16RP4FP (20 pin Plastic DIP)



●EPL16P8FD、EPL16RP8FD、EPL16RP6FD、EPL16RP4FD (20 pin CERDIP with window)



●EPL16P8FJ、EPL16RP8FJ、EPL16RP6FJ、EPL16RP4FJ
(20 pin PLCC)



●EPL16P8FS、EPL16RP8FS、EPL16RP6FS、EPL16RP4FS
(20 pin SOP)