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To ;

TENTATIVE

SPECIFICATIONS

Product Type 160 Output LCD Common Driver

Model No. LH153D

※This tentative specifications contains 17 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

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- ·Medical equipment related to life support, etc.

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●Please direct all queries regarding the products covered herein to a sales representative of the company.

Contents

1. Summary

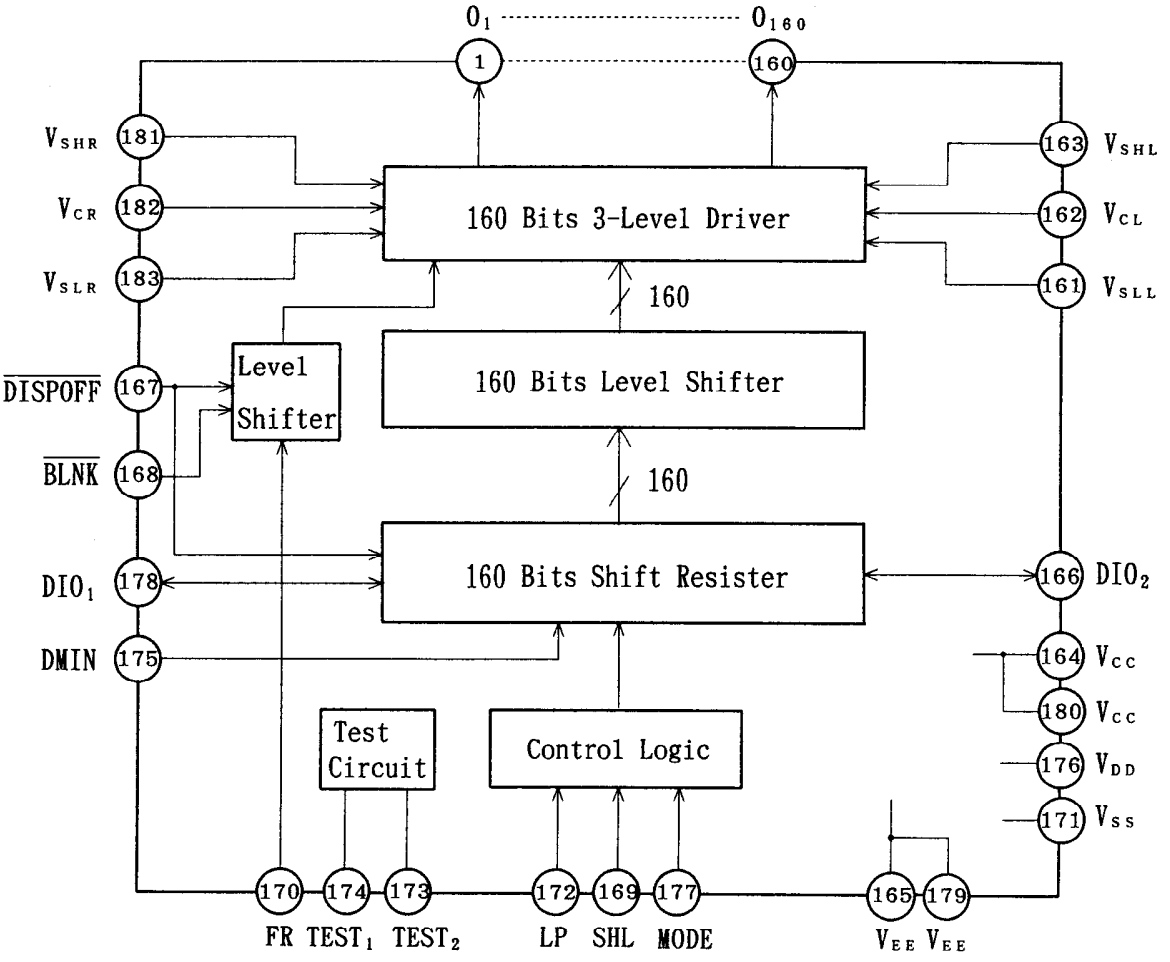
The LH153D is a 160 output common driver LSI suitable for driving large scale dot matrix LC panels using as low voltage segment driving method. Through the use of SST (Super Slim TCP) technology, it is ideal for substantially decreasing the size of the frame section of the LC module. When combined with the Segment Driver LH155E(SST) and Power-Supply IC LR3694 and LR3696 power supply ICs, it is possible to constitute a low power consumption LCD module.

2. Features

- Supply voltage for LC drive : +20.0 to +45.0 V
- Number of LC drive outputs : 160
- Level of LC drive outputs : 3
- Correspond to low voltage segment driving method
- Controllable input signal from directly Controller
- Low power consumption
- Supply voltage for the logic system : +2.4 to +5.5 V
- Low output impedance : 600 Ω(Typ.)
- Shift clock frequency : 4.0 MHz (Max.) (V_{DD}=+4.5 to +5.5 V)
  : 3.0 MHz (Max.) (V_{DD}=+2.4 to +4.5 V)
- Built-in 160-bits bidirectional shift register(divisible into 80-bits x2)
- Shift register circuit reset function when $\overline{DISPOFF}$ active
- Available in a single mode(160-bits shift register) or in a dual mode (80-bits shift register x2)
  - ① $O_1 \rightarrow O_{160}$ Single mode
  - ② $O_{160} \rightarrow O_1$ Single mode
  - ③ $O_1 \rightarrow O_{80}$, $O_{81} \rightarrow O_{160}$ Dual mode
  - ④ $O_{160} \rightarrow O_{81}$, $O_{80} \rightarrow O_1$ Dual mode

  Shift direction that mentioned above is pin-selectable.
- CMOS silicon gate process(P-type Silicon Substrate)
- Supports high capacity LC panel display when combined with the LH155E Segment Driver
- Package : 183 pin TCP (Tape Carrier Package)
- Not designed or rated as radiation hardened

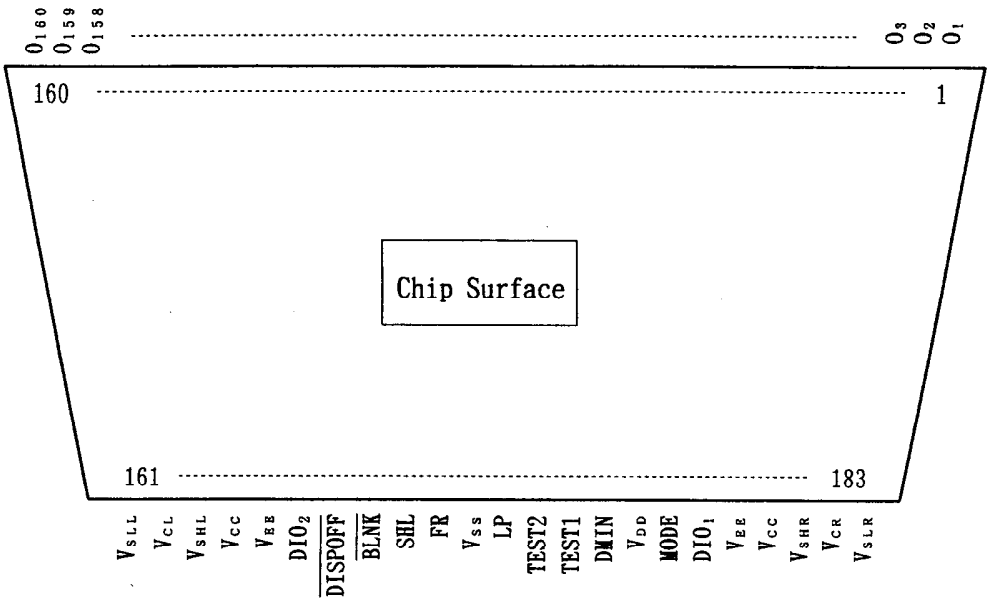
3. Block Diagram



4. Functional Operation of Each Block

Block	Function
Shift Register	Shifts data from the data input pin on the falling edge of the LP signal, based on the data shift direction received from the control logic block.
Level Shifter	The logic voltage signal is level-shifted to the LC drive voltage level, and outputs to the driver block.
3-Level Driver	Drives the LC driver output pins from the shift register data, selecting one of 3 levels (V_{SH}, V_C, V_{SL}) based on the FR, and $\overline{DISPOFF}$ signals.
Control Logic	Controls the shift register's direction of data shift in response to a SHL signal input.
Test Circuit	Test circuit is for the test. In general usage, it doesn't act.

5. Pin Configuration

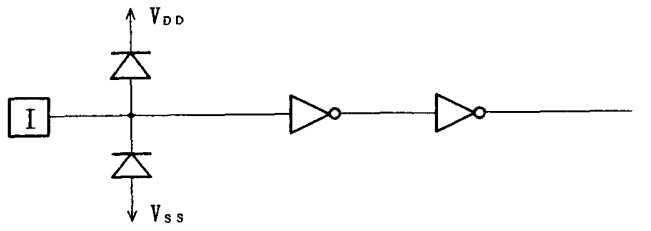


6. Pin Descriptions

6-1. Pin Designations

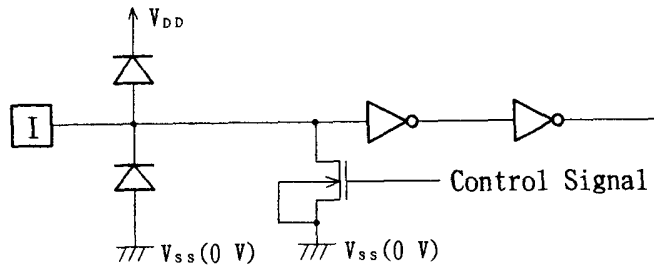
Pin No.	Symbol	I/O	Designation
1 ~ 160	O_1 ~O_{160}	O	LC drive output
161,183	V_{SLL},V_{SLR}	-	Power supply for LC drive
162,182	V_{CL},V_{CR}	-	Power supply for LC drive
163,181	V_{SHL},V_{SHR}	-	Power supply for LC drive
164,180	V_{CC}	-	Power supply for LC drive
165,179	V_{EE}	-	Power supply for LC drive
166	DIO_2	I/O	Data input/output for shift resister
167	$\overline{DISPOFF}$	I	Control input for unselect output level
168	$\overline{BLNK}$	I	Control input for blanking period
169	SHL	I	Shift direction selection for shift register
170	FR	I	AC-converting signal input for LC drive waveform
171	V_{SS}	-	Power supply for logic system(0 V)
172	LP	I	Shift clock input for shift register
173	$TEST_2$	I	Test mode selection input
174	$TEST_1$	I	Test mode selection input
175	DMIN	I	Dual mode data input
176	V_{DD}	-	Power supply for logic system(+2.4 to +5.5 V)
177	MODE	I	Mode selection input
178	DIO_1	I/O	Data input/output for shift register

6-2. Input/Output Circuits



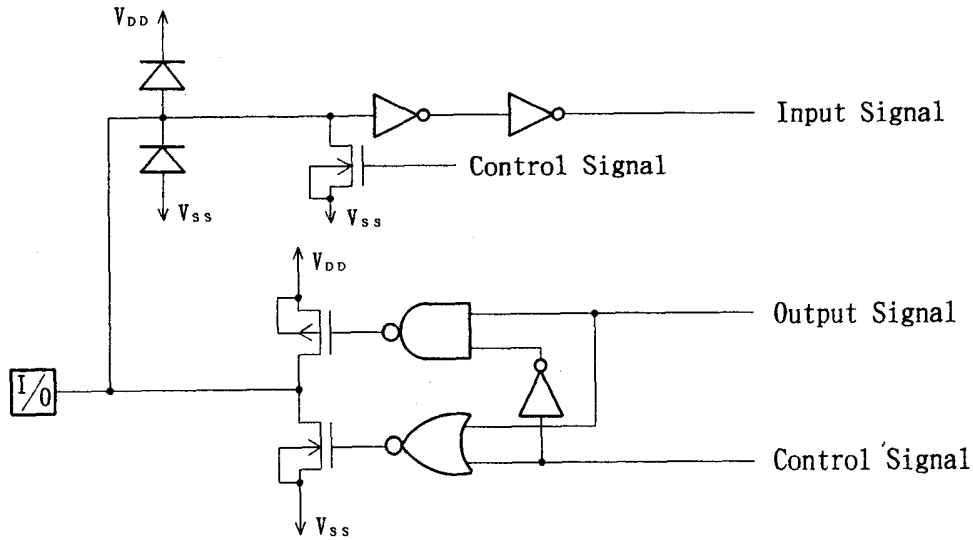
【Applicable pins】
SHL, MODE, $\overline{DISPOFF}$
BLNK, FR, LP

Fig.1 Input Circuit(1)



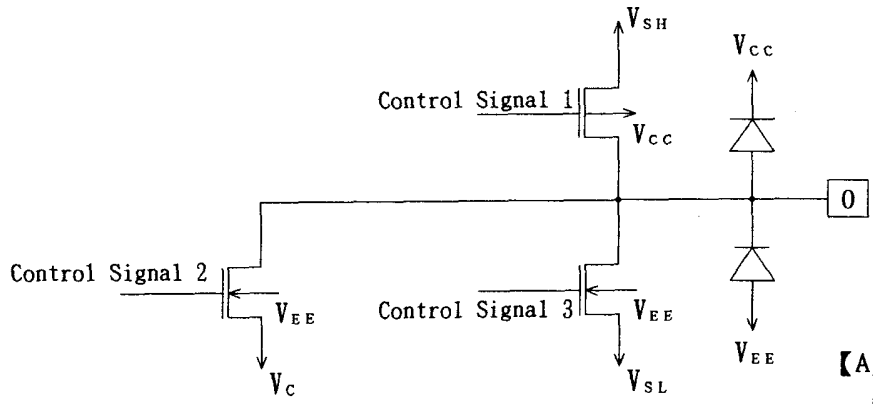
【Applicable pins】
DMIN

Fig.2 Input Circuit(2)



【Applicable pins】
DIO_1, DIO_2

Fig.3 Input/Output Circuit



【Applicable pins】
O_1-O_{160}

Fig.4 LC Drive Output Circuit

7. Description of Functional Operations

7-1. Pin Functions

Symbol	Function
V_{DD}	Logic system power supply pin connects to +2.4 to +5.5 V
V_{SS}	Logic system power supply pin connects to 0 V
V_{EE}	Power supply pin for LC drive
V_{CC}	Power supply pin for LC drive
V_{SHL}, V_{SHR} V_{CL}, V_{CR} V_{SLL}, V_{SLR}	Power supply pin for LC driver voltage bias. •Normally, the bias voltage used is set by a resistor divider. •Ensure that voltages are set such that $V_{EE} \leqq V_{SL} < V_C < V_{SH} \leqq V_{CC}$ •To further reduce the difference between the output waveforms of LC driver output pins O_1 and O_{160}, externally connect V_{iR} and V_{iL} (i=SH,C,SL).
DIO_1	Bidirectional shift register shift data input/output pin •Input pin for right shift, output pin for left shift. When DIO_1 is used as input pin for right shift, it will be pull-down. When DIO_1 is used as output pin for left shift, it won't be pull-down.
DIO_2	Bidirectional shift register shift data input/output pin •Input pin for left shift, output pin for right shift. When DIO_2 is used as input pin for left shift, it will be pull-down. When DIO_2 is used as output pin for right shift, it won't be pull-down.
LP	Bidirectional shift register shift clock pulse input pin •Data is shifted on the falling edge of the clock pulse.
SHL	Bidirectional shift register shift direction selection pin •Data is shifted $O_1 \rightarrow O_{160}$ when set to V_{SS} level "L", and data is shifted $O_{160} \rightarrow O_1$ when set to V_{DD} level "H".
$\overline{DISPOFF}$	Control input pin for output deselect level •The input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit. •When set to V_{SS} level "L", the LC drive output pins (O_1-O_{160}) are set to level V_C. •While set to "L", the contents of the shift register are reset not reading data. When the $\overline{DISPOFF}$ function is canceled, the driver outputs deselect level (V_C), and the shift data is reading on the falling edge of the LP. That time, if $\overline{DISPOFF}$ removal time can not keep regulation what is shown AC characteristics (Page 11), the shift data is not reading correctly.
$\overline{BLNK}$	Control input pin for blanking period •This input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit. •When BLNK=L, blanking period mode is selected, the LC drive output pins(O_1-O_{160}) are set V_C level. At this time, shift registers are active(not reset).

Symbol	Function
MODE	Mode select pin •When set V_{SS} level "L", Single Mode operation is selected, when set to V_{DD} level "H", Dual Mode operation is selected.
DMIN	Dual Mode data input pin •According to the data shift direction of the data shift register, data can be input starting from the 81st bit. When the chip is used as Dual Mode, DMIN will be pull-down. When the chip is used as Single Mode, DMIN won't be pull-down.
FR	AC conversion signal for output waveform •The input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit. •Generally, input a frame inversion signal. •Output level of this driver is defined by shift register's output (Latch data) and FR signal. •Truth table is shown in 7-2-1.
$TEST_1$ $TEST_2$	Test mode selection pins •During normal operation, please fix V_{SS} level "L".
O_1-O_{160}	LC driver output pins •Corresponding to each bit of the shift register, one level (V_{SH}, V_C, V_{SL})is selected and output.

7-2. Functional Operations

7-2-1. Truth Table

FR	Latch Data	$\overline{DISPOFF}$	$\overline{BLNK}$	Driver Output Voltage Level (O_1-O_{160})
L	L	H	H	V_C
L	H	H	H	V_{SH}
H	L	H	H	V_C
H	H	H	H	V_{SL}
X	X	H	L	V_C
X	X	L	X	V_C

Here, $V_{EE} \leqq V_{SL} < V_C < V_{SH} \leqq V_{CC}$, L:$V_{SS}$(0 V), H:$V_{DD}$(+2.4 V to +5.5 V), x : Don't care

【Note】"Don't care" should be fixed to "H" or "L", avoiding floating.
There are two kinds of power supply (logic level voltage, LC drive voltage) for LCD driver. Please supply regular voltage which assigned by specification for each power pin.

7-2-2. Relationship between the Data I/O Pins and Data Transfer Direction

MODE	SHL	DIO_1	DIO_2	DMIN	Data Transfer Direction
L (Single)	L(shift to right)	Input	Output	X	$O_1 \rightarrow O_{160}$
	H(shift to left)	Output	Input	X	$O_{160} \rightarrow O_1$
H (Dual)	L(shift to right)	Input	Output	Input	$O_1 \rightarrow O_{80}$
					$O_{81} \rightarrow O_{160}$
	H(shift to left)	Output	Input	Input	$O_{160} \rightarrow O_{81}$
					$O_{80} \rightarrow O_1$

Here, L:V_{SS}(0 V), H:V_{DD}(+2.4 V to +5.5 V)

【Note】"Don't care" should be fixed to "H" or "L", avoiding floating.

7-2-3. Connection Examples for Plural Common Drivers

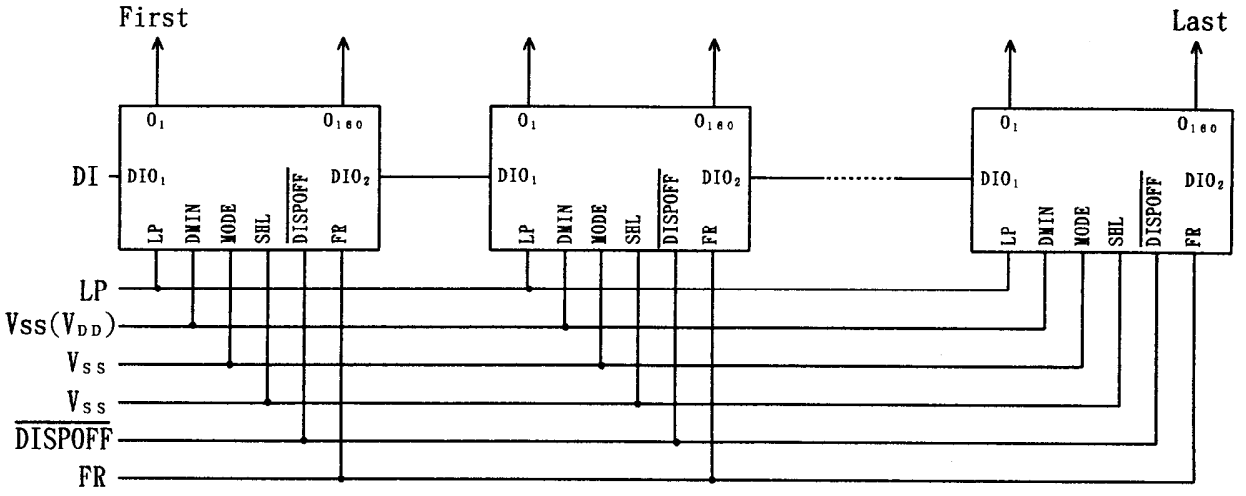


Fig. 1 Single Mode (Shifting toward right)

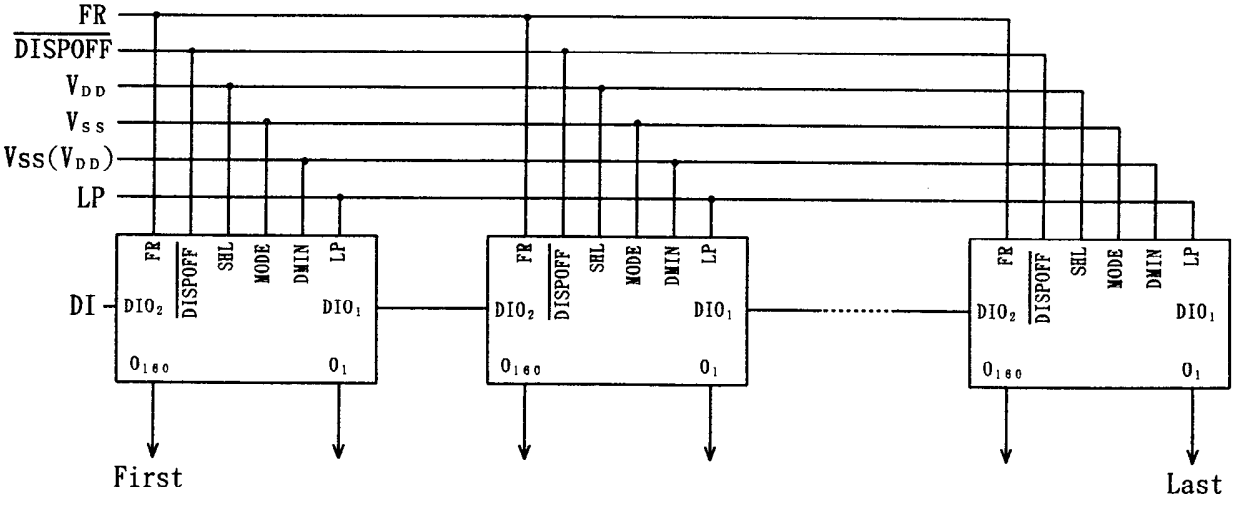


Fig. 2 Single Mode (Shifting toward left)

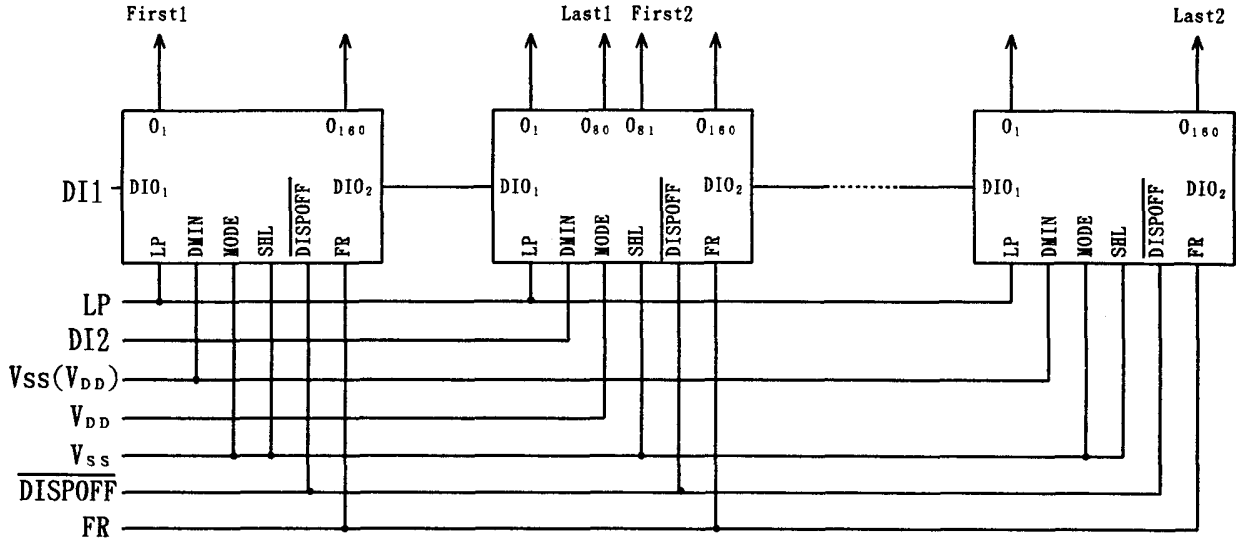


Fig. 3 Dual Mode (Shifting toward right)

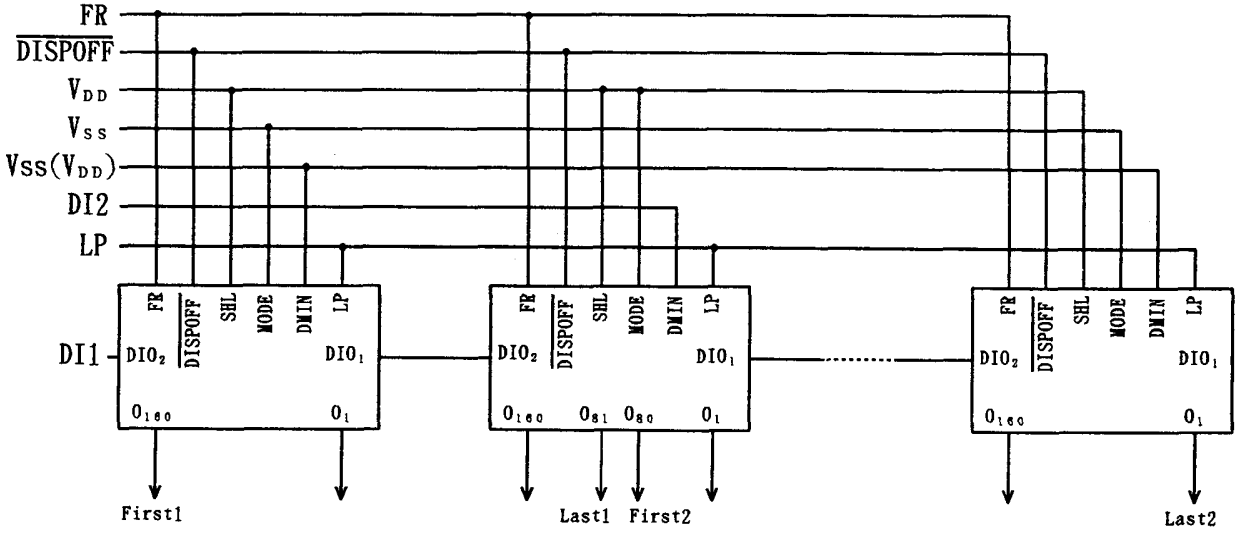


Fig. 4 Dual Mode (Shifting toward left)

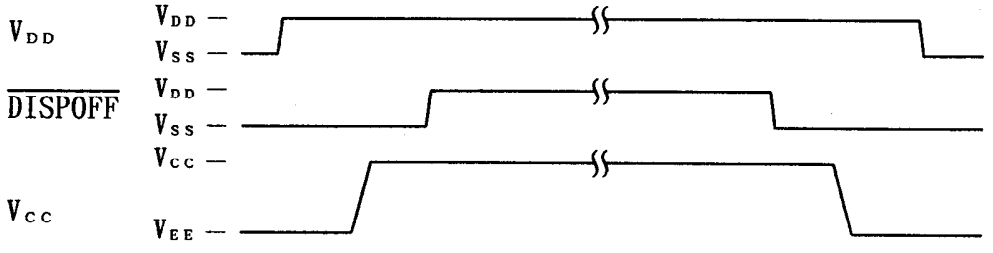
8. Precaution

○Precaution when connecting or disconnecting the power

This LSI has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if a voltage is supplied to the LC drive power supply while the logic system power supply is floating.
The detail is as follows.

- When connecting the power supply, connect the LC drive power after connecting the logic system power. Furthermore, when disconnecting the LC power, disconnect the logic system power after disconnecting the LC drive power.
- We recommend you connecting the serial resistor (50 to 100Ω) or fuse to the drive power V_{CC} of the system as a current limitter. And set up the suitable value of the resistor in consideration of LC display grade.

And when connecting the logic power supply, the logic condition of this LSI inside is insecurity.Therefore connect the LC drive power supply after resetting logic condition of this LSI inside on $\overline{DISPOFF}$ funtion. After that, cancel the $\overline{DISPOFF}$ function after the LC drive power supply has become stable. Furthermore, when disconnecting the power, set the LC drive output pins to level V_C on $\overline{DISPOFF}$ function. After that, disconnect the logic system power after disconnecting the LC drive power.
When connecting the power supply, show the following recommend sequence.



9. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Applicable pins	Ratings	Unit
Supply voltage (1)	V_{DD}	Ta=25 ℃ Referenced to V_{EE}	V_{DD}	V_{EE}-0.3 to V_{EE}+31.0	V
	V_{SS}		V_{SS}	V_{EE}-0.3 to V_{EE}+31.0	V
	V_{DD}-V_{SS}		V_{DD}, V_{SS}	-0.3 to +7.0	V
Supply voltage (2)	V_{CC}		V_{CC}	V_{EE}-0.3 to V_{EE}+48.0	V
	V_{SH}		V_{SHL}, V_{SHR}	V_{EE}-0.3 to V_{CC}+0.3	V
	V_C		V_{CL}, V_{CR}	V_{EE}-0.3 to V_{CC}+0.3	V
	V_{SL}		V_{SLL}, V_{SLR}	V_{EE}-0.3 to V_{CC}+0.3	V
Input voltage	V_I		DIO_1, DIO_2, DMIN, SHL, LP, MODE, FR, $\overline{DISPOFF}$, $\overline{BLNK}$, $TEST_1$, $TEST_2$	V_{SS}-0.3 to V_{DD}+0.3	V
Storage temperature	T_{stg}			-45 to +125	℃

10. Recommended Operating Conditions

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Supply voltage(1)	V_{DD}	Note Referenced to V_{SS}	V_{DD}	V_{SS}+2.4		V_{SS}+5.5	V
Supply voltage(2)	V_{CC}		V_{CC}	V_{SS}+12.5		V_{SS}+25	V
Supply voltage(3)	V_{EE}		V_{EE}	V_{SS}-20		V_{SS}-7.5	V
Operating temperature	T_{opr}			-30		+85	℃

【Note】 Keep the following relation : $V_{EE} \leqq V_{SL} < V_C < V_{SH} \leqq V_{CC}$

11. Electrical Characteristics

11-1. DC Characteristics

(V_{SS}=0 V, V_{DD}=+2.4 to +5.5 V, V_{CC}-V_{EE}=+20 to +45.0 V, Ta=-30 to +85 ℃)

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Input voltage	V_{IH}		DIO_1, DIO_2, DMIN, SHL, LP, MODE, FR, $\overline{DISPOFF}$, $\overline{BLNK}$	0.8V_{DD}			V
	V_{IL}					0.2V_{DD}	V
Output voltage	V_{OH}	I_{OH}=-0.4 mA	DIO_1, DIO_2	V_{DD}-0.4			V
	V_{OL}	I_{OL}=+0.4 mA				+0.4	V
Input leakage current	I_{LIH}	V_I=V_{DD}	SHL, MODE, LP, FR, $\overline{DISPOFF}$, $\overline{BLNK}$			+10.0	μA
	I_{LIL}	V_I=V_{SS}	SHL, MODE, DMIN, LP, FR, $\overline{DISPOFF}$, $\overline{BLNK}$, DIO_1, DIO_2			-10.0	μA
Input pull-down current	I_{PD}	V_I=V_{DD}	DIO_1, DIO_2, DMIN			+100.0	μA
Output resistance	R_{ON}	|ΔV_{ON}|=0.5 V*1	O_1-O_{160}		0.6	1.0	kΩ
Stand-by current (1)	I_{STB1}	*2	V_{DD}			20.0	μA
Stand-by current (2)	I_{STB2}	*2	V_{CC}			20.0	μA
Consumed current (1)	I_{DD}	*3	V_{DD}			30.0	μA
Consumed current (2)	I_{CC}	*3	V_{CC}			30.0	μA

【Note】 *1 : V_{CC}=V_{SH}=+22.5 V, V_C=+2.5 V, V_{EE}=V_{SL}=-17.5 V, V_{DD}=+5.0 V

*2: V_{CC}=V_{SH}=+25 V, V_C=+2.5 V, V_{EE}=V_{SL}=-20 V, V_{DD}=+5.0 V, V_I=V_{SS}

*3: V_{CC}=V_{SH}=+25 V, V_C=+2.5 V, V_{EE}=V_{SL}=-20 V, V_{DD}=+5.0 V

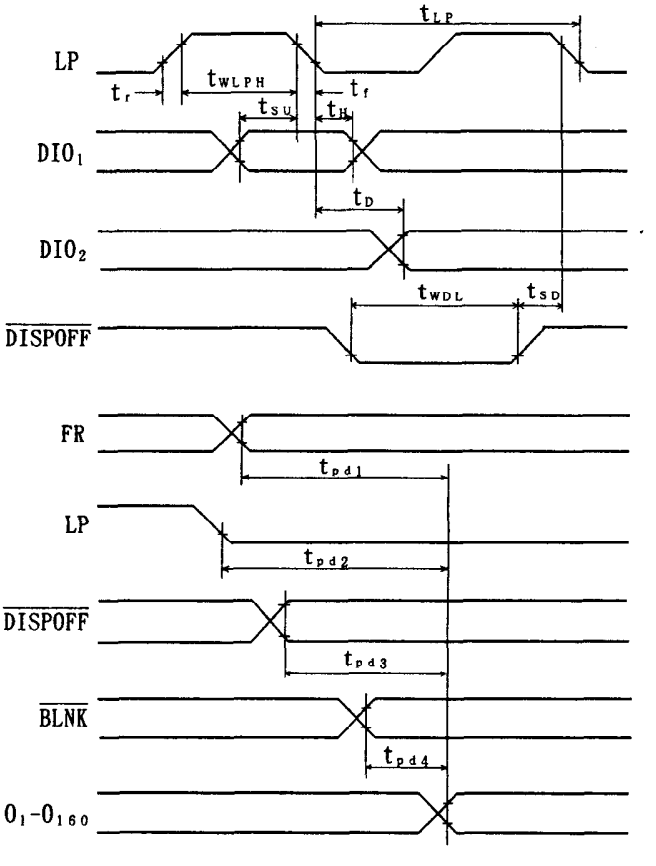
f_{LP}=12.8 kHz, f_{FR}=80 Hz. 1/160 Duty operation, No-load

11-2. AC Characteristics

(V_{SS}=0 V, V_{DD}=+2.4 to +5.5 V, V_{CC}-V_{EE}=+20 to +45 V, Ta=-30 to +85 ℃)

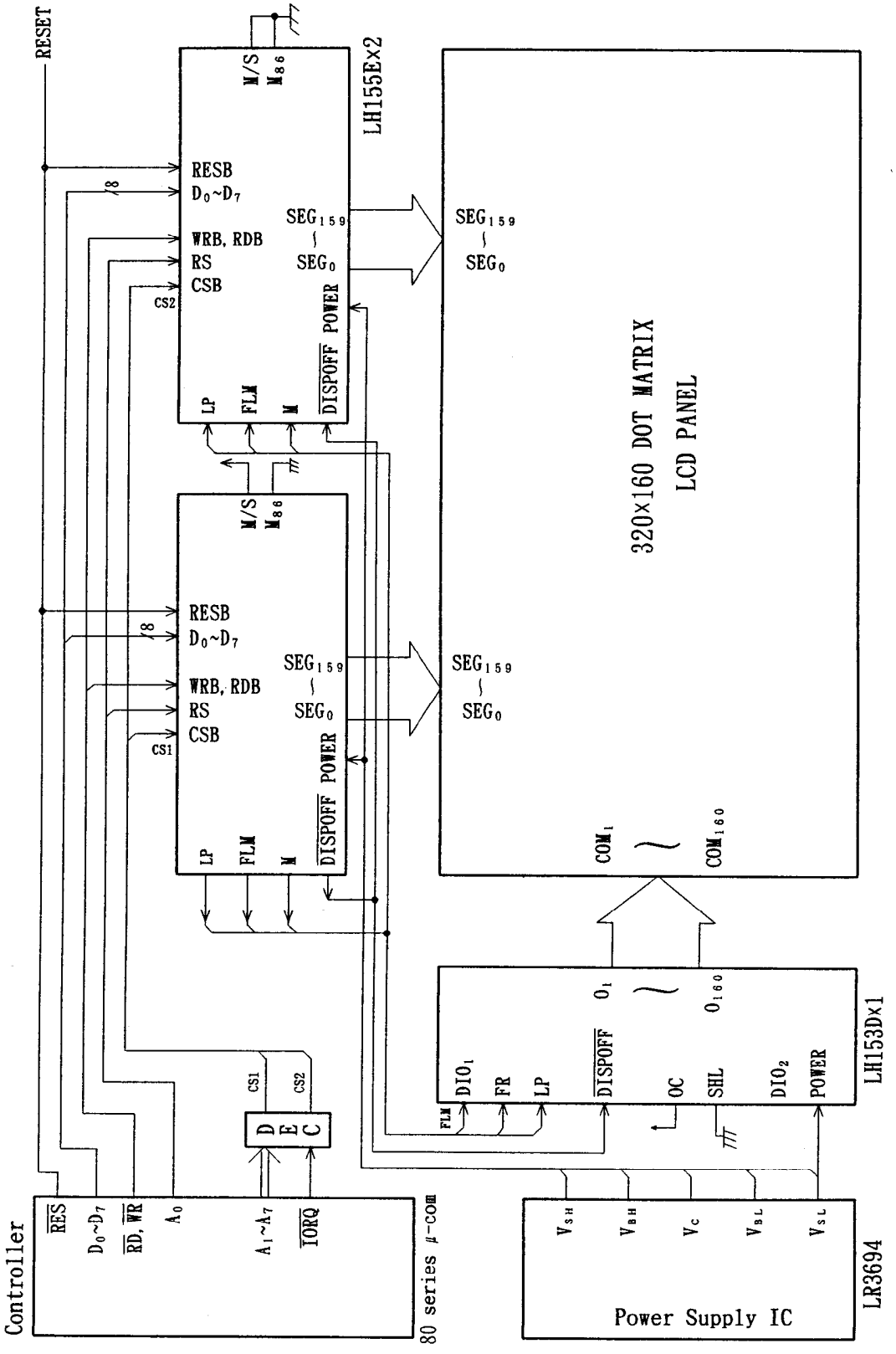
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift clock period	t_{LP}	V_{DD}=+4.5 to +5.5 V	250			ns
		V_{DD}=+2.4 to +4.5 V	330			ns
Shift clock "H" pulse width	t_{WLPH}	V_{DD}=+4.5 to +5.5 V	30			ns
		V_{DD}=+2.4 to +4.5 V	60			ns
Shift clock "L" pulse width	t_{WLPL}	V_{DD}=+4.5 to +5.5 V	120			ns
		V_{DD}=+2.4 to +4.5 V	170			ns
Data setup time	t_{SU}		50			ns
Data hold time	t_H		50			ns
Input signal rise time	t_r				50	ns
Input signal fall time	t_f				50	ns
$\overline{DISPOFF}$ removal time	t_{SD}		120			ns
$\overline{DISPOFF}$ "L" pulse width	t_{WDL}		1.2			μs
Output delay time (1)	t_D	C_L=15 pF V_{DD}=+4.5 to +5.5 V			170	ns
		C_L=15 pF V_{DD}=+2.4 to +4.5 V			250	ns
Output delay time (2)	t_{pd1}, t_{pd2}	C_L=15 pF			1.2	μs
Output delay time (3)	t_{pd3}	C_L=15 pF			1.2	μs
Output delay time (4)	t_{pd4}	C_L=15 pF			1.2	μs

11-3. Timing Diagram



[SHL="L"]
Timing chart

12. Example of System configuration



13. Example of Typical Characteristic

(Ta=+25 ℃, V_{SS}=0 V, V_{DD}=+5.0 V)

Parameter	Min.	Typ.	Max.	Unit
Typical Fundamental Rating Propagation Delay Time		10		ns