PM5386

S/UNI® 4xJET

4-Channel ATM and Bit-HDLC User Network Interface

Register Description

Proprietary and Confidential

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Legal Information

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2	May 2003	Updated based on release version of 12xJET register data sheet
1	March 2003	Issue 1 created.

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1 Definitions

The following table defines the abbreviations for the S/UNI® 4xJET device.

Term	Definition
AIS	Alarm Indication Signal
ASSP	Application Specific Standard Product
ATM	Asynchronous Transfer Mode
BER	Bit Error Rate
BIP	Byte Interleaved Parity
CBI	Common Bus Interface
CMOS	Complementary Metal Oxide Semiconductor
COFA	Change of Frame Alignment
CPPM	Cell and PLCP Performance Monitor
CRC	Cyclic Redundancy Check
CSU	Clock Synthesis Unit
D3E3MA	DS3 / E3 TO STS-1/STM-0 Mapper / Synchronizer
D3E3MD	STS-1/STM-0 TO E3 / DS3 Demapper / Desynchronizer
DLL	Digital Delay Lock Loop
DS1	Digital Signal Level 1
DS3	Digital Signal Level 3
E3 FRMR	ITU-T G.832 E3, G.751 E3 Framer
E3 TRAN	CCITT G.832 E3, G.751 E3 Transmitter
ERDI	Enhanced Remote Defect Indication
ESD	Electrostatic Discharge
EXZS	Excess Zeros
FAS	Framing Alignment Signal
F-bit	Framing Bit
FCS	Frame Check Sequence
FEAC	Far End Alarm Control
FEBE	Far End Block Error also referred to as REI
FERF	Far End Receive Failure
FERR	Framing Bit Error
FIFO	First-In First-Out
GFC	Generic Flow Control
HCS	Header Check Sequence
HDLC	High-level Data Link Layer
ISDN	Integrated Services Digital network
ITU	International Telecommunications Union
J2 FRMR	J2 Framer
J2 TRAN	J2 Transmitter
JAT	Digital Jitter Attenuator

Term	Definition
JTAG	Joint Test Action Group
LAN	Local Area Network
LCD	Loss of Cell Delineation
LCV	Line Code Violation
LFSR	Linear Feedback Shift Register
LOF	Loss of Frame
LOP	Loss of Pointer
LOS	Loss of Signal
LOT	Loss of Transition
NC	No Connect, indicates an unused pin
NDF	New Data Flag
NNI	Network-Network Interface
NRZ	Non Return to Zero
ODL	Optical Data Link
OOF	Out of Frame
PERR	Parity Error
PHY	Physical Layer
PLCP	Physical Layer Convergence Procedure
PLL	Phase-Locked Loop
PMDL	Path Maintenance Data Link
PMON	E3/T3 Performance Monitor
POS	Packet Over SONET
PPP	Point-to-Point Protocol
PRGD	Pseudo Random Sequence Generator/ Detector
PRGM	Pseudo Random Sequence Generator/Monitor
PSL	Path Signal Label
PSLM	Path Signal Label Mismatch
RAI	Receive Alarm Indication
RBOC	Bit Oriented Code Detector
RDI	Remote Defect Indication
RDLC	Data Link Receiver
RED	Receive Error Detection
RHPP	Receive High Order Path Processor
RTTP	Receive Trail Trace Processor
RXCP	Receive ATM Cell Processor
RXFP	Receive Packet over SONET Frame Processor
SARC	SONET/SDH Alarm Reporting Controller
SD	Signal Degrade (alarm)
SDH	Synchronous Digital Hierarchy
SF	Signal Fail

Term	Definition
SMDS	Switched Multi-Megabit Data Service
SONET	Synchronous Optical Network
SPE	Synchronous Payload Envelope
SPLR	SMDS PLCP Layer Receiver
SPLT	SMDS PLCP Layer Transmitter
SPTB	SONET/SDH Path Trace Buffer
T3 FRMR	T3 (DS3) Framer
T3 TRAN	T3 (DS3) Transmitter
TAP	Test Access Port
TDPR	Transmit Data Link Controller with Performance Report Interface
THPP	Transmit High Order Path Processor
TIM	Trace Identifier Mismatch
TIU	Trace Identifier Unstable
TOH	Transport Overhead
TSBGA	Tape Super Ball Grid Array
TTTP	Transmit Trail Trace Processor
TXCP	Transmit ATM Cell Processor
TXFP	Transmit Packet Over SONET Frame Processor
UI	Unit Interval
UNI	User-Network Interface
VCI	Virtual Connection Indicator
VPI	Virtual Path Indicator
WAN	Wide Area Network
XBOC	Bit-Oriented Code Transmitter
XOR	Exclusive OR logic operator

2 References

1. PMC-2021632 “PM5386 S/UNI 4xJET ASSP Telecom Standard Product Data Sheet,” February 2003.

3 Normal Mode Register Description

3.1 Microprocessor Interface

The microprocessor interface block provides normal and test mode registers, and the logic required to connect to the microprocessor interface. The normal mode registers are required for normal operation, and test mode registers are used to enhance the testability of the S/UNI 4xJET. In the following section, every register is documented and identified using the register number.

Table 1 Top Level Register Memory Map

Address	Register Description
0-1FF	Channel #0 Configuration and Status Registers
200-3FF	Reserved
400-5FF	Channel #2 Configuration and Status Registers
600-11FF	Reserved
1200-13FF	Channel #1 Configuration and Status Registers
1400-15FF	Reserved
1600-17FF	Channel #3 Configuration and Status Registers
1800-1FFF	System Interface Configuration and Status Registers
2000-3FFF	Reserved for Test

As shown by the top-level register map in Table 1, each channel is represented by a repeat addressable structure. Table 2 describes every normal mode register for a channel's address space. The channel offset is shown for channel #0 with all other channels similarly located by the address spaces listed above.

Table 2 Per Channel Register Memory Map

Address	Register Description
000	Channel Configuration #1
001	Channel Configuration #2
002	Channel Transmit Configuration #1
003	Channel Receive Configuration #1
004	Channel Data Link and FERF/RAI Control
005	Channel Interrupt Status #1
006	Channel Reset and Performance Monitor Update
007	Channel Clock Activity Monitor #1
008	SPLR Configuration
009	SPLR Interrupt Enable
00A	SPLR Interrupt Status
00B	SPLR Status
00C	SPLT Configuration

Address	Register Description
00D	SPLT Control
00E	SPLT Diagnostics and G1 Octet
00F	SPLT F1 Octet
010	PMON Change of PMON Performance Meters
011	PMON Interrupt Enable/Status
012-013	PMON Reserved
014	PMON Line Code Violation Event Count LSB
015	PMON Line Code Violation Event Count MSB
016	PMON Framing Bit Error Event Count LSB
017	PMON Framing Bit Error Event Count MSB
018	PMON Excessive Zeros Count LSB
019	PMON Excessive Zeros Count MSB
01A	PMON Parity Error Event Count LSB
01B	PMON Parity Error Event Count MSB
01C	PMON Path Parity Error/E3-FRMERR Event Count LSB
01D	PMON Path Parity Error/E3-FRMERR Event Count MSB
01E	PMON FEBE/J2-EXZS Event Count LSB
01F	PMON FEBE/J2-EXZS Event Count MSB
020	CPPM Reserved
021	CPPM Change of CPPM Performance Meter
022	CPPM BIP Error Count LSB
023	CPPM BIP Error Count MSB
024	CPPM Framing Error Event Count LSB
025	CPPM Framing Error Event Count MSB
026	CPPM FEBE Count LSB
027	CPPM FEBE Count MSB
028-02F	CPPM Reserved
030	DS3 FRMR Configuration
031	DS3 FRMR Interrupt Enable (ACE = 0)
031	DS3 FRMR Additional Configuration (ACE = 1)
032	DS3 FRMR Interrupt Status
033	DS3 FRMR Status
034	DS3 TRAN Configuration
035	DS3 TRAN Diagnostics
036-037	DS3 TRAN Reserved
038	E3 FRMR Framing Options
039	E3 FRMR Maintenance Options
03A	E3 FRMR Framing Interrupt Enable
03B	E3 FRMR Framing Interrupt Indication and Status
03C	E3 FRMR Maintenance Event Interrupt Enable

Address	Register Description
03D	E3 FRMR Maintenance Event Interrupt Indication
03E	E3 FRMR Maintenance Event Status
03F	E3 FRMR Reserved
040	E3 TRAN Framing Options
041	E3 TRAN Status and Diagnostic Options
042	E3 TRAN BIP-8 Error Mask
043	E3 TRAN Maintenance and Adaptation Options
044	J2 FRMR Configuration
045	J2 FRMR Status
046	J2 FRMR Alarm Interrupt Enable
047	J2 FRMR Alarm Interrupt Status
048	J2 FRMR Error/X-bit Interrupt Enable
049	J2 FRMR Error/X-bit Interrupt Status
04A-04B	J2 FRMR Reserved
04C	J2 TRAN Configuration
04D	J2 TRAN Diagnostics
04E	J2 TRAN TS97 Signaling
04F	J2 TRAN TS98 Signaling
050	RDLC Configuration
051	RDLC Interrupt Control
052	RDLC Status
053	RDLC Data
054	RDLC Primary Address Match
055	RDLC Secondary Address Match
056	RDLC Reserved
057	RDLC Reserved
058	TDPR Configuration
059	TDPR Upper Transmit Threshold
05A	TDPR Lower Interrupt Threshold
05B	TDPR Interrupt Enable
05C	TDPR Interrupt Status/UDR Clear
05D	TDPR Transmit Data
05E-05F	TDPR Reserved
060	RXCP Configuration 1
061	RXCP Configuration 2
062	RXCP FIFO/UTOPIA Control & Configuration
063	RXCP Interrupt Enables and Counter Status
064	RXCP Status/Interrupt Status
065	RXCP LCD Count Threshold (MSB)
066	RXCP LCD Count Threshold (LSB)

Address	Register Description
067	RXCP Idle Cell Header Pattern
068	RXCP Idle Cell Header Mask
069	RXCP Reserved
06A	RXCP HCS Error Count
06B	RXCP Received Cell Count LSB
06C	RXCP Received Cell Count
06D	RXCP Received Cell Count MSB
06E	RXCP Idle Cell Count LSB
06F	RXCP Idle Cell Count
070	RXCP Idle Cell Count MSB
071-07F	RXCP Reserved
080	TXCP Configuration 1
081	TXCP Configuration 2
082	TXCP Transmit Cell Status
083	TXCP Interrupt Enable/Status
084	TXCP Idle Cell Header Control
085	TXCP Idle Cell Payload Control
086	TXCP Transmit Cell Count LSB
087	TXCP Transmit Cell Count
088	TXCP Transmit Cell Count MSB
089-08F	TXCP Reserved
090	TTB Control
091	TTB Trail Trace Identifier Status
092	TTB Indirect Address
093	TTB Indirect Data
094	TTB Expected Payload Type Label
095	TTB Payload Type Label Control/Status
096	TTB Indirect Access Trigger
097	TTB Reserved
098	RBOC Configuration/Interrupt Enable
099	RBOC Interrupt Status
09A	XBOC Control Register
09B	XBOC Code
09C-09D	Channel Reserved
09E	Channel Miscellaneous Configuration #1
09F	Channel FRMR LOF Status
0A0	PRGD Control
0A1	PRGD Interrupt Enable/Status
0A2	PRGD Length
0A3	PRGD Tap

Address	Register Description
0A4	PRGD Error Insertion
0A5-0A7	PRGD Reserved
0A8	PRGD Pattern Insertion Register #1
0A9	PRGD Pattern Insertion Register #2
0AA	PRGD Pattern Insertion Register #3
0AB	PRGD Pattern Insertion Register #4
0AC	PRGD Pattern Detector Register #1
0AD	PRGD Pattern Detector Register #2
0AE	PRGD Pattern Detector Register #3
0AF	PRGD Pattern Detector Register #4
0B0-0FF	Channel Reserved
100	Channel Transmit Configuration #2
101	Channel Receive Configuration #2
102	Channel Transmit Timeslot Configuration #1
103	Channel Transmit Timeslot Configuration #2
104	Channel Transmit Timeslot Configuration #3
105	Channel Receive Timeslot Configuration #1
106	Channel Transmit Address Configuration
107	Channel Receive Address Configuration
108	Channel Transmit Bit HDLC Configuration
109	Channel Receive Bit HDLC Configuration
10A	Channel Interrupt Status #2
10B	Channel Clock Activity Monitor #2
10C	Channel Loopback Configuration
10D	Channel Receive Timeslot Configuration #2
10E	Channel Receive Timeslot Configuration #3
10F	Channel Reserved
110	Channel Receive Performance Count LSB
111	Channel Receive Performance Count MSB
112	Channel Auxiliary Framer Configuration
113	Channel Data Path Configuration
114	Channel Serial Cross Connect Configuration
115	Channel Auxiliary Framer Data Link and XFERF/RAI Control
116	Channel Auxiliary Framer LOF Status
117	Channel D3E3MA DS3/E3-AIS Enable
118	Channel FRMSTAT Control
119	Channel Miscellaneous Configuration #2
11A-11F	Reserved
120	D3E3MD Configuration
121	D3E3MD Status/Interrupt Status

Address	Register Description
122	D3E3MD Interrupt Enable
123-127	D3E3MD Reserved
128	D3E3MA Control
129	D3E3MA Interrupt Status
12A	D3E3MA Interrupt Enable
12B-12F	D3E3MA Reserved
130	RDLC DEMAPPER Configuration
131	RDLC DEMAPPER Interrupt Control
132	RDLC DEMAPPER Status
133	RDLC DEMAPPER Data
134	RDLC DEMAPPER Primary Address Match
135	RDLC DEMAPPER Secondary Address Match
136-137	RDLC DEMAPPER Reserved
138	TDPR MAPPER Configuration
139	TDPR MAPPER Upper Transmit Threshold
13A	TDPR MAPPER Lower Interrupt Threshold
13B	TDPR MAPPER Interrupt Enable
13C	TDPR MAPPER Interrupt Status/UDR Clear
13D	TDPR MAPPER Transmit Data
013E-13F	TDPR MAPPER Reserved
140	RXFP Configuration
141	RXFP Configuration/Interrupt Enable
142	RXFP Interrupt Status
143	RXFP Minimum Packet Length
144	RXFP Maximum Packet Length LSB
145	RXFP Maximum Packet Length MSB
146	RXFP Receive Initiation Level
148	RXFP Receive Byte Counter LSB
149	RXFP Receive Byte Counter
14A	RXFP Receive Byte Counter
14B	RXFP Receive Byte Counter MSB
14C	RXFP Receive Frame Counter LSB
14D	RXFP Receive Frame Counter
14E	RXFP Receive Frame Counter MSB
14F	RXFP Aborted Frame Count LSB
150	RXFP Aborted Frame Count MSB
151	RXFP FCS Error Frame Count LSB
152	RXFP FCS Error Frame Count MSB
153	RXFP Minimum Length Error Frame Count LSB
154	RXFP Minimum Length Error Frame Count MSB

Address	Register Description
155	RXFP Maximum Length Error Frame Count LSB
156	RXFP Maximum Length Error Frame Count MSB
157-15F	RXFP Reserved
160	TXFP Interrupt Enable/Status
161	TXFP Configuration
162	TXFP Control
165	TXFP Transmit Byte Count LSB
166	TXFP Transmit Byte Count
167	TXFP Transmit Byte Count
168	TXFP Transmit Byte Count MSB
169	TXFP Transmit Frame Count LSB
16A	TXFP Transmit Frame Count
16B	TXFP Transmit Frame Count MSB
16C	TXFP Transmit User Aborted Frame Count LSB
16D	TXFP Transmit User Aborted Frame Count MSB
16E	TXFP Transmit Underrun/Error Aborted Frame Count LSB
16F	TXFP Transmit Underrun/Error Aborted Frame Count MSB
170	PMON AUX Change of PMON Performance Meters
171	PMON AUX Interrupt Enable/Status
172-175	PMON AUX Reserved
176	PMON AUX Framing Bit Error Event Count LSB
177	PMON AUX Framing Bit Error Event Count MSB
178-179	PMON AUX Reserved
17A	PMON AUX Parity Error Event Count LSB
17B	PMON AUX Parity Error Event Count MSB
17C	PMON AUX Path Parity Error/E3-FRMERR Event Count LSB
17D	PMON AUX Path Parity Error/E3-FRMERR Event Count MSB
17E	PMON AUX FEBE Event Count LSB
17F	PMON AUX FEBE Event Count MSB
180	DS3 FRMR AUX Configuration
181	DS3 FRMR AUX Interrupt Enable (ACE = 0)
181	DS3 FRMR AUX Additional Configuration (ACE = 1)
182	DS3 FRMR AUX Interrupt Status
183	DS3 FRMR AUX Status
184-187	DS3 FRMR AUX Reserved
188	E3 FRMR AUX Framing Options
189	E3 FRMR AUX Maintenance Options
18A	E3 FRMR AUX Framing Interrupt Enable
18B	E3 FRMR AUX Framing Interrupt Indication and Status
18C	E3 FRMR AUX Maintenance Event Interrupt Enable

Address	Register Description
18D	E3 FRMR AUX Maintenance Event Interrupt Indication
18E	E3 FRMR AUX Maintenance Event Status
18F	E3 FRMR AUX Reserved
190	J2 FRMR AUX Configuration
191	J2 FRMR AUX Status
192	J2 FRMR AUX Alarm Interrupt Enable
193	J2 FRMR AUX Alarm Interrupt Status
194	J2 FRMR AUX Error/X-bit Interrupt Enable
195	J2 FRMR AUX Error/X-bit Interrupt Status
196-197	J2 FRMR AUX Reserved
198	RDLC AUX Configuration
199	RDLC AUX Interrupt t Control
19A	RDLC AUX Status
19B	RDLC AUX Data
19C	RDLC AUX Primary Address Match
19D	RDLC AUX Secondary Address Match
19E-19F	RDLC AUX Reserved
1A0	TTB AUX Control Register
1A1	TTB AUX Trail Trace Identifier Status
1A2	TTB AUX Indirect Address Register
1A3	TTB AUX Indirect Data Register
1A4	TTB AUX Expected Payload Type Label Register
1A5	TTB AUX Payload Type Label Control/Status
1A6	TTB AUX Indirect Access Trigger
1A7	TTB AUX Reserved
1A8	RBOC AUX Configuration/Interrupt Enable
1A9	RBOC AUX Interrupt Status
1AA-1AF	RBOC AUX Reserved
1B0	RJAT PLL Configuration
1B1	RJAT Interrupt Status
1B2	RJAT Status and FIFO Control
1B3	RJAT DLL Backdoor
1B4	RJAT ROOL Configuration
1B5-1B7	RJAT Reserved
1B8	TJAT PLL Configuration
1B9	TJAT Interrupt Status
1BA	TJAT Status and FIFO Control
1BB	TJAT DLL Backdoor
1BC	TJAT ROOL Configuration
1BD-1BF	TJAT Reserved

Address	Register Description
1C0-1FF	Channel Reserved

Notes

- For all register accesses, CSB must be low.
- As show by the top-level register map in Table 1, the Level 3 System Interface registers are located together in memory similar to a channel interface. Table 3 lists the registers for the Level 3 System Interface and SONET/SDH interfaces.

Table 3 System Interface Register Memory Map

Address	Register Description
1800	S/UNI 4xJET Master Reset and Identity
1801	S/UNI 4xJET Master Configuration
1802	S/UNI 4xJET Reserved
1803	S/UNI 4xJET Master Receive Configuration
1804	S/UNI 4xJET Telecom Bus Parity
1805	S/UNI 4xJET Transmit Telecom Bus Synchronization Delay
1806	S/UNI 4xJET Reserved
1807	S/UNI 4xJET Master Interrupt Status #1
1808	S/UNI 4xJET Master Interrupt Status #2
1809	S/UNI 4xJET Master Interrupt Status #3
180A	S/UNI 4xJET Master Clock Activity & Input Monitor
180B	S/UNI 4xJET Master Loopback Configuration
180C	S/UNI 4xJET Reserved
180D	S/UNI 4xJET Transmit Timeslot Enable
180E-180F	S/UNI 4xJET Reserved
1810	RUL3 Interface Configuration
1811	RUL3 Interrupt Status/Configuration
1812	RUL3 ATM Level 3 FIFO Configuration
1813	RUL3 ATM Level 3 Signal Label
1814	RUL3 POS Level 3 Configuration
1815	RUL3 POS Level 3 Signal Label
1816	RUL3 POS Level 3 Transfer Size
1818	RUL3 Channel #0, #4, #8 Mode Configuration
1819	RUL3 Channel #1, #5, #9 Mode Configuration
181A	RUL3 Channel #2, #6, #10 Mode Configuration
181B	RUL3 Channel #3, #7, #11 Mode Configuration
181C-181F	RUL3 Reserved
1820	TUL3 Interface Configuration
1821	TUL3 Interrupt Status/Enable #1
1822	TUL3 Interrupt Status/Enable #2
1823	TUL3 ATM Level 3 FIFO Configuration

Address	Register Description
1824	TUL3 ATM Level 3 Signal Label
1825	TUL3 POS Level 3 FIFO Low Water Mark
1826	TUL3 POS Level 3 FIFO High Water Mark
1827	TUL3 POS Level 3 Signal Label
1829	TUL3 Channel #0, #4, #8 Mode Configuration
182A	TUL3 Channel #1, #5, #9 Mode Configuration
182B	TUL3 Channel #2, #6, #10 Mode Configuration
182C	TUL3 Channel #3, #7, #11 Mode Configuration
182D-182E	TUL3 Reserved
1830	DLL RUL3 Configuration
1832	DLL RUL3 Delay Tap Status
1833	DLL RUL3 Control Status
1834	DLL TUL3 Configuration
1836	DLL TUL3 Delay Tap Status
1837	DLL TUL3 Control Status
1838-183F	Reserved
1840	SARC Indirect Address
1841-1847	SARC Reserved
1848	SARC Path Configuration
1849	SARC Path RALM Enable
184A	SARC Path Downstream AIS-P Enable
184B	SARC TU3 Tributary Path Configuration
184C	SARC TU3 Tributary Path RALM Enable
184D	SARC TU3 Tributary Path Downstream AIS-V Enable
184E-184F	SARC Reserved
1850	SARC Path LOP-P Pointer Status
1851	SARC Path LOP-P Pointer Interrupt Enable
1852	SARC Path LOP-P Pointer Interrupt Status
1853	SARC Path AIS-P Pointer Status
1854	SARC Path AIS-P Pointer Interrupt Enable
1855	SARC Path AIS-P Pointer Interrupt Status
1856-1857	SARC Reserved
1858	SARC TU3 Tributary Path LOP-V Pointer Status
1859	SARC TU3 Tributary Path LOP-V Pointer Interrupt Enable
185A	SARC TU3 Tributary Path LOP-V Pointer Interrupt Status
185B	SARC TU3 Tributary Path AIS-V Pointer Status
185C	SARC TU3 Tributary Path AIS-V Pointer Interrupt Enable
185D	SARC TU3 Tributary Path AIS-V Pointer Interrupt Status
185E-185F	SARC Reserved
1860-187F	S/UNI 4xJET Reserved

Address	Register Description
1880	RHPP Indirect Address
1881	RHPP Indirect Data
1882	RHPP Payload Configuration
1883	RHPP Counter Update
1884	RHPP Path Interrupt Status
1885	RHPP Pointer Concatenation Processing Disable
1886-1887	RHPP Unused
1888	RHPP Pointer Interpreter Status STS-1/STM-0 #1
1889	RHPP Pointer Interpreter Interrupt Enable STS-1/STM-0 #1
188A	RHPP Pointer Interpreter Interrupt Status STS-1/STM-0 #1
188B	RHPP Error Monitor Status STS-1/STM-0 #1
188C	RHPP Error Monitor Interrupt Enable STS-1/STM-0 #1
188D	RHPP Error Monitor Interrupt Status STS-1/STM-0 #1
188E-188F	RHPP Reserved STS-1/STM-0 #1
1890	RHPP Pointer Interpreter Status STS-1/STM-0 #2
1891	RHPP Pointer Interpreter Interrupt Enable STS-1/STM-0 #2
1892	RHPP Pointer Interpreter Interrupt Status STS-1/STM-0 #2
1893	RHPP Error Monitor Status STS-1/STM-0 #2
1894	RHPP Error Monitor Interrupt EnableSTS-1/STM-0 #2
1895	RHPP Error Monitor Interrupt Status STS-1/STM-0 #2
1896-1897	RHPP Reserved STS-1/STM-0 #2
1898	RHPP Pointer Interpreter Status STS-1/STM-0 #3
1899	RHPP Pointer Interpreter Interrupt Enable STS-1/STM-0 #3
189A	RHPP Pointer Interpreter Interrupt Status STS-1/STM-0 #3
189B	RHPP Error Monitor Status STS-1/STM-0 #3
189C	RHPP Error Monitor Interrupt Enable STS-1/STM-0 #3
189D	RHPP Error Monitor Interrupt Status STS-1/STM-0 #3
189E-189F	RHPP Reserved STS-1/STM-0 #4
18A0	RHPP Pointer Interpreter Status STS-1/STM-0 #4
18A1	RHPP Pointer Interpreter Interrupt Enable STS-1/STM-0 #4
18A2	RHPP Pointer Interpreter Interrupt Status STS-1/STM-0 #4
18A3	RHPP Error Monitor Status STS-1/STM-0 #4
18A4	RHPP Error Monitor Interrupt EnableSTS-1/STM-0 #4
18A5	RHPP Error Monitor Interrupt Status STS-1/STM-0 #4
18A6-18A7	RHPP Reserved STS-1/STM-0 #4
18A8	RHPP Pointer Interpreter Status STS-1/STM-0 #5
18A9	RHPP Pointer Interpreter Interrupt Enable STS-1/STM-0 #5
18AA	RHPP Pointer Interpreter Interrupt Status STS-1/STM-0 #5
18AB	RHPP Error Monitor Status STS-1/STM-0 #5
18AC	RHPP Error Monitor Interrupt Enable STS-1/STM-0 #5

Address	Register Description
18AD	RHPP Error Monitor Interrupt Status STS-1/STM-0 #5
18AE-18AF	RHPP Reserved STS-1/STM-0 #5
18B0	RHPP Pointer Interpreter Status STS-1/STM-0 #6
18B1	RHPP Pointer Interpreter Interrupt Enable STS-1/STM-0 #6
18B2	RHPP Pointer Interpreter Interrupt Status STS-1/STM-0 #6
18B3	RHPP Error Monitor Status STS-1/STM-0 #6
18B4	RHPP Error Monitor Interrupt Enable STS-1/STM-0 #6
18B5	RHPP Error Monitor Interrupt Status STS-1/STM-0 #6
18B6-18B7	RHPP Reserved STS-1/STM-0 #6
18B8	RHPP Pointer Interpreter Status STS-1/STM-0 #7
18B9	RHPP Pointer Interpreter Interrupt Enable STS-1/STM-0 #7
18BA	RHPP Pointer Interpreter Interrupt Status STS-1/STM-0 #7
18BB	RHPP Error Monitor Status STS-1/STM-0 #7
18BC	RHPP Error Monitor Interrupt Enable STS-1/STM-0 #7
18BD	RHPP Error Monitor Interrupt Status STS-1/STM-0 #7
18BE-18BF	RHPP Reserved STS-1/STM-0 #7
18C0	RHPP Pointer Interpreter Status STS-1/STM-0 #8
18C1	RHPP Pointer Interpreter Interrupt Enable STS-1/STM-0 #8
18C2	RHPP Pointer Interpreter Interrupt Status STS-1/STM-0 #8
18C3	RHPP Error Monitor Status STS-1/STM-0 #8
18C4	RHPP Error Monitor Interrupt Enable STS-1/STM-0 #8
18C5	RHPP Error Monitor Interrupt Status STS-1/STM-0 #8
18C6-18C7	RHPP Reserved STS-1/STM-0 #8
18C8	RHPP Pointer Interpreter Status STS-1/STM-0 #9
18C9	RHPP Pointer Interpreter Interrupt Enable STS-1/STM-0 #9
18CA	RHPP Pointer Interpreter Interrupt Status STS-1/STM-0 #9
18CB	RHPP Error Monitor Status STS-1/STM-0 #9
18CC	RHPP Error Monitor Interrupt Enable STS-1/STM-0 #9
18CD	RHPP Error Monitor Interrupt Status STS-1/STM-0 #9
18CE-18CF	RHPP Reserved STS-1/STM-0 #9
18D0	RHPP Pointer Interpreter Status STS-1/STM-0 #10
18D1	RHPP Pointer Interpreter Interrupt Enable STS-1/STM-0 #10
18D2	RHPP Pointer Interpreter Interrupt Status STS-1/STM-0 #10
18D3	RHPP Error Monitor Status STS-1/STM-0 #10
18D4	RHPP Error Monitor Interrupt EnableSTS-1/STM-0 #10
18D5	RHPP Error Monitor Interrupt Status STS-1/STM-0 #10
18D6-18D7	RHPP Reserved STS-1/STM-0 #10
18D8	RHPP Pointer Interpreter Status STS-1/STM-0 #11
18D9	RHPP Pointer Interpreter Interrupt Enable STS-1/STM-0 #11
18DA	RHPP Pointer Interpreter Interrupt Status STS-1/STM-0 #11

Address	Register Description
18DB	RHPP Error Monitor Status STS-1/STM-0 #11
18DC	RHPP Error Monitor Interrupt Enable STS-1/STM-0 #11
18DD	RHPP Error Monitor Interrupt Status STS-1/STM-0 #11
18DE-18DF	RHPP Reserved STS-1/STM-0 #11
18E0	RHPP Pointer Interpreter Status STS-1/STM-0 #12
18E1	RHPP Pointer Interpreter Interrupt Enable STS-1/STM-0 #12
18E2	RHPP Pointer Interpreter Interrupt Status STS-1/STM-0 #12
18E3	RHPP Error Monitor Status STS-1/STM-0 #12
18E4	RHPP Error Monitor Interrupt Enable STS-1/STM-0 #12
18E5	RHPP Error Monitor Interrupt Status STS-1/STM-0 #12
18E6-18E7	RHPP Reserved STS-1/STM-0 #12
18E8-18FF	RHPP Reserved
1900	RHPP TU3 Indirect Address
1901	RHPP TU3 Indirect Data
1902	RHPP TU3 Payload Configuration
1903	RHPP TU3 Counter Update
1904	RHPP TU3 Path Interrupt Status
1905	RHPP TU3 Pointer Concatenation Processing Disable
1906-1907	RHPP TU3 Unused
1908	RHPP TU3 Pointer Interpreter Status STS-1/STM-0 #1
1909	RHPP TU3 Pointer Interpreter Interrupt Enable STS-1/STM-0 #1
190A	RHPP TU3 Pointer Interpreter Interrupt Status STS-1/STM-0 #1
190B	RHPP TU3 Error Monitor Status STS-1/STM-0 #1
190C	RHPP TU3 Error Monitor Interrupt Enable STS-1/STM-0 #1
190D	RHPP TU3 Error Monitor Interrupt Status STS-1/STM-0 #1
190E-190F	RHPP TU3 Reserved STS-1/STM-0 #1
1910	RHPP TU3 Pointer Interpreter Status STS-1/STM-0 #2
1911	RHPP TU3 Pointer Interpreter Interrupt Enable STS-1/STM-0 #2
1912	RHPP TU3 Pointer Interpreter Interrupt Status STS-1/STM-0 #2
1913	RHPP TU3 Error Monitor Status STS-1/STM-0 #2
1914	RHPP TU3 Error Monitor Interrupt EnableSTS-1/STM-0 #2
1915	RHPP TU3 Error Monitor Interrupt Status STS-1/STM-0 #2
1915-1917	RHPP TU3 Reserved STS-1/STM-0 #2
1918	RHPP TU3 Pointer Interpreter Status STS-1/STM-0 #3
1919	RHPP TU3 Pointer Interpreter Interrupt Enable STS-1/STM-0 #3
191A	RHPP TU3 Pointer Interpreter Interrupt Status STS-1/STM-0 #3
191B	RHPP TU3 Error Monitor Status STS-1/STM-0 #3
191C	RHPP TU3 Error Monitor Interrupt Enable STS-1/STM-0 #3
191D	RHPP TU3 Error Monitor Interrupt Status STS-1/STM-0 #3
191E-191F	RHPP TU3 Reserved STS-1/STM-0 #3

Address	Register Description
1920	RHPP TU3 Pointer Interpreter Status STS-1/STM-0 #4
1921	RHPP TU3 Pointer Interpreter Interrupt Enable STS-1/STM-0 #4
1922	RHPP TU3 Pointer Interpreter Interrupt Status STS-1/STM-0 #4
1923	RHPP TU3 Error Monitor Status STS-1/STM-0 #4
1924	RHPP TU3 Error Monitor Interrupt Enable STS-1/STM-0 #4
1925	RHPP TU3 Error Monitor Interrupt Status STS-1/STM-0 #4
1926-1927	RHPP TU3 Reserved STS-1/STM-0 #4
1928	RHPP TU3 Pointer Interpreter Status STS-1/STM-0 #5
1929	RHPP TU3 Pointer Interpreter Interrupt Enable STS-1/STM-0 #5
192A	RHPP TU3 Pointer Interpreter Interrupt Status STS-1/STM-0 #5
192B	RHPP TU3 Error Monitor Status STS-1/STM-0 #5
192C	RHPP TU3 Error Monitor Interrupt Enable STS-1/STM-0 #5
192D	RHPP TU3 Error Monitor Interrupt Status STS-1/STM-0 #5
192E-192F	RHPP TU3 Reserved STS-1/STM-0 #5
1930	RHPP TU3 Pointer Interpreter Status STS-1/STM-0 #6
1931	RHPP TU3 Pointer Interpreter Interrupt Enable STS-1/STM-0 #6
1932	RHPP TU3 Pointer Interpreter Interrupt Status STS-1/STM-0 #6
1933	RHPP TU3 Error Monitor Status STS-1/STM-0 #6
1934	RHPP TU3 Error Monitor Interrupt Enable STS-1/STM-0 #6
1935	RHPP TU3 Error Monitor Interrupt Status STS-1/STM-0 #6
1936-1937	RHPP TU3 Reserved STS-1/STM-0 #6
1938	RHPP TU3 Pointer Interpreter Status STS-1/STM-0 #7
1939	RHPP TU3 Pointer Interpreter Interrupt Enable STS-1/STM-0 #7
193A	RHPP TU3 Pointer Interpreter Interrupt Status STS-1/STM-0 #7
193B	RHPP TU3 Error Monitor Status STS-1/STM-0 #7
193C	RHPP TU3 Error Monitor Interrupt Enable STS-1/STM-0 #7
193D	RHPP TU3 Error Monitor Interrupt Status STS-1/STM-0 #7
193E-193F	RHPP TU3 Reserved STS-1/STM-0 #7
1940	RHPP TU3 Pointer Interpreter Status STS-1/STM-0 #8
1941	RHPP TU3 Pointer Interpreter Interrupt Enable STS-1/STM-0 #8
1942	RHPP TU3 Pointer Interpreter Interrupt Status STS-1/STM-0 #8
1943	RHPP TU3 Error Monitor Status STS-1/STM-0 #8
1944	RHPP TU3 Error Monitor Interrupt Enable STS-1/STM-0 #8
1945	RHPP TU3 Error Monitor Interrupt Status STS-1/STM-0 #8
1946-1947	RHPP TU3 Reserved STS-1/STM-0 #8
1948	RHPP TU3 Pointer Interpreter Status STS-1/STM-0 #9
1949	RHPP TU3 Pointer Interpreter Interrupt Enable STS-1/STM-0 #9
194A	RHPP TU3 Pointer Interpreter Interrupt Status STS-1/STM-0 #9
194B	RHPP TU3 Error Monitor Status STS-1/STM-0 #9
194C	RHPP TU3 Error Monitor Interrupt Enable STS-1/STM-0 #9

Address	Register Description
194D	RHPP TU3 Error Monitor Interrupt Status STS-1/STM-0 #9
194E-194F	RHPP TU3 Reserved STS-1/STM-0 #9
1950	RHPP TU3 Pointer Interpreter Status STS-1/STM-0 #10
1951	RHPP TU3 Pointer Interpreter Interrupt Enable STS-1/STM-0 #10
1952	RHPP TU3 Pointer Interpreter Interrupt Status STS-1/STM-0 #10
1953	RHPP TU3 Error Monitor Status STS-1/STM-0 #10
1954	RHPP TU3 Error Monitor Interrupt Enable STS-1/STM-0 #10
1955	RHPP TU3 Error Monitor Interrupt Status STS-1/STM-0 #10
1956-1957	RHPP TU3 Reserved STS-1/STM-0 #10
1958	RHPP TU3 Pointer Interpreter Status STS-1/STM-0 #11
1959	RHPP TU3 Pointer Interpreter Interrupt Enable STS-1/STM-0 #11
195A	RHPP TU3 Pointer Interpreter Interrupt Status STS-1/STM-0 #11
195B	RHPP TU3 Error Monitor Status STS-1/STM-0 #11
195C	RHPP TU3 Error Monitor Interrupt Enable STS-1/STM-0 #11
195D	RHPP TU3 Error Monitor Interrupt Status STS-1/STM-0 #11
195E-195F	RHPP TU3 Reserved STS-1/STM-0 #11
1960	RHPP TU3 Pointer Interpreter Status STS-1/STM-0 #12
1961	RHPP TU3 Pointer Interpreter Interrupt Enable STS-1/STM-0 #12
1962	RHPP TU3 Pointer Interpreter Interrupt Status STS-1/STM-0 #12
1963	RHPP TU3 Error Monitor Status STS-1/STM-0 #12
1964	RHPP TU3 Error Monitor Interrupt Enable STS-1/STM-0 #12
1965	RHPP TU3 Error Monitor Interrupt Status STS-1/STM-0 #12
1966-1967	RHPP TU3 Reserved STS-1/STM-0 #12
1968-197F	RHPP TU3 Reserved
1980	THPP Indirect Address
1981	THPP Indirect Data
1982	THPP Payload Configuration
1983-1987	THPP Reserved
1988	THPP TU3 Indirect Address
1989	THPP TU3 Indirect Data
198A	THPP TU3 Payload Configuration
198B-198F	THPP TU3 Reserved
19B0-19B7	S/UNI 4xJET Reserved
19B8	RTTP Path Indirect Address
19B9	RTTP Path Indirect Data
19BA	RTTP Path Trace Unstable Status
19BB	RTTP Path Trace Unstable Interrupt Enable
19BC	RTTP Path Trace Unstable Interrupt Status
19BD	RTTP Path Trace Mismatch Status
19BE	RTTP Path Trace Mismatch Interrupt Enable

Address	Register Description
19BF	RTTP Path Trace Mismatch Interrupt Status
19C0	RTTP TU3 Tributary Path Indirect Address
19C1	RTTP TU3 Tributary Path Indirect Data
19C2	RTTP TU3 Tributary Path Trace Unstable Status
19C3	RTTP TU3 Tributary Path Trace Unstable Interrupt Enable
19C4	RTTP TU3 Tributary Path Trace Unstable Interrupt Status
19C5	RTTP TU3 Tributary Path Trace Mismatch Status
19C6	RTTP TU3 Tributary Path Trace Mismatch Interrupt Enable
19C7	RTTP TU3 Tributary Path Trace Mismatch Interrupt Status
19C8- 19CF	S/UNI 4xJET Reserved
19D0	TTTP Path Indirect Address
19D1	TTTP Path Indirect Data
19D2-19D7	TTTP Path Reserved
19D8	TTTP TU3 Tributary Path Indirect Address
19D9	TTTP TU3 Tributary Path Indirect Data
19DA-19DF	TTTP TU3 Tributary Path Reserved
19E0	PRGM Line Indirect Address
19E1	PRGM Line Indirect Data
19E2	PRGM Line Generator Payload Configuration
19E3	PRGM Line Monitor Payload Configuration
19E4	PRGM Line Monitor Byte Error Interrupt Status
19E5	PRGM Line Monitor Byte Error Interrupt Enable
19E6	PRGM Line Monitor B1/E1 Bytes Interrupt Status
19E7	PRGM Line Monitor B1/E1 Bytes Interrupt Enable
19E9	PRGM Line Monitor Synchronization Interrupt Status
19EA	PRGM Line Monitor Synchronization Interrupt Enable
19EB	PRGM Line Monitor Synchronization Status
19EC	PRGM Line Counter Update
1AA0	Transmit Telecom DLL Configuration
1AA3	Transmit Telecom DLL Control Status
1AAC-1FEF	S/UNI 4xJET Reserved
1FF0	S/UNI 4xJET Transmit L2 Tristate Control LSB
1FF1	S/UNI 4xJET Transmit L2 Tristate Control MSB
1FF2	S/UNI 4xJET Receive L2 Tristate Control LSB
1FF3	S/UNI 4xJET Receive L2 Tristate Control MSB
1FF4-3FFF	S/UNI 4xJET Reserved

Normal mode registers are used to configure and monitor the operation of the S/UNI 4xJET. Normal mode registers (as opposed to test mode registers) are selected when A[13] is low.

Notes on Normal Mode Register Bits

1. For all register accesses, CSB must be low.

2. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

3. All configuration bits that can be written into can also be read back. This allows the processor controlling the S/UNI 4xJET to determine the programming state of the block.

4. Writeable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.

5. Writing into read-only normal mode register bit locations does not affect S/UNI 4xJET operation unless otherwise noted. Performance monitoring counter registers are a common exception.

6. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the S/UNI 4xJET operates as intended, reserved register bits must be written with their default value as indicated by the register bit description.

7. Writing any data to the S/UNI 4xJET Master Reset and Identity register (address 0x1800) simultaneously loads all the performance monitoring registers in the device.

   Writing to a Channel Reset and Performance Monitor Update register (channel address 0x006) will simultaneously load all the performance monitor registers in the channel.

8. Writing any data to the performance register in question may individually trigger the performance registers in each block. In some cases, all performance registers in the block are loaded. In other cases, only the specific register being written will load. See the register descriptions for the performance register in question for more information.

3.2 Initialization Script

This initialization script is to be performed after any reset of the S/UNI 4xJET device. Table 4 details the writes that must be performed.

Table 4 Initialization Writes and Values

Address(es)	Value to Write	Description
0x0206 0x0606 0x0806 0x0A06 0x0C06 0x0E06 0x1006 0x1406	0x0080	Reserved Register settings
0x0306 0x0706 0x0806 0x0B06 0x0D06 0x0F06 0x1106 0x1506	0x0020	Reserved Register settings
0x0307 0x0707 0x0807 0x0B07 0x0D07 0x0F07 0x1107 0x1507	0x0020	Reserved Register settings
0x0313 0x0713 0x0813 0x0B13 0x0D13 0x0F13 0x1113 0x1513	0x0000	Reserved Register settings
0x0319 0x0719 0x0819 0x0B19 0x0D19 0x0F19 0x1119 0x1519	0x0001	Reserved Register settings
0x1306	0x0008	Channel 1 : DTADRMASK[4:0] setup for normal operation
0x1307	0x0008	Channel 1 : DRADRMASK[4:0] setup for normal operation
0x1706	0x0008	Channel 3 : DTADRMASK[4:0] setup for normal operation

Address(es)	Value to Write	Description
0x1707	0x0008	Channel 3 : DRADRMASK[4:0] setup for normal operation
0x1802	0x0002	Reserved Register settings
0x1803	0x0082	Reserved Register settings
0x19A0	0x0000	Reserved Register settings
0x19A1	0x0000	Reserved Register settings
0x19A2	0x0187	Reserved Register settings

3.3 Channel Level Registers

Register 0x000, 0x400, 0x1200, 0x1600: Channel Configuration #1

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	1
Bit 6	R/W	DS27_53	1
Bit 5	R/W	TOCTA	0
Bit 4	R/W	FRMRONLY	0
Bit 3	R/W	LOOPT	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	PLOOP	0

PLOOP

The PLOOP bit controls the DS3, E3, or J2 payload loopback from the FRMR to the TRAN.

When a logic 0 is written to PLOOP, DS3, E3, or J2 payload loopback is disabled. When a logic 1 is written to PLOOP, the DS3, E3, or J2 overhead bits are regenerated and inserted into the received DS3, E3, or J2 stream and the resulting stream is transmitted using TRAN.

The TFRM[1:0] (channel address 0x002) and RFRM[1:0] (channel address 0x003) bits must be set to the same value for PLOOP to work properly.

This loopback has been further illustrated in PMC-2021632 “SUNI 4xJET ASSP Telecom Standard Product Data Sheet”.

LOOPT

The LOOPT bit selects the serial transmit timing source.

When a logic 1 is written to LOOPT, the serial transmitter is loop-timed to the serial receiver. In this mode, the receive clock (RCLK[x]) is used as the transmit timing source. The transmit nibble stuffing is derived from the nibble stuffing in the receive PLCP frame (for DS3 or E3 PLCP frame transmission). The FIXSTUFF bit (channel address 0x00C) must be set to logic 0 if the LOOPT bit is set to logic 1.

When a logic 0 is written to LOOPT, the transmit clock (TICLK) is used as the transmit timing source. The nibble stuffing is derived from the REF8KI input, or is fixed internally (as determined by the FIXSTUFF bit in channel address 0x00C) for DS3 or E3 PLCP frame transmission only.

Setting the LOOPT bit disables the effect of the TXREF (channel address 0x002) bit thereby forcing flow-through timing.

This timing loopback has been further illustrated in PMC-2021632 “SUNI 4xJET ASSP Telecom Standard Product Data Sheet.”

FRMRONLY

The FRMRONLY bit controls what drives the inputs to the TRAN. When a logic 1 is written to FRMRONLY, the input to the TRAN is controllable via the TRANSEL register bit (channel address 0x113). When a logic 0 is written to FRMRONLY, the TRAN is driven by the SPLT.

TOCTA

The TOCTA bit enables octet-alignment or nibble-alignment of the transmit cell stream to the transmission overhead when the arbitrary transmission format is chosen (TFRM[1:0] = 11 binary and SPLT Configuration register bit EXT = 1). This bit has no effect when DS3, G.751 E3, G.832 E3, J2, T1, or E1 formats are selected since octet or nibble alignment is specified for these formats.

When the arbitrary transmission format is chosen and TOCTA is set to logic 1, the ATM cell nibbles or octets are aligned to the arbitrary transmission format overhead boundaries (as set by the TIOHM[x] input). Nibble alignment is chosen if the FORM[1:0] bits in the SPLT Configuration are set to 00. Byte alignment is chosen if these FORM[1:0] bits are set to any other value. The number of TICLK[x] periods between transmission format overhead bit positions must be divisible by 4 (for nibble alignment) or 8 (for byte alignment). When TOCTA is set to logic 0, no octet alignment is performed , and there is no restriction on the number of TICLK[x] periods between transmission format overhead bit positions.

DS27_53

The DS27_53 bit is used to select between the long data structure (27 words in 16-bit mode and 53 bytes in 16-bit mode) and the short data structure (26 words in 16-bit mode and 52 bytes in 32-bit mode) on the ATM interface.

When DS27_53 is set to logic one, the RXCP and TXCP blocks are configured to operate with the long data structure. When DS27_53 is set to logic zero, the RXCP and TXCP are configured to operate with the short data structure. This bit is intended for use when operating in Level 2 UTOPIA mode (SMODE[2:0] = “X00”).

When configured for Level 3 UTOPIA, Level 3 POS-PHY, or Level 2 POS-PHY, this bit should be ser to logic 1.

Register 0x001, 0x401, 0x1201, 0x1601: Channel Configuration #2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	TXMFPI	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	TXMFPO	0
Bit 0	R/W	RXMFPO	0

RXMFPO

The RXMFPO bit controls which mode of the RFPO/RMFPO[x] output is valid. If RXMFPO is a logic 1, then RMFPO[x] will be available. If RXMFPO is a logic 0, then RFPO[x] will be available.

RFPO/RMFPO[x] has been further illustrated in PMC-2021632 “SUNI 4xJET ASSP Telecom Standard Product Data Sheet” Pin Description Section.

TXMFPO

The TXMFPO bit controls which mode of the TFPO/TMFPO[x] output is valid. If TXMFPO is a logic 1, then TMFPO[x] will be available. If TXMFPO is a logic 0, then TFPO[x] will be available.

TFPO/TMFPO[x] has been further illustrated in PMC-2021632 “SUNI 4xJET ASSP Telecom Standard Product Data Sheet” Pin Description Section.

TXMFPI

The TXMFPI bit controls which mode of the TFPI/TMFPI[x] input is valid. If TXMFPI is a logic 1, then TMFPI[x] will be expected. If TXMFPI is a logic 0, then TFPI[x] will be expected.

TFPI/TMFPI[x] has been further illustrated in PMC-2021632 “SUNI 4xJET ASSP Telecom Standard Product Data Sheet” Pin Description Section.

Register 0x002, 0x402, 0x1202, 0x1602: Channel Transmit Configuration #1

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	TFRM[1]	0
Bit 6	R/W	TFRM[0]	0
Bit 5	R/W	TXREF	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	TUNI	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	TPOSINV	0
Bit 0	R/W	TNEGINV	0

TNEGINV

The TNEGINV bit provides polarity control for outputs TNEG/TOHM[x]. When a logic 0 is written to TNEGINV, the TNEG/TOHM[x] output is not inverted. When a logic 1 is written to TNEGINV, the TNEG/TOHM[x] output is inverted.

TPOSINV

The TPOSINV bit provides polarity control for outputs TPOS/TDATO[x]. When a logic 0 is written to TPOSINV, the TPOS/TDATO[x] output is not inverted. When a logic 1 is written to TPOSINV, the TPOS/TDATO[x] output is inverted.

TUNI

The TUNI bit enables the S/UNI 4xJET to transmit unipolar or bipolar DS3, E3, or J2 data streams.

When a logic 1 is written to TUNI, the S/UNI 4xJET transmits unipolar DS3, E3, or J2 data on TDATO[x]. When TUNI is logic 1, the TOHM[x] output indicates the start of the DS3 M-Frame (the X1 bit), the start of the E3 frame (bit 1 of the frame), or the first framing bit of the J2 multi-frame.

When a logic 0 is written to TUNI, the S/UNI 4xJET transmits B3ZS-encoded DS3 data, HDB3-encoded E3 data, or B8ZS-encoded J2 data on TPOS[x] and TNEG[x]. The TUNI bit has no effect if TFRM[1:0] is set to 11 binary as the output data is automatically configured for unipolar format.

TXREF

The TXREF register bit determines if TICLK[0] and TIOHM/TFPI/TMFPI[0] should be used as the reference transmit clock and overhead/frame pulse, respectively, instead of TICLK[x] and TIOHM/TFPI/TMFPI[x]. If TXREF is set to a logic 1, then TICLK[0] and TIOHM/TFPI/TMFPI[0] will be used as the reference transmit clock and overhead/frame pulse, respectively. If TXREF is set to a logic 0, then TICLK[x] and TIOHM/TFPI/TMFPI[x] will be used as the reference transmit clock and overhead/frame pulse, respectively, for channel x. If loop-timing is enabled (LOOPT = 1), the TXREF bit has no effect on the corresponding channel.

When TXREF is set to logic 1, the unused TICLK[x] and TIOHM/TFPI/TMFPI[x] should be tied to power or ground and not left floating.

TFRM[1:0]

The TFRM[1:0] bits determine the frame structure of the transmitted signal according to the following table:

Table 5 Channel TFRM[1:0] Transmit Frame Structure Configurations

TFRM[1:0]	Transmit Frame Structure
00	DS3 (C-bit parity or M23 depending on the setting of the CBIT bit in the DS3 TRAN Configuration register)
01	E3 (G.751 or G.832 depending on the setting of the FORMAT[1:0] bits in the E3 TRAN Framing Options register)
10	J2 (G.704 and NTT compliant framing format)
11	DS1/E1/Arbitrary framing format - If the EXT bit in the SPLT Configuration register is a logic 0, then DS1 or E1 direct-mapped or PLCP framing is selected (via the PLCPEN and FORM[1:0] bits in the SPLT Configuration register) and TIOHM[x] should be tied low. If EXT is a logic 1, then the arbitrary framing format is selected and overhead positions are indicated by the TIOHM[x] input pin.

Register 0x003, 0x403, 0x1203, 0x1603: Channel Receive Configuration #1

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	RFRM[1]	0
Bit 6	R/W	RFRM[0]	0
Bit 5	R/W	LOFINT[1]	0
Bit 4	R/W	LOFINT[0]	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	RPOSINV	0
Bit 0	R/W	RNEGINV	0

RNEGINV

The RNEGINV bit provides polarity control for input RNEG/RLCV/ROHM[x]. When a logic 0 is written to RNEGINV, the input RNEG/RLCV/ROHM[x] is not inverted. When a logic 1 is written to RNEGINV, the input RNEG/RLCV/ROHM[x] is inverted.

RPOSINV

The RPOSINV bit provides polarity control for input RPOS/RDATI[x]. When a logic 0 is written to RPOSINV, the input RPOS/RDATI[x] is not inverted. When a logic 1 is written to RPOSINV, the input RPOS/RDATI[x] is inverted.

LOFINT[1:0]

The LOFINT[1:0] bits determine the integration period used for asserting and deasserting E3 and DS3 Loss of Frame or J2 extended Loss of Frame on the FRMLOF register bit of the Channel FRMR LOF Status register (channel address 0x09F) and on the FRMSTAT[x] output pin if this function is enabled by the LOFEN register bit of the Channel FRMSTAT Control Register (channel address 0x118). The integration times are selected as follows:

Table 6 Channel LOF[1:0] Integration Period Configuration

LOFINT[1:0]	Integration Period
00	3ms
01	2ms
10	1ms
11	Reserved

RFRM[1:0]

The RFRM[1:0] bits determine the expected frame structure of the received signal according to the following table:

Table 7 Channel RFRM[1:0] Receive Frame Structure Configurations

RFRM[1:0]	Expected Receive Frame Structure
00	DS3 (C-bit parity or M23 depending on the setting of the CBE bit in the DS3 FRMR Configuration register)
01	E3 (G.751 or G.832 depending on the setting of the FORMAT[1:0] bits in the E3 FRMR Framing Options register)
10	J2 (G.704 and NTT compliant framing format)
11	DS1/E1/Arbitrary framing format - when EXT in the SPLR Configuration register is a logic 0, then DS1 or E1 direct-mapped or PLCP framing is selected (via the PLCPEN and FORM[1:0] bits in the SPLR Configuration register) and the frame alignment is indicated by the ROHM[x] input pin. When EXT is a logic 1, then the arbitrary framing format is selected and overhead bit positions are indicated by the ROHM[x] input pin.

Register 0x004, 0x404, 0x1204, 0x1604: Channel Data Link and FERF/RAI Control

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	LCDEN	1
Bit 6	R/W	AISEN	1
Bit 5	R/W	RBLEN	1
Bit 4	R/W	OOFEN	1
Bit 3	R/W	LOSEN	1
Bit 2	R/W	TNETOP	0
Bit 1	R/W	RNETOP	0
Bit 0	R/W	DLINV	0

DLINV

The DLINV bit provides polarity control for the DS3 C-bit Parity path maintenance data link which is located in the 3 C-bits of M-subframe 5. When a logic 1 is written to DLINV, the path maintenance data link is inverted before being processed. When a logic 0 is written to DLINV, the path maintenance data link is not inverted before being processed.

The rationale behind this bit is as follows: currently ANSI standard T1.107 specifies that the C-bits (which carry the path maintenance data link) be set to all-zeros while the AIS maintenance signal is transmitted. The data link is obviously inactive during AIS transmission, and ideally the HDLC idle sequence (all-ones) should be transmitted. By inverting the data link, the all-zeros C-bit pattern becomes an idle sequence and the data link is terminated gracefully. Although this inversion is currently not specified in ANSI T1.107a, this bit is provided to safe-guard the Channel in case the inversion is required in the future.

RNETOP

The RNETOP bit enables the Network Operator Byte (NR) extracted from the G.832 E3 stream to be terminated by the internal HDLC receiver, RDLC. When RNETOP is logic 1, the NR byte is extracted from the G.832 stream and terminated by RDLC. When RNETOP is logic 0, the GC byte is extracted from the G.832 stream and terminated by RDLC.

Both the NR byte and the GC byte are extracted and output on the ROH pin for external processing.

TNETOP

The TNETOP bit enables the Network Operator Byte (NR) inserted in the G.832 E3 stream to be sourced by the internal HDLC transmitter, TDPR. When TNETOP is logic 1, the NR byte is inserted into the G.832 stream through the TDPR block; the GC byte of the G.832 E3 stream is sourced by through the TOH and TOHINS pins. If TOH and TOHINS are not active, then an all-ones signal will be inserted into the GC byte. When TNETOP is logic 0, the GC byte is inserted into the G.832 stream through the TDPR block; the NR byte of the G.832 E3 stream is sourced by the TOH and TOHINS pins. If TOH and TOHINS are not active, then an all-ones signal will be inserted into the NR byte.

For G.751 E3 streams, the National Use bit is sourced by the TDPR block if TNETOP and the NATUSE bit (channel address 0x041) are both logic 0. If either TNETOP or NATUSE is logic 1, the National Use bit will be sourced from the NATUSE register bit (channel address 0x041).

If the Channel is configured for DS3 or J2 operation, TNETOP has no effect. The DS3 C-bit Parity and J2 datalink is inserted into the DS3 or J2 stream through the internal HDLC transmitter TDPR.

The TOH and TOHINS input pins can be used to overwrite the values of these overhead bits in the serial transmit stream.

LOSEN

The LOSEN bit enables the serial receive loss of signal indication to automatically generate a FERF indication in the serial transmit stream. This bit operates regardless of framer selected (DS3, E3, or J2). When LOSEN is logic 1, assertion of the LOS indication by the framer causes a FERF (RAI in G.751 or J2 mode) to be transmitted by TRAN for the duration of the LOS assertion. When LOSEN is logic 0, assertion of the LOS indication does not cause transmission of a FERF/RAI.

For the RAI to be automatically transmitted when in J2 format, the FEAC[5:0] bits in the XBOC Code register (channel address 0x09B) must all be set to logic 1. If the XBOC FEAC code is to be transmitted in J2 mode, LOSEN, OOFEN, AISEN, and LCDEN should all be set to logic 0.

OOFEN

The OOFEN bit enables the receive out of frame indication to automatically generate a FERF indication (RAI in G.751 or J2 mode) in the serial transmit stream. This bit operates when the E3 or J2 framer is selected or when the DS3 framer is selected and the RBLEN bit is logic 0. When OOFEN is logic 1, assertion of the OOF indication by the framer causes a FERF/RAI to be transmitted by TRAN for the duration of the OOF assertion. When OOFEN is logic 0, assertion of the OOF indication does not cause transmission of a FERF/RAI.

For the RAI to be automatically transmitted when in J2 format, the FEAC[5:0] bits in the XBOC Code register (channel address 0x09B) must all be set to logic 1. If the XBOC FEAC code is to be transmitted in J2 mode, LOSEN, OOFEN, AISEN, and LCDEN should all be set to logic 0.

RBLEN

The RBLEN bit enables the receive RED alarm (persistent out of frame) indication to automatically generate a FERF indication in the DS3 transmit stream, or a BIP8 error detection in the E3 G.832 Framer to generate a FEBE indication in the E3 G.832 transmit stream, or an LOF to generate a RLOF indication (A-bit) in the J2 transmit stream. When the E3 G.751 framer is selected, this bit has no effect. When RBLEN is logic 1 and TFRM[1:0] is 00 binary and RFRM[1:0] is 00 binary, assertion of the RED indication by the framer causes a FERF to be transmitted by DS3_TRAN for the duration of the RED assertion. When RBLEN is logic 0, assertion of the RED indication does not cause transmission of a FERF. When RBLEN is logic 1 and TFRM[1:0] is 01 binary and RFRM[1:0] is 01 binary, any BIP8 error indication by the E3 G.832 framer causes a FEBE to be generated by the E3 G.832 TRAN. When RBLEN is logic 0, BIP8 errors detected by the E3 framer do not cause FEBEs to be generated by the E3_TRAN. When RBLEN is logic 1 and TFRM[1:0] is 10 binary and RFRM[1:0] is 10 binary, any LOF error indication by the J2 framer causes the RLOF bit (also known as the A bit) to be set in the J2 transmit stream. When RBLEN is logic 0, LOF errors detected by the J2 framer do not cause the RLOF bit to be set in the serial transmit stream.

AISEN

The AISEN bit enables the serial receive alarm indication signal to automatically generate a FERF indication (RAI in G.751 or J2 mode) in the serial transmit stream. This bit operates regardless of framer selected (DS3, E3, or J2). When AISEN is logic 1, assertion of the AIS indication (physical AIS for J2) by the framer causes a FERF/RAI to be transmitted by TRAN for the duration of the AIS assertion. When AISEN is logic 0, assertion of the AIS indication does not cause transmission of a FERF/RAI.

For the RAI to be automatically transmitted when in J2 format, the FEAC[5:0] bits in the XBOC Code register (channel address 0x09B) must all be set to logic 1. If the XBOC FEAC code is to be transmitted in J2 mode, LOSEN, OOFEN, AISEN, and LCDEN should all be set to logic 0.

LCDEN

The LCDEN bit enables the receive loss of cell delineation indication to automatically generate a FERF indication (RAI in G.751 or J2 mode) in the serial transmit stream. When LCDEN is logic 1, assertion of the LCD indication by the receive FIFO causes a FERF/RAI to be transmitted by the transmitter for the duration of the LCD assertion. When LCDEN is logic 0, assertion of the LCD indication does not cause transmission of a FERF/RAI. This bit is intended for use when operating in serial ATM mode. When configured for operating in serial bit-HDLC mode this bit should be set to logic 0.

For the RAI to be automatically transmitted when in J2 format, the FEAC[5:0] bits in the XBOC Code register (channel address 0x09B) must all be set to logic 1. If the XBOC FEAC code is to be transmitted in J2 mode, LOSEN, OOFEN, AISEN, and LCDEN should all be set to logic 0.

Register 0x005, 0x405, 0x1205, 0x1605: Channel Interrupt Status #1

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	SPLRI/TTBI	X
Bit 6	R	TXCPI	X
Bit 5	R	RXCPI	X
Bit 4	R	RBOCI/PRGDI	X
Bit 3	R	FRMRI/LOFI	X
Bit 2	R	PMONI	X
Bit 1	R	TDPRI	X
Bit 0	R	RDLCI	X

SPLRI/TTBI, TXCPI, RXCPI, RBOCI/PRGDI, FRMRI/LOFI, PMONI, TDPRI, RDLCI

These bits are interrupt status indicators. These bits identify the block that is the source of a pending interrupt. The SPLRI/TTBI bit will be logic 1 if either the SPLR or the TTB block has produced the interrupt. The RBOCI/PRGDI bit will be logic 1 if either the RBOC or PRGD block has produced the interrupt. The FRMRI/LOFI will be logic 1 if either the FRMR (J2, E3, or T3 - whichever one is enabled) or the E3, T3, or J2 Extended Loss of Frame signal (FRMLOFI from channel address 0x09F) is the source of the interrupt. This register is typically used by interrupt service routines to determine the source of a Channel interrupt.

Register 0x006, 0x406, 0x1206, 0x1606: Channel Reset and Performance Monitor Update

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	CHRST	0
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R	TIP	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

This register is used for performance monitor updates, and channel software resets. Writing any value except 8h into this register initiates latching of all performance monitor counts in the PMON, RXCP, TXCP, RXFP, and TXFP blocks in the channel. The TIP register bit is used to signal when the latching is complete.

The CPPM counter registers are not latched by writing to this register. Counters in the CPPM can only be updated by writing to CPPM counter registers (channel addresses 0x022 to 0x027).

TIP

The TIP bit is set to a logic one when any value is written to this register. Such a write initiates an accumulation interval transfer and loads all the performance meter registers in the PMON, PMON AUX, PRGD, RXCP, TXCP, RXFP, and TXFP blocks in the channel.

TIP remains high while the transfer is in progress, and is set to a logic zero when the transfer is complete. TIP can be polled by a microprocessor to determine when the accumulation interval transfer is complete.

Note that when configured for Cell/Packet direct mapped to SONET/SDH it is not a requirement to provide TICLK[x] and RCLK[x] since the serial interface is unused. To prevent TIP from getting stuck high when in this mode, need to set SQUELCHTIP (channel address 0x119) to logic 1.

CHRST

The CHRST bit allows the channel to be reset under software control. If the CHRST bit is a logic one, the channel is held in reset. This bit is not self clearing. Therefore, a logic zero must be written to bring the channel out of reset. Holding the channel in a reset state places it into a low power stand-by mode. A hardware reset or top level reset using RESET clears the CHRST bit, thus negating the software reset. Otherwise, the effect of the channel software reset is equivalent to that of a hardware reset.

Register 0x007, 0x407, 0x1207, 0x1607: Channel Clock Activity Monitor #1

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	RCLKA	X
Bit 2	R	TICLKA	X
Bit 1	R	TFCLKA	X
Bit 0	R	RFCLKA	X

RFCLKA

The RFCLKA bit monitors for low to high transitions on the RFCLK input. RFCLKA is set high on a rising edge of RFCLK, and is set low when this register is read.

TFCLKA

The TFCLKA bit monitors for low to high transitions on the TFCLK input. TFCLKA is set high on a rising edge of TFCLK, and is set low when this register is read.

TICLKA

The TICLKA bit monitors for low to high transitions on the TICLK[x] input. TICLKA is set high on a rising edge of TICLK[x], and is set low when this register is read.

RCLKA

The RCLKA bit monitors for low to high transitions on the RCLK[x] input. RCLKA is set high on a rising edge of RCLK[x], and is set low when this register is read.

Register 0x008, 0x408, 0x1208, 0x1608: SPLR Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	FORM[1]	0
Bit 6	R/W	FORM[0]	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	REFRAME	0
Bit 2	R/W	PLCPEN	0
Bit 1	—	Unused	X
Bit 0	R/W	EXT	0

EXT

The EXT bit disables the internal transmission system sublayer timeslot counter from identifying DS1, DS3, E1, J2, E3 G.751, or E3 G.832 overhead bits. The EXT bit allows transmission formats that are unsupported by the internal timeslot counter to be supported using the ROHM[x] input. When a logic 0 is written to EXT, input transmission system overhead (for DS1, DS3, E1, J2, E3 G.751, and E3 G.832 formats) is indicated using the internal timeslot counter. This counter is synchronized to the transmission system frame alignment using the ROHM[x] (for DS1 or E1 ATM direct-mapped formats), or by the integral framer block (for the DS3, J2, E3 G.751, or E3 G.832 formats).

When a logic 1 is written to EXT, indications on ROHM[x] identify each transmission system overhead bit.

PLCPEN

The PLCPEN bit enables PLCP framing. When a logic 1 is written to PLCPEN, PLCP framing is enabled. The PLCP format is specified by the FORM[1:0] bits in this register. When a logic 0 is written to PLCPEN, PLCP related functions in the SPLR block are disabled.

This bit is intended for use when operating in PLCP mapped ATM modes for DS3, E3 G.751, E1, and DS1 framing formats and has been further illustrated in PMC-2021632 “SUNI 4xJET ASSP Telecom Standard Product Data Sheet” Operations Section. When configured for any other operating mode, this bit should be set to logic 0.

REFRAME

The REFRAME bit is used to trigger reframing. When a logic 1 is written to REFRAME, the SPLR is forced out of PLCP frame and a new search for frame alignment is initiated. Note that only a logic 0 to logic 1 transition of the REFRAME bit triggers reframing; multiple write operations are required to ensure such a transition.

FORM[1:0]

The FORM[1:0] bits select the PLCP frame format as shown below. These bits must be set to "11" if E1 direct mapped mode is being used (PLCPEN=0 and EXT=1).

Table 8 SPLR FORM[1:0] Configurations

FORM[1]	FORM[0]	PLCP Framing Format
0	0	DS3
0	1	E3 G.751
1	0	DS1
1	1	E1

Register 0x009, 0x409, 0x1209, 0x1609: SPLR Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	FEBEE	0
Bit 5	R/W	COLSSE	0
Bit 4	R/W	BIPEE	0
Bit 3	R/W	FEE	0
Bit 2	R/W	YELE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	OOFE	0

OOFE

The OOFE bit enables interrupt generation when a PLCP out of frame defect is declared or removed. The interrupt is enabled when a logic 1 is written.

LOFE

The LOFE bit enables interrupt generation when a PLCP loss of frame defect is declared or removed. The interrupt is enabled when a logic 1 is written.

YELE

The YELE bit enables interrupt generation when a PLCP yellow alarm defect is declared or removed. The interrupt is enabled when a logic 1 is written.

FEE

The FEE bit enables interrupt generation when the SPLR detects a PLCP framing octet error. The interrupt is enabled when a logic 1 is written.

BIPEE

The BIPEE bit enables interrupt generation when the SPLR detects a PLCP bit interleaved parity error. The interrupt is enabled when a logic 1 is written.

COLSSE

The COLSSE bit enables interrupt generation when the SPLR detects a change of PLCP link status. The interrupt is enabled when a logic 1 is written.

FEBEE

The FEBEE bit enables interrupt generation when the SPLR detects a PLCP far end block error. The interrupt is enabled when a logic 1 is written.

Register 0x00A, 0x40A, 0x120A, 0x160A: SPLR Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R	FEBEI	X
Bit 5	R	COLSSI	X
Bit 4	R	BIPEI	X
Bit 3	R	FEI	X
Bit 2	R	YELI	X
Bit 1	R	LOFI	X
Bit 0	R	OOFI	X

OOFI

The OOFI bit is set to logic 1 when a PLCP out of frame defect is detected or removed. The OOF defect state is contained in the SPLR Status Register. The OOFI bit position is set to logic 0 when this register is read.

LOFI

The LOFI bit is set to logic 1 when a PLCP loss of frame defect is detected or removed. The LOF defect state is contained in the SPLR Status Register. The LOFI bit position is set to logic 0 when this register is read.

YELI

The YELI bit is set to logic 1 when a PLCP yellow alarm defect is detected or removed. The yellow alarm defect state is contained in the SPLR Status Register. The YELI bit position is set to logic 0 when this register is read.

FEI

The FEI bit is set to logic 1 when a PLCP framing octet error is detected. A framing octet error is generated when one or more errors are detected in the framing alignment octets (A1, and A2), or the path overhead identification octets. The FEI bit position is set to logic 0 when this register is read.

BIPEI

The BIPEI bit is set to logic 1 when a PLCP bit interleaved parity (BIP) error is detected. BIP errors are detected using the B1 byte in the PLCP path overhead. The BIPEI bit position is set to logic 0 when this register is read.

COLSSI

The COLSSI bit is set to logic 1 when a PLCP change of link status signal code is detected. The link status signal code is contained in the path status octet (G1). Link status signal codes are required in systems implementing the IEEE-802.6 DQDB protocol. A change of link status event occurs when two consecutive and identical link status codes are received that differ from the current code. The COLSSI bit position is set to logic 0 when this register is read.

FEBEI

The FEBEI bit is set to logic 1 when a PLCP far end block error (FEBE) is detected. FEBE errors are indicated in the PLCP path status octet (G1). The FEBEI bit position is set to logic 0 when this register is read.

Register 0x00B, 0x40B, 0x120B, 0x160B: SPLR Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R	LSS[2]	X
Bit 5	R	LSS[1]	X
Bit 4	R	LSS[0]	X
Bit 3	—	Unused	X
Bit 2	R	YELV	X
Bit 1	R	LOFV	X
Bit 0	R	OOFV	X

OOFV

The OOFV bit indicates the current PLCP out of frame defect state. When an error is detected in both the A1 and A2 octets or when an error is detected in two consecutive path overhead identifier octets, OOFV is set to logic 1. When the S/UNI 4xJET has found two valid, consecutive sets of A1 and A2 octets with two valid and sequential path overhead identifier octets, the OOFV bit is set to logic 0.

LOFV

The LOFV bit indicates the current PLCP loss of frame defect state. The loss of frame defect state is an integrated version of the out of frame defect state. The declaration/removal times for the loss of frame defect state depends on the selected PLCP format, and are summarized in the table below:

Table 9 SPLR PLCP LOF Declaration/Removal Times

PLCP Format	Declaration (ms)	Removal (ms)
DS3	1	12
E3 G.751	1.12	10
DS1	25	250
E1	20	200

If the OOF defect state is transient, the LOF counter is decremented at a rate 1/12 (DS3 PLCP) or 1/10 (DS1 or E1 PLCP) or 1/9 (G.751 E3 PLCP) of the incrementing rate.

YELV

The YELV bit indicates the current PLCP yellow alarm defect state. YELV is set to a logic 1 when ten or more consecutive frames are received with the yellow bit (contained in the path status octet) set to a logic 1. YELV is set to a logic 0 when ten or more consecutive frames are received with the yellow bit (contained in the path status octet) set to a logic 0.

LSS[2:0]

The LSS[2:0] bits contain the current link status signal code. Link status signal codes are required in systems implementing the IEEE-802.6 DQDB protocol. LSS[2:0] is updated when two consecutive and identical link status signal codes are received.

Register 0x00C, 0x40C, 0x120C, 0x160C: SPLT Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	FORM[1]	0
Bit 6	R/W	FORM[0]	0
Bit 5	R/W	M1TYPE	0
Bit 4	R/W	M2TYPE	0
Bit 3	R/W	FIXSTUFF	0
Bit 2	R/W	PLCPEN	0
Bit 1	—	Unused	X
Bit 0	R/W	EXT	0

EXT

The EXT bit disables the internal transmission system sublayer timeslot counter from identifying DS1, DS3, E1, J2, E3 G.751, or E3 G.832 overhead bits. The EXT bit allows transmission formats that are unsupported by the internal timeslot counter and must be supported using the TIOHM[x] input. When a logic 0 is written to EXT, input transmission system overhead (for DS1, DS3, E1, J2, E3 G.751, and E3 G.832 formats) is indicated using the internal timeslot counter. This counter flywheels to create the appropriate transmission system alignment. This alignment is indicated on the TOHM[x] output. When a logic 1 is written to EXT, indications on TIOHM[x] identify each transmission system overhead bit. These indications flow through the S/UNI 4xJET and appear on the TOHM[x] output where they mark the transmission system overhead placeholder positions in the TDATO[x] stream.

This bit is intended for use when operating in arbitrary framing mode (TFRM[1:0] = “11”), or in flexible bandwidth mode (FBWEN = ‘1’) and has been further illustrated in PMC-2021632 “SUNI 4xJET ASSP Telecom Standard Product Data Sheet” Operations Section. When configured for any other operating mode, this bit should be set to logic 0.

PLCPEN

The PLCPEN bit enables PLCP frame insertion. When a logic 1 is written to PLCPEN, DS3, E3 G.751, DS1, or E1 PLCP framing is inserted. The PLCP format is specified by the FORM[1:0] bits in this register. When a logic 0 is written to PLCPEN, PLCP related functions in the SPLT block are disabled.

This bit is intended for use when operating in PLCP mapped ATM modes for DS3, E3 G.751, E1, and DS1, framing formats and has been further illustrated in PMC-2021632 "SUNI 4xJET ASSP Telecom Standard Product Data Sheet" Operations Section. When configured for any other operating mode, this bit should be set to logic 0.

FIXSTUFF

The FIXSTUFF bit controls the transmit PLCP frame octet/nibble stuffing used for DS3 and G.751 E3 PLCP frame formats. When a logic 0 is written to FIXSTUFF, stuffing is determined by the REF8KI input. When a logic 1 is written to FIXSTUFF and the DS3 PLCP frame format is enabled, a nibble is stuffed into the 13 nibble trailer twice every three stuff opportunities (i.e. 13, 14, 14 nibbles). This stuff ratio provides for a nominal PLCP frame rate of 125.0002366 µs (an error of 1.9 ppm). When the G.751 E3 PLCP frame format is enabled, 18, 19, or 20 octets are stuffed into the trailer depending on the alignment of the G.751 E3 frame, and the G.751 E3 PLCP frame. This yields a nominal PLCP frame rate of 125 µs.

M2TYPE

The M2TYPE bit selects the type of code transmitted in the M2 octet. These codes are required in systems implementing the IEEE-802.6 DQDB protocol. When a logic 0 is written to M2TYPE, the fixed pattern type 0 code is transmitted in the M2 octet. When a logic 1 is written to M2TYPE, the 1023 cyclic code pattern (starting with B6 hexadecimal and ending with 8D hexadecimal) is transmitted in the M2 octet. Please refer to TA-TSY-000772, Issue 3 and Supplement 1, for details on the codes.

M1TYPE

The M1TYPE bit selects the type of code transmitted in the M1 octet. These codes are required in systems implementing the IEEE-802.6 DQDB protocol. When a logic 0 is written to M1TYPE, the fixed pattern type 0 code is transmitted in the M1 octet. When a logic 1 is written to M1TYPE, the 1023 cyclic code pattern (starting with B6 hexadecimal and ending with 8D hexadecimal) is transmitted in the M1 octet. Please refer to TA-TSY-000772, Issue 3 and Supplement 1, for details on the codes.

FORM[1:0]

When EXT = 0 and PLCPEN = 0, the FORM[1:0] bits and the TFRM[1:0] bits in the S/UNI 4xJET Transmit Configuration register select the ATM direct-mapped transmission frame format as shown below. When EXT = 0 and PLCPEN = 1, the FORM[1:0] bits along with the TFRM[1:0] bits select the transmission and PLCP frame format as shown below. When EXT = 1 and TOCTA = 1, then the FORM[1:0] bits control the cell alignment with respect to the transmission overhead given on TIOHM[x] as shown below. The FORM bits have no effect if EXT = 1 and TOCTA = 0.

Table 10 SPLT FORM[1:0] Configurations

FORM[1]	FORM[0]	PLCP or ATM Direct-mapped Framing Format/Cell Alignment
0	0	DS3 / nibble
0	1	E3 or J2 / byte
1	0	DS1 / byte
1	1	E1 / byte

Register 0x00D, 0x40D, 0x120D, 0x160D: SPLT Control

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	SRCZN	0
Bit 5	R/W	SRCF1	0
Bit 4	R/W	SRCB1	0
Bit 3	R/W	SRCG1	0
Bit 2	R/W	SRCM1	0
Bit 1	R/W	SRCM2	0
Bit 0	R/W	SRCC1	0

The SRCxx bits refer to the THPINS/TPH inputs that correspond to their respective PLCP overhead byte (C1, M2, M1, G1, B1, F1, ZN). Refer to Transmit Overhead Insertion Section in the SUNI 4xJET ASSP Telecom Standard Product Data Sheet (PMC-2021632) for overhead alignment details regarding TPHINS/TPH.

SRCC1

The SRCC1 bit value ORed with input TPHINS selects the source for the C1 octet on a bit by bit basis. If the OR results in a logic 0, the C1 bit position is derived internally as specified by the FIXSTUFF bit in the SPLT Configuration Register. If the OR results in a logic 1, the C1 bit position is inserted with the value sampled on TPH.

SRCM2

The SRCM2 bit value ORed with input TPHINS selects the source for the M2 octet on a bit by bit basis. If the OR results in a logic 0, the M2 bit position is derived internally as specified by the M2TYPE bit in the SPLT Configuration Register. If the OR results in a logic 1, the M2 bit position is inserted with the value sampled on TPH.

The M2 octet is set to logic 0 (as required by the ATM Forum User Network Interface specification) by writing this bit with a logic 1, and inserting all-zeros via TPH and TPHINS during M2 octet position.

SRCM1

The SRCM1 bit value ORed with input TPHINS selects the source for the M1 octet on a bit by bit basis. If the OR results in a logic 0, the M1 bit position is derived internally as specified by the M1TYPE bit in the SPLT Configuration Register. If the OR results in a logic 1, the M1 bit position is inserted with the value sampled on TPH.

The M1 octet is set to logic 0 (as required by the ATM Forum User Network Interface specification) by writing this bit with a logic 1, and inserting all-zeros via TPH and TPHINS during M1 octet position.

SRCG1

The SRCG1 bit value ORed with input TPHINS selects the source for the G1 octet on a bit by bit basis. If the OR results in a logic 0, the G1 bit position is derived internally as required. If the OR results in a logic 1, the G1 bit position is inserted with the value sampled on TPH.

SRCB1

The SRCB1 bit value ORed with input TPHINS selects the source for the B1 octet on a bit by bit basis. If the OR results in a logic 0, the internally calculated bit interleaved parity value is inserted in the B1 bit position. If the OR results in a logic 1, the B1 bit position is inserted with the value sampled on TPH.

SRCF1

The SRCF1 bit value ORed with input TPHINS selects the source for the F1 octet on a bit by bit basis. If the OR results in a logic 0, the F1 bit position is determined by the SPLT F1 Octet Register. If the OR results in a logic 1, the F1 bit position is inserted with the value sampled on TPH.

SRCZN

The SRCZN bit value ORed with input TPHINS selects the source for the Zn octets (where n=1 to 4 for the DS1 or E1 PLCP frame formats, n=1 to 6 for the DS3 PLCP frame format, and n=1 to 3 for the G.751 E3 PLCP frame format) on a bit by bit basis. If the OR results in a logic 0, the Zn bit position is forced to a logic 0. If the OR results in a logic 1, the Zn bit position is inserted with the value sampled on TPH.

Register 0x00E, 0x40E, 0x120E, 0x160E: SPLT Diagnostics and G1 Octet

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	DPFRM	0
Bit 6	R/W	DAFRM	0
Bit 5	R/W	DB1	0
Bit 4	R/W	DFEBE	0
Bit 3	R/W	YEL	0
Bit 2	R/W	LSS[2]	0
Bit 1	R/W	LSS[1]	0
Bit 0	R/W	LSS[0]	0

LSS[2:0]

The LSS[2:0] bits control the value inserted in the link status signal code bit positions of the path status octet (G1). These bits should be written with logic 0 when implementing an ATM Forum UNI-compliant DS3 interface.

YEL

The YEL bit controls the yellow signal bit position in the path status octet (G1). When a logic 1 is written to YEL, the PLCP yellow alarm signal is transmitted.

DFEBE

The DFEBE bit controls the insertion of far end block errors in the PLCP frame. When DFEBE is written with a logic 1, a single FEBE is inserted each PLCP frame. When DFEBE is written with a logic 0, FEBEs are indicated based on receive PLCP bit interleaved parity errors.

DB1

The DB1 bit controls the insertion of bit interleaved parity (BIP) errors in the PLCP frame. When DB1 is written with a logic 1, a single BIP error is inserted in each PLCP frame. When DB1 is written with a logic 0, the bit interleaved parity is calculated and inserted normally.

DAFRM

The DAFRM bit controls the insertion of frame alignment pattern errors. When DAFRM is written with a logic 1, a single bit error is inserted in each A1 octet, and in each A2 octet. When DAFRM is written with a logic 0, the frame alignment pattern octets are inserted normally.

DPFRM

The DPFRM bit controls the insertion of parity errors in the path overhead identification (POHID) octets. When DPFRM is written with a logic 1, a parity error is inserted in each POHID octet. When DPFRM is written with a logic 0, the POHID octets are inserted normally.

Register 0x00F, 0x40F, 0x120F, 0x160F: SPLT F1 Octet

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	F1[7]	0
Bit 6	R/W	F1[6]	0
Bit 5	R/W	F1[5]	0
Bit 4	R/W	F1[4]	0
Bit 3	R/W	F1[3]	0
Bit 2	R/W	F1[2]	0
Bit 1	R/W	F1[1]	0
Bit 0	R/W	F1[0]	0

F1[7:0]

The F1[7:0] bits contain the value inserted in the path user channel octet (F1). F1[7] is the most significant bit, and is transmitted first. F1[0] is the least significant bit and is the last bit transmitted in the octet.

Register 0x010, 0x410, 0x1210, 0x1610: PMON Change of PMON Performance Meters

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	LCVCH	X
Bit 4	R	FERRCH	X
Bit 3	R	EXZS	X
Bit 2	R	PERRCH	X
Bit 1	R	CPERRCH	X
Bit 0	R	FEBECH	X

FEBECH

The FEBECH bit is set to logic 1 if one or more FEBE events (or J2 EXZS events when the J2 framing format is selected) have occurred during the latest PMON accumulation interval.

CPERRCH

The CPERRCH bit is set to logic 1 if one or more path parity error events (or E3 frame error events when the E3 G.832 framing format is selected) have occurred during the latest PMON accumulation interval.

PERRCH

The PERRCH bit is set to logic 1 if one or more parity error events (or J2 CRC-5 errors) have occurred during the latest PMON accumulation interval.

EXZS

The EXZS bit is set to logic 1 if one or more summed line code violation events in DS3 mode have occurred during the latest PMON accumulation interval.

FERRCH

The FERRCH bit is set to logic 1 if one or more F-bit or M-bit error events have occurred during the latest PMON accumulation interval.

LCVCH

The LCVCH bit is set to logic 1 if one or more line code violation events have occurred during the latest PMON accumulation interval.

Register 0x011, 0x411, 0x1211, 0x1611: PMON Interrupt Enable/Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	INTE	0
Bit 1	R	INTR	X
Bit 0	R	OVR	X

OVR

The OVR bit indicates the overrun status of the PMON holding registers. A logic 1 in this bit position indicates that a previous interrupt has not been cleared before the end of the next accumulation interval, and that the contents of the holding registers have been overwritten. A logic 0 indicates that no overrun has occurred. This bit is reset to logic 0 when this register is read.

INTR

The INTR bit indicates the current status of the interrupt signal. A logic 1 in this bit position indicates that a transfer of counter values to the holding registers has occurred; a logic 0 indicates that no transfer has occurred. The INTR bit is set to logic 0 when this register is read.

INTE

The INTE bit enables the generation of an interrupt when the PMON counter values are transferred to the holding registers. When a logic 1 is written to INTE, the interrupt generation is enabled.

Register 0x014, 0x414, 0x1214, 0x1614: PMON Line Code Violation Event Count LSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

Register 0x015, 0x415, 0x1215, 0x1615: PMON Line Code Violation Event Count MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	LCV[15]	X
Bit 6	R	LCV[14]	X
Bit 5	R	LCV[13]	X
Bit 4	R	LCV[12]	X
Bit 3	R	LCV[11]	X
Bit 2	R	LCV[10]	X
Bit 1	R	LCV[9]	X
Bit 0	R	LCV[8]	X

LCV[15:0]

LCV[15:0] represents the number of DS3, E3, or J2 line code violation errors that have been detected by the FRMR since the last time the LCV counter was polled.

This counter (and all other counters in the PMON) is polled by writing to any of the PMON counter registers (channel addresses 0x014 to 0x01F) or to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800). Such a write transfers the internally accumulated count to the LCV Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 0x016, 0x416, 0x1216, 0x1616: PMON Framing Bit Error Event Count LSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	FERR[7]	X
Bit 6	R	FERR[6]	X
Bit 5	R	FERR[5]	X
Bit 4	R	FERR[4]	X
Bit 3	R	FERR[3]	X
Bit 2	R	FERR[2]	X
Bit 1	R	FERR[1]	X
Bit 0	R	FERR[0]	X

Register 0x017, 0x417, 0x1217, 0x1617: PMON Framing Bit Error Event Count MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R	FERR[9]	X
Bit 0	R	FERR[8]	X

FERR[9:0]

FERR[9:0] represents the number of DS3 F-bit and M-bit errors, or E3 or J2 framing pattern errors, that have been detected by the FRMR since the last time the framing error counter was polled. This counter is paused when the corresponding framer has lost frame alignment.

This counter (and all other counters in the PMON) is polled by writing to any of the PMON counter registers (channel addresses 0x014 to 0x01F) or to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800). Such a write transfers the internally accumulated count to the FERR Error Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 0x018, 0x418, 0x1218, 0x1618: PMON Excessive Zero Count LSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	EXZS[7]	X
Bit 6	R	EXZS[6]	X
Bit 5	R	EXZS[5]	X
Bit 4	R	EXZS[4]	X
Bit 3	R	EXZS[3]	X
Bit 2	R	EXZS[2]	X
Bit 1	R	EXZS[1]	X
Bit 0	R	EXZS[0]	X

Register 0x019, 0x419, 0x1219, 0x1619: PMON Excessive Zero Count MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	EXZS[15]	X
Bit 6	R	EXZS[14]	X
Bit 5	R	EXZS[13]	X
Bit 4	R	EXZS[12]	X
Bit 3	R	EXZS[11]	X
Bit 2	R	EXZS[10]	X
Bit 1	R	EXZS[9]	X
Bit 0	R	EXZS[8]	X

EXZS[15:0]

In DS3 mode, EXZS[15:0] represents the number of summed Excessive Zeros (EXZS) that occurred during the previous accumulation interval. One or more excessive zeros occurrences within an 85 bit DS3 information block is counted as one summed excessive zero. Excessive zeros are accumulated by this register only when the EXZSO and EXZDET are logic 1 in the DS3 FRMR Additional Configuration Register. This register accumulates summed line code violations when the EXZSO is logic 0. The count of summed line code violations is defined as the number of DS3 information blocks (85 bits) that contain one or more line code violations since the last time the summed LCV counter was polled.

This counter (and all other counters in the PMON) is polled by writing to any of the PMON counter registers (channel addresses 0x014 to 0x01F) or to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800). Such a write transfers the internally accumulated count to the EXZS Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 0x01A, 0x41A, 0x121A, 0x161A: PMON Parity Error Event Count LSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	PERR[7]	X
Bit 6	R	PERR[6]	X
Bit 5	R	PERR[5]	X
Bit 4	R	PERR[4]	X
Bit 3	R	PERR[3]	X
Bit 2	R	PERR[2]	X
Bit 1	R	PERR[1]	X
Bit 0	R	PERR[0]	X

Register 0x01B, 0x41B, 0x121B, 0x161B: PMON Parity Error Event Count MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	PERR[15]	X
Bit 6	R	PERR[14]	X
Bit 5	R	PERR[13]	X
Bit 4	R	PERR[12]	X
Bit 3	R	PERR[11]	X
Bit 2	R	PERR[10]	X
Bit 1	R	PERR[9]	X
Bit 0	R	PERR[8]	X

PERR[15:0]

PERR[15:0] represents the number of DS3 P-bit errors, the number of E3 G.832 BIP-8 errors or the number of J2 CRC-5 errors that have been detected by the FRMR since the last time the parity error counter was polled. This counter is paused when the corresponding framer has lost frame alignment.

This counter (and all other counters in the PMON) is polled by writing to any of the PMON counter registers (channel addresses 0x014 to 0x01F) or to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800). Such a write transfers the internally accumulated count to the PERR Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 0x01C, 0x41C, 0x121C, 0x161C: PMON Path Parity Error/E3-FRMERR Event Count LSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	CPERR/FRMERR[7]	X
Bit 6	R	CPERR/FRMERR[6]	X
Bit 5	R	CPERR/FRMERR[5]	X
Bit 4	R	CPERR/FRMERR[4]	X
Bit 3	R	CPERR/FRMERR[3]	X
Bit 2	R	CPERR/FRMERR[2]	X
Bit 1	R	CPERR/FRMERR[1]	X
Bit 0	R	CPERR/FRMERR[0]	X

Register 0x01D, 0x41D, 0x121D, 0x161D: PMON Path Parity Error/E3-FRMERR Event Count MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	CPERR/FRMERR[13]	X
Bit 4	R	CPERR/FRMERR[12]	X
Bit 3	R	CPERR/FRMERR[11]	X
Bit 2	R	CPERR/FRMERR[10]	X
Bit 1	R	CPERR/FRMERR[9]	X
Bit 0	R	CPERR/FRMERR[8]	X

CPERR/FRMERR[13:0]

CPERR/FRMERR[13:0] represents the number of DS3 path parity errors, or the number of E3 G.832 frame errors that have been detected by the FRMR since the last time the parity/frame error counter was polled. This counter is forced to zero when configured for J2 applications. This counter is paused when the corresponding framer has lost frame alignment.

This counter (and all other counters in the PMON) is polled by writing to any of the PMON counter registers (channel addresses 0x014 to 0x01F) or to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800). Such a write transfers the internally accumulated count to the CPERR Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 0x01E, 0x41E, 0x121E, 0x161E: PMON FEBE/J2-EXZS Event Count LSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	FEBE/J2-EXZS[7]	X
Bit 6	R	FEBE/J2-EXZS[6]	X
Bit 5	R	FEBE/J2-EXZS[5]	X
Bit 4	R	FEBE/J2-EXZS[4]	X
Bit 3	R	FEBE/J2-EXZS[3]	X
Bit 2	R	FEBE/J2-EXZS[2]	X
Bit 1	R	FEBE/J2-EXZS[1]	X
Bit 0	R	FEBE/J2-EXZS[0]	X

Register 0x01F, 0x41F, 0x121F, 0x161F: PMON FEBE/J2-EXZS Event Count MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	FEBE/J2-EXZS[13]	X
Bit 4	R	FEBE/J2-EXZS[12]	X
Bit 3	R	FEBE/J2-EXZS[11]	X
Bit 2	R	FEBE/J2-EXZS[10]	X
Bit 1	R	FEBE/J2-EXZS[9]	X
Bit 0	R	FEBE/J2-EXZS[8]	X

FEBE/J2-EXZS[13:0]

FEBE/J2-EXZS[13:0] represents the number of DS3 or E3 G.832 far end block errors that have been detected by the FRMR since the last time the FEBE error counter was polled.

In J2 mode, FEBE/J2-EXZS[13:0] represents the number of Excessive Zeros (EXZS is a string of 8 or more consecutive zeros) that have occurred during the previous accumulation interval.

This counter (and all other counters in the PMON) is polled by writing to any of the PMON counter registers (channel addresses 0x014 to 0x01F) or to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800). Such a write transfers the internally accumulated count to the FEBE Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 0x021, 0x421, 0x1221, 0x1621: CPPM Change of CPPM Performance Meters

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R	FEBECH	X
Bit 1	R	FECH	X
Bit 0	R	BIPECH	X

BIPECH

The BIPECH bit is set to logic 1 if one or more PLCP bit interleaved parity error events have occurred since the last CPPM accumulation interval.

FECH

The FECH bit is set to logic 1 if one or more PLCP frame alignment pattern octet errors, or path overhead identification octet errors have occurred since the last CPPM accumulation interval.

FEBECH

The FEBECH bit is set to logic 1 if one or more PLCP far end block error events have occurred since the last CPPM accumulation interval.

Register 0x022, 0x422, 0x522, 0x1622: CPPM B1 Error Count LSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	B1E[7]	X
Bit 6	R	B1E[6]	X
Bit 5	R	B1E[5]	X
Bit 4	R	B1E[4]	X
Bit 3	R	B1E[3]	X
Bit 2	R	B1E[2]	X
Bit 1	R	B1E[1]	X
Bit 0	R	B1E[0]	X

Register 0x023, 0x423, 0x1223, 0x1623: CPPM B1 Error Count MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	B1E[15]	X
Bit 6	R	B1E[14]	X
Bit 5	R	B1E[13]	X
Bit 4	R	B1E[12]	X
Bit 3	R	B1E[11]	X
Bit 2	R	B1E[10]	X
Bit 1	R	B1E[9]	X
Bit 0	R	B1E[8]	X

B1E[15:0]

B1E[15:0] represents the number of PLCP bit interleaved parity (BIP) errors that have been detected since the last time the B1 error counter was polled.

This counter (and all other counters in the CPPM) is polled by writing to any of the CPPM counter registers (channel addresses 0x022 to 0x027). Such a write transfers the internally accumulated count to the B1 Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. The transfer and reset is carried out in a manner that coincident events are not lost. B1 errors are not accumulated when the S/UNI 4xJET has declared a PLCP loss of frame defect state.

This transfer occurs within 67 RCLK periods (1.5 µs for the DS3 bit rate; 1.95µs for the E3 bit rate) of the write.

Register 0x024, 0x424, 0x1224, 0x1624: CPPM Framing Error Event Count LSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	FE[7]	X
Bit 6	R	FE[6]	X
Bit 5	R	FE[5]	X
Bit 4	R	FE[4]	X
Bit 3	R	FE[3]	X
Bit 2	R	FE[2]	X
Bit 1	R	FE[1]	X
Bit 0	R	FE[0]	X

Register 0x025, 0x425, 0x1225, 0x1625: CPPM Framing Error Event Count MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	FE[11]	X
Bit 2	R	FE[10]	X
Bit 1	R	FE[9]	X
Bit 0	R	FE[8]	X

FE[11:0]

FE[11:0] represents the number of PLCP framing pattern octet errors and path overhead identification octet errors that have been detected since the last time the framing error event counter was polled.

This counter (and all other counters in the CPPM) is polled by writing to any of the CPPM counter registers (channel addresses 0x022 to 0x027). Such a write transfers the internally accumulated count to the Framing Error Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. The transfer and reset is carried out in a manner that coincident events are not lost. Framing error errors are not accumulated when the S/UNI 4xJET has declared a PLCP loss of frame defect state.

This transfer occurs within 67 RCLK periods (1.5 µs for the DS3 bit rate; 1.95µs for the E3 bit rate) of the write.

Register 0x026, 0x426, 0x1226, 0x1626: CPPM FEBE Count LSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register 0x027, 0x427, 0x1227, 0x1627: CPPM FEBE Count MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	FEBE[15]	X
Bit 6	R	FEBE[14]	X
Bit 5	R	FEBE[13]	X
Bit 4	R	FEBE[12]	X
Bit 3	R	FEBE[11]	X
Bit 2	R	FEBE[10]	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

FEBE[11:0]

FEBE[11:0] represents the number of PLCP far end block errors (FEBE) that have been detected since the last time the FEBE error counter was polled.

This counter (and all other counters in the CPPM) is polled by writing to any of the CPPM counter registers (channel addresses 0x022 to 0x027). Such a write transfers the internally accumulated count to the FEBE Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. The transfer and reset is carried out in a manner that coincident events are not lost. FEBE errors are not accumulated when the S/UNI 4xJET has declared a PLCP loss of frame defect state.

This transfer occurs within 67 RCLK periods (1.5 µs for the DS3 bit rate; 1.95µs for the E3 bit rate) of the write.

Register 0x030, 0x430, 0x1230, 0x1630: DS3 FRMR Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	AISPAT	1
Bit 6	R/W	FDET	0
Bit 5	R/W	MBDIS	0
Bit 4	R/W	M3O8	0
Bit 3	R/W	UNI	0
Bit 2	R/W	REFR	0
Bit 1	R/W	AISC	0
Bit 0	R/W	CBE	0

CBE

The CBE bit enables the DS3 C-bit parity application. When a logic 1 is written to CBE, C-bit parity mode is enabled. When a logic 0 is written to CBE, the DS3 M23 format is selected. While the C-bit parity application is enabled, C-bit parity error events, far end block errors are accumulated.

AISC

The AISC bit controls the algorithm used to detect the alarm indication signal (AIS). When a logic 1 is written to AISC, the algorithm checks that a framed DS3 signal with all C-bits set to logic 0 is observed for a period of time before declaring AIS. The payload contents are checked to the pattern selected by the AISPAT bit. When a logic 0 is written to AISC, the AIS detection algorithm is determined solely by the settings of AISPAT and AISONES register bits (see bit mapping table in the Additional Configuration Register description).

REFR

The REFR bit initiates a DS3 reframe. When a logic 1 is written to REFR, the DS3 FRMR is forced out-of-frame, and a new search for frame alignment is initiated. Note that only a low to high transition of the REFR bit triggers reframing; multiple write operations are required to ensure such a transition.

UNI

The UNI bit configures the DS3 FRMR to accept either dual-rail or single-rail DS3 stream. When a logic 1 is written to UNI, the DS3 FRMR accepts a single-rail DS3 stream. When a logic 0 is written to UNI, the DS3 FRMR accepts a B3ZS-encoded dual-rail DS3 stream.

What sources the DS3 stream is selectable via the FRMRSEL (channel address 0x113) register bit. When a logic 1 is written to FRMRSEL, the D3E3MD sources a single-rail DS3 stream and UNI should be set to logic 1. When a logic 0 is written to FRMRSEL, the receive serial interface sources a single-rail or dual-rail DS3 stream on RPOS/RDATI[x] and RNEG/RLCV/ROHM[x]. In this case, when UNI is set to logic 1, the DS3 FRMR accepts a single-rail DS3 stream and accumulates line code violations on the RNEG/RLCV/ROHM[x] input.

M3O8

The M3O8 bit controls the DS3 out of frame decision criteria. When a logic 1 is written to M3O8, DS3 out of frame is declared when 3 of 8 framing bits (F-bits) are in error. When a logic 0 is written to M3O8, the 3 of 16 framing bits in error criteria is used, as recommended in ANSI T1.107.

MBDIS

The MBDIS bit disables the use of M-bit errors as a criteria for losing frame alignment. When MBDIS is set to logic 1, M-bit errors are disabled from causing an OOF; the loss of frame criteria is based solely on the number of F-bit errors selected by the M3O8 bit. When MBDIS is set to logic 0, errors in either M-bits or F-bits are enabled to cause an OOF. When MBDIS is logic 0, an OOF can occur when one or more M-bit errors occur in 3 out of 4 consecutive M-frames, or when the F-bit error ratio selected by the M3O8 bit is exceeded.

FDET

The FDET bit selects the fast detection timing for AIS, IDLE and RED. When FDET is set to logic 1, the AIS, IDLE, and RED detection time is 2.23 ms; when FDET is set to logic 0, the detection time is 13.5 ms.

AISPAT

The AISPAT bit controls the pattern used to detect the alarm indication signal (AIS). When a logic 1 is written to AISPAT, the AIS detection algorithm checks that a framed DS3 signal containing the repeating pattern 1010... is present. The C-bits are checked for the value specified by the AISC bit setting. When a logic 0 is written to AISPAT, the AIS detection algorithm is determined solely by the settings of AISC and AISONES register bits (see bit mapping table in the Additional Configuration Register description).

Register 0x031, 0x431, 0x1231, 0x1631: DS3 FRMR Interrupt Enable (ACE=0)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	COFAE	0
Bit 6	R/W	REDE	0
Bit 5	R/W	CBITE	0
Bit 4	R/W	FERFE	0
Bit 3	R/W	IDLE	0
Bit 2	R/W	AISE	0
Bit 1	R/W	OOFE	0
Bit 0	R/W	LOSE	0

The DS3 FRMR Interrupt Enable register is provided at channel address 031H when the ACE bit in channel address 033H is set to logic 0.

LOSE

The LOSE bit enables interrupt generation when a DS3 loss of signal defect is declared or removed. The interrupt is enabled when a logic 1 is written.

OOFE

The OOFE bit enables interrupt generation when a DS3 out of frame defect is declared or removed. The interrupt is enabled when a logic 1 is written.

AISE

The AISE bit enables interrupt generation when the DS3 AIS maintenance signal is detected or removed. The interrupt is enabled when a logic 1 is written.

IDLE

The IDLE bit enables interrupt generation when the DS3 IDLE maintenance signal is detected or removed. The interrupt is enabled when a logic 1 is written.

FERFE

The FERFE bit enables interrupt generation when a DS3 far end receive failure defect is declared or removed. The interrupt is enabled when a logic 1 is written.

CBITE

The CBITE bit enables interrupt generation when the DS3 FRMR detects a change of state in the DS3 application identification channel. The interrupt is enabled when a logic 1 is written.

REDE

The REDE bit enables an interrupt to be generated when a change of state of the DS3 RED indication occurs. The DS3 RED indication is visible in the REDV bit location of the DS3 FRMR Status register. When REDE is set to logic 1, the interrupt output, INTB, is set low when the state of the RED indication changes.

COFAE

The COFAE bit enables interrupt generation when the DS3 FRMR detects a DS3 change of frame alignment. The interrupt is enabled when a logic 1 is written.

Register 0x031, 0x431, 0x1231, 0x1631: DS3 FRMR Additional Configuration (ACE=1)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	AISONES	0
Bit 4	R/W	BPVO	0
Bit 3	R/W	EXZSO	0
Bit 2	R/W	EXZDET	0
Bit 1	R/W	SALGO	0
Bit 0	R/W	DALGO	0

The DS3 FRMR Additional Configuration register is provided at channel address 031H when the ACE bit in channel address 033H is set to logic 1.

DALGO

The DALGO bit determines the criteria used to decode a valid B3ZS signature. When DALGO is set to logic 1, a valid B3ZS signature is declared and 3 zeros substituted whenever a zero followed by a bipolar violation of the opposite polarity to the last observed BPV is seen. When the DALGO bit is set to logic 0, a valid B3ZS signature is declared and the 3 zeros are substituted whenever a zero followed by a bipolar violation is observed.

SALGO

The SALGO bit determines the criteria used to establish a valid B3ZS signature used to map BPVs to line code violation indications. Any BPV that is not part of a valid B3ZS signature is indicated as an LCV. When the SALGO bit is set to logic 1, a valid B3ZS signature is declared whenever a zero followed by a bipolar violation is observed. When SALGO is set to logic 0, a valid B3ZS signature is declared whenever a zero followed by a bipolar violation of the opposite polarity to the last observed BPV is seen.

EXZDET

The EXZDET bit determines the type of zero occurrences to be included in the LCV indication. When EXZDET is set to logic 1, the occurrence of an excessive zero generates a single pulse indication that is used to indicate an LCV. When EXZDET is set to logic 0, every occurrence of 3 consecutive zeros generates a pulse indication that is used to indicate an LCV. For example, if a sequence of 15 consecutive zeros were received, with EXZDET=1 only a single LCV would be indicated for this string of excessive zeros; with EXZDET=0, five LCVs would be indicated for this string (i.e. one LCV for every 3 consecutive zeros).

EXZSO

The EXZSO bit enables only summed zero occurrences to be accumulated in the PMON EXZS Count Registers. When EXZSO is set to logic 1, any excessive zeros occurrences over an 85 bit period increments the PMON EXZS counter by one. When EXZSO is set to logic 0, summed LCVs are accumulated in the PMON EXZS Count Registers. A summed LCV is defined as the occurrence of either BPVs not part of a valid B3ZS signature or 3 consecutive zeros (or excessive zeros if EXZDET=1) occurring over an 85 bit period; each summed LCV occurrence increment the PMON EXZS counter by one.

BPVO

The BPVO bit enables only bipolar violations to indicate line code violations and be accumulated in the PMON LCV Count Registers. When BPVO is set to logic 1, only BPVs not part of a valid B3ZS signature generate an LCV indication and increment the PMON LCV counter. When BPVO is set to logic 0, both BPVs not part of a valid B3ZS signature, and either 3 consecutive zeros or excessive zeros generate an LCV indication and increment the PMON LCV counter.

Table 11 DS3 FRMR EXZS/LCV Count Configurations

Register Bit			Counter Function	
EXZSO	**BPVO**	**EXZDET**	**PMON EXZ Count**	**PMON LCV Count**
0	0	0	Summed LCVs	BPVs & every 3 consecutive zeros
0	0	1	Summed LCVs	BPVs & every string of 3+ consecutive zeros
0	1	0	Reserved	Reserved
0	1	1	Reserved	Reserved
1	0	0	Summed excessive zeros	BPVs & every 3 consecutive zeros
1	0	1	Summed excessive zeros	BPVs & every string of 3+ consecutive zeros
1	1	0	Summed excessive zeros	Only BPVs
1	1	1	Summed excessive zeros	Only BPVs

AISONES

The AISONES bit controls the pattern used to detect the alarm indication signal (AIS) when both AISPAT and AISC bits in DS3 FRMR Configuration register are logic 0; if either AISPAT or AISC are logic 1, the AISONES bit is ignored.

When a logic 0 is written to AISONES, the algorithm checks that a framed all-ones payload pattern (1111...) signal is observed for a period of time before declaring AIS. Only the payload bits are observed to follow an all-ones pattern, the overhead bits (X, P, M, F, C) are ignored.

When a logic 1 is written to AISONES, the algorithm checks that an unframed all-ones pattern (1111...) signal is observed for a period of time before declaring AIS. In this case, all the bits, including the overhead, are observed to follow an all-ones pattern. The valid combinations of AISPAT, AISC, and AISONES bits are summarized below:

Table 12 DS3 FRMR AIS Configurations

AISPAT	AISC	AISONES	AIS Detected
1	0	X	Framed DS3 stream containing repeating 1010… pattern; overhead bits ignored.
0	1	X	Framed DS3 stream containing C-bits all logic 0; payload bits ignored.
1	1	X	Framed DS3 stream containing repeating 1010… pattern in the payload, C-bits all logic 0, and X-bits=1. This can be detected by setting both AISPAT and AISC high, and declaring AIS only when AISV=1 and FERFV=0 (Register x33).
0	0	0	Framed DS3 stream containing all-ones payload pattern; overhead bits ignored.
0	0	1	Unframed all-ones DS3 stream.

Register 0x032, 0x432, 0x1232, 0x1632: DS3 FRMR Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	COFAI	X
Bit 6	R	REDI	X
Bit 5	R	CBITI	X
Bit 4	R	FERFI	X
Bit 3	R	IDLI	X
Bit 2	R	AISI	X
Bit 1	R	OOFI	X
Bit 0	R	LOSI	X

LOSI

The LOSI bit is set to logic 1 when a loss of signal defect is detected or removed. The LOSI bit position is set to logic 0 when this register is read.

OOFI

The OOFI bit is set to logic 1 when an out of frame defect is detected or removed. The OOFI bit position is set to logic 0 when this register is read.

AISI

The AISI bit is set to logic 1 when the DS3-AIS maintenance signal is detected or removed. The AISI bit position is set to logic 0 when this register is read.

IDLI

The IDLI bit is set to logic 1 when the DS3-IDLE maintenance signal is detected or removed. The IDLI bit position is set to logic 0 when this register is read.

FERFI

The FERFI bit is set to logic 1 when a FERF defect is detected or removed. The FERFI bit position is set to logic 0 when this register is read.

CBITI

The CBITI bit is set to logic 1 when a change of state is detected in the DS3 application identification channel. The CBITI bit position is set to logic 0 when this register is read.

REDI

The REDI bit indicates that a change of state of the DS3 RED indication has occurred. The DS3 RED indication is visible in the REDV bit location of the DS3 FRMR Status register. When the REDI bit is a logic 1, a change in the RED state has occurred. When the REDI bit is logic 0, no change in the RED state has occurred.

COFAI

The COFAI bit is set to logic 1 when a change of frame alignment is detected. A COFA is generated when a new DS3 frame alignment is determined that differs from the last known frame alignment. The COFAI bit position is set to logic 0 when this register is read.

Register 0x033, 0x433, 0x1233, 0x1633: DS3 FRMR Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	ACE	0
Bit 6	R	REDV	X
Bit 5	R	CBITV	X
Bit 4	R	FERFV	X
Bit 3	R	IDLV	X
Bit 2	R	AISV	X
Bit 1	R	OOFV	X
Bit 0	R	LOSV	X

LOSV

The LOSV bit indicates the current loss of signal defect state. LOSV is a logic 1 when a sequence of 175 zeros is detected on the B3ZS encoded DS3 receive stream. LOSV is a logic 0 when a signal with a ones density greater than 33% for 175 ± 1 bit periods is detected.

OOFV

The OOFV bit indicates the current DS3 out of frame defect state. When the DS3 FRMR has lost frame alignment and is searching for the new alignment, OOFV is set to logic 1. When the DS3 FRMR has found frame alignment, the OOFV bit is set to logic 0.

AISV

The AISV bit indicates the alarm indication signal state. When the DS3 FRMR detects the AIS maintenance signal, AISV is set to logic 1.

IDLV

The IDLV bit indicates the IDLE signal state. When the DS3 FRMR detects the IDLE maintenance signal, IDLV is set to logic 1.

FERFV

The FERFV bit indicates the current far end receive failure defect state. When the DS3 FRMR detects an M-frame with the X1 and X2 bits both set to zero, FERFV is set to logic 1. When the S/UNI 4xJET detects an M-frame with the X1 and X2 bits both set to one, FERFV is set to logic 0.

CBITV

The CBITV bit indicates the application identification channel (AIC) state. CBITV is set to logic 1 (indicating the presence of the C-bit parity application) when the AIC bit is set high for 63 consecutive M-frames. CBITV is set to logic 0 (indicating the presence of the M23 or SYNTRAN applications) when AIC is set low for 2 or more M-frames in the last 15.

REDV

The REDV bit indicates the current state of the DS3 RED indication. When the REDV bit is a logic 1, the DS3 FRMR frame alignment acquisition circuitry has been out of frame for 2.23 ms (or for 13.5 ms when FDET is logic 0). When the REDV bit is logic 0, the frame alignment circuitry has found frame (i.e. OOFV=0) for 2.23 ms (or 13.5 ms if FDET=0).

ACE

The ACE bit selects the Additional Configuration Register. This register is located at channel address 031H, and is only accessible when the ACE bit is set to logic 1. When ACE is set to logic 0, the Interrupt Enable register is accessible at channel address 031H.

Register 0x034, 0x434, 0x1234, 0x1634: DS3 TRAN Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	CBTRAN	0
Bit 6	R/W	AIS	0
Bit 5	R/W	IDL	0
Bit 4	R/W	FERF	0
Bit 3	R/W	Reserved	0
Bit 2	—	Unused	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	CBIT	0

CBIT

The CBIT bit enables the DS3 C-bit parity application. When CBIT is written with a logic 1, C-bit parity is enabled, and the DS3-TRAN modifies the C-bits as required to include the path maintenance data link, the FEAC channel, the far end block error indication, and the path parity. When CBIT is written with a logic 0, the M23 application is selected, and each C-bit is set to logic 1 by the DS3-TRAN except for the first C-bit of the frame, which is forced to toggle every frame.

Note that the C-bits may be modified as required using the DS3 overhead access port (TOH) regardless of the setting of this bit.

FERF

The FERF bit enables insertion of the far end receive failure maintenance signal in the DS3 stream. The FERF bit is logically ORed with the LOS, OOF, RED, AIS, and LCD indications from the DS3 FRMR and RXCP when the LOSEN, OOFEN, RBLEN, AISEN, and LCDEN register bits (in the Channel Data Link and FERF/RAI Control register) are set to logic 1 respectively. In addition, the FERF bit is logically ORed with the OOF, RED, and AIS indications from the DS3 FRMR AUX when the OOFEN, RBLEN, and AISEN register bits (in the Channel Auxiliary Framer Data Link and FERF/RAI Control register) are set to logic 1 respectively. When the OR of the three signals is logic 1, the X1 and X2 overhead bit positions are set to logic 0. When the OR of the three signals is logic 0, the X1 and X2 overhead bit positions in the DS3 stream are set to logic 1.

IDL

The IDL bit enables insertion of the idle maintenance signal in the DS3 stream. When IDL is written with a logic 1, the DS3 payload is overwritten with the repeating pattern 1100.... The DS3 overhead bit insertion (X, P, M F, and C) continues normally. When IDL is written with a logic 0, the idle signal is not inserted.

AIS

The AIS bit enables insertion of the AIS maintenance signal in the DS3 stream. When AIS is written with a logic 1, the DS3 payload is overwritten with the repeating pattern 1010.... The DS3 overhead bit insertion (X, P, M and F) continues normally. The values inserted in the C-bits during AIS transmission are controlled by the CBTRAN bit in this register. When AIS is written with a logic 0, the AIS signal is not inserted. The CBIT bit in this register must be written to a logic 1 whenever AIS is a logic 1.

CBTRAN

The CBTRAN bit controls the C-bit values during AIS transmission. When CBTRAN is written with a logic 0, the C-bits are overwritten with zeros during AIS transmission as specified in ANSI T1.107. When CBTRAN is written with a logic 1, C-bit insertion continues normally (as controlled by the CBIT bit in this register) during AIS transmission.

Register 0x035, 0x435, 0x1235, 0x1635: DS3 TRAN Diagnostic

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	DLOS	0
Bit 6	R/W	DLCV	0
Bit 5	—	Unused	X
Bit 4	R/W	DFERR	0
Bit 3	R/W	DMERR	0
Bit 2	R/W	DCPERR	0
Bit 1	R/W	DPERR	0
Bit 0	R/W	DFEBE	0

DFEBE

The DFEBE bit controls the insertion of far end block errors in the DS3 stream. When DFEBE is written with a logic 1, and the C-bit parity application is enabled, the three C-bits in M-subframe 4 are set to a logic 0. When DFEBE is written with a logic 0, FEBEs are indicated based on receive framing bit errors and path parity errors.

DPERR

The DPERR bit controls the insertion of parity errors (P-bit errors) in the DS3 stream. When DPERR is written with a logic 1, the P-bits are inverted before insertion. When DPERR is written with a logic 0, the parity is calculated and inserted normally.

DCPERR

The DCPERR bit controls the insertion of path parity errors in the DS3 stream. When DCPERR is written with a logic 1 and the C-bit parity application is enabled, the three C-bits in M-subframe 3 are inverted before insertion. When DCPERR is written with a logic 0, the path parity is calculated and inserted normally.

DMERR

The DMERR bit controls the insertion of M-bit framing errors in the DS3 stream. When DMERR is written with a logic 1, the M-bits are inverted before insertion. When DMERR is written with a logic 0, the M-bits are inserted normally.

DFERR

The DFERR bit controls the insertion of F-bit framing errors in the DS3 stream. When DFERR is written with a logic 1, the F-bits are inverted before insertion. When DFERR is written with a logic 0, the F-bits are inserted normally.

DLCV

The DLCV bit controls the insertion of a single line code violation in the DS3 stream. When DLCV is written with a logic 1, a line code violation is inserted by generating an incorrect polarity of violation in the next B3ZS signature. The data being transmitted must therefore contain periods of three consecutive zeros in order for the line code violation to be inserted. For example, line code violations may not be inserted when transmitting AIS, but may be inserted when transmitting the idle signal. DLCV is automatically cleared upon insertion of the line code violation.

DLOS

The DLOS bit controls the insertion of loss of signal in the DS3 stream. When DLOS is written with a logic 1, the data on outputs TPOS/TDATO[x] and TNEG/TOHM[x] is forced to continuous zeros.

Register 0x038, 0x438, 0x1238, 0x1638: E3 FRMR Framing Options

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	UNI	0
Bit 3	R/W	FORMAT[1]	0
Bit 2	R/W	FORMAT[0]	0
Bit 1	R/W	REFRDIS	0
Bit 0	R/W	REFR	0

REFR

A transition from logic 0 to logic 1 in the REFR bit position forces the E3 FRMR to initiate a search for frame alignment. The bit must be cleared to logic 0, then set to logic 1 again to initiate subsequent searches for frame alignment.

REFRDIS

The REFRDIS bit disables reframing under the consecutive framing bit error condition once frame alignment has been found, leaving reframing to be initiated only by software via the REFR bit. A logic 1 in the REFRDIS bit position causes the E3 FRMR to remain "locked in frame" once initial frame alignment has been found. A logic 0 allows reframing to occur when four consecutive framing patterns are received in error.

FORMAT[1:0]

The FORMAT[1:0] bits determine the framing mode used for pattern matching when finding frame alignment and for generating the output status signals. The FORMAT[1:0] bits select one of two framing formats:

Table 13 E3 FRMR FORMAT[1:0] Configurations

FORMAT[1]	FORMAT[0]	Framing Format Selected
0	0	G.751 E3 format
0	1	G.832 E3 format
1	0	Reserved
1	1	Reserved

UNI

The UNI bit configures the E3 FRMR to accept either dual-rail or single-rail E3 stream. When a logic 1 is written to UNI, the E3 FRMR accepts a single-rail E3 stream. When a logic 0 is written to UNI, the E3 FRMR accepts a HDB3-encoded dual-rail E3 stream.

What sources the E3 stream is selectable via the FRMRSEL register bit. When a logic 1 is written to FRMRSEL, the D3E3MD sources a single-rail E3 stream and UNI should be set to logic 1. When a logic 0 is written to FRMRSEL, the receive serial interface sources a single-rail or dual-rail E3 stream on RPOS/RDATI[x] and RNEG/RLCV/ROHM[x]. In this case, when UNI is set to logic 1, the E3 FRMR accepts a single-rail E3 stream and accumulates line code violations on the RNEG/RLCV/ROHM[x] input.

Register 0x039, 0x439, 0x1239, 0x1639: E3 FRMR Maintenance Options

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	WORDBIP	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	WORDERR	0
Bit 2	R/W	PYLD&JUST	0
Bit 1	R/W	FERFDET	0
Bit 0	R/W	TMARKDET	0

TMARKDET

The TMARKDET bit determines the persistency check performed on the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte). When TMARKDET is logic 1, the Timing Marker bit must be in the same state for 5 consecutive frames before the TIMEMK status is changed to that state. When TMARKDET is logic 0, the Timing Marker bit must be in the same state for 3 consecutive frames. When a framing mode other than G.832 is selected, the setting of the TMARKDET bit is ignored.

FERFDET

The FERFDET bit determines the persistency check performed on the Far End Receive Failure (FERF) bit (bit 1 of the G.832 Maintenance and Adaptation byte) or on the Remote Alarm indication (RAI) bit (bit 11 of the frame in G.751 mode). When FERFDET is logic 1, the FERF, or RAI, bit must be in the same state for 5 consecutive frames before the FERF/RAI status is changed to that state. When FERFDET is logic 0, the FERF, or RAI, bit must be in the same state for 3 consecutive frames.

PYLD&JUST

The PYLD&JUST bit selects whether the justification service bits and the tributary justification bits in framing mode G.751 is indicated as overhead or payload. When PYLD&JUST is logic 1, the justification service bits and the tributary justification bits are indicated as payload. When PYLD&JUST is logic 0, the justification service and tributary justification bits are indicated as overhead.

PYLD&JUST must be set to logic 1 when configured for E3 G.751 ATM applications.

WORDERR

The WORDERR bit selects whether the framing bit error indication pulses accumulated in PMON indicate all bit errors in the framing pattern or only one error for one or more errors in the framing pattern. When WORDERR is logic 1, the FERR indication to PMON pulses once per frame, accumulating one error for one or more framing bit errors occurred. When WORDERR is logic 0, the FERR indication to PMON pulses for each and every framing bit error that occurs; PMON accumulates all framing bit errors.

WORDBIP

The WORDBIP bit selects whether the parity bit error indication pulses to the E3-TRAN block indicate all bit errors in the BIP-8 pattern or only one error for one or more errors in the BIP-8 pattern. When WORDBIP is logic 1, the parity error indication to the E3-TRAN block pulses once per frame, indicating that one or more parity bit errors occurred. When WORDBIP is logic 0, the parity error indication to the E3-TRAN block pulses for each and every parity bit error that occurs.

WORDBIP should be set to logic 1 when configured for E3 G.832 applications.

Register 0x03A, 0x43A, 0x123A, 0x163A: E3 FRMR Framing Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	CZDE	0
Bit 3	R/W	LOSE	0
Bit 2	R/W	LCVE	0
Bit 1	R/W	COFAE	0
Bit 0	R/W	OOFE	0

OOFE

The OOFE bit is an interrupt enable. When OOFE is logic 1, a change of state of the OOF status generates an interrupt and sets the INTB output to logic 0. When OOFE is logic 0, changes of state of the OOF status are disabled from causing interrupts on the INTB output.

COFAE

The COFAE bit is an interrupt enable. When COFAE is logic 1, a change of frame alignment generates an interrupt and sets the INTB output to logic 0. When COFAE is logic 0, changes of frame alignment are disabled from causing interrupts on the INTB output.

LCVE

The LCVE bit is an interrupt enable. When LCVE is logic 1, detection of a line code violation generates an interrupt and sets the INTB output to logic 0. When LCVE is logic 0, occurrences of line code violations are disabled from causing interrupts on the INTB output.

LOSE

The LOSE bit is an interrupt enable. When LOSE is logic 1, a change of state of the loss-of-signal generates an interrupt and sets the INTB output to logic 0. When LOSE is logic 0, occurrences of loss-of-signal are disabled from causing interrupts on the INTB output.

CZDE

The CZDE bit is an interrupt enable. When CZDE is logic 1, detection of four consecutive zeros in the HDB3-encoded stream generates an interrupt and sets the INTB output to logic 0. When CZDE is logic 0, occurrences of consecutive zeros are disabled from causing interrupts on the INTB output.

Register 0x03B, 0x43B, 0x123B, 0x163B: E3 FRMR Framing Interrupt Indication and Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R	CZDI	X
Bit 5	R	LOSI	X
Bit 4	R	LCVI	X
Bit 3	R	COFAI	X
Bit 2	R	OOFI	X
Bit 1	R	LOS	X
Bit 0	R	OOF	X

OOF

The OOF bit indicates the current state of the E3 FRMR. When OOF is logic 1, the E3 FRMR is out of frame alignment and actively searching for the new alignment. While OOF is high all status indications and overhead extraction continue with the previous known alignment. When OOF is logic 0, the E3 FRMR has found a valid frame alignment and is operating in a maintenance mode, indicating framing bit errors, and extracting and processing overhead bits. During reset, OOF is set to logic 1, but the setting may change prior to the register being read.

LOS

The LOS bit indicates the current state of the Loss-Of-Signal detector. When LOS is logic 1, the E3 FRMR has received 32 consecutive RCLK cycles containing zeros on the HDB3 encoded E3 receive stream. When LOS is logic 0, the E3 FRMR has received 32 consecutive RCLK cycles containing no occurrences of 4 consecutive zeros. The LOS bit is forced to logic 0 if the UNI bit is logic 1. During reset, LOS is set to logic 0, but the setting may change prior to the register being read.

OOFI

A logic 1 OOFI bit indicates a change in the OOF status. The OOFI bit is cleared to logic 0 upon the completion of the register read. When OOFI is logic 0, it indicates that no OOF state change has occurred since the last time this register was read.

COFAI

The COFAI bit indicates that a change of frame alignment between the previous alignment and the newly found alignment has occurred. When COFAI is logic 1, the last high-to-low transition on the OOF signal resulted in the new frame alignment differing from the previous one. The COFAI bit is cleared to logic 0 upon the completion of the register read. When COFAI is logic 0, it indicates that no change in frame alignment has occurred when OOF went low.

LCVI

The LCVI bit indicates that a line code violation has occurred. When LCVI is logic 1, a line code violation on the RPOS/RDATI[x] and RNEG/RLCV/ROHM[x] inputs was detected since the last time this register was read. The LCVI bit is cleared to logic 0 upon the completion of the register read. When LCVI is logic 0, it indicates that no line code violation was detected since the last register read. When the UNI bit in the Framing Options register is logic 1, the LCVI is forced to logic 0.

LOSI

The LOSI bit indicates that a state transition occurred on the LOS status signal. When LOSI is logic 1, a high-to-low or low-to-high transition occurred on the LOS status signal since the last time this register was read. The LOSI bit is cleared to logic 0 upon the completion of the register read. When LOSI is logic 0, it indicates that no state change has occurred on LOS since the last time this register was read. When the UNI bit in the Framing Options register is logic 1, the LOSI is forced to logic 0.

CZDI

The CZDI bit indicates that four consecutive zeros in the HDB3-encoded stream have been detected. CZDI is asserted to a logic 1, whenever the CZD signal is asserted. The CZDI bit is cleared to a logic 0 upon the completion of the register read. When CZDI is logic 0, it indicates that no occurrences of four consecutive zeros was detected since the last register read. When the UNI bit in the Framing Options register is logic 1, the CZDI indication is forced to logic 0.

The interrupt indications within this register work independently from the interrupt enable bits, allowing the microprocessor to poll the register to determine the state of the framer. The indication bits (bits 2, 3, 4, 5, and 6 of this register) are cleared to logic 0 after the register is read; the INTB output is also cleared to logic 1 if the interrupt was generated by any of these five events.

Register 0x03C, 0x43C, 0x123C, 0x163C: E3 FRMR Maintenance Event Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	FERRE	0
Bit 6	R/W	PERRE	0
Bit 5	R/W	AISDE	0
Bit 4	R/W	FERFE	0
Bit 3	R/W	FEBEE	0
Bit 2	R/W	PTYPEE	0
Bit 1	R/W	TIMEMKE	0
Bit 0	R/W	NATUSEE	0

NATUSEE

The NATUSEE bit is an interrupt enable. When NATUSEE is logic 1, an interrupt is generated on the INTB output when the National Use bit (bit 12 of the frame in G.751 E3 mode) changes state. When NATUSEE is logic 0, changes in state of the National Use bit does not cause an interrupt on INTB.

TIMEMKE

The TIMEMKE bit is an interrupt enable. When TIMEMKE is logic 1, an interrupt is generated on the INTB output when the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte) changes state after the selected persistency check is applied. When TIMEMKE is logic 0, changes in state of the Timing Marker bit does not cause an interrupt on INTB.

PTYPEE

The PTYPEE bit is an interrupt enable. When PTYPEE is logic 1, an interrupt is generated on the INTB output when the Payload Type bits (bits 3, 4, and 5 of the G.832 Maintenance and Adaptation byte) change state. When PTYPEE is logic 0, changes in state of the Payload Type bits does not cause an interrupt on INTB.

FEBEE

The FEBEE bit is an interrupt enable. When FEBEE is logic 1, an interrupt is generated on the INTB output when the Far End Block Error indication bit (bit 2 of the G.832 Maintenance and Adaptation byte) changes state. When FEBEE is logic 0, changes in state of the FEBE bit does not cause an interrupt on INTB.

FERFE

The FERFE bit is an interrupt enable. When FERFE is logic 1, an interrupt is generated on the INTB output when the Far End Receive Failure indication bit (bit 1 of the G.832 Maintenance and Adaptation byte), or when the Remote Alarm indication bit (bit 11 of the frame in G.751) changes state after the selected persistency check is applied. When FERFE is logic 0, changes in state of the FERF or RAI bit does not cause an interrupt on INTB.

AISDE

The AISDE bit is an interrupt enable. When AISDE is logic 1, an interrupt is generated on the INTB output when the AISD indication changes state. When AISDE is logic 0, changes in state of the AISD signal does not cause an interrupt on INTB.

PERRE

The PERRE bit is an interrupt enable. When PERRE is logic 1, an interrupt is generated on the INTB output when a BIP-8 error (in G.832 mode) is detected. When PERRE is logic 0, occurrences of BIP-8 errors do not cause an interrupt on INTB.

FERRE

The FERRE bit is an interrupt enable. When FERRE is logic 1, an interrupt is generated on the INTB output when a framing bit error is detected. When FERRE is logic 0, occurrences of framing bit errors do not cause an interrupt on INTB.

Register 0x03D, 0x43D, 0x123D, 0x163D: E3 FRMR Maintenance Event Interrupt Indication

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	FERRI	0
Bit 6	R	PERRI	0
Bit 5	R	AISDI	0
Bit 4	R	FERFI	0
Bit 3	R	FEBEI	0
Bit 2	R	PTYPEI	0
Bit 1	R	TIMEMKI	0
Bit 0	R	NATUSEI	0

NATUSEI

The NATUSEI bit is a transition Indication. When NATUSEI is logic 1, a change of state of the National Use bit (bit 12 of the frame in G.751 E3 mode) has occurred. When NATUSEI is logic 0, no change of state of the National Use bit has occurred since the last time this register was read.

TIMEMKI

The TIMEMKI bit is a transition indication. When TIMEMKI is logic 1, a change in state of the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte) has occurred. When TIMEMKI is logic 0, no changes in the state of the Timing Marker bit occurred since the last time this register was read.

PTYPEI

The PTYPEI bit is a transition indication. When PTYPEI is logic 1, a change of state of the Payload Type bits (bits 3,4,5 of the G.832 Maintenance and Adaptation byte) has occurred. When PTYPEI is logic 0, no changes in the state of the Payload Type bits has occurred since the last time this register was read.

FEBEI

The FEBEI bit is a transition indication. When FEBEI is logic 1, a change of state of the Far End Block Error indication bit (bit 2 of the G.832 Maintenance and Adaptation byte) has occurred. When FEBEI is logic 0, no changes in the state of the FEBE bit has occurred since the last time this register was read.

FERFI

The FERFI bit is a transition indication. When FERFI is logic 1, a change of state of the Far End Receive Failure indication bit (bit 1 of the G.832 Maintenance and Adaptation byte), or when the Remote Alarm indication bit (bit 12 of the frame in G.751) has occurred. When FERFI is logic 0, no changes in the state of the FERF or RAI bit has occurred since the last time this register was read.

AISDI

The AISDI bit is a transition indication. When AISDI is logic 1, a change in state of the AISD indication has occurred. When AISDI is logic 0, no changes in the state of the AISD signal has occurred since the last time this register was read.

PERRI

The PERRI bit is an event indication. When PERRI is logic 1, the occurrence of one or more BIP-8 errors (in G.832 mode) has been detected. When PERRI is logic 0, no occurrences of BIP-8 errors have occurred since the last time this register was read.

FERRI

The FERRI bit is an event indication. When FERRI is logic 1, the occurrence of one or more framing bit error has been detected. When FERRI is logic 0, no occurrences of framing bit errors have occurred since the last time this register was read.

The transition/event interrupt indications within this register work independently from the interrupt enable bits, allowing the microprocessor to poll the register to determine the activity of the maintenance events. The contents of this register are cleared to logic 0 after the register is read; the INTB output is also cleared to logic 1 if the interrupt was generated by any of the Maintenance Event outputs.

Register 0x03E, 0x43E, 0x123E, 0x163E: E3 FRMR Maintenance Event Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	AISD	X
Bit 6	R	FERF/RAI	X
Bit 5	R	FEBE	X
Bit 4	R	PTYPE[2]	X
Bit 3	R	PTYPE[1]	X
Bit 2	R	PTYPE[0]	X
Bit 1	R	TIMEMK	X
Bit 0	R	NATUSE	X

NATUSE

The NATUSE bit reflects the state of the extracted National Use bit (bit 12 of the frame in G.751 E3 mode).

TIMEMK

The TIMEMK bit reflects the state of the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte).

PTYPE[2:0]

The PTYPE[2:0] bits reflect the state of the Payload Type bits (bits 3,4,5 of the G.832 Maintenance and Adaptation byte). These bits are not latched and should be read 2 or 3 times in rapid succession to ensure a coherent binary value.

FEBE

The FEBE bit reflects the state of the Far End Block Error indication bit (bit 2 of the G.832 Maintenance and Adaptation byte).

FERF

The FERF bit reflects the value of the Far End Receive Failure indication bit (bit 1 of the G.832 Maintenance and Adaptation byte), or the value of the Remote Alarm indication bit (bit 11 of the frame in G.751) when the value has been the same for either 3 or 5 consecutive frames.

AISD

The AISD bit reflects the state of the AIS detection circuitry. When AISD is logic 1, less than 8 zeros (in G.832 mode), or less than 5 zeros (in G.751 mode), were detected during one complete frame period while the E3 FRMR is out of frame alignment. When AISD is logic 0, 8 or more zeros (in G.832 mode), or 5 or more zeros (in G.751 mode), were detected during one complete frame period, or the E3 FRMR has found frame alignment.

Register 0x040, 0x440, 0x1240, 0x1640: E3 TRAN Framing Options

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	FORMAT[1]	0
Bit 0	R/W	FORMAT[0]	0

FORMAT[1:0]

The FORMAT[1:0] bits determine the framing mode used for framing pattern when generating the formatted output data stream. The FORMAT[1:0] bits select one of two framing formats:

Table 14 E3 TRAN FORMAT[1:0] Configurations

FORMAT[1]	FORMAT[0]	Framing Format Selected
0	0	G.751 E3 format
0	1	G.832 E3 format
1	0	Reserved
1	1	Reserved

Register 0x041, 0x441, 0x1241, 0x1641: E3 TRAN Status and Diagnostic Options

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	PYLD&JUST	0
Bit 5	R/W	CPERR	0
Bit 4	R/W	DFERR	0
Bit 3	R/W	DLCV	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	TAIS	0
Bit 0	R/W	NATUSE	1

NATUSE

The NATUSE bit determines the default value of the National Use bit inserted into the G.751 E3 frame overhead. The value of the NATUSE bit is logically ORed with the bit collected once per frame from the internal HDLC transmitter (if TNETOP is set to logic 1). When TNETOP is logic 0, the NATUSE bit controls the value of the National Use bit. When NATUSE is logic 1, the National Use bit (bit 12 in G.751) is forced to logic 1 regardless of the bit input from the internal HDLC transmitter or the setting of TNETOP. When NATUSE is logic 0, the National Use bit is set to the value sampled from the internal HDLC transmitter if TNETOP is logic 0. Otherwise, the National Use bit will be set to logic 0. If the E3-TRAN is configured for G.832 mode, this bit is ignored.

TAIS

The TAIS bit enables AIS signal transmission. When TAIS is logic 1, the all 1's AIS signal is transmitted. When TAIS is logic 0, the normal data is transmitted.

DLCV

The DLCV bit selects whether a line code violation is generated for diagnostic purposes. When DLCV changes from logic 0 to logic 1, single LCV is generated; in HDB3, the LCV is generated by causing a bipolar violation pulse of the same polarity to the previous bipolar violation. To generate another LCV, the DLCV register bit must be first be written to logic 0 and then to logic 1 again.

DFERR

The DFERR bit selects whether the framing pattern is corrupted for diagnostic purposes. When DFERR is logic 1, the framing pattern inserted into the output data stream is inverted. When DFERR is logic 0, the unaltered framing pattern inserted into the output data stream.

CPERR

The CPERR bit enables continuous generation of BIP-8 errors for diagnostic purposes. When CPERR is logic 1, the calculated BIP-8 value is continuously inverted according to the error mask specified by the BIP-8 Error Mask register and inserted into the G.832 EM byte. When CPERR is logic 0, the calculated BIP-8 value is altered only once, according to the error mask specified by the BIP-8 Error Mask register, and inserted into the EM byte.

PYLD&JUST

The PYLD&JUST bit selects whether the justification service bits and the tributary justification bits in framing modes G.751 is indicated as overhead or payload. When PYLD&JUST is logic 1, the justification service bits and the tributary justification bits are indicated as payload. When PYLD&JUST is logic 0, the justification service and tributary justification bits are indicated as overhead.

PYLD&JUST must be set to logic 1 when configured for E3 G.751 ATM applications.

Register 0x042, 0x442, 0x1242, 0x1642: E3 TRAN BIP-8 Error Mask

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	MBIP[7]	0
Bit 6	R/W	MBIP[6]	0
Bit 5	R/W	MBIP[5]	0
Bit 4	R/W	MBIP[4]	0
Bit 3	R/W	MBIP[3]	0
Bit 2	R/W	MBIP[2]	0
Bit 1	R/W	MBIP[1]	0
Bit 0	R/W	MBIP[0]	0

MBIP[7:0]

The MBIP[7:0] bits act as an error mask to cause the transmitter to insert up to 8 BIP-8 errors. The contents of this register are XORed with the calculated BIP-8 byte and inserted into the G.832 EM byte of the frame. A logic 1 in any MBIP bit position causes that bit position in the EM byte to be inverted. Writing this register with a mask value causes that mask to be applied only once; if continuous BIP-8 errors are desired, the CPERR bit in the Status and Diagnostic Options register can be used.

Register 0x043, 0x443, 0x1243, 0x1643: E3 TRAN Maintenance and Adaptation Options

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	FERF/RAI	0
Bit 6	R/W	FEBE	0
Bit 5	R/W	PTYPE[2]	0
Bit 4	R/W	PTYPE[1]	0
Bit 3	R/W	PTYPE[0]	0
Bit 2	R/W	TUMFRM[1]	0
Bit 1	R/W	TUMFRM[0]	0
Bit 0	R/W	TIMEMK	0

TIMEMK

The TIMEMK bit determines the state of the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte). When TIMEMK is set to logic 1, the Timing Marker bit in the MA byte is set to logic 1. When TIMEMK is set to logic 0, the Timing Marker bit in the MA byte is set to logic 0.

TUMFRM[1:0]

The TUMFRM[1:0] bits reflect the value to be inserted in the Tributary Unit Multi-frame bits (bits 6, and 7 of the G.832 Maintenance and Adaptation byte). These bits are logically ORed with the TUMFRM[1:0] overhead signals from the TOH input before being inserted in the MA byte.

PTYPE[2:0]

The PTYPE[2:0] bits reflect the value to be inserted in the Payload Type bits (bits 3, 4, and 5 of the G.832 Maintenance and Adaptation byte).

FEBE

The FEBE bit reflects the value to be inserted in the Far End Block Error indication bit (bit 2 of the G.832 Maintenance and Adaptation byte). The FEBE bit value is logically ORed with the FEBE indication generated as a result of E3FEBEMODE[1:0] register bits. When the FEBE bit is logic 1, bit 2 of the G.832 MA byte is set to logic 1. When the FEBE bit is logic 0, a FEBE indication causes bit 2 of the MA byte to be set to logic 1.

What causes the FEBE indication is configurable via the E3FEBEMODE[1:0] register bits (in the Channel Data Path Configuration register) and illustrated in Table 28.

FERF/RAI

The FERF/RAI bit reflects the value to be inserted in the Far End Receive Failure indication bit (bit 1 of the G.832 Maintenance and Adaptation byte), or the value of the Remote Alarm indication bit (bit 11 of the frame in G.751). The FERF/RAI bit is logically ORed with the LOS, OOF, AIS, and LCD indications from the E3 FRMR and RXCP when the LOSEN, OOFEN, AISEN, and LCDEN register bits (in the Channel Data Link and FERF/RAI Control register) are set to logic 1 respectively. In addition, the FERF/RAI bit is logically ORed with the OOF, and AIS indications from the E3 FRMR AUX when the OOFEN, and AISEN register bits (in the Channel Auxiliary Framer Data Link and FERF/RAI Control register) are set to logic 1 respectively. When the OR of the three signals is logic 1, the FERF or RAI bit in the frame is set to logic 1. When the OR of the three signals is logic 0, the FERF or RAI bit is set to logic 0.

Register 0x044, 0x444, 0x1244, 0x1644: J2 FRMR Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	UNI	0
Bit 5	R/W	REFRAME	0
Bit 4	R/W	FLOCK	0
Bit 3	R/W	CRC_REFR	0
Bit 2	R/W	SFRME	0
Bit 1	R/W	LOSTHR[1]	1
Bit 0	R/W	LOSTHR[0]	1

LOSTHR[1:0]

The Loss of Signal Threshold bits select the number of consecutive zeroes required before the J2 FRMR will declare Loss of Signal (LOS), and the number of bit periods without an occurrence of excess zeroes that must pass before the J2 FRMR will deassert Loss of Signal. The thresholds are as follows:

Table 15 J2 FRMR LOS Threshold Configurations

LOSTHR[1]	LOSTHR[0]	Threshold
0	0	15
0	1	31
1	0	63
1	1	255

Thus, if LOSTHR[1:0] = 11 binary, LOS will be declared after the 255th consecutive binary zero, and deasserted when 255 bit periods have passed without an occurrence of a string of eight or more consecutive zeroes.

SFRME

When the Single Framing Bit Error (SFRME) bit is set to logic 1, then the J2 FRMR will indicate (to the PMON) a single framing error for every J2 multi-frame which contains one or more framing errors. When the SFRME bit is set to logic 0, the J2 FRMR will identify every framing error to the PMON.

CRC_REFR

When the CRC Reframe Enable bit is set to logic 1, an alternate framing algorithm is enabled, which uses the CRC-5 check to detect framing to a mimic pattern in the payload or signaling bits. The framer, once it has seen at least one correct framing pattern, begins looking for correct CRC-5s as well. If it observes three consecutive correct framing patterns, and two correct CRC-5 sequences, then frame is declared. Otherwise, a reframe is initiated. When CRC_REFR is set to logic 0, the framing algorithm simply searches for three consecutive correct framing patterns.

FLOCK

When the FLOCK bit is set to logic 1, the J2 FRMR is prevented from declaring Loss of Frame and searching for a new frame alignment due to framing-pattern errors. In this case, the J2 FRMR will only search for frame alignment when the REFRAME register bit transitions from logic 0 to logic 1.

REFRAME

Writing the REFRAME bit logic 1 forces the J2 FRMR to declare loss of frame, and begin searching for a new alignment. In order to force another reframe, REFRAME must be written with logic 0, and then logic 1 again.

UNI

The UNI bit configures the J2 FRMR to accept either a dual-rail or single-rail J2 stream. When a logic 1 is written to UNI, the J2 FRMR accepts a single-rail J2 stream. When a logic 0 is written to UNI, the J2 FRMR accepts a B8ZS-encoded dual-rail J2 stream. When UNI is set to logic 1, then the LOS, LOSI, and EXZI indications cannot be used.

Note that FRMRSEL should always be set to logic 0 in J2 mode of operation. When a logic 0 is written to FRMRSEL, the receive serial interface sources a single-rail or dual-rail J2 stream on RPOS/RDATI[x] and RNEG/RLCV/ROHM[x]. In this case, when UNI is set to logic 1, the J2 FRMR accepts a single-rail J2 stream and accumulates line code violations on the RNEG/RLCV/ROHM[x] input.

Register 0x045, 0x445, 0x1245, 0x1645: J2 FRMR Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	LOS	X
Bit 6	R	LOF	X
Bit 5	—	Unused	X
Bit 4	R	RAI	X
Bit 3	R	RLOF	X
Bit 2	—	Unused	X
Bit 1	R	PHYAIS	X
Bit 0	R	PLDAIS	X

LOS, LOF, RAI, RLOF, PHYAIS, PLDAIS

These register bits reflect the current state of the Loss of Signal (LOS), Loss of Frame (LOF), Remote Alarm Indication (RAI), Remote Loss of Frame (RLOF, also known as the A-bit), Physical AIS (PHYAIS), and Payload AIS (PLDAIS) conditions.

Register 0x046, 0x446, 0x1246, 0x1646: J2 FRMR Alarm Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	LOSE	0
Bit 6	R/W	LOFE	0
Bit 5	R/W	COFAE	0
Bit 4	R/W	RAIE	0
Bit 3	R/W	RLOFE	0
Bit 2	R/W	RLOF_THR	1
Bit 1	R/W	PHYAISE	0
Bit 0	R/W	PLDAISE	0

PLDAISE

When PLDAISE is logic 1, the J2 FRMR will generate an interrupt when a change is detected in the Payload AIS condition.

PHYAISE

When PHYAISE is logic 1, the J2 FRMR will generate an interrupt when a change is detected in the Physical AIS condition.

RLOF_THR

The RLOF Threshold bit determines the number of consecutive A-bits that are required for the state of RLOF to change. When RLOF_THR is logic 0, RLOF is asserted when the A-bit has been logic 1 for three consecutive frames, and deasserted when the A-bit has been logic 0 for three consecutive frames. When RLOF_THR is logic 1, RLOF is asserted when the A-bit has been logic 1 for five consecutive frames, and deasserted when the A-bit has been logic 0 for five consecutive frames. The default setting is that five consecutive A-bits are required.

RLOFE

When RLOFE is logic 1, the J2 FRMR will generate an interrupt when RLOF changes state.

RAIE

When RAIE is logic 1, the J2 FRMR will generate an interrupt when RAI changes state.

COFAE

When COFAE is logic 1, the J2 FRMR will generate an interrupt when a change of frame alignment occurs.

LOFE

When LOFE is logic 1, the J2 FRMR will generate an interrupt when LOF changes state.

LOSE

When LOSE is logic 1, the J2 FRMR will generate an interrupt when the LOS condition changes state. Note that the LOS bit is not valid when the UNI bit is set in the J2 FRMR Configuration Register.

Register 0x047, 0x447, 0x1247, 0x1647: J2 FRMR Alarm Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	LOSI	X
Bit 6	R	LOFI	X
Bit 5	R	COFAI	X
Bit 4	R	RAII	X
Bit 3	R	RLOFI	X
Bit 2	—	Unused	X
Bit 1	R	PHYAISI	X
Bit 0	R	PLDAISI	X

LOSI

The LOSI bit is set to logic 1 if a change occurs in the LOS condition. LOSI is cleared when this register is read.

LOFI

The LOFI bit is set to logic 1 if a change occurs in the state of LOF. LOFI is cleared when this register is read.

COFAI

The COFAI bit is set to logic 1 if a change in frame alignment occurs. COFAI is cleared when this register is read.

RAII

The RAII bit is set to logic 1 if a change in the value of RAI occurs. RAII is cleared when this register is read.

RLOFI

The RLOFI bit is set to logic 1 if a change in the value of RLOF occurs. RLOFI is cleared when this register is read.

PHYAISI

The PHYAISI bit is set to logic 1 if a change in the condition of PHYAIS occurs. PHYAISI is cleared when this register is read.

PLDAISI

The PLDAISI bit is set to logic 1 if a change in the condition of PLDAIS occurs. PLDAISI is cleared when this register is read.

Register 0x048, 0x448, 0x1248, 0x1648: J2 FRMR Error/Xbit Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	CRCEE	0
Bit 6	R/W	FRMEE	0
Bit 5	R/W	BPVE	0
Bit 4	R/W	EXZE	0
Bit 3	R/W	XBITE	0
Bit 2	—	Unused	X
Bit 1	R/W	XBIT_DEB	0
Bit 0	R/W	XBIT_THR	0

XBIT_THR

When XBIT_THR is set to logic 1, then XBIT_THR controls the debouncing threshold of the X-bit indications in the J2 FRMR Error/Xbit Interrupt Status Register. When XBIT_THR is logic 0, the threshold is set to 3 consecutive multi-frames; when XBIT_THR is logic 1, the threshold is set to 5 consecutive multi-frames.

XBIT_DEB

When XBIT_DEB is set to logic 0, the X-bit indications in the J2 FRMR Error/Xbit Interrupt Status Register reflect the most recent value of the X-bits. When XBIT_DEB is set to logic 1, the X-bit indications change value only when an X-bit has maintained its value for 3 or 5 consecutive multi-frames, depending on the setting of XBIT_THR.

XBITE

When XBITE is logic 1, the J2 FRMR will generate an interrupt when any of the X-bits (X1, X2, X3) change state. Because the XBIT interrupt is generated when the X-bit indications change, the interrupt is debounced along with them via the XBIT_DEB and XBIT_THR bits.

EXZE

When EXZE is logic 1, the J2 FRMR will generate an interrupt upon the reception of a string of eight-or-more consecutive zeroes. EXZE has no effect when UNI is set to logic 1 in the J2 FRMR Configuration Register.

BPVE

When BPVE is logic 1, the J2 FRMR will generate an interrupt upon the reception of a bipolar violation which is not part of a valid B8ZS code (when UNI is set to logic 0 in the J2 FRMR Configuration Register) or on the reception of a logic 1 on RNEG/RLCV/ROHM[x] (when UNI is set to logic 1).

FRMEE

When FRMEE is logic 1, the J2 FRMR will generate an interrupt upon the reception of an errored framing bit.

CRCEE

When CRCEE is logic 1, the J2 FRMR will generate an interrupt if a multi-frame fails its CRC-5 check.

Register 0x049, 0x449, 0x1249, 0x1649: J2 FRMR Error/Xbit Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	CRCEI	X
Bit 6	R	FRMEI	X
Bit 5	R	BPVI	X
Bit 4	R	EXZI	X
Bit 3	R	XBITI	X
Bit 2	R	X3	X
Bit 1	R	X2	X
Bit 0	R	X1	X

X1, X2, X3

The X1, X2, and X3 bits reflect the most recent (debounced if XBIT_DEB is set to logic 1) value of bits 785, 786, and 787 respectively of frame 3 of each multi-frame. These bits are the spare or 'X-bits.'

XBITI

The XBITI bit is set to logic 1 if a change in the debounced (if XBIT_DEB is set to logic 1) X-bits (X1, X2, and X3) is detected. XBITI is cleared when this register is read.

EXZI

The EXZI bit is set to logic 1 upon reception of eight-or-more consecutive zeroes. EXZI remains logic 0 while UNI is set to logic 1 in the J2_FRMR Configuration Register. EXZI is cleared when this register is read.

BPVI

The BPVI bit is set to logic 1 if a bipolar violation that is not part of a valid B8ZS code occurs (when UNI is logic 0 in the J2 FRMR Configuration Register) or if a 0 to 1 transition is detected on RNEG/RLCV/ROHM[x] (when UNI is logic 1). BPVI is cleared when this register is read.

FRMEI

The FRMEI bit is set to logic 1 if an errored framing bit occurs. FRMEI is cleared when this register is read.

CRCEI

The CRCEI bit is set to logic 1 if a failed CRC-5 check occurs. CRCEI is cleared when this register is read.

Register 0x04C, 0x44C, 0x124C, 0x164C: J2 TRAN Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	X3SET	1
Bit 2	R/W	X2SET	1
Bit 1	R/W	X1SET	1
Bit 0	R/W	RLOF	0

RLOF

The RLOF bit controls the state of the A-bit in the J2 stream. The RLOF bit is logically ORed with the LOS, OOF, LOF, AIS, and LCD indications from the J2 FRMR and RXCP when the LOSEN, OOFEN, RBLEN, AISEN, and LCDEN register bits (in the Channel Data Link and FERF/RAI Control register) are set to logic 1 respectively. In addition, the RLOF bit is logically ORed with the OOF, LOF, and AIS indications from the J2 FRMR AUX when the OOFEN, RBLEN, and AISEN register bits (in the Channel Auxiliary Framer Data Link and FERF/RAI Control register) are set to logic 1 respectively. When the OR of the three signals is logic 1, the A-bit is set to logic 1. When the OR of the three signals is logic 0, the A-bit is set to logic 0.

X1SET

The X1SET bit controls the state of the X1 bit (bit 785 in the third frame of a J2 multi-frame). When X1SET is a logic 1, the X1 bit is set to logic 1. When X1SET is a logic 0, the X1 bit is set to logic 0.

X2SET

The X2SET bit controls the state of the X2 bit (bit 786 in the third frame of a J2 multi-frame). When X2SET is a logic 1, the X2 bit is set to logic 1. When X2SET is a logic 0, the X2 bit is set to logic 0.

X3SET

The X3SET bit controls the state of the X3 bit (bit 787 in the third frame of a J2 multi-frame). When X3SET is a logic 1, the X3 bit is set to logic 1. When X3SET is a logic 0, the X3 bit is set to logic 0.

Register 0x04D, 0x44D, 0x124D, 0x164D: J2 TRAN Diagnostic

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	PLDAIS	0
Bit 4	R/W	PHYAIS	0
Bit 3	R/W	DCRC	0
Bit 2	R/W	DLOS	0
Bit 1	R/W	DBPV	0
Bit 0	R/W	DFERR	0

DFERR

The DFERR bit controls the insertion of framing alignment signal errors. When DFERR is set to logic 1, the framing alignment signal is inverted. When DFERR is set to logic 0, the framing alignment signal is not inverted.

DBPV

The DBPV bit controls the insertion of single bipolar violations. When DBPV bit transitions from 0 to 1, a violation is generated by masking the first violation pulse of a B8ZS signature. To generate another violation, this bit must first be written to 0 and then to logic 1 again. When DBPV is a logic 0, no violation is generated.

DLOS

When set to logic 1, the DLOS bit forces the unipolar and bipolar outputs of the J2 TRAN to be all-zeros. When DLOS is logic 0, the outputs of the J2 TRAN operate normally.

DCRC

When set to logic 1, a the CRC-5 check bits (e_{1-5}) are inverted before transmission. DCRC inverts the e_{1-5} bits even if CDIS of the J2 TRAN Configuration register is set to logic 1.

PHYAIS

When set to logic 1, PHYAIS will cause the J2 TRAN to transmit an all 1's Alarm Indication Signal (AIS).

PLDAIS

When set to logic 1, PLDAIS will cause the J2 TRAN to insert all 1's in the payload data bits. When PLDAIS is a logic 0, data is processed normally through the J2 TRAN.

Register 0x04E, 0x44E, 0x124E, 0x164E: J2 TRAN TS97 Signaling

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	TS97[1]	1
Bit 6	R/W	TS97[2]	1
Bit 5	R/W	TS97[3]	1
Bit 4	R/W	TS97[4]	1
Bit 3	R/W	TS97[5]	1
Bit 2	R/W	TS97[6]	1
Bit 1	R/W	TS97[7]	1
Bit 0	R/W	TS97[8]	1

TS97[1:8]

The TS97[1:8] bits control what is inserted into timeslot 97 in the J2 frame. TS97[1] is the first bit transmitted of timeslot 97.

Register 0x04F, 0x44F, 0x124F, 0x164F: J2 TRAN TS98 Signaling

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	TS98[1]	1
Bit 6	R/W	TS98[2]	1
Bit 5	R/W	TS98[3]	1
Bit 4	R/W	TS98[4]	1
Bit 3	R/W	TS98[5]	1
Bit 2	R/W	TS98[6]	1
Bit 1	R/W	TS98[7]	1
Bit 0	R/W	TS98[8]	1

TS98[1:8]

The TS98[1:8] bits control what is inserted into timeslot 98 in the J2 frame. TS98[1] is the first bit transmitted of timeslot 98.

Register 0x050, 0x450, 0x1250, 0x1650: RDLC Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	MEN	0
Bit 2	R/W	MM	0
Bit 1	R/W	TR	0
Bit 0	R/W	EN	0

The RDLC block has been further illustrated in PMC-2021632 “SUNI 4xJET ASSP Telecom Standard Product Data Sheet.”

EN

The EN bit controls the overall operation of the RDLC. When EN is set to logic 1, RDLC is enabled; when set to logic 0, RDLC is disabled. When RDLC is disabled, the RDLC FIFO buffer and interrupts are all cleared. When RDLC is enabled, it will immediately begin looking for flags.

TR

Setting the terminate reception (TR) bit to logic 1 forces the RDLC to immediately terminate the reception of the current data frame, empty the RDLC FIFO buffer, clear the interrupts, and begin searching for a new flag sequence. The RDLC handles a terminate reception event in the same manner as it would the toggling of the EN bit from logic 1 to logic 0 and back to logic 1. Thus, the RDLC state machine will begin searching for flags. An interrupt will be generated when the first flag is detected. The TR bit will reset itself to logic 0 after the register write operation is completed and a rising and falling edge occurs on the internal datalink clock input. If the RDLC Configuration Register is read after this time, the TR bit value returned will be logic 0.

MM

Setting the Match Mask (MM) bit to logic 1 ignores the PA[1:0] bits of the Primary Address Match Register, the SA[1:0] bits of the Secondary Address Match Register, and the two least significant bits of the universal all-ones address when performing the address comparison.

MEN

Setting the Match Enable (MEN) bit to logic 1 enables the detection and storage in the RDLC FIFO of only those packets whose first data byte matches either of the bytes written to the Primary or Secondary Match Address Registers, or the universal all-ones address. When the MEN bit is logic 0, all packets received are written into the RDLC FIFO.

Register 0x051, 0x451, 0x1251, 0x1651: RDLC Interrupt Control

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	INTE	0
Bit 6	R/W	INTC[6]	0
Bit 5	R/W	INTC[5]	0
Bit 4	R/W	INTC[4]	0
Bit 3	R/W	INTC[3]	0
Bit 2	R/W	INTC[2]	0
Bit 1	R/W	INTC[1]	0
Bit 0	R/W	INTC[0]	0

INTC[6:0]

The INTC[6:0] bits control the assertion of FIFO fill level set point interrupts. The value of INTC[6:0] = ‘b0000000 sets the interrupt FIFO fill level to 128.

INTE

The Interrupt Enable bit (INTE) must set to logic 1 to allow the internal interrupt status to be propagated to the INTB output. When the INTE bit is logic 0 the RDLC will not assert INTB.

The contents of the Interrupt Control Register should only be changed when the EN bit in the RDLC Configuration Register is logic 0. This prevents any erroneous interrupt generation.

Register 0x052, 0x452, 0x1252, 0x1652: RDLC Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	FE	X
Bit 6	R	OVR	X
Bit 5	R	COLS	X
Bit 4	R	PKIN	X
Bit 3	R	PBS[2]	X
Bit 2	R	PBS[1]	X
Bit 1	R	PBS[0]	X
Bit 0	R	INTR	X

Consecutive reads of the RDLC Status and Data registers should not occur at rates greater than 1/10 that of the clock selected by the LINESYSCLK bit of the Channel Misc. #1 register (channel address 0x09E).

INTR

The interrupt (INTR) bit reflects the status of the internal RDLC interrupt. If the INTE bit in the RDLC Interrupt Control Register is set to logic 1, a RDLC interrupt (INTR is a logic 1) will cause INTB to be asserted low. The INTR register bit will be set to logic 1 when one of the following conditions occurs:

- The number of bytes specified in the RDLC Interrupt Control register have been received on the data link and written into the FIFO.
- RDLC FIFO buffer overrun has been detected.
- The last byte of a packet has been written into the RDLC FIFO.
- The last byte of an aborted packet has been written into the RDLC FIFO.
- Transition of receiving all-ones to receiving flags has been detected.

PBS[2:0]

The packet byte status (PBS[2:0]) bits indicate the status of the data last read from the FIFO as indicated in the following table:

Table 16 RDLC PBS[2:0] Data Status

PBS[2:0]	Data Status
000	The data byte read from the FIFO is not special.
001	The data byte read from the FIFO is the dummy byte that was written into the FIFO when the first HDLC flag sequence (01111110) was detected. This indicates that the data link became active.
010	The data byte read from the FIFO is the dummy byte that was written into the FIFO when the HDLC abort sequence (01111111) was detected. This indicates that the data link became inactive.
011	Unused.
100	The data byte read from the FIFO is the last byte of a normally terminated packet with no CRC error and the packet received had an integer number of bytes.
101	The data byte read from the FIFO must be discarded because there was a non-integer number of bytes in the packet.
110	The data byte read from the FIFO is the last byte of a normally terminated packet with a CRC error. The packet was received in error.
111	The data byte read from the FIFO is the last byte of a normally terminated packet with a CRC error and a non-integer number of bytes. The packet was received in error.

PKIN

The Packet In (PKIN) bit is logic 1 when the last byte of a non-aborted packet is written into the FIFO. The PKIN bit is cleared to logic 0 after the RDLC Status Register is read.

COLS

The Change of Link Status (COLS) bit is set to logic 1 if the RDLC has detected the HDLC flag sequence (01111110) or HDLC abort sequence (01111111) in the data. This indicates that there has been a change in the data link status. The COLS bit is cleared to logic 0 by reading this register or by clearing the EN bit in the RDLC Configuration Register. For each change in link status, a byte is written into the FIFO. If the COLS bit is found to be logic 1 then the RDLC FIFO must be read until empty. The status of the data link is determined by the PBS[2:0] bits associated with the data read from the RDLC FIFO.

OVR

The overrun (OVR) bit is set to logic 1 when data is written over unread data in the RDLC FIFO buffer. This bit is not reset to logic 0 until after the Status Register is read. While the OVR bit is logic 1, the RDLC and RDLC FIFO buffer are held in the reset state, causing the COLS and PKIN bits to be reset to logic 0.

FE

The FIFO buffer empty (FE) bit is set to logic 1 when the last RDLC FIFO buffer entry is read. The FE bit goes to logic 0 when the FIFO is loaded with new data.

Register 0x053, 0x453, 0x1253, 0x1653: RDLC Data

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	RD[7]	X
Bit 6	R	RD[6]	X
Bit 5	R	RD[5]	X
Bit 4	R	RD[4]	X
Bit 3	R	RD[3]	X
Bit 2	R	RD[2]	X
Bit 1	R	RD[1]	X
Bit 0	R	RD[0]	X

Consecutive reads of the RDLC Status and Data registers should not occur at rates greater than 1/10 that of the clock selected by the LINESYSCLK bit of the Channel Misc. #1 register (channel address 0x09E).

RD[7:0]

RD[7:0] contains the received data link information. RD[0] corresponds to the first received bit of the data link message.

This register reads from the RDLC 128-byte FIFO buffer. If data is available, the FE bit in the FIFO Input Status Register is logic 0.

When an overrun is detected, an interrupt is generated and the FIFO buffer is held cleared until the RDLC Status Register is read.

Register 0x054, 0x454, 0x1254, 0x1654: RDLC Primary Address Match

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	PA[7]	1
Bit 6	R/W	PA[6]	1
Bit 5	R/W	PA[5]	1
Bit 4	R/W	PA[4]	1
Bit 3	R/W	PA[3]	1
Bit 2	R/W	PA[2]	1
Bit 1	R/W	PA[1]	1
Bit 0	R/W	PA[0]	1

PA[7:0]

The first byte received after a flag character is compared against the contents of this register. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. PA[0] corresponds to the first received bit of the data link message. The MM bit in the Configuration Register is used mask off PA[1:0] during the address comparison.

Register 0x055, 0x455, 0x1255, 0x1655: RDLC Secondary Address Match

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	SA[7]	1
Bit 6	R/W	SA[6]	1
Bit 5	R/W	SA[5]	1
Bit 4	R/W	SA[4]	1
Bit 3	R/W	SA[3]	1
Bit 2	R/W	SA[2]	1
Bit 1	R/W	SA[1]	1
Bit 0	R/W	SA[0]	1

SA[7:0]

The first byte received after a flag character is compared against the contents of this register. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. SA[0] corresponds to the first received bit data link message. The MM bit in the Configuration Register is used mask off SA[1:0] during the address comparison.

Register 0x058, 0x458, 0x1258, 0x1658: TDPR Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	FLGSHARE	1
Bit 6	R/W	FIFOCLR	0
Bit 5	R/W	Reserved	0
Bit 4	—	Unused	X
Bit 3	R/W	EOM	0
Bit 2	R/W	ABT	0
Bit 1	R/W	CRC	1
Bit 0	R/W	EN	0

Consecutive writes to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register and reads of the TDPR Interrupt Status/UDR Clear register should not occur at rates greater than 1/8th that of the clock selected by the LINESYSCLK bit of the Channel Misc. #1 register (channel address 0x09E).

The TDPR block has been further illustrated in PMC-2021632 SUNI 4xJET ASSP Telecom Standard Product Data Sheet."

EN

The EN bit enables the TDPR functions. When EN is set to logic 1, the TDPR is enabled and flag sequences are sent until data is written into the TDPR Transmit Data register. When the EN bit is set to logic 0, the TDPR is disabled and an all 1's Idle sequence is transmitted on the datalink.

CRC

The CRC enable bit controls the generation of the CCITT_CRC frame check sequence (FCS). Setting the CRC bit to logic 1 enables the CCITT-CRC generator and appends the 16-bit FCS to the end of each message. When the CRC bit is set to logic 0, the FCS is not appended to the end of the message. The CRC type used is the CCITT-CRC with generator polynomial $x^{16} + x^{12} + x^{5} + 1$. The high order bit of the FCS word is transmitted first.

ABT

The Abort (ABT) bit controls the sending of the 7 consecutive ones HDLC abort code. Setting the ABT bit to a logic 1 causes the 01111111 code (the 0 is transmitted first) to be transmitted after the current byte from the TDPR FIFO is transmitted. The TDPR FIFO is then reset. All data in the TDPR FIFO will be lost. Aborts are continuously sent and the FIFO is held in reset until this bit is reset to a logic 0. At least one Abort sequence will be sent when the ABT bit transitions from logic 0 to logic 1.

EOM

The EOM bit indicates that the last byte of data written in the Transmit Data register is the end of the present data packet. If the CRC bit is set then the 16-bit FCS word is appended to the last data byte transmitted and a continuous stream of flags is generated. The EOM bit is automatically cleared upon a write to the TDPR Transmit Data register.

FIFOCLR

The FIFOCLR bit resets the TDPR FIFO. When set to logic 1, FIFOCLR will cause the TDPR FIFO to be cleared.

FLGSHARE

The FLGSHARE bit configures the TDPR to share the opening and closing flags between successive frames. If FLGSHARE is logic 1, then the opening and closing flags between successive frames are shared. If FLGSHARE is logic 0, then separate closing and opening flags are inserted between successive frames.

Register 0x059, 0x459, 0x1259, 0x1659: TDPR Upper Transmit Threshold

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	UTHR[6]	1
Bit 5	R/W	UTHR[5]	0
Bit 4	R/W	UTHR[4]	0
Bit 3	R/W	UTHR[3]	0
Bit 2	R/W	UTHR[2]	0
Bit 1	R/W	UTHR[1]	0
Bit 0	R/W	UTHR[0]	0

UTHR[6:0]

The UTHR[6:0] bits define the TDPR FIFO fill level which will automatically cause the bytes stored in the TDPR FIFO to be transmitted. Once the fill level exceeds the UTHR[6:0] value, transmission will begin. Transmission will not stop until the last complete packet is transmitted and the TDPR FIFO fill level is below UTHR[6:0] + 1.

The value of UTHR[6:0] must always be greater than the value of LINT[6:0] unless both values are equal to 00H.

Register 0x05A, 0x45A, 0x125A, 0x165A: TDPR Lower Interrupt Threshold

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	LINT[6]	0
Bit 5	R/W	LINT[5]	0
Bit 4	R/W	LINT[4]	0
Bit 3	R/W	LINT[3]	0
Bit 2	R/W	LINT[2]	1
Bit 1	R/W	LINT[1]	1
Bit 0	R/W	LINT[0]	1

LINT[6:0]

The LINT[6:0] bits define the TDPR FIFO fill level which causes an internal interrupt (LFILLI) to be generated. Once the TDPR FIFO level decrements to empty or to a value less than LINT[6:0], LFILLI and BLFILL register bits will be set to logic 1. LFILLI will cause an interrupt on INTB if LFILLE is set to logic 1.

The value of LINT[6:0] must always be less than the value of UTHR[6:0] unless both values are equal to 00H.

Register 0x05B, 0x45B, 0x125B, 0x165B: TDPR Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	FULLE	0
Bit 2	R/W	OVRE	0
Bit 1	R/W	UDRE	0
Bit 0	R/W	LFILLE	0

LFILLE

The LFILLE enables a transition to logic 1 on LFILLI to generate an interrupt on INTB. If LFILLE is a logic 1, a transition to logic 1 on LFILLI will generate an interrupt on INTB. If LFILLE is a logic 0, a transition to logic 1 on LFILLI will not generate an interrupt on INTB.

UDRE

The UDRE enables a transition to logic 1 on UDRI to generate an interrupt on INTB. If UDRE is a logic 1, a transition to logic 1 on UDRI will generate an interrupt on INTB. If UDRE is a logic 0, a transition to logic 1 on UDRI will not generate an interrupt on INTB.

OVRE

The OVRE enables a transition to logic 1 on OVRI to generate an interrupt on INTB. If OVRE is a logic 1, a transition to logic 1 on OVRI will generate an interrupt on INTB. If OVRE is a logic 0, a transition to logic 1 on OVRI will not generate an interrupt on INTB.

FULLE

The FULLE enables a transition to logic 1 on FULLI to generate an interrupt on INTB. If FULLE is a logic 1, a transition to logic 1 on FULLI will generate an interrupt on INTB. If FULLE is a logic 0, a transition to logic 1 on FULLI will not generate an interrupt on INTB.

Register 0x05C, 0x45C, 0x125C, 0x165C: TDPR Interrupt Status/UDR Clear

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R	FULL	X
Bit 5	R	BLFILL	X
Bit 4	R	Unused	X
Bit 3	R	FULLI	X
Bit 2	R	OVRI	X
Bit 1	R	UDRI	X
Bit 0	R	LFILLI	X

Consecutive writes to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register and reads of the TDPR Interrupt Status/UDR Clear register should not occur at rates greater than 1/8th that of the clock selected by the LINESYSCLK bit of the Channel Misc. #1 register (channel address 0x09E).

LFILLI

The LFILLI bit will transition to logic 1 when the TDPR FIFO level transitions to empty or falls below the value of LINT[6:0] programmed in the TDPR Lower Interrupt Threshold register. LFILLI will assert INTB if it is a logic 1 and LFILLE is programmed to logic 1. LFILLI is cleared when this register is read.

UDRI

The UDRI bit will transition to 1 when the TDPR FIFO underruns. That is, the TDPR was in the process of transmitting a packet when it ran out of data to transmit. UDRI will assert INTB if it is a logic 1 and UDRE is programmed to logic 1. UDRI is cleared when this register is read.

OVRI

The OVRI bit will transition to 1 when the TDPR FIFO overruns. That is, the TDPR FIFO was already full when another data byte was written to the TDPR Transmit Data register. OVRI will assert INTB if it is a logic 1 and OVRE is programmed to logic 1. OVRI is cleared when this register is read.

FULLI

The FULLI bit will transition to logic 1 when the TDPR FIFO is full. FULLI will assert INTB if it is a logic 1 and FULLE is programmed to logic 1. FULLI is cleared when this register is read.

BLFILL

The BLFILL bit is set to logic 1 if the current FIFO fill level is below the LINT[7:0] level or is empty.

FULL

The FULL bit reflects the current condition of the TDPR FIFO. If FULL is a logic 1, the TDPR FIFO already contains 128-bytes of data and can accept no more.

Register 0x05D, 0x45D, 0x125D, 0x165D: TDPR Transmit Data

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	TD[7]	X
Bit 6	R/W	TD[6]	X
Bit 5	R/W	TD[5]	X
Bit 4	R/W	TD[4]	X
Bit 3	R/W	TD[3]	X
Bit 2	R/W	TD[2]	X
Bit 1	R/W	TD[1]	X
Bit 0	R/W	TD[0]	X

Consecutive writes to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register and reads of the TDPR Interrupt Status/UDR Clear register should not occur at rates greater than 1/8th that of the clock selected by the LINESYSCLK bit of the Channel Misc. #1 register (channel address 0x09E).

TD[7:0]

The TD[7:0] bits contain the data to be transmitted on the data link. Data written to this register is serialized and transmitted (TD[0] is transmitted first).

Register 0x060, 0x460, 0x1260, 0x1660: RXCP Configuration 1

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	DDSCR	0
Bit 6	R/W	HDSCR	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	HCSADD	1
Bit 1	R/W	HCSDQB	0
Bit 0	R/W	Reserved	0

HCSDQDB

The HCSDQDB bit enables HCS checking for either ATM type cells or DQDB type cells. When logic 0, ATM type cells are processed by checking all 4 octets in the header for HCS validation. When logic 1, DQDB cells are processed by checking only 3 of the header octets (octets 2, 3 and 4) for HCS validation.

HCSADD

The HCSADD bit controls the addition of the coset polynomial, $x^6+x^4+x^2+1$, to the HCS octet prior to comparison. When HCSADD is a logic 1, the polynomial is added, and the resulting HCS is compared. When HCSADD is a logic 0, the polynomial is not added, and the unmodified HCS is compared.

HDSCR

HDSCR enables the self-synchronous $x^{43} + 1$ descrambler to continue running through the bytes which should contain the ATM cell headers. When HDSCR is set to logic 0, the descrambling polynomial will function only over the ATM payload bytes. When HDSCR is set to logic 1, the descrambling polynomial will function over all bytes, including the 5 ATM header bytes. This function is available for use in a transparent mode where “cells” are scrambled at the source to prevent the generation of "killer" sequences.

DDSCR

The DDSCR bit controls the descrambling of the cell payload with the polynomial $x^{43} + 1$. When DDSCR is set to logic 1, cell payload descrambling is disabled. When DDSCR is set to logic 0, payload descrambling is enabled.

Register 0x061, 0x461, 0x1261, 0x1661: RXCP Configuration 2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	CCDIS	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	IDLEPASS	0
Bit 4	R/W	IN52	0
Bit 3	R/W	ALIGN[1]	0
Bit 2	R/W	ALIGN[0]	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

ALIGN[1:0]

ALIGN[1:0] configures the RXCP to perform cell delineation based on byte, nibble, or bit wide search algorithms when ATM Direct Mapping is used. Cell alignment is relative to overhead bits in the serial input data stream. The ALIGN[1:0] bits are valid only if ATM direct mapping is used - PLCP framing must be disabled. Recommended settings for DS3, E3, and J2 are shown.

Table 17 RXCP Cell Delineation Algorithm Base

ALIGN[1:0]	Cell Delineation Algorithm Base
00	Bit
01	Nibble (DS3)
10	Byte (E3,J2, E1, T1)
11	Unused

IN52

The IN52 bit defines the number of bytes contained in incoming cells. When IN52 is a logic '0', incoming cells are 53 bytes in length. When IN52 is a logic '1', incoming cells are 52 bytes in length. In order for ATM cell delineation to function properly, incoming cells must be 53 bytes in length including a valid HCS byte. The HCS byte can be stripped off on the Utopia side using the DS27_53 register bit. If the S/UNI 4xJET is operating in a transparent mode, incoming "cells" may be composed of 52 or 53 bytes without an HCS byte. In this case, the CCDIS register bit should be set to disable cell delineation, and the DS27_53 register bit should be set so that it is consistent with IN52.

IDLEPASS

The IDLEPASS bit controls the function of the Idle Cell filter. When IDLEPASS is written with a logic 0, all cells that match the Idle Cell Header Pattern and Idle Cell Header Mask are filtered out. When IDLEPASS is a logic 1, the Idle Cell Header Pattern and Mask registers are ignored. The default state of this bit and the bits in the Idle Cell Header Mask and Idle Cell Header Pattern Registers enable the dropping of idle cells.

CCDIS

The CCDIS bit can be used to disable all cell filtering and cell delineation. All payload data read by the RXCP is passed into its FIFO without the requirement of having to find cell delineation first. If PLCP framing is disabled, then alignment of the data read out of the ATM interface with respect to the line overhead is set by the ALIGN[1:0] bits of this register.

Register 0x062, 0x462, 0x1262, 0x1662: RXCP FIFO/UTOPIA Control & Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	RXPTYP	0
Bit 6	—	Unused	X
Bit 5	R/W	RCAINV	0
Bit 4	R/W	RCALEVEL0	1
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R/W	FIFORST	0

FIFORST

The FIFORST bit is used to reset the four-cell receive FIFO. When FIFORST is set to logic 0, the FIFO operates normally. When FIFORST is set to logic 1, the FIFO is immediately emptied and further writes into the FIFO are ignored (no incoming ATM cells will be stored in the FIFO). The FIFO remains empty and continues to ignore writes until a logic 0 is written to FIFORST.

See the Operations Section in PMC-2021632 on resetting the receive and transmit FIFOs.

RCALEVEL0

The RCALEVEL0 register bit selects the behavior of RCA when it deasserts (transition to logic 0 if RCAINV is logic 0, or transition to logic 1 if RCAINV is logic 1) as the receive FIFO empties. When RCALEVEL0 is set to logic 1, RCA indicates that the receive FIFO is empty. RCA , if polled, will deassert on the rising RFCLK edge after Payload byte 24 is output. When RCALEVEL0 is set to logic 0, RCA, if polled, indicates that the receive FIFO is near empty. RCA, if polled, will deassert on the rising RFCLK edge after Payload byte 19 is output.

RCALEVEL0 must be set low when the system interface is configured for Level 3 operation.

RCAINV

The RCAINV bit inverts the polarity of the RCA output signal. When RCAINV is a logic 1, the polarity of RCA is inverted and RCA at logic 0 means there is a receive cell available to be read). When RCAINV is a logic 0, the polarity of RCA is not inverted.

RCAINV must be set low when the system interface is configured for Level 3 operation.

RXPTYP

The RXPTYP bit selects even or odd parity for output RXPRTY. When set to logic 1, output RXPRTY is the even parity bit for outputs RDAT[15:0]. When RXPTYP is set to logic 0, RXPRTY is the odd parity bit for outputs RDAT[15:0].

RXPTYP must be set low when the system interface is configured for Level 3 operation.

Register 0x063, 0x463, 0x1263, 0x1663: RXCP Interrupt Enables and Counter Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	XFERI	X
Bit 6	R	OVR	X
Bit 5	—	Unused	X
Bit 4	R/W	XFERE	0
Bit 3	R/W	OOCDE	0
Bit 2	R/W	HCSE	0
Bit 1	R/W	FOVRE	0
Bit 0	R/W	LCDE	0

LCDE

The LCDE bit enables the generation of an interrupt due to a change in the LCD state. When LCDE is set to logic 1, the interrupt is enabled.

FOVRE

The FOVRE bit enables the generation of an interrupt due to a FIFO overrun error condition. When FOVRE is set to logic 1, the interrupt is enabled.

HCSE

The HCSE bit enables the generation of an interrupt due to the detection HCS error. When HCSE is set to logic 1, the interrupt is enabled.

OOCDE

The OOCDE bit enables the generation of an interrupt due to a change in cell delineation state. When OOCDE is set to logic 1, the interrupt is enabled.

XFERE

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the RXCP Count registers. When XFERE is set to logic 1, the interrupt is enabled.

OVR

The OVR bit is the overrun status of the RXCP Performance Monitoring Count registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFERI being logic 1) has not been acknowledged before the next accumulation interval has occurred and that the contents of the RXCP Count registers have been overwritten. OVR is set to logic 0 when this register is read.

XFERI

The XFERI bit indicates that a transfer of RXCP Performance Monitoring Count data has occurred. A logic 1 in this bit position indicates that the RXCP Count registers have been updated. This update is initiated by writing to one of the RXCP Count register locations or to the S/UNI 4xJET Master Reset and Identity register. XFERI is set to logic 0 when this register is read.

Register 0x064, 0x464, 0x1264, 0x1664: RXCP Status/Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	OOCDV	X
Bit 6	R	LCDV	X
Bit 5	—	Unused	X
Bit 4	R	OOCDI	X
Bit 3	—	Unused	X
Bit 2	R	HCSI	X
Bit 1	R	FOVRI	X
Bit 0	R	LCDI	X

LCDI

The LCDI bit is set high when there is a change in the loss of cell delineation (LCD) state. This bit is reset immediately after a read to this register.

FOVRI

The FOVRI bit is set high when an attempt is made to write into the channel buffer when it is already full. This bit is reset immediately after a read to this register. Continuous over-writing of the channel buffer results in only one interrupt.

HCSI

The HCSI bit is set high when an HCS error is detected. This bit is reset immediately after a read to this register.

OOCDI

The OOCDI bit is set high when the RXCP enters or exits the SYNC state. The OOCDV bit indicates whether the RXCP is in the SYNC state or not. The OOCDI bit is reset immediately after a read to this register.

LCDV

The LCDV bit gives the Loss of Cell Delineation state. When LCD is logic 1, an out of cell delineation (OCD) defect has persisted for the number of cells specified in the LCD Count Threshold register. When LCD is logic 0, no OCD has persisted for the number of cells specified in the LCD Count Threshold register. The cell time period can be varied by using the LCDC[7:0] register bits in the RXCP LCD Count Threshold register.

OOCDV

The OOCDV bit indicates the cell delineation state. When OOCDV is high, the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states and is hunting for the cell boundaries. When OOCDV is low, the cell delineation state machine is in the 'SYNC' state and cells are passed through the receive FIFO.

Register 0x065, 0x465, 0x1265, 0x1665: RXCP LCD Count Threshold (MSB)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	LCDC[10]	0
Bit 1	R/W	LCDC[9]	0
Bit 0	R/W	LCDC[8]	1

Register 0x066, 0x466, 0x1266, 0x1666: RXCP LCD Count Threshold (LSB)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	LCDC[7]	0
Bit 6	R/W	LCDC[6]	1
Bit 5	R/W	LCDC[5]	1
Bit 4	R/W	LCDC[4]	0
Bit 3	R/W	LCDC[3]	1
Bit 2	R/W	LCDC[2]	0
Bit 1	R/W	LCDC[1]	0
Bit 0	R/W	LCDC[0]	0

LCDC[10:0]

The LCDC[10:0] bits represent the number of consecutive cell periods the receive cell processor must be out of cell delineation before loss of cell delineation (LCD) is declared. Likewise, LCD is not deasserted until receive cell processor is in cell delineation for the number of cell periods specified by LCDC[10:0].

The default value of LCD[10:0] is 360, which translates to the following integration periods:

Table 18 RXCP LCD Integration Periods

Format	Average Cell Period	Default LCD Integration Period
DS3 Direct Mapping	9.59 µs	3.45 ms
DS3 PLCP	10.42 µs	3.75 ms
E3 G.751 Direct Mapping	12.46 µs	4.49 ms
E3 G.751 PLCP	13.89 µs	5.00 ms
E3 G.832	12.50 µs	4.50 ms
J2 Direct Mapping	69.01 µs	24.84 ms
DS1 Direct Mapping	276.00 µs	99.40 ms
DS1 PLCP	300.00 us	108.00 ms
E1 Direct Mapping	220.83 µs	79.50 ms
E1 PLCP	237.50 µs	85.50 ms

Register 0x067, 0x467, 0x1267, 0x1667: RXCP Idle Cell Header Pattern

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	GFC[3]	0
Bit 6	R/W	GFC[2]	0
Bit 5	R/W	GFC[1]	0
Bit 4	R/W	GFC[0]	0
Bit 3	R/W	PTI[2]	0
Bit 2	R/W	PTI[1]	0
Bit 1	R/W	PTI[0]	0
Bit 0	R/W	CLP	1

CLP

The CLP bit contains the pattern to match in the eighth bit of the fourth octet of the 53-octet cell, in conjunction with the Match Header Mask Register. The IDLEPASS bit in the Configuration 2 Register must be set to logic zero to enable dropping of cells matching this pattern.

PTI[2:0]

The PTI[2:0] bits contain the pattern to match in the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell, in conjunction with the Idle Cell Header Mask Register. The IDLEPASS bit in the Configuration 2 Register must be set to logic zero to enable dropping of cells matching this pattern.

GFC[3:0]

The GFC[3:0] bits contain the pattern to match in the first, second, third, and fourth bits of the first octet of the 53-octet cell, in conjunction with the Idle Cell Header Mask Register. The IDLEPASS bit in the Configuration 2 Register must be set to logic zero to enable dropping of cells matching this pattern. Note that an all-zeros pattern must be present in the VPI and VCI fields of the idle or unassigned cell.

Register 0x068, 0x468, 0x1268, 0x1668: RXCP Idle Cell Header Mask

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	MGFC[3]	1
Bit 6	R/W	MGFC[2]	1
Bit 5	R/W	MGFC[1]	1
Bit 4	R/W	MGFC[0]	1
Bit 3	R/W	MPTI[2]	1
Bit 2	R/W	MPTI[1]	1
Bit 1	R/W	MPTI[0]	1
Bit 0	R/W	MCLP	1

MCLP

The CLP bit contains the mask pattern for the eighth bit of the fourth octet of the 53-octet cell. This mask is applied to the Idle Cell Header Pattern Register to select the bits included in the cell filter. A logic one in this bit position enables the MCLP bit in the pattern register to be compared. A logic zero causes the masking of the MCLP bit.

MPTI[2:0]

The MPTI[2:0] bits contain the mask pattern for the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell. This mask is applied to the Idle Cell Header Pattern Register to select the bits included in the cell filter. A logic one in any bit position enables the corresponding bit in the pattern register to be compared. A logic zero causes the masking of the corresponding bit.

MGFC[3:0]

The MGFC[3:0] bits contain the mask pattern for the first, second, third, and fourth bits of the first octet of the 53-octet cell. This mask is applied to the Idle Cell Header Pattern Register to select the bits included in the cell filter. A logic one in any bit position enables the corresponding bit in the pattern register to be compared. A logic zero causes the masking of the corresponding bit.

Register 0x06A, 0x46A, 0x126A, 0x166A: RXCP HCS Error Count

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	HCS[7]	X
Bit 6	R	HCS[6]	X
Bit 5	R	HCS[5]	X
Bit 4	R	HCS[4]	X
Bit 3	R	HCS[3]	X
Bit 2	R	HCS[2]	X
Bit 1	R	HCS[1]	X
Bit 0	R	HCS[0]	X

HCS[7:0]

The HCS[7:0] bits indicate the number of HCS error events that occurred during the last accumulation interval.

This counter (and all other counters in the RXCP) is polled by writing to any of the RXCP counter registers (channel addresses 0x069 to 0x070) or to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800). Such a write transfers the internally accumulated count to the UHCS Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 0x06B, 0x46B, 0x126B, 0x166B: RXCP Receive Cell Counter (LSB)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	RCELL[7]	X
Bit 6	R	RCELL[6]	X
Bit 5	R	RCELL[5]	X
Bit 4	R	RCELL[4]	X
Bit 3	R	RCELL[3]	X
Bit 2	R	RCELL[2]	X
Bit 1	R	RCELL[1]	X
Bit 0	R	RCELL[0]	X

Register 0x06C, 0x46C, 0x126C, 0x166C: RXCP Receive Cell Counter

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	RCELL[15]	X
Bit 6	R	RCELL[14]	X
Bit 5	R	RCELL[13]	X
Bit 4	R	RCELL[12]	X
Bit 3	R	RCELL[11]	X
Bit 2	R	RCELL[10]	X
Bit 1	R	RCELL[9]	X
Bit 0	R	RCELL[8]	X

Register 0x06D, 0x46D, 0x126D, 0x166D: RXCP Receive Cell Counter (MSB)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	RCELL[23]	X
Bit 6	R	RCELL[22]	X
Bit 5	R	RCELL[21]	X
Bit 4	R	RCELL[20]	X
Bit 3	R	RCELL[19]	X
Bit 2	R	RCELL[18]	X
Bit 1	R	RCELL[17]	X
Bit 0	R	RCELL[16]	X

RCELL[23:0]

The RCELL[23:0] bits indicate the number of cells received and written into the receive FIFO during the last accumulation interval. Cells received and filtered due to HCS errors or Idle cell matches are not counted. The counter should be polled every second to avoid saturation.

This counter (and all other counters in the RXCP) is polled by writing to any of the RXCP counter registers (channel addresses 0x069 to 0x070) or to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800). Such a write transfers the internally accumulated count to the RCELL Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 0x06E, 0x46E, 0x126E, 0x166E: RXCP Idle Cell Counter (LSB)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	ICELL[7]	X
Bit 6	R	ICELL[6]	X
Bit 5	R	ICELL[5]	X
Bit 4	R	ICELL[4]	X
Bit 3	R	ICELL[3]	X
Bit 2	R	ICELL[2]	X
Bit 1	R	ICELL[1]	X
Bit 0	R	ICELL[0]	X

Register 0x06F, 0x46F, 0x126F, 0x166F: RXCP Idle Cell Counter

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	ICELL[15]	X
Bit 6	R	ICELL[14]	X
Bit 5	R	ICELL[13]	X
Bit 4	R	ICELL[12]	X
Bit 3	R	ICELL[11]	X
Bit 2	R	ICELL[10]	X
Bit 1	R	ICELL[9]	X
Bit 0	R	ICELL[8]	X

Register 0x070, 0x470, 0x1270, 0x1670: RXCP Idle Cell Counter (MSB)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	ICELL[23]	X
Bit 6	R	ICELL[22]	X
Bit 5	R	ICELL[21]	X
Bit 4	R	ICELL[20]	X
Bit 3	R	ICELL[19]	X
Bit 2	R	ICELL[18]	X
Bit 1	R	ICELL[17]	X
Bit 0	R	ICELL[16]	X

ICELL[23:0]

The ICELL[23:0] bits indicate the number of idle cells received during the last accumulation interval. The counter should be polled every second to avoid saturation.

This counter (and all other counters in the RXCP) is polled by writing to any of the RXCP counter registers (channel addresses 0x069 to 0x070) or to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800). Such a write transfers the internally accumulated count to the CHCS Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 0x080, 0x480, 0x1280, 0x1680: TXCP Configuration 1

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	TPTYP	0
Bit 6	R/W	TCALEVEL0	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	HCSDQDB	0
Bit 3	R/W	HCSB	0
Bit 2	R/W	HCSADD	1
Bit 1	R/W	DSCR	0
Bit 0	R/W	FIFORST	0

FIFORST

The FIFORST bit is used to reset the four cell transmit FIFO. When FIFORST is set to logic zero, the FIFO operates normally. When FIFORST is set to logic one, the FIFO is immediately emptied and ignores writes. The FIFO remains empty and continues to ignore writes until a logic zero is written to FIFORST. Null/unassigned cells are transmitted until a subsequent cell is written to the FIFO.

See Operations Section in the S/UNI 4xJET Data Sheet (PMC-2021632) on resetting the receive and transmit FIFOs.

DSCR

The DSCR bit controls the scrambling of the cell payload. When DSCR is a logic one, cell payload scrambling is disabled. When DSCR is a logic zero, payload scrambling is enabled. In the case where HSCR is logic one, the payload will be scrambled (along with the header) regardless of the setting of the DSCR bit.

HCSADD

The HCSADD bit controls the addition of the coset polynomial, $x^6+x^4+x^2+1$, to the HCS octet prior to insertion in the synchronous payload envelope. When HCSADD is a logic one, the polynomial is added, and the resulting HCS is inserted. When HCSADD is a logic zero, the polynomial is not added, and the unmodified HCS is inserted. HCSADD takes effect unconditionally regardless of whether a null/unassigned cell is being transmitted or whether the HCS octet has been read from the FIFO.

HCSB

The active low HCSB bit enables the internal generation and insertion of the HCS octet into the transmit cell stream. When HCSB is logic zero, the HCS is generated and inserted internally. When the HCSB and DS27_53 register bits are logic one, the HCS octet read from the transmit FIFO is inserted transparently into the transmit cell stream, but the TXCP will still generate and insert the HCS octet for idle cells. If HCSB is logic one and the 26 word data structure is selected (DS27_53 is logic 0), then no HCS octet is inserted in the transmit data stream.

HCSDQDB

The HCSDQDB bit controls the cell header octets included in the HCS calculation. When a logic 1 is written to HCSDQDB, header octets, 2, 3, and 4 are included in the HCS calculation as required by IEEE-802.6 DQDB specification. When a logic 0 is written to HCSDQDB, all four header octets are included in the HCS calculation as required by the ATM Forum UNI specification and ITU-T Recommendation I.432.

TCALEVEL0

The active high TCA level 0 bit, TCALEVEL0 determines what output TCA indicates when it deasserts (transitions to logic 0 if TCAINV is logic 0, or transitions to logic 1 if TCAINV is logic 1). When TCALEVEL0 is set to logic 1, TCA indicates that the transmit FIFO is full and can accept no more writes. TCA, if polled, will deassert on the rising TFCLK edge when Payload word 23 is sampled. When TCALEVEL0 is set to logic zero, TCA indicates that the transmit FIFO is near full. TCA, if polled, will deassert on the rising TFCLK edge when Payload word 19 is sampled.

TCALEVEL0 must be set low when the system interface is configured for Level 3 operation.

TPTYP

The TPTYP bit selects even or odd parity for input TPRTY. When set to logic one, input TPRTY is the even parity bit for the TDAT[15:0] input bus. When set to logic zero, input TPRTY is the odd parity bit for the TDAT[15:0] input bus.

TCALEVEL0 must be set low when the system interface is configured for Level 3 operation.

Register 0x081, 0x481, 0x1281, 0x1681: TXCP Configuration 2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	TCAINV	0
Bit 3	R/W	FIFODP[1]	0
Bit 2	R/W	FIFODP[0]	0
Bit 1	R/W	DHCS	0
Bit 0	R/W	HCSCTLEB	0

HCSCTLEB

The active low HCS control enable, HCSCTLEB bit enables the XORing of the HCS Control byte with the generated HCS. When set to logic zero, the HCS Control byte provided in the third word of the 27 word data structure is XORed with the generated HCS. When set to logic one, XORing is disabled and the HCS Control byte is ignored.

For normal operation, the HCS Control byte in the ATM cell structure transferred on the system interface should always be 0x00. If not, the HCSCTRLEB register should be set to logic one to prevent corruption of the HCS byte.

DHCS

The DHCS bit controls the insertion of HCS errors for diagnostic purposes. When DHCS is set to logic one, the HCS octet is inverted prior to insertion in the synchronous payload envelope. DHCS takes effect unconditionally regardless of whether a null/unassigned cell is being transmitted or whether the HCS octet has been read from the FIFO. DHCS occurs after any error insertion caused by the Control Byte in the 27-word data structure.

FIFODP[1:0]

The FIFODP[1:0] bits determine the transmit FIFO cell depth at which TCA deasserts. FIFO depth control may be important in systems where the cell latency through the TXCP must be minimized. When the FIFO is filled to the specified depth, the transmit cell available signal, TCA is deasserted. Note that regardless of what fill level FIFODP[1:0] is set to, the transmit cell processor can store 4 complete cells.

FIFODP[1:0] must be set to "00" binary when the system interface is configured for Level 3 operation.

The selectable FIFO cell depths are shown below:

Table 19 TXCP FIFO Depth Configurations

FIFODP[1]	FIFODP[0]	FIFO DEPTH
0	0	4 cells
0	1	3 cells
1	0	2 cells
1	1	1 cell

TCAINV

The TCAINV bit inverts the polarity of the TCA output signal. When TCAINV is a logic 1, the polarity of TCA is inverted (TCA at logic 0 means there is transmit cell space available to be written to). When TCAINV is a logic 0, the polarity of TCA is not inverted.

TCAINV must be set low when the system interface is configured for Level 3 operation.

Register 0x082, 0x482, 0x1282, 0x1682: TXCP Cell Count Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	XFERE	0
Bit 6	R	XFERI	X
Bit 5	R	OVR	X
Bit 4	—	Unused	X
Bit 3	R/W	Reserved	1
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

OVR

The OVR bit is the overrun status of the Transmit Cell Count registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFERI being logic 1) has not been acknowledged before the next accumulation interval has occurred and that the contents of the Transmit Cell Count registers have been overwritten. OVR is set to logic 0 when this register is read.

XFERI

The XFERI bit indicates that a transfer of Transmit Cell Count data has occurred. A logic 1 in this bit position indicates that the Transmit Cell Count registers have been updated. This update is initiated by writing to any of the Transmit Cell Count registers (channel addresses 0x086 to 0x088) or to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800). XFERI is set to logic 0 when this register is read.

XFERE

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the Transmit Cell Count registers. When XFERE is set to logic 1, the interrupt is enabled.

Register 0x083, 0x483, 0x1283, 0x1683: TXCP Interrupt Enable/Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	TPRTYE	0
Bit 6	R/W	FOVRE	0
Bit 5	R/W	TSOCE	0
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R	TPRTYI	X
Bit 1	R	FOVRI	X
Bit 0	R	TSOCI	X

TSOCI

The TSOCI bit is set high when the TSOC input is sampled high during any position other than the first word of the selected data structure. The write address counter is reset to the first word of the data structure when TSOC is sampled high. This bit is reset immediately after a read to this register.

TSOCI should be ignored when the system interface is configured for Level 3 operation.

FOVRI

The FOVRI bit is set high when an attempt is made to write into the FIFO when it is already full. This bit is reset immediately after a read to this register

TPRTYI

The TPRTYI bit indicates if a parity error was detected on the TDAT[15:0] input bus. When logic one, the TPRTYI bit indicates a parity error over the active TDAT[15:0] bus. Odd or even parity is selected using the TPTYPE bit.

TPRTYI should be ignored when the system interface is configured for Level 3 operation.

TSOCE

The TSOCE bit enables the generation of an interrupt when the TSOC input is sampled high during any position other than the first word of the selected data structure. When TSOCE is set to logic one, the interrupt is enabled.

TSOCE must be set low when the system interface is configured for Level 3 operation.

FOVRE

The FOVRE bit enables the generation of an interrupt due to an attempt to write the FIFO when it is already full. When FOVRE is set to logic one, the interrupt is enabled.

TPRTYE

The TPRTYE bit enables transmit parity interrupts. When set to logic one, parity errors are indicated on INTB and TPRTYI. When set to logic zero, parity errors are indicated using bit TPRTYI but are not indicated on output INTB.

TPRTYE must be set low when the system interface is configured for Level 3 operation.

Register 0x084, 0x484, 0x1284, 0x1684: TXCP Idle Cell Header Control

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	GFC[3]	0
Bit 6	R/W	GFC[2]	0
Bit 5	R/W	GFC[1]	0
Bit 4	R/W	GFC[0]	0
Bit 3	R/W	PTI[2]	0
Bit 2	R/W	PTI[1]	0
Bit 1	R/W	PTI[0]	0
Bit 0	R/W	CLP	1

CLP

The CLP bit contains the eighth bit position of the fourth octet of the idle/unassigned cell pattern. Cell rate decoupling is accomplished by transmitting idle cells when the TXCP detects that no outstanding cells exist in the transmit FIFO.

PTI[2:0]

The PTI[2:0] bits contains the fifth, sixth, and seventh bit positions of the fourth octet of the idle/unassigned cell pattern. Idle cells are transmitted when the TXCP detects that no outstanding cells exist in the transmit FIFO.

GFC[3:0]

The GFC[3:0] bits contain the first, second, third, and fourth bit positions of the first octet of the idle/unassigned cell pattern. Idle/unassigned cells are transmitted when the TXCP detects that no outstanding cells exist in the transmit FIFO. The all-zeros pattern is transmitted in the VCI and VPI fields of the idle cell.

Register 0x085, 0x485, 0x1285, 0x1685: TXCP Idle Cell Payload Control

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	PAYLD[7]	0
Bit 6	R/W	PAYLD[6]	1
Bit 5	R/W	PAYLD[5]	1
Bit 4	R/W	PAYLD[4]	0
Bit 3	R/W	PAYLD[3]	1
Bit 2	R/W	PAYLD[2]	0
Bit 1	R/W	PAYLD[1]	1
Bit 0	R/W	PAYLD[0]	0

PAYLD[7:0]

The PAYLD[7:0] bits contain the pattern inserted in the idle cell payload. Idle cells are inserted when the TXCP detects that the transmit FIFO contains no outstanding cells. PAYLD[7] is the most significant bit and is the first bit transmitted. PAYLD[0] is the least significant bit.

Register 0x086, 0x486, 0x1286, 0x1686: TXCP Transmit Cell Count (LSB)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	TCELL[7]	X
Bit 6	R	TCELL[6]	X
Bit 5	R	TCELL[5]	X
Bit 4	R	TCELL[4]	X
Bit 3	R	TCELL[3]	X
Bit 2	R	TCELL[2]	X
Bit 1	R	TCELL[1]	X
Bit 0	R	TCELL[0]	X

Register 0x087, 0x487, 0x1287, 0x1687: TXCP Transmit Cell Count

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	TCELL[15]	X
Bit 6	R	TCELL[14]	X
Bit 5	R	TCELL[13]	X
Bit 4	R	TCELL[12]	X
Bit 3	R	TCELL[11]	X
Bit 2	R	TCELL[10]	X
Bit 1	R	TCELL[9]	X
Bit 0	R	TCELL[8]	X

Register 0x088, 0x488, 0x1288, 0x1688: TXCP Transmit Cell Count (MSB)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	TCELL[23]	X
Bit 6	R	TCELL[22]	X
Bit 5	R	TCELL[21]	X
Bit 4	R	TCELL[20]	X
Bit 3	R	TCELL[19]	X
Bit 2	R	TCELL[18]	X
Bit 1	R	TCELL[17]	X
Bit 0	R	TCELL[16]	X

TCELL[23:0]

The TCELL[23:0] bits indicate the number of cells read from the transmit FIFO and inserted into the transmission stream during the last accumulation interval. Idle cells inserted into the transmission stream are not counted. The counter should be polled every second to avoid saturating.

This counter is polled by writing to any of the TXCP counter registers (channel addresses 0x086 to 0x088) or to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800). Such a write transfers the internally accumulated count to the TCELL Count Registers and simultaneously resets the internal counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Transmit Cell Counter registers. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 0x090, 0x490, 0x1290, 0x1690: TTB Control

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	ZEROEN96	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	RTIUIE	0
Bit 4	R/W	RTIMIE	0
Bit 3	R/W	PER5	0
Bit 2	R/W	TNULL	1
Bit 1	R/W	NOSYNC	0
Bit 0	R/W	Reserved	0

NOSYNC

The NOSYNC bit disables synchronization to the Trail Trace message. When NOSYNC is set high, synchronization is disabled and the bytes of the Trail Trace message are captured by the TTB in a circular buffer. When NOSYNC is set low, the TTB synchronizes to the byte with the most significant bit set high and places that byte in the first location in the capture buffer page.

TNULL

The transmit null (TNULL) bit controls the insertion of all-zeros into the outgoing Trail Trace message. The null insertion should be used when microprocessor accesses that change the outgoing trail trace message are being performed. When TNULL is set high, an all-zeros byte is inserted to the transmit stream. When this bit is set low, the contents of the transmit trace buffer are sent.

PER5

The receive trace identifier persistency bit (PER5) controls the number of times that persistency check is made in order to accept the received message. When this bit is set high, five identical message required in order to accept the message. When this bit set low, three unchanged consecutive messages are required.

RTIMIE

The receive trace identifier mismatch interrupt enable (RTIMIE) controls the activation of INTB when comparison between the accepted identifier message and the expected identifier message changes state from match to mismatch and vice versa (RTIM). When RTIMIE is set high, changes in match state will activate the interrupt (INTB) output. When RTIMIE set low, path trace message match state changes will not affect INTB.

RTIUIE

The receive trace identifier unstable interrupt enable (RTIUIE) controls the activation of INTB when the receive identifier message changes state from stable to unstable and vice versa (RTIU). When RTIUIE is set high, changes in the receive path trace identifier stable/unstable (RTIU) state will activate the interrupt (INTB) output. When RTIUIE is set low, path trace identifier state changes will not affect INTB.

ZEROEN

The zero enable bit (ZEROEN) enables TIM assertion and removal based on an all-zeros path trace message string. When ZEROEN is set high, all-zeros path trace message strings are considered when entering and exiting TIM states (message is compare with the expected one and RTIM is set accordingly). When ZEROEN is set low, all-zeros path trace message strings are ignored (RTIM gets zero when message becomes persistent even if the message does not match the expected one). This register bit does not affect RTIU assertion or removal.

Register 0x091, 0x491, 0x1291, 0x1691: TTB Trail Trace Identifier Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	RTIUI	X
Bit 2	R	RTIUV	X
Bit 1	R	RTIMI	X
Bit 0	R	RTIMV	X

RTIMV

The receive trace identifier mismatch value status bit (RTIMV) is set high when the accepted message differs from the expected message. The accepted message is the last message to have been received 5 times consecutively. RTIMV is set low when the accepted message is equal to the expected message. If the accepted trail trace message string is all-ZEROs, the mismatch is not declared unless the ZEROEN register bit in the Control register is set.

RTIMI

The receive trace identifier mismatch indication status bit (RTIMI) is set high when the trace identifier match/mismatch status (RTIMV) of the trace identifier framer changes state. This bit (and the interrupt) are cleared when this register is read.

RTIUV

The receive trace identifier unstable value status bit is set high when 8 trace messages mismatching against their immediate predecessor message have been received without persistent message being detected. The unstable counter is incremented on each message that mismatches its predecessor and is cleared on the reception of a persistent message (3 or 5 consecutive matching messages). RTIUV is set high when the unstable counter reaches 8. RTIUV is set low and the unstable counter cleared once a persistent message has been received.

RTIUI

The receive trail trace identifier unstable interrupt status bit is set high when the path trace identifier unstable status (RTIUV) changes state. The setting of this bit is dependent on the unstable status (RTIUV) which is dependent on the Trace Identifier Mode. This bit and the interrupt are cleared when this register is read.

Register 0x092, 0x492, 0x1292, 0x1692: TTB Indirect Address

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	A[7]	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

A[7:0]

The indirect read address bits (A[7:0]) indexes into the trail trace identifier buffers. Addresses 0 to 15 reference the transmit message buffer which contains the identifier message to be inserted into the TR byte of the E3 G.832 transmit stream. Addresses 64 to 79 reference the receive accepted message page. A receive message is accepted into this page when it is received unchanged three or five times consecutively as determined by the PER5 bit setting. Addresses 128 to 143 reference the receive capture page while addresses 192 to 207 reference the receive expected page. The receive capture page contains the identifier bytes extracted from the receive stream. The receive expected page contains the expected trace identifier message down-loaded from the microprocessor.

Table 20 TTB RAM Contents

A[7:0]	RAM Contents
0-15	Transmit Trace Message
64-79	Receive Accepted Trace Message
128-143	Receive Captured Trace Message
192-207	Receive Expected Trace Message

Register 0x093, 0x493, 0x1293, 0x1693: TTB Indirect Data

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	D[7]	0
Bit 6	R/W	D[6]	0
Bit 5	R/W	D[5]	0
Bit 4	R/W	D[4]	0
Bit 3	R/W	D[3]	0
Bit 2	R/W	D[2]	0
Bit 1	R/W	D[1]	0
Bit 0	R/W	D[0]	0

D[7:0]

The indirect data bits (D[7:0]) contain either the data read from a message buffer after an indirect read operation has completed, or the data to be written to the RAM for an indirect write operation. Note that the write data must be set up in this register before an indirect write is initiated. Data read from this register reflects the value written until the completion of a subsequent indirect read operation. The current and accepted message pages should be read at least twice and the result of the successive reads compared for consistency. The TTB keeps overwriting these message pages and consequently the result of a read can be composed of multiple messages.

Register 0x094, 0x494, 0x1294, 0x1694: TTB Expected Payload Type Label

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	EXPLD[2]	0
Bit 1	R/W	EXPLD[1]	0
Bit 0	R/W	EXPLD[0]	0

EXPLD[2:0]

The EXPLD[2:0] bits contain the expected payload type label bits of the G.832 E3 Maintenance and Adaptation (MA) byte. The EXPLD[2:0] bits are compared with the received payload type label extracted from the receive stream. A payload type label mismatch (PLDM) is declared if the received payload type bits differs from the expected payload type. If enabled, an interrupt is asserted upon declaration and removal of PLDM.

For compatibility with old equipment that inserts 000B for unequipped or 001B for equipped, regardless of the payload type, the receive payload type label mismatch mechanism is based on the following table:

Table 21 TTB Payload Type Match Configurations

Expected	Received	Action
000	000	Match
000	001	Mismatch
000	XXX	Mismatch
001	000	Mismatch
001	001	Match
001	XXX	Match
XXX	000	Mismatch
XXX	001	Match
XXX	XXX	Match

Expected	Received	Action
XXX	YYY	Mismatch

Note: XXX, YYY = anything except 000B or 001B, and XXX is not equal to YYY.

Register 0x095, 0x495, 0x1295, 0x1695: TTB Payload Type Label Control/Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	RPLDUIE	0
Bit 6	R/W	RPLDMIE	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	PLDMODE	0
Bit 3	R	RPLDUI	X
Bit 2	R	RPLDUV	X
Bit 1	R	RPLDMI	X
Bit 0	R	RPLDMV	X

RPLDMV

The receive payload type label mismatch status bit (RPLDMV) is dependent on the PLD Mode. In Mode 1, this bit reports the match/mismatch status between the expected and the accepted payload type label. RPLDMV is set high when the accepted PLD differs from the expected PLD written by the microprocessor. RPLDMV is set low when the accepted PLD matches the expected PLD. In Mode 2, this bit reports the match/mismatch status between the expected and the received payload type label. RPLDMV is set high when the received PLD differs from the expected PLD written by the microprocessor. RPLDMV is set low when the accepted PLD matches the expected PLD.

RPLDMI

The receive payload type label mismatch interrupt status bit (RPLDMI) is set high when the match/mismatch (RPLDMV) status between the accepted and the expected payload type label changes state. The setting of this bit is dependent on the unstable status (RPLDMV) which is dependent on the PLD Mode. This bit (and the interrupt) is cleared when this register is read.

RPLDUV

The receive payload type label unstable status bit (RPLDUV) is independent on the PLD Mode. This bit reports the stable/unstable status of the payload type label in the receive stream. RPLDUV is set high when 5 labels that differ from its immediate predecessor is received. RPLDUV is set low and the unstable label count is reset when 5 consecutive identical labels are received.

RPLDUI

The receive payload type label unstable interrupt status bit (RPLDUI) is set high when the stable/unstable (RPLDUV) status of the payload type label changes state. This bit (and the interrupt) are cleared when this register is read.

PLDMODE

The PLD Mode is used to set the mode used for the payload type label alarm algorithms. Setting this bit to low sets the PLD Mode to Mode 1. Setting this bit to high sets the PLD Mode to Mode 2.

RPLDMIE

The receive payload type label mismatch interrupt enable bit (RPLDMIE) controls the activation of INTB when the comparison between accepted and the expected payload type label changes state from match to mismatch and vice versa. When RPLDMIE is set high, changes in match state (RPLDMI) activates the interrupt (INTB) output. When RPLDMIE is set low, payload type label state changes will not affect INTB.

RPLDUIE

The receive payload type label unstable interrupt enable bit (RPLDUIE) controls the activation of INTB when the received payload type label changes state from stable to unstable and vice versa. When RPLDUIE is set high, changes in stable state (RPLDUI)activates the interrupt (INTB) output. When RPLDUIE is set low, payload type label state changes will not affect INTB.

Register 0x096, 0x496, 0x1296, 0x1696: TTB Indirect Access Trigger

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	BUSY	0
Bit 6	R/W	RWB	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

RWB

The access control bit (RWB) selects between an indirect read or write access to the static page of the trace message buffer. Writing to this register initiates an external microprocessor access to the static page of the trace message buffer. When RWB is set high, a read access is initiated. The data read can be found in the TTB Indirect Data register. When RWB is set low, a write access is initiated. The data in the TTB Indirect Data register will be written to the addressed location in the static page.

BUSY

The BUSY bit reports whether a previously initiated indirect read or write to the trace message RAM has been completed. BUSY is set high upon writing to the TTB Indirect Access Trigger register, and stays high until the initiated access has completed. At this point, BUSY is set low. This register should be polled to determine when new data is available in the TTB Indirect Data register. The maximum latency for the BUSY to return low is 10 µs.

Register 0x098, 0x498, 0x1298, 0x1698: RBOC Configuration/Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	IDLE	0
Bit 1	R/W	AVC	0
Bit 0	R/W	FEACE	0

FEACE

The FEACE bit enables the generation of an interrupt when a valid far end alarm and control (FEAC) code is detected. When a logic 1 is written to FEACE, the interrupt generation is enabled.

AVC

The AVC bit position selects the validation criterion used in determining a valid FEAC code. When a logic 0 is written to AVC, a FEAC code is validated when 8 out of the last 10 received codes are identical. The FEAC code is removed when 2 out of the last 10 received code do not match the validated code. When a logic 1 is written to AVC, a FEAC code is validated when 4 out of the last 5 received codes are identical. The FEAC code is removed when a single received FEACs does not match the validated code.

IDLE

The IDLE bit enables the generation of an interrupt when a validated FEAC is removed. When a logic 1 is written to IDLE, the interrupt generation is enabled.

Register 0x099, 0x499, 0x1299, 0x1699: RBOC Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	IDLI	X
Bit 6	R	FEACI	X
Bit 5	R	FEAC[5]	X
Bit 4	R	FEAC[4]	X
Bit 3	R	FEAC[3]	X
Bit 2	R	FEAC[2]	X
Bit 1	R	FEAC[1]	X
Bit 0	R	FEAC[0]	X

FEAC[5:0]

The FEAC[5:0] bits contain the received far end alarm and control channel codes. The FEAC[5:0] bits are set to all-ones ("111111") when no code has been validated.

FEACI

The FEACI bit is set to logic 1 when a new FEAC code is validated. The FEAC code value is contained in the FEAC[5:0] bits. The FEACI bit position is set to logic 0 when this register is read.

IDLI

The IDLI bit is set to logic 1 when a validated FEAC code is removed. The FEAC[5:0] bits are set to all-ones when the code is removed. The IDLI bit position is set to logic 0 when this register is read.

Register 0x09A, 0x49A, 0x129A, 0x169A: XBOC Control Register

Bit	Type	Function	Default
15	—	Unused	X
14	—	Unused	X
13	—	Unused	X
12	—	Unused	X
11	—	Unused	X
10	—	Unused	X
9	—	Unused	X
8	—	Unused	X
7	R	FEACSMPI	X
6	R/W	FEACSMPE	0
5	R	RDY	X
4	—	Unused	X
3	R/W	RPT[3]	0
2	R/W	RPT[2]	0
1	R/W	RPT[1]	0
0	R/W	RPT[0]	0

RPT[3:0]

These bits contain the 4 bit repeat count used to determine the number (RPT[3:0] + 1) of consecutive, identical, 16-bit bit-oriented code patterns to be transmitted before sampling the XBOC Code Register again. In the event that the FEAC[5:0] value does not change, the same bit oriented code pattern will be repeated continuously. The RPT[3:0] bits can be changed at any time, and are sampled at the same time as the XBOC Code register (channel address 0x09B) (channel address 0x09B).

RDY

The RDY bit is set to logic 1 when the XBOC Code Register and RPT[3:0] are sampled by the XBOC, indicating that the XBOC Code Register is ready to be updated with a new FEAC[5:0]. Whenever FEAC[5:0] is updated, the RDY bit goes low, indicating that the new FEAC[5:0] has not yet been accepted by the XBOC state machine.

FEACSMPE

Setting FEACSMPE to logic 1 enables a hardware interrupt on the INTB output when FEACSMPI is logic 1.

FEACSMPI

The FEACSMPI bit is set to logic 1 when the XBOC Code Register, and RPT[3:0] are sampled by the XBOC, indicating that the XBOC Code Register is ready to be updated with a new FEAC[5:0]. Whenever the XBOC Control Register is read, the FEACSMPI bit is cleared.

Register 0x09B, 0x49B, 0x129B, 0x169B: XBOC Code

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	FEAC[5]	1
Bit 4	R/W	FEAC[4]	1
Bit 3	R/W	FEAC[3]	1
Bit 2	R/W	FEAC[2]	1
Bit 1	R/W	FEAC[1]	1
Bit 0	R/W	FEAC[0]	1

FEAC[5:0]

FEAC[5:0] contain the six bit code that is transmitted on the far end alarm and control channel (FEAC). The transmitted code consists of a 16 bit sequence that is repeated continuously. The sequence consists of 8 ones followed by a zero, followed by the six bit code sequence transmitted in order FEAC0, FEAC1, ..., FEAC5, followed by a zero. The all-ones sequence is inserted in the FEAC channel when FEAC[5:0] is written with all-ones.

Note: If configured for J2 transmission format (TFRM[1:0] is 10 binary) and any of LCDEN, AISEN, OOFEN, LOSEN are set to logic 1 in the Channel Data Link and FERF/RAI Control, FEAC[5:0] in this register must all be set to logic 1 for proper RAI transmission upon detection of LCD, PHYAIS, LOF, or LOS by the J2 FRMR. Otherwise, the code configured by the FEAC[5:0] bits of this register will be transmitted instead of the RAI.

Register 0x09E, 0x49E, 0x129E, 0x169E: Channel Miscellaneous Configuration #1

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	AISOOF	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	TPRBS	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	FORCELOS	0
Bit 0	R/W	LINESYSCLK	0

LINESYSCLK

LINESYSCLK is used to select the high-speed system clock which the TDPR and RDLC transmit and receive HDLC controllers use as a reference. If LINESYSCLK is set to logic 1, then the RDLC uses the receive line clock selected by FRMRSEL (Channel Data Path Configuration 0x113) and the TDPR uses the transmit line clock selected by TRANSEL and TJATTICLKSEL (Channel Data Path Configuration 0x113) as its high-speed system reference clock. If LINESYSCLK is set to logic 0, the RDLC uses the receive system interface clock (RFCLK) and the TDPR uses the transmit system interface clock (TFCLK) as its high-speed system reference clock respectively.

The read/write access rate to the RDLC and TDPR are limited by their high-speed reference clock frequency. Data and Configuration settings can be written into the TDPR at a maximum rate equal to 1/8 of its high-speed reference clock frequency. Data and status indications can be read from the TDPR at a maximum rate equal to 1/8 of its high-speed reference clock frequency. Data and status indications can be read from the RDLC at a maximum rate equal to 1/10 of its high-speed reference clock frequency.

Instantaneous variations in the high-speed reference clock frequencies (e.g. jitter in the receive line clock) must be considered when determining the procedure used to read and write the TDPR and RDLC registers.

FORCELOS

FORCELOS is used to force a Loss of Signal (LOS) condition on the transmit unipolar or bipolar data outputs TPOS/TDATO[x] and TNEG[x]. When FORCELOS is logic 1, the TPOS/TDATO[x] and TNEG[x] outputs will be forced to logic 0. When FORCELOS is logic 0, the TPOS/TDATO[x] and TNEG[x] outputs will operate normally.

TPRBS

Register bit TPRBS is used to insert a pseudo-random binary sequence into the serial transmit stream in place of other payload data on TPOS/TDATO[x] and TNEG[x]/TOHM[x]. The exact nature of the PRBS is configurable through the PRGD registers (channel addresses 0x0A0 to 0x0AF).

AISOOF

The AISOOF bit allows the receive data output stream on RDATO[x] to be forced to all 1's when the DS3, E3, or J2 FRMR loses frame. When AISOOF is set to logic 1, RDATO[x] will be forced to all 1's when frame alignment is lost. When AISOOF is set to logic 0, RDATO[x] will continue to output raw data even when frame alignment is lost.

Register 0x09F, 0x49F, 0x129F, 0x169F: Channel FRMR LOF Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	FRMLOF	X
Bit 6	R/W	FRMLOFE	0
Bit 5	R	FRMLOFI	X
Bit 4	R/W	J2SIGTHRU	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

J2SIGTHRU

The J2SIGTHRU bit allows the signaling bits (timeslots 97 and 98 in the J2 frame) on TDATI[x] to pass transparently through the J2 TRAN. When J2SIGTHRU is logic 1, timeslots 97 and 98 are passed transparently through from TDATI[x]. When J2SIGTHRU is logic 0, timeslots 97 and 98 are sourced from the J2 TRAN TS97 Signaling and J2 TRAN TS98 Signaling registers respectively.

If J2SIGTHRU is set to logic 1 and TPRBS (S/UNI 4xJET Misc. register) is also set to logic 1, the transmitted PRBS will continue through timeslots 97 and 98.

J2SIGTHRU is only valid in framer only mode (FRMRONLY=1, S/UNI 4xJET Configuration 1 register).

FRMLOFI

The FRMLOFI bit shows that a transition has occurred on the FRMLOF state. When FRMLOFI is logic 1, the FRMLOF state has changed since the last read of this register. The FRMLOFI bit is cleared whenever this register is read.

FRMLOFE

The FRMLOFE bit enables the generation of an interrupt due to a change in the FRMLOF state. When FRMLOFE is a logic 1, the interrupt is enabled.

FRMLOF

The FRMLOF bit shows the current state of the E3/T3 LOF or the J2 Extended LOF indication (depending on which mode is enabled). When FRMLOF is logic 1, the framer has lost frame synchronization for greater than 1ms, 2ms, or 3ms depending on the setting of the LOFINT[1:0] bits in the S/UNI 4xJET Receive Configuration register.

Register 0x0A0, 0x4A0, 0x12A0, 0x16A0: PRGD Control

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	PDR[1]	0
Bit 6	R/W	PDR[0]	0
Bit 5	R/W	QRSS	0
Bit 4	R/W	PS	0
Bit 3	R/W	TINV	0
Bit 2	R/W	RINV	0
Bit 1	R/W	AUTOSYNC	1
Bit 0	R/W	MANSYNC	0

MANSYNC

The MANSYNC bit is used to initiate a manual resynchronization of the pattern detector. A low to high transition on MANSYNC initiates the resynchronization.

AUTOSYNC

The AUTOSYNC bit enables the automatic resynchronization of the pattern detector. The automatic resynchronization is activated when 6 or more bit errors are detected in the last 64-bit periods. When AUTOSYNC is a logic 1, the auto resynchronization feature is enabled. When AUTOSYNC is a logic 0, the auto synchronization feature is disabled, and pattern resynchronization is accomplished using the MANSYNC bit.

RINV

The RINV bit controls the logical inversion of the receive data stream before processing. When RINV is a logic 1, the received data is inverted before being processed by the pattern detector. When RINV is a logic 0, the received data is not inverted.

TINV

The TINV bit controls the logical inversion of the generated data stream. When TINV is a logic 1, the data is inverted. When TINV is a logic 0, the data is not inverted.

PS

The PS bit selects the generated pattern. When PS is a logic 1, a repetitive pattern is generated. When PS is a logic 0, a pseudo-random pattern is generated.

The PS bit must be programmed to the desired setting before programming any other PRGD registers, or the transmitted pattern may be corrupted. Any time the setting of the PS bit is changed, the rest of the PRGD registers should be reprogrammed.

QRSS

The QRSS bit enables the zero suppression feature required when generating the QRSS sequence. When QRSS is a logic 1, a one is forced in the TDATO stream when the following 14 bit positions are all-zeros. When QRSS is a logic 0, the zero suppression feature is disabled.

PDR[1:0]

The PDR[1:0] bits select the content of the four pattern detector registers (channel addresses 0x0AC to 0x0AF) to be any one of the pattern receive registers, the error count holding registers, or the bit count holding registers. The selection is shown in the following table:

Table 22 PRGD Pattern Detector Register Configuration

PDR[1:0]	PDR#1	PDR#2	PDR#3	PDR#4
00, 01	Pattern Receive (LSB)	Pattern Receive	Pattern Receive	Pattern Receive (MSB)
10	Error Count (LSB)	Error Count	Error Count	Error Count (MSB)
11	Bit Count (LSB)	Bit Count	Bit Count	Bit Count (MSB)

Register 0x0A1, 0x4A1, 0x12A1, 0x16A1: PRGD Interrupt Enable/Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	SYNCE	0
Bit 6	R/W	BEE	0
Bit 5	R/W	XFERE	0
Bit 4	R	SYNCV	X
Bit 3	R	SYNCI	X
Bit 2	R	BEI	X
Bit 1	R	XFERI	X
Bit 0	R	OVR	X

SYNCE

The SYNCE bit enables the generation of an interrupt when the pattern detector changes synchronization state. When SYNCE is set to logic 1, the interrupt is enabled.

BEE

The BEE bit enables the generation of an interrupt when a bit error is detected in the receive data. When BEE is set to logic 1, the interrupt is enabled.

XFERE

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the receive pattern registers, the bit counter holding registers, and the error counter holding registers. When XFERE is set to logic 1, the interrupt is enabled.

SYNCV

The SYNCV bit indicates the synchronization state of the pattern detector. When SYNCV is a logic 1 the pattern detector is synchronized (the pattern detector has observed at least 32 consecutive error free bit periods). When SYNCV is a logic 0, the pattern detector is out of sync (the pattern detector has detected 6 or more bit errors in a 64 bit period window).

SYNCI

The SYNCI bit indicates that the detector has changed synchronization state since the last time this register was read. If SYNCI is logic 1, then the pattern detector has gained or lost synchronization at least once. SYNCI is set to logic 0 when this register is read.

BEI

The BEI bit indicates that one or more bit errors have been detected since the last time this register was read. When BEI is set to logic 1, at least one bit error has been detected. BEI is set to logic 0 when this register is read.

XFERI

The XFERI bit indicates that a transfer of pattern detector data has occurred. A logic 1 in this bit position indicates that the pattern receive registers, the bit counter holding registers and the error counter holding registers have been updated. This update is initiated by writing to one of the pattern detector register locations, or by writing to the S/UNI 4xJET Identification, Master Reset, and Global Monitor Update register (006). XFERI is set to logic 0 when this register is read.

OVR

The OVR bit is the overrun status of the pattern detector registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFERI being logic 1) has not been acknowledged before the next accumulation interval has occurred and that the contents of the pattern receive registers, the bit counter holding registers and the error counter holding registers have been overwritten. OVR is set to logic 0 when this register is read.

Register 0x0A2, 0x4A2, 0x12A2, 0x16A2: PRGD Length

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	PL[4]	0
Bit 3	R/W	PL[3]	0
Bit 2	R/W	PL[2]	0
Bit 1	R/W	PL[1]	0
Bit 0	R/W	PL[0]	0

PL[4:0]

PL[4:0] determine the length of the generated pseudo random or repetitive pattern. The pattern length is equal to the value of PL[4:0] + 1.

Register 0x0A3, 0x4A3, 0x12A3, 0x16A3: PRGD Tap

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	PT[4]	0
Bit 3	R/W	PT[3]	0
Bit 2	R/W	PT[2]	0
Bit 1	R/W	PT[1]	0
Bit 0	R/W	PT[0]	0

PT[4:0]

PT[4:0] determine the feedback tap position of the generated pseudo random pattern. The feedback tap position is equal to the value of PT[4:0] + 1.

Register 0x0A4, 0x4A4, 0x12A4, 0x16A4: PRGD Error Insertion Register

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	EVENT	0
Bit 2	R/W	EIR[2]	0
Bit 1	R/W	EIR[1]	0
Bit 0	R/W	EIR[0]	0

EIR[2:0]

The EIR[2:0] bits control the insertion of a programmable bit error rate as indicated in the following table:

Table 23 PRGD Generated Bit Error Rate Configurations

EIR[2:0]	Generated Bit Error Rate
000	No errors inserted
001	10^{-1}
010	10^{-2}
011	10^{-3}
100	10^{-4}
101	10^{-5}
110	10^{-6}
111	10^{-7}

EVENT

A low to high transition on the EVENT bit causes a single bit error to be inserted in the generated pattern. This bit must be cleared and set again for a subsequent error to be inserted.

Register 0x0A8, 0x4A8, 0x12A8, 0x16A8: PRGD Pattern Insertion #1

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	PI[7]	0
Bit 6	R/W	PI[6]	0
Bit 5	R/W	PI[5]	0
Bit 4	R/W	PI[4]	0
Bit 3	R/W	PI[3]	0
Bit 2	R/W	PI[2]	0
Bit 1	R/W	PI[1]	0
Bit 0	R/W	PI[0]	0

Register 0x0A9, 0x4A9, 0x12A9, 0x16A9: PRGD Pattern Insertion #2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	PI[15]	0
Bit 6	R/W	PI[14]	0
Bit 5	R/W	PI[13]	0
Bit 4	R/W	PI[12]	0
Bit 3	R/W	PI[11]	0
Bit 2	R/W	PI[10]	0
Bit 1	R/W	PI[9]	0
Bit 0	R/W	PI[8]	0

Register 0x0AA, 0x4AA, 0x12AA, 0x16AA: PRGD Pattern Insertion #3

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	PI[23]	0
Bit 6	R/W	PI[22]	0
Bit 5	R/W	PI[21]	0
Bit 4	R/W	PI[20]	0
Bit 3	R/W	PI[19]	0
Bit 2	R/W	PI[18]	0
Bit 1	R/W	PI[17]	0
Bit 0	R/W	PI[16]	0

Register 0x0AB, 0x4AB, 0x12AB, 0x16AB: PRGD Pattern Insertion #4

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	PI[31]	0
Bit 6	R/W	PI[30]	0
Bit 5	R/W	PI[29]	0
Bit 4	R/W	PI[28]	0
Bit 3	R/W	PI[27]	0
Bit 2	R/W	PI[26]	0
Bit 1	R/W	PI[25]	0
Bit 0	R/W	PI[24]	0

PI[31:0]

PI[31:0] contain the data that is loaded in the pattern generator each time a new pattern (pseudo random or repetitive) is to be generated. When a pseudo random pattern is to be generated, PI[31:0] should be set to 0xFFFFFFFF. The data is loaded each time pattern insertion register #4 is written. Pattern insertion registers #1 - #3 should be loaded with the desired data before pattern register #4 is written.

Register 0x0AC, 0x4AC, 0x12AC, 0x16AC: PRGD Pattern Detector #1

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	PD[7]	0
Bit 6	R	PD[6]	0
Bit 5	R	PD[5]	0
Bit 4	R	PD[4]	0
Bit 3	R	PD[3]	0
Bit 2	R	PD[2]	0
Bit 1	R	PD[1]	0
Bit 0	R	PD[0]	0

Register 0x0AD, 0x4AD, 0x12AD, 0x16AD: PRGD Pattern Detector #2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	PD[15]	0
Bit 6	R	PD[14]	0
Bit 5	R	PD[13]	0
Bit 4	R	PD[12]	0
Bit 3	R	PD[11]	0
Bit 2	R	PD[10]	0
Bit 1	R	PD[9]	0
Bit 0	R	PD[8]	0

Register 0x0AE, 0x4AE, 0x12AE, 0x16AE: PRGD Pattern Detector #3

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	PD[23]	0
Bit 6	R	PD[22]	0
Bit 5	R	PD[21]	0
Bit 4	R	PD[20]	0
Bit 3	R	PD[19]	0
Bit 2	R	PD[18]	0
Bit 1	R	PD[17]	0
Bit 0	R	PD[16]	0

Register 0x0AF, 0x4AF, 0x12AF, 0x16AF: PRGD Pattern Detector #4

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	PD[31]	0
Bit 6	R	PD[30]	0
Bit 5	R	PD[29]	0
Bit 4	R	PD[28]	0
Bit 3	R	PD[27]	0
Bit 2	R	PD[26]	0
Bit 1	R	PD[25]	0
Bit 0	R	PD[24]	0

PD[31:0]

PD[31:0] contain the pattern detector data. The values contained in these registers are determined by the PDR[1:0] bits in the control register.

When PDR[1:0] is set to 00 or 01, PD[31:0] contain the pattern receive register. The 32 bits received immediately before the last accumulation interval are present on PD[31:0}. PD[31] contains the first of the 32 received bits, PD[0] contains the last of the 32 received bits.

When PDR[1:0] is set to 10, PD[31:0] contain the error counter holding register. The value in this register represents the number of bit errors that have been accumulated since the last accumulation interval. Note that bit errors are not accumulated while the pattern detector is out of sync.

When PDR[1:0] is set to 11, PD[31:0] contain the bit counter holding register. The value in this register represents the total number of bits that have been received since the last accumulation interval.

The value of PD[31:0] is polled by writing to any of the PRGD pattern detector registers (channel addresses 0x0AC to 0x0AF) or to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800).

Register 0x100, 0x500, 0x1300, 0x1700: Channel Transmit Configuration #2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	TXAU3STS1EN	1
Bit 12	—	Unused	X
Bit 11	R/W	TPAISTU3EN	0
Bit 10	R/W	FSONESEN	0
Bit 9	R/W	OHONESEN	0
Bit 8	R/W	TPAISEN	0
Bit 7	R/W	SS_H1[1]	1
Bit 6	R/W	SS_H1[0]	0
Bit 5	R/W	SS_CONCAT[1]	0
Bit 4	R/W	SS_CONCAT[0]	0
Bit 3	R/W	TU3LOCK0595B	0
Bit 2	R/W	AU3LOCK0522B	0
Bit 1	R/W	TXAU3TU3B	1
Bit 0	R/W	TXDIRMAPEN	0

TXDIRMAPEN

The Transmit Direct Map Enable bit controls the mapping of the payload data into the provisioned timeslot in the TX_STI. When logic 0, the payload mapping is asynchronous DS3/E3 sourced via the D3E3MA. When logic 1, the payload mapping is direct mapped ATM or PPP over SONET sourced via the TXCP/TXFP.

TXAU3TU3B

The Transmit AU3TU3B bit configures the channel for either AU3 or TU3 transmission. When logic 0, the channel is configured to process one third of a VC-4 payload mapped via a TU3. When logic 1, the channel is configured to process AU3 mapped SONET/SDH frames.

AU3LOCK0522B

This bit controls the generation of the J1 Path Overhead Byte location for the transmit direction, and thus, the AU3 H1 H2 pointer value for the transmit direction. When set to logic 0, the H1 H2 pointer value is set at 522. This is the normal pointer location for ATM configuration (as specified by the ATM Forum). When set to logic 1, the H1 H2 pointer value is set at 0.

TU3LOCK0595B

This bit controls the generation of the J1 TU3 Tributary Path Overhead Byte location for the transmit direction, and thus, the TU3 H1 H2 pointer value for the transmit direction. When set to logic 0, the H1 H2 pointer value is set at 595. When set to logic 1, the H1 H2 pointer value is set at 0.

SS_CONCAT[1:0]

These register bits control the value inserted into the SS field of the concatenated H1 AU pointer byte for a concatenated provisioned timeslot.

SS_H1[1:0]

These register bits control the value inserted into the SS field of the non-concatenated H1 AU pointer byte for a non-concatenated provisioned timeslot.

TPAISEN

The Transmit Path AIS Enable bit enables the insertion of path AIS on the transmit Telecom interface for a provisioned timeslot. When logic 0, the TX_STI does not generate path AIS in the provisioned timeslot. When logic 1, the TX_STI generates path AIS in the provisioned timeslot to the Transmit Telecom.

OHONESEN

The Overhead Ones Enable bit controls the insertion of the section/line/path/tributary path overhead for a provisioned timeslot. When logic 0, the TX_STI will insert 00h for all overhead bytes. When logic 1, the TX_STI will insert FFh for all overhead bytes.

FSONESEN

The Fixed Stuff Ones Enable bit controls the insertion of the fixed stuff bytes for a provisioned timeslot. When logic 0, the TX_STI will insert 00h for all fixed stuff bytes. When logic 1, the TX_STI will insert FFh for all fixed stuff bytes.

TPAISTU3EN

The Transmit TU3 Tributary Path AIS Enable bit enables the insertion of TU3 tributary path AIS on the transmit Telecom interface for a provisioned timeslot. When logic 0, the TX_STI does not generate TU3 tributary path AIS in the provisioned timeslot. When logic 1, the TX_STI generates TU3 tributary path AIS in the provisioned timeslot to the Transmit Telecom.

TXAU3STS1EN

The Transmit AU3 STS-1 Enable bit controls the generation of the fixed stuff byte locations for the transmit direction. When set to logic 0, the fixed stuff byte insertion occurs in column 1 of the synchronous payload envelope for fixed stuff enabled timeslots as indicated by TXSTSFSEN[11:0]. When set to logic 1, the fixed stuff byte insertion occurs in column 30 and 59 of the synchronous payload envelope.

Register 0x101, 0x501, 0x1301, 0x1701: Channel Receive Configuration #2

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	RXAU3STS1EN	1
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	LCDDIS	0
Bit 1	R/W	RXAU3TU3B	1
Bit 0	R/W	RXDIRMAPEN	0

RXDIRMAPEN

The Receive Direct Map Enable bit controls the extraction of the payload data from the SONET/SDH stream. When logic 0, the D3E3MD block processes the extracted SONET/SDH stream, providing DS3 or E3 de-mapped channels. When logic 1, the cell and frame processors are used to extract the SONET/SDH stream directly, and no DS3 or E3 processing through the Framer/Transmitter and demapper is performed.

RXAU3TU3B

The Receive AU3TU3B bit configures the channel for either SONET/AU3 or TU3 reception. When logic 0, the channel is configured to process a portion of an SDH TU3 frame. When logic 1, the channel is configured to process SONET or SDH AU3 frames.

LCDDIS

This bit controls the (loss of cell delineation) LCD alarm signal to the SONET/SDH SARC block. When LCDDIS is a logic 0, the LCD alarm is not squelched. When LCDDIS is a logic 1, the LCD alarm is squelched.

RXAU3STS1EN

The Receive AU3 STS-1 Enable bit controls the detection of fixed stuff bytes in the receive direction. When set to logic 0, the fixed stuff bytes are located in column 1 of the synchronous payload envelope for fixed stuff enabled timeslots as indicated by RXSTSFSEN[11:0]. When set to logic 1, the fixed stuff bytes are located in column 30 and 59 of the synchronous payload envelope.

Register 0x102, 0x502, 0x1302, 0x1702: Channel Transmit Timeslot Configuration #1

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	TXSTSEN[11]	0
Bit 10	R/W	TXSTSEN[10]	0
Bit 9	R/W	TXSTSEN[9]	0
Bit 8	R/W	TXSTSEN[8]	0
Bit 7	R/W	TXSTSEN[7]	0
Bit 6	R/W	TXSTSEN[6]	0
Bit 5	R/W	TXSTSEN[5]	0
Bit 4	R/W	TXSTSEN[4]	0
Bit 3	R/W	TXSTSEN[3]	0
Bit 2	R/W	TXSTSEN[2]	0
Bit 1	R/W	TXSTSEN[1]	0
Bit 0	R/W	TXSTSEN[0]	0

TXSTSEN[11:0]

The TXSTSEN bit provides arbitrary STS-1/STM-0 granularity provisioning for a given channel. When TXSTSEN[x] is logic 1, the corresponding timeslot is provisioned to be overwritten by the TX_STI. When TXSTSEN[x] is logic 0, the corresponding timeslot is passed through the TX_STI unmodified.

The setting of these bits has been further illustrated in PMC-2021632 “SUNI 4xJET ASSP Telecom Standard Product Data Sheet” Operations Section.

Register 0x103, 0x503, 0x1303, 0x1703: Channel Transmit Timeslot Configuration #2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	TXSTSCEN[11]	0
Bit 10	R/W	TXSTSCEN[10]	0
Bit 9	R/W	TXSTSCEN[9]	0
Bit 8	R/W	TXSTSCEN[8]	0
Bit 7	R/W	TXSTSCEN[7]	0
Bit 6	R/W	TXSTSCEN[6]	0
Bit 5	R/W	TXSTSCEN[5]	0
Bit 4	R/W	TXSTSCEN[4]	0
Bit 3	R/W	TXSTSCEN[3]	0
Bit 2	R/W	TXSTSCEN[2]	0
Bit 1	R/W	TXSTSCEN[1]	0
Bit 0	R/W	TXSTSCEN[0]	0

TXSTSCEN[11:0]

The TXSTSCEN bit provides arbitrary STS-1/STM-0 granularity concatenation provisioning for a given channel. When TXSTSCEN[x] is logic 1, the corresponding timeslot is marked as concatenated and the TX_STI inserts H1, H2 AU3 pointers as concatenation indicators. When TXSTSCEN[x] is logic 0, the corresponding timeslot is not marked as concatenated and the TX_STI inserts H1, H2 AU3 pointers based on AU3LOCK0522B configuration bit.

The setting of these bits has been further illustrated in PMC-2021632 “SUNI 4xJET ASSP Telecom Standard Data Sheet” Operations Section.

Register 0x104, 0x504, 0x1304, 0x1704: Channel Transmit Timeslot Configuration #3

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	TXSTSFSEN[11]	0
Bit 10	R/W	TXSTSFSEN[10]	0
Bit 9	R/W	TXSTSFSEN[9]	0
Bit 8	R/W	TXSTSFSEN[8]	0
Bit 7	R/W	TXSTSFSEN[7]	0
Bit 6	R/W	TXSTSFSEN[6]	0
Bit 5	R/W	TXSTSFSEN[5]	0
Bit 4	R/W	TXSTSFSEN[4]	0
Bit 3	R/W	TXSTSFSEN[3]	0
Bit 2	R/W	TXSTSFSEN[2]	0
Bit 1	R/W	TXSTSFSEN[1]	0
Bit 0	R/W	TXSTSFSEN[0]	0

TXSTSFSEN[11:0]

The TXSTSFSEN bit provides arbitrary STS-1/STM-0 granularity fixed stuff provisioning for a given channel. This configuration register only has effect on the column immediately following the SONET/SDH transport overhead. When TXSTSFSEN[x] is logic 1, the corresponding timeslot is marked as fixed stuff and the value inserted by the TX_STI is determined based on FSONESEN configuration. When TXSTSFSEN[x] is logic 0, the corresponding timeslot is not marked as fixed stuff and the TX_STI inserts payload or overhead data based on TXSTSEN[x], STSCEN[x], and OHONESEN configuration.

The setting of these bits has been further illustrated in PMC-2021632 “SUNI 4xJET ASSP Telecom Standard Product Data Sheet” Operations Section.

Register 0x105, 0x505, 0x1305, 0x1705: Channel Receive Timeslot Configuration #1

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	RXSTSEN[11]	0
Bit 10	R/W	RXSTSEN[10]	0
Bit 9	R/W	RXSTSEN[9]	0
Bit 8	R/W	RXSTSEN[8]	0
Bit 7	R/W	RXSTSEN[7]	0
Bit 6	R/W	RXSTSEN[6]	0
Bit 5	R/W	RXSTSEN[5]	0
Bit 4	R/W	RXSTSEN[4]	0
Bit 3	R/W	RXSTSEN[3]	0
Bit 2	R/W	RXSTSEN[2]	0
Bit 1	R/W	RXSTSEN[1]	0
Bit 0	R/W	RXSTSEN[0]	0

RXSTSEN[11:0]

The RXSTSEN bit provides arbitrary STS-1/STM-0 granularity provisioning for a given channel. When RXSTSEN[x] is logic 1, the corresponding timeslot is provisioned to be extracted by the RX_STI. When RXSTSEN[x] is logic 0, the corresponding timeslot is passed through the RX_STI unmodified.

The setting of these bits has been further illustrated in PMC-2021632 “SUNI 4xJET ASSP Telecom Standard Product Data Sheet” Operations Section.

Register 0x106, 0x506, 0x1306, 0x1706: Channel Transmit Address Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	TXATMBPOS	0
Bit 5	R/W	TXSQUELCHEN	0
Bit 4	R/W	DTADRMASK[4]	0
Bit 3	R/W	DTADRMASK[3]	0
Bit 2	R/W	DTADRMASK[2]	0
Bit 1	R/W	DTADRMASK[1]	0
Bit 0	R/W	DTADRMASK[0]	0

DTADRMASK[4:0]

The Device Transmit Address Mask (DTADRMASK[4:0]) bits provide full channel programmability in Level 2 mode of operation and constrained channel programmability in Level 3 mode of operation. In Level 2 Operation, when a bit is logic 1, the corresponding TADR[4:0] bit is inverted. When a bit is logic 0, the corresponding TADR[4:0] bit remains unmodified. In Level 2 Operation on channels 1 and 3, all bits except DTADRMASK[3] operates as discussed above, when DTADRMASK[3] for channels 1 and 3 is logic 1, the corresponding TADR[3] bit remains unmodified, and when TDADRMASK[3] for channels 1 and 3 is logic 0, the corresponding TADR[3] bit is inverted. For Level 3 Operation, Table 24 shows the constrained channel programmability values.

Table 24 Channel Constrained Level 3 Channel Programmability

TADR/RADR (Decimal)	TADR/RADR (Binary)	Available Masks (Binary)	Resulting Channel Address (Binary)	Resulting Channel Address (Decimal)
0	00000	00000 00100 01000	00000 00100 01000	0 4 8
1	00001	01000 01100 00000	00001 00101 01001	1 5 9

TADR/RADR (Decimal)	TADR/RADR (Binary)	Available Masks (Binary)	Resulting Channel Address (Binary)	Resulting Channel Address (Decimal)
2	00010	00000 00100 01000	00010 00110 01010	2 6 10
3	00011	01000 01100 00000	00011 00111 01011	3 7 11

TXSQUELCHEN

The transmit squelch enable bit is used to squelch the channel TCA_PTPA, and STPA outputs in Level 2 UTOPIA or Level 2 POSPHY operation.

When TXSQUELCHEN is logic 1, TCA_PTPA, and STPA are held low irrespective of the transmit port address (TADR[4:0]). When TXSQUELCHEN is logic 0, TCA_PTPA are driven by the channel in response to a valid address cycle on TADR[4:0].

This bit in conjunction with DTADRMASK[4:0] can be used to broadcast a transmit port address (TADR[4:0]) to multiple channels. This is achieved by masking one or more channel addresses using DTADRMASK[4:0] to respond to a single TADR[4:0] and squelching all but one of the duplicated channels TCA_PTPA, and STPA outputs using TXSQUELCHEN.

When the system side interface is configured for Level 3 operation, TXSQUELCHEN must be set to logic 0 for proper operation.

TXATMBPOS

The transmit ATM/POS mode bit is used to configure the channel for ATM or packet operation when in POS-PHY L2 or UTOPIA L2 operation. When TXATMBPOS is logic 0, the channel is configured for ATM transmission. When TXATMBPOS is logic 1, the channel is configured for packet transmission.

When the system side interface is configured for Level 3 processing this bit has no effect.

Register 0x107, 0x507, 0x1307, 0x1707: Channel Receive Address Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	RXATMBPOS	0
Bit 5	R/W	RXSQLCHEN	0
Bit 4	R/W	DRADRMASK[4]	0
Bit 3	R/W	DRADRMASK[3]	0
Bit 2	R/W	DRADRMASK[2]	0
Bit 1	R/W	DRADRMASK[1]	0
Bit 0	R/W	DRADRMASK[0]	0

DRADRMASK[4:0]

The Device Receive Address Mask bits provide full channel programmability in Level 2 operation and constrained channel programmability in Level 3 operation. In Level 2 Operation, when a bit is logic 1, the corresponding L2 RADR[4:0] bit is inverted. When a bit is logic 0, the corresponding L2 RADR[4:0] bit remains unmodified. In Level 2 Operation on channels 1 and 3, all bits except DTADRMASK[3] operates as discussed above, when DTADRMASK[3] for channels 1 and 3 is logic 1, the corresponding TADR[3] bit remains unmodified, and when TDADRMASK[3] for channels 1 and 3 is logic 0, the corresponding TADR[3] bit is inverted. For Level 3 Operation, Table 24 shows the constrained channel programmability values.

RXSQLCHEN

The receive squelch enable bit is used to squelch the channel RCA_RVAL, RPA, RSOC_RSOP, REOP, RERR, RMOD[1:0], RPRTY, and RDAT[31:0] outputs in Level 2 UTOPIA or Level 2 POSPHY operation.

When RXSQUELCHEN is logic 1, the RCA_RVAL, RPA, RSOC_RSOP, REOP, RERR, RMOD[1:0], RPRTY, and RDAT[31:0] outputs are held low irrespective of the receive port address (RADR[4:0]). When RXSQUELCHEN is logic 0, RCA_RVAL, RPA, RSOC_RSOP, REOP, RERR, RMOD[1:0], RPRTY, and RDAT[31:0] outputs are driven by the channel in response to a valid address cycle on RADR[4:0].

When the system side interface is configured for Level 3 operation, RXSQUELCHEN must be set to logic 0 for proper operation.

RXATMBPOS

The receive ATM/POS mode bit is used to configure the channel for ATM or packet operation when in POS-PHY L2 or UTOPIA L2 operation. When RXATMBPOS is logic 0, the channel is configured for ATM reception. When TXATMBPOS is logic 1, the channel is configured for packet or HDLC reception.

When the system side interface is configured for Level 3 processing this bit has no effect.

Register 0x108, 0x508, 0x1308, 0x1708: Channel Transmit Bit HDLC Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	FRST	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	IDLE	0
Bit 6	R/W	FLAG[2]	0
Bit 5	R/W	FLAG[1]	0
Bit 4	R/W	FLAG[0]	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	TXINVERT	0
Bit 0	R/W	TXDELIN	1

TXDELIN

The transmit delineate enable bit (TXDELIN) configures the bit HDLC processor to perform flag sequence insertion and bit stuffing on the outgoing data stream. When TXDELIN is set high, flag sequence insertion, and bit stuffing is performed on the outgoing bit HDLC data stream. When TXDELIN is set low, the bit HDLC processor does not perform any processing (flag sequence insertion, nor bit stuffing) on the outgoing stream.

TXINVERT

The transmit data inversion bit (TXINVERT) configures the bit HDLC processor to logically invert the outgoing HDLC stream. When TXINVERT is set to one, the outgoing HDLC stream is logically inverted. The outgoing HDLC stream is not inverted when INVERT is set to zero.

FLAG[2:0]

The FLAG bits control the operation of the bit HDLC processor. This configures the minimum number of flags or bytes of idle bits inserted between HDLC packets. The minimum number of flags or bytes of idle (8 bits of 1's) inserted between HDLC packets is shown in Table 25.

Table 25 Channel Bit HDLC Flag Settings

FLAG[2:0]	Minimum Number of Flag/Idle Bytes
000	1 flag / 0 Idle byte
001	2 flags / 0 idle byte
010	5 flags / 3 idle bytes
011	9 flags / 7 idle bytes
100	17 flags / 15 idle bytes
101	33 flags / 31 idle bytes
110	65 flags / 63 idle bytes
111	129 flags / 127 idle bytes

IDLE

The inter-frame time fill bit (IDLE) configures the bit HDLC processor to use flag bytes or HDLC idle as the inter-frame time fill between HDLC packets. When IDLE is set low, the bit HDLC processor uses flag bytes as the inter-frame time fill. When IDLE is set high, the bit HDLC processor uses HDLC idle (all-one's bit with no bit-stuffing pattern is transmitted) as the inter-frame time fill.

FRST

The FIFO reset bit (FRST) configures the bit HDLC processor to reset the internal FIFO. When FRST is set to one, the FIFO is forced into a reset state. When FRST is set to zero, the FIFO is in normal operation.

See the Operations Section in PMC-2021632 on resetting the receive and transmit FIFOs.

Register 0x109, 0x509, 0x1309, 0x1709: Channel Receive Bit HDLC Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	OCTETEE	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	RXINVERT	0
Bit 0	R/W	RXDELIN	1

RXDELIN

The receive delineate enable bit (RXDELIN) configures the bit HDLC processor to perform flag sequence extraction and bit destuffing on the incoming data stream. When RXDELIN is set high, flag sequence extraction, and bit destuffing is performed on the incoming HDLC data stream. When RXDELIN is set low, the bit HDLC processor does not perform any processing (flag sequence extraction, nor bit destuffing) on the incoming data stream.

RXINVERT

The receive data inversion bit (RXINVERT) configures the bit HDLC processor to logically invert the incoming HDLC stream prior to processing. When RXINVERT is set to one, the incoming HDLC stream is logically inverted. The incoming HDLC stream is not inverted when INVERT is set to zero.

OCTETEE

OCTETEE controls the assertion of the channel interrupt when octet misalignment events occur. When OCTETEE is set high, the INTB output is deasserted when OCTETEI is one. When OCTETEE is set low, the OCTETEI bit has no effect on INTB.

Register 0x10A, 0x50A, 0x130A, 0x170A: Channel Interrupt Status #2

Bit	Type	Function	Default
Bit 15	R	AUXFRMRLOFI	X
Bit 14	R	TJATI	X
Bit 13	R	RJATI	X
Bit 12	R	OCTETEI	X
Bit 11	R	RBOCAUXI	X
Bit 10	R	TTBAUXI	X
Bit 9	R	RDLCAUXI	X
Bit 8	R	FRMRAUXI	X
Bit 7	R	PMONAUXI	X
Bit 6	R	TXFPI	X
Bit 5	R	RXFPI	X
Bit 4	R	TDPRMAPI	X
Bit 3	R	RDLCDEMAPI	X
Bit 2	R	D3E3MAI	X
Bit 1	R	D3E3MDI	X
Bit 0	R	XBOCI	X

When the interrupt output INTB goes low, this register allows the source of the active interrupt to be identified down to the block level for the channel. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

XBOCI

The XBOCI bit is high when an interrupt request is active from the XBOC block. The XBOC interrupt sources are enabled in the XBOC Configuration Register (channel address 0x09A).

D3E3MDI

The D3E3MDI bit is high when an interrupt request is active from the D3E3MD block. The D3E3MD interrupt sources are enabled in the D3E3MD Interrupt Enable Register (channel address 0x122).

D3E3MAI

The D3E3MAI bit is high when an interrupt request is active from the D3E3MA block. The D3E3MA interrupt sources are enabled in the D3E3MA Interrupt Enable Register (channel address 0x12A).

RDLCDEMAPI

The RDLCDEMAPI bit is high when an interrupt request is active from the RDLC Demapper block. The RDLC Demapper interrupt sources are enabled in the RDLC Demapper Interrupt Control Register (channel address 0x131).

TDPRMAPI

The TDPRMAPI bit is high when an interrupt request is active from the TDPR Mapper block. The TDPR Mapper interrupt sources are enabled in the TDPR Mapper Interrupt Enable Register (channel address 0x13B).

RXFPI

The RXFPI bit is high when an interrupt request is active from the RXFP block. The RXFP interrupt sources are enabled in the RXFP Configuration/Interrupt Enable Register (channel address 0x141).

TXFPI

The TXFPI bit is high when an interrupt request is active from the TXFP block. The TXFP interrupt sources are enabled in the TXFP Interrupt Enable/Status Register (channel address 0x160).

PMONAUXI

The PMONAUXI bit is high when an interrupt request is active from the auxiliary PMON block. The auxiliary PMON interrupt sources are enabled in the PMON AUX Interrupt Enable/Status Register (channel address 0x171).

FRMRAUXI

The FRMRAUXI bit is high when an interrupt request is active from the auxiliary FRMR block which includes DS3 FRMR AUX, E3 FRMR AUX, and J2 FRMR AUX framers. The auxiliary FRMR interrupt sources are enabled in the DS3 FRMR AUX Interrupt Enable Register (channel address 0x181) , E3 FRMR AUX Framing Interrupt Enable and Maintenance Event Interrupt Enable Registers (channel address 0x18A and 0x18C respectively), and J2 FRMR AUX Alarm Interrupt Enable and Error/X-bit Interrupt Enable Registers (channel address 0x192 and 0x194 respectively).

RDLCAUXI

The RDLCAUXI bit is high when an interrupt request is active from the auxiliary RDLC block. The auxiliary RDLC interrupt sources are enabled in the RDLC AUX Interrupt Control Register (channel address 0x131).

TTBAUXI

The TTBAUXI bit is high when an interrupt request is active from the auxiliary TTB block. The auxiliary TTB interrupt sources are enabled in the TTB AUX Control Register (channel address 0x1A0).

RBOCAUXI

The RBOCAUXI bit is high when an interrupt request is active from the auxiliary RBOC block. The auxiliary RBOC interrupt sources are enabled in the RBOC AUX Configuration/Interrupt Enable Register (channel address 0x1A8).

OCTETEI

The octet error interrupt (OCTETEI) bit is high when an interrupt request is active from the bit HDLC processor. The OCTETE interrupt source is enabled in the Channel Receive Bit HDLC Configuration Register (channel address 0x109).

RJATI

The RJATI bit is high when an interrupt request is active from the RJAT block. The RJAT interrupt sources are enabled in the RJAT Interrupt Status Register (channel address 0x1B1).

TJATI

The TJATI bit is high when an interrupt request is active from the TJAT block. The TJAT interrupt sources are enabled in the TJAT Interrupt Status Register (channel address 0x1B9).

AUXFRMRLOFI

The Auxiliary Framer Loss of Frame Interrupt bit is high when an interrupt request is active from the FRMR AUX block. The AUXFRMRLOF interrupt source is enabled in the Channel Auxiliary Framer LOF Status Register (channel address 0x116).

Register 0x10B, 0x50B, 0x130B, 0x170B: Channel Clock Activity Monitor #2

Bit	Type	Function	Default
Bit 15	R	Unused	X
Bit 14	R	Unused	X
Bit 13	R	Unused	X
Bit 12	R	Unused	X
Bit 11	R	Unused	X
Bit 10	R	Unused	X
Bit 9	R	Unused	X
Bit 8	R	Unused	X
Bit 7	R	Unused	X
Bit 6	R	Unused	X
Bit 5	R	Unused	X
Bit 4	R	Unused	X
Bit 3	R	Unused	X
Bit 2	R	EFBWCLKA	X
Bit 1	R	DCLKA	X
Bit 0	R	GCKA	X

GCKA

The GCKA bit monitors for low to high transitions on the internal STS-1/STM-0 rate clock GCK. GCKA is set high on a rising edge of GCK, and is set low when this register is written.

DCLKA

The DCLKA bit monitors for low to high transitions on the internal STS-1/STM-0 rate clock DCLK. DCLKA is set high on a rising edge of DCLK, and is set low when this register is written.

EFBWCLKA

The EFBWCLKA bit monitors for low to high transitions on EFBWCLK[x].

Register 0x10C, 0x50C, 0x130C, 0x170C: Channel Loopback Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R/W	TXXPDLE	0

TXXPDLE

The Transmit Cell/Frame Processor Diagnostic Loopback, TXXPDLE bit enables the channel's diagnostic loopback where the channel's Transmit ATM and POS Processors (TXCP and TXFP respectively) are directly connected to the Receive ATM and POS Processor (RXCP and RXFP respectively).

When TXXPDLE is logic one, loopback is enabled with a data rate OCLK/12 (6.48Mbyte/s). Under this operating condition, the channel does not operate normally in the transmit direction or receive direction.

When TXXPDLE is logic zero, the channel operates normally.

When setting TXXPDLE to logic one, TXDIRMAPEN and RXDIRMAPEN must be set to logic 1 for proper operation.

Register 0x10D, 0x50D, 0x130D, 0x170D: Channel Receive Timeslot Configuration #2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	RXSTSMEN[11]	0
Bit 10	R/W	RXSTSMEN[10]	0
Bit 9	R/W	RXSTSMEN[9]	0
Bit 8	R/W	RXSTSMEN[8]	0
Bit 7	R/W	RXSTSMEN[7]	0
Bit 6	R/W	RXSTSMEN[6]	0
Bit 5	R/W	RXSTSMEN[5]	0
Bit 4	R/W	RXSTSMEN[4]	0
Bit 3	R/W	RXSTSMEN[3]	0
Bit 2	R/W	RXSTSMEN[2]	0
Bit 1	R/W	RXSTSMEN[1]	0
Bit 0	R/W	RXSTSMEN[0]	0

RXSTSMEN[11:0]

The RXSTSMEN bit provides arbitrary STS-1/STM-0 granularity master timeslot provisioning for a given channel. The master timeslot is used by all slave timeslots in the RX_STI to indicate the POH position in addition to path alarm information. When RXSTSMEN[x] is logic 1, the corresponding timeslot is marked as a master timeslot. When RXSTSMEN[x] is logic 0, the timeslot is marked as a slave timeslot.

The setting of these bits has been further illustrated in PMC-2021632 “SUNI 4xJET ASSP Telecom Standard Product Data Sheet” Operations Section.

Register 0x10E, 0x50E, 0x130E, 0x170E: Channel Receive Timeslot Configuration #3

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	RXSTSFSEN[11]	0
Bit 10	R/W	RXSTSFSEN[10]	0
Bit 9	R/W	RXSTSFSEN[9]	0
Bit 8	R/W	RXSTSFSEN[8]	0
Bit 7	R/W	RXSTSFSEN[7]	0
Bit 6	R/W	RXSTSFSEN[6]	0
Bit 5	R/W	RXSTSFSEN[5]	0
Bit 4	R/W	RXSTSFSEN[4]	0
Bit 3	R/W	RXSTSFSEN[3]	0
Bit 2	R/W	RXSTSFSEN[2]	0
Bit 1	R/W	RXSTSFSEN[1]	0
Bit 0	R/W	RXSTSFSEN[0]	0

RXSTSFSEN[11:0]

The RXSTSFSEN bit controls the detection of fixed stuff bytes in the RX_STI in conjunction with RXAU3STS1EN. This configuration register only has effect on column 1 of the SPE when RXAU3STS1EN is logic 0. When RXSTSFSEN[x] is logic 1, the corresponding timeslot [x] is marked as fixed stuff. When RXSTSFSEN[x] is logic 0 the corresponding timeslot is not marked as fixed stuff and contains payload data.

The setting of these bits has been further illustrated in PMC-2021632 “SUNI 4xJET ASSP Telecom Standard Product Data Sheet” Operations Section.

Register 0x110, 0x510, 0x1310, 0x1710: Receive Performance Count LSB

Bit	Type	Function	Default
Bit 15	R	RCNT[15]	0
Bit 14	R	RCNT[14]	0
Bit 13	R	RCNT[13]	0
Bit 12	R	RCNT[12]	0
Bit 11	R	RCNT[11]	0
Bit 10	R	RCNT[10]	0
Bit 9	R	RCNT[9]	0
Bit 8	R	RCNT[8]	0
Bit 7	R	RCNT[7]	0
Bit 6	R	RCNT[6]	0
Bit 5	R	RCNT[5]	0
Bit 4	R	RCNT[4]	0
Bit 3	R	RCNT[3]	0
Bit 2	R	RCNT[2]	0
Bit 1	R	RCNT[1]	0
Bit 0	R	RCNT[0]	0

Register 0x111, 0x511, 0x1311, 0x1711: Receive Performance Count MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	RCNT[23]	0
Bit 6	R	RCNT[22]	0
Bit 5	R	RCNT[21]	0
Bit 4	R	RCNT[20]	0
Bit 3	R	RCNT[19]	0
Bit 2	R	RCNT[18]	0
Bit 1	R	RCNT[17]	0
Bit 0	R	RCNT[16]	0

RCNT[23:0]

The RCNT[23:0] bits indicate the number of cells or packets received during the last accumulation interval. When the channel is configured for ATM traffic, the number of valid received ATM cells are counted. When the channel is configured for packet trace, the number of valid end of packets are counted.

This counter exists after the RXCP/RXFP FIFO allowing it to count the number of actual received items. Since the RUL3 does not drop cells or packet information, RCNT[23:0] supplies an accurate count. However, when compared to the performance counters in RXCP/RXFP, RCNT[23:0] may differ slightly due to the number of items stored in the RXCP/RXFP FIFO.

This counter is polled by writing to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800). Such a write transfers the internally accumulated count to the RCELL Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 0x112, 0x512, 0x1312, 0x1712: Channel Auxiliary Framer Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	R/W	Reserved	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	R/W	MFPEN	0
Bit 9	R/W	RFRM[1]	0
Bit 8	R/W	RFRM[0]	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	—	Unused	X
Bit 4	R/W	LOFINT[1]	0
Bit 3	R/W	LOFINT[0]	0
Bit 2	R/W	LINESYSCLK	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

LINESYSCLK

LINESYSCLK is used to select the high-speed system clock which the RDLC AUX HDLC controller uses as a reference. If LINESYSCLK is set to logic 1, then the RDLC AUX uses the serial clock selected by AUXFRMRSEL register bit (channel address 0x113) as its high-speed system reference clock. If LINESYSCLK is set to logic 0, the RDLC AUX uses the receive system interface clock (RFCLK) as its high-speed system reference clock respectively.

The read/write access rate to the RDLC AUX is limited by the high-speed reference clock frequency. Data and status indications can be read from the RDLC AUX at a maximum rate equal to 1/10 of its high-speed reference clock frequency.

Instantaneous variations in the high-speed reference clock frequency (e.g. jitter in the receive line clock) must be considered when determining the procedure used to read and write the RDLC AUX registers.

LOFINT[1:0]

The LOFINT[1:0] bits determine the integration period used for asserting and deasserting E3 and DS3 Loss of Frame or J2 extended Loss of Frame on the AUXFRMLOF register bit of the Channel Auxiliary Framer LOF Status register and on the FRMSTAT[11:0] output pins (if this function is enabled by the AUXLOFEN register bit of the Channel FRMSTAT Control Register). The integration times are selected as follows:

Table 26 Channel Auxiliary LOF[1:0] Integration Period Configuration

LOFINT[1:0]	Integration Period
00	3ms
01	2ms
10	1ms
11	Reserved

RFRM[1:0]

The RFRM[1:0] bits determine the expected frame structure of the received signal according to the following table:

Table 27 Channel Auxiliary RFRM[1:0] Receive Frame Structure Configurations

RFRM[1:0]	Expected Receive Frame Structure
00	DS3 (C-bit parity or M23 depending on the setting of the CBE bit in the DS3 FRMR AUX Configuration register)
01	E3 (G.751 or G.832 depending on the setting of the FORMAT[1:0] bits in the E3 FRMR AUX Framing Options register)
10	J2 (G.704 and NTT compliant framing format)
11	Reserved

MFPEN

The MFPEN bit controls whether the Auxiliary FRMR generates a frame pulse or a multi-frame pulse. If MFPEN is a logic 1, then the auxiliary FRMR will generate a multi-frame pulse. If MFPEN is a logic 0, then the auxiliary FRMR will generate a frame pulse.

Register 0x113, 0x513, 0x1313, 0x1713: Channel Data Path Configuration

Bit	Type	Function	Default
Bit 15	R/W	FBWEN	0
Bit 14	R/W	TJATTICLKSEL	0
Bit 13	R/W	TJATREFSEL	0
Bit 12	R/W	Reserved	1
Bit 11	R/W	REFE3DS3B	0
Bit 10	R/W	E3_1524_1508	0
Bit 9	R/W	D3E3MASEL	0
Bit 8	R/W	DS3AUXFEBEEN	0
Bit 7	R/W	AUXFRMRSEL	0
Bit 6	R/W	DS3FEBEEN	0
Bit 5	R/W	FRMRSEL	0
Bit 4	R/W	TRANTDIS	0
Bit 3	R/W	E3TRANTRACESEL	0
Bit 2	R/W	E3FEBEMODE[1]	0
Bit 1	R/W	E3FEBEMODE[0]	0
Bit 0	R/W	TRANSEL	0

TRANSEL

The TRAN Select bit controls what drives the inputs to the TRAN when FRMRONLY is logic 1. When TRANSEL is logic 0, the TRAN is driven by the transmit auxiliary interface. When TRANSEL is logic 1, the TRAN is driven by the Auxiliary FRMR.

E3FEBEMODE[1:0]

The E3 FEBE Mode (E3FEBEMODE[1:0]) bits control what defect sources a Far End Block Error indication (setting of bit 2 of the G.832 Maintenance and Adaptation byte) by the E3-TRAN according to the following table:

Table 28 Channel E3 FEBE Source

E3FEBEMODE[1:0]	FEBE Indication
00	E3 FRMR detection BIP-8 error
01	Reserved
10	Reserved
11	E3 FRMR AUX detection of BIP-8 error

E3TRANTRACESEL

The E3 TRAN TRACE Select bit controls what drives E3 G.832 trail trace to the E3 TRAN. When E3TRANTRACESEL is logic 0, the trail trace is sourced from the TTB. When E3TRANTRACESEL is logic 1, the trail trace is sourced from the TTB AUX.

TRANTDIS

The TRAN Transmit Disable bit disables all overhead insertion in the DS3/E3 Transmitters. When logic 0, overhead insertion is enabled in the DS3/E3 Transmitters. When logic 1, overhead insertion is disabled in the DS3/E3 Transmitters.

This bit is intended for use when operating in clear channel PDH over SONET/SDH mode and has been further illustrated in PMC-2021632 "SUNI 4xJET ASSP Telecom Standard Product Data Sheet" Operations Section.

When configured for any other operating mode, this bit should be set to logic 0.

FRMRSEL

The FRMRSEL Select bit controls what drives the FRMR (through the RJAT). When logic 0, the FRMR is driven by the serial interface. When logic 1, the FRMR is driven by the D3E3MD.

DS3FEBEEN

The DS3 FEBE Enable bit enables the alarm feedback to the DS3 TRAN from the DS3 FRMR. When logic 1, the FEBE alarm feedback signal from the DS3 FRMR is enabled. When logic 0, the FEBE alarm feedback signal from the DS3 FRMR is disabled.

AUXFRMRSEL

The Auxiliary FRMR Select bit controls what drives the auxiliary FRMR. When logic 0, the auxiliary FRMR is driven by the auxiliary interface. When logic 1, the auxiliary FRMR is driven by the D3E3MD.

DS3AUXFEBEEN

The Auxiliary DS3 FEBE Enable bit enables the alarm feedback to the DS3 TRAN from the auxiliary DS3 FRMR. When logic 1, the FEBE alarm feedback signal from the auxiliary DS3 FRMR is enabled. When logic 0, the FEBE alarm feedback signal from the auxiliary DS3 FRMR is disabled.

D3E3MASEL

The D3E3MA Select bit controls what drives the D3E3MA. When logic 0, the D3E3MA is driven by TRAN. When logic 1, the D3E3MA is driven by the FRMR.

E3_1524_1508

The E3 1524_1508 mode bit controls the payload insertion/extraction into bits 13, 14, 15, and 16 of the E3 G.751 frame (directly following the RAI and Na bits). When logic 0, the bits 13, 14, 15, and 16 are set to 1, 1, 0, and 0. When logic 1, the these bits are accessible for payload mapping. The available payload bits in the E3 G.751 frame are dependent on E3_1524_1508 and PYLD&JUST in the E3-TRAN and E3 FRMR, and has been summarized in the following table:

Table 29 Channel E3 G.751 Available Payload

E3_1524_1508	PYLD&JUST	# Payload Bits
0	0	1504
0	1	1520
1	0	1508
1	1	1524

When used to transport ATM cells direct mapped, or PLCP mapped, into E3 G.751 this bit should be set to logic 0. Also, when configured for a PDH mode other than E3 G.751 this bit should be set to logic 0.

REFE3DS3B

The REFCLK E3/DS3 select bit controls the serial line reference clock used by the TJAT, RJAT, and D3E3MD. When logic 0, the reference clock is DS3_REFCLK. When logic 1, the reference clock is E3_REFCLK.

TJATREFSEL

The TJAT Reference Select bit controls what clock is used as a reference to the TJAT. When logic 0, the TJAT uses TICLK[x] as a reference clock. When logic 1, the TJAT uses RCLK_IFBWCLK[x] as a reference clock.

This bit is intended for use for a secondary loop-timed mode of operation. The serial transmit timing source is loop-timed to the serial receiver by setting this bit to logic 1 in addition to TJATTICLKSEL (channel address 0x113). The transmit nibble stuffing is derived from the nibble stuffing in the receive PLCP frame (for DS3 or E3 PLCP frame transmission). The FIXSTUFF bit (channel address 0x00C) must be set to logic 0 in this loop-timed mode of operation.

This timing loopback has been further illustrated in PMC-2021632 “SUNI 4xJET ASSP Telecom Standard Product Data Sheet.”

TJATTICLKSEL

The Transmit JAT TICLK select bit selects the serial transmit timing source used by the SPLT, TRAN, and AUX FRMR. When logic 0, the transmit timing source is a delayed version of TICLK[x]. When logic 1, the transmit timing source is a smoothed output clock generated by the TJAT.

Setting the TJATTICLKSEL bit disables the effect of the TXREF (channel address 0x002) bit thereby forcing flow-through timing.

FBWEN

The Flexible Bandwidth Enable bit provisions the channel to access the flexible bandwidth (BW) interface. When logic 0, the channel is not provisioned to interface with the flexible BW interface. When logic 1, the channel is provisioned to interface with the flexible BW interface.

When not configured for flexible BW operation, this bit should be set to logic 0.

Register 0x114, 0x514, 0x1314, 0x1714: Channel Serial Cross Connect Configuration

Bit	Type	Function	Default
Bit 15	R/W	RXCHSEL[3]	0
Bit 14	R/W	RXCHSEL[2]	0
Bit 13	R/W	RXCHSEL[1]	0
Bit 12	R/W	RXCHSEL[0]	0
Bit 11	R/W	TXCHEN[3]	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	TXCHEN[1]	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	TXCHEN[2]	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	TXCHEN[0]	0

TXCHEN[3:0]

The Transmit Channel Enable (TXCHEN) bits control what serial links the channel will drive. When TXCHEN[x] is logic 0, the serial link (TPOS[x], TNEG[x], and TCLK[x]) is not driven by the channel. When TXCHEN[x] is logic 1, the serial link (TPOS[x], TNEG[x], and TCLK[x]) is driven by the channel. The default value of the register is such that channel N defaults to source only the corresponding serial link (TPOS[N], TNEG[N], and TCLK[N]).

RXCHSEL[3:0]

The Receive Channel Select (RXCHSEL) bits control what serial link will drive the channel. The RXCHSEL register bits form a binary representation to decode the serial link (RPOS/RDATI[x][x], RNEG/RLCV/ROHM[x], and RCLK[x]) that will drive the channel, where 0H corresponds to serial link 0 (X = 0), 9H corresponds to serial link 1, 2H corresponds to serial link 2, and BH corresponds to serial link 3.

RXCHSEL[3:0] is valid from 0H-BH, any other programmed value will disable all processing of the serial link in the channel.

The default value of the register is such that channel N defaults to sink the corresponding serial link (RPOS/RDATI[x][N], RNEG/RLCV/ROHM[x][N], RCLK[N]).

Register 0x115, 0x515, 0x1315, 0x1715: Channel Auxiliary Framer Data Link and XFERF/RAI Control

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	AISEN	0
Bit 5	R/W	RBLEN	0
Bit 4	R/W	OOFEN	0
Bit 3	R/W	Reserved	0
Bit 2	—	Unused	X
Bit 1	R/W	RNETOP	0
Bit 0	R/W	DLINV	0

DLINV

The DLINV bit provides polarity control for the DS3 C-bit Parity path maintenance data link which is located in the 3 C-bits of M-subframe 5. When a logic 1 is written to DLINV, the path maintenance data link is inverted before being processed.

The rationale behind this bit is as follows: currently ANSI standard T1.107 specifies that the C-bits (which carry the path maintenance data link) be set to all-zeros while the AIS maintenance signal is transmitted. The data link is obviously inactive during AIS transmission, and ideally the HDLC idle sequence (all-ones) should be transmitted. By inverting the data link, the all-zeros C-bit pattern becomes an idle sequence and the data link is terminated gracefully. Although this inversion is currently not specified in ANSI T1.107a, this bit is provided to safeguard the S/UNI 4xJET in case the inversion is required in the future.

RNETOP

The RNETOP bit enables the Network Operator Byte (NR) extracted from the G.832 E3 stream to be terminated by the internal HDLC receiver, RDLC AUX. When RNETOP is logic 1, the NR byte is extracted from the G.832 stream and terminated by RDLC AUX. When RNETOP is logic 0, the GC byte is extracted from the G.832 stream and terminated by RDLC AUX.

OOFEN

The OOFEN bit optionally enables the receive out of frame indication to automatically generate a FERF indication (RAI in G.751 or J2 mode) in the serial transmit stream. This bit operates when the E3 or J2 auxiliary framer is selected or when the DS3 auxiliary framer is selected and the RBLEN bit is logic 0. When OOFEN is logic 1, assertion of the OOF indication by the auxiliary framer causes a FERF/RAI to be transmitted by TRAN for the duration of the OOF assertion. When OOFEN is logic 0, assertion of the OOF indication does not cause transmission of a FERF/RAI.

For the RAI to be automatically transmitted when in J2 format, the FEAC[5:0] bits in the XBOC Code register (channel address 0x09B) must all be set to logic 1. If the XBOC FEAC code is to be transmitted in J2 mode, LOSEN, OOFEN, and AISEN should all be set to logic 0.

The auxiliary framer is commonly used solely for bidirectional performance monitoring, with no alarm feedback to the TRAN. This bit should be set to logic 0 if no alarm feedback is required.

RBLEN

The RBLEN bit enables the receive RED alarm (persistent out of frame) indication to automatically generate a FERF indication in the DS3 transmit stream, or a BIP8 error detection in the E3 G.832 auxiliary framer to generate a FEBE indication in the E3 G.832 transmit stream, or an LOF to generate a RLOF indication (A-bit) in the J2 transmit stream. When the E3 G.751 auxiliary framer is selected, this bit has no effect. When RBLEN is logic 1 and TFRM[1:0] is 00 binary and RFRM[1:0] is 00 binary, assertion of the RED indication by the auxiliary framer causes a FERF to be transmitted by DS3_TRAN for the duration of the RED assertion. When RBLEN is logic 0, assertion of the RED indication does not cause transmission of a FERF. When RBLEN is logic 1 and TFRM[1:0] is 01 binary and RFRM[1:0] is 01 binary, any BIP8 error indication by the E3 G.832 auxiliary framer causes a FEBE to be generated by the E3 G.832 TRAN. When RBLEN is logic 0, BIP8 errors detected by the E3 auxiliary framer do not cause FEBEs to be generated by the E3_TRAN. When RBLEN is logic 1 and TFRM[1:0] is 10 binary and RFRM[1:0] is 10 binary, any LOF error indication by the J2 framer causes the RLOF bit (also known as the A bit) to be set in the J2 transmit stream. When RBLEN is logic 0, LOF errors detected by the J2 auxiliary framer do not cause the RLOF bit to be set in the serial transmit stream.

The auxiliary framer is commonly used solely for bidirectional performance monitoring, with no alarm feedback to the TRAN. This bit should be set to logic 0 if no alarm feedback is required.

AISEN

The AISEN bit enables the receive alarm indication signal to automatically generate a FERF indication (RAI in G.751 or J2 mode) in the serial transmit stream. This bit operates regardless of auxiliary framer selected (DS3, E3, or J2). When AISEN is logic 1, assertion of the AIS indication (physical AIS for J2) by the auxiliary framer causes a FERF/RAI to be transmitted by TRAN for the duration of the AIS assertion. When AISEN is logic 0, assertion of the AIS indication does not cause transmission of a FERF/RAI.

For the RAI to be automatically transmitted when in J2 format, the FEAC[5:0] bits in the XBOC Code register (channel address 0x09B) must all be set to logic 1. If the XBOC FEAC code is to be transmitted in J2 mode, LOSEN, OOFEN, and AISEN should all be set to logic 0.

The auxiliary framer is commonly used solely for bidirectional performance monitoring, with no alarm feedback to the TRAN. This bit should be set to logic 0 if no alarm feedback is required.

Register 0x116, 0x516, 0x1316, 0x1716: Channel Auxiliary Framer LOF Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R	AUXFRMRLOF	0
Bit 0	R/W	AUXFRMRLOFE	0

AUXFRMRLOFE

The AUXFRMRLOFE bit enables the generation of an interrupt due to a change in the AUXFRMRLOF state. When AUXFRMRLOFE is a logic 1, the interrupt is enabled.

AUXFRMRLOF

The AUXFRMRLOF bit shows the current state of the auxiliary E3/T3 LOF or the J2 Extended LOF indication (depending on which mode is enabled). When AUXFRMRLOF is logic 1, the auxiliary framer has lost frame synchronization for greater than 1ms, 2ms, or 3ms depending on the setting of the LOFINT[1:0] bits in the Channel Auxiliary Configuration register.

Register 0x117, 0x517, 0x1317, 0x1717: Channel D3E3MA DS3/E3-AIS Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	R/W	ROOLEN	0
Bit 9	R/W	AUXLOFEN	0
Bit 8	R/W	AUXAISEN	0
Bit 7	R/W	AUXRBLEN	0
Bit 6	R/W	AUXOOFEN	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	LOFEN	0
Bit 3	R/W	AISEN	0
Bit 2	R/W	RBLEN	0
Bit 1	R/W	OOFEN	0
Bit 0	R/W	LOSEN	0

LOSEN

The LOS enable bit allows the loss of signal defect to be ORed into the DS3/E3-AIS generation control to the D3E3MA. When the LOSEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable DS3/E3-AIS generation control to the D3E3MA. When the LOSEN bit is set low, the corresponding defect indication does not affect the DS3/E3-AIS generation control to the D3E3MA.

OOFEN

The OOF enable bit allows the out of frame defect to be ORed into the DS3/E3-AIS generation control to the D3E3MA. When the OOFEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable DS3/E3-AIS generation control to the D3E3MA. When the OOFEN bit is set low, the corresponding defect indication does not affect the DS3/E3-AIS generation control to the D3E3MA.

RBLEN

The RBL enable bit allows the receive RED alarm (persistent out of frame) defect to be ORed into the DS3/E3-AIS generation control to the D3E3MA. When the RBLEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable DS3/E3-AIS generation control to the D3E3MA. When the RBLEN bit is set low, the corresponding defect indication does not affect the DS3/E3-AIS generation control to the D3E3MA.

AISEN

The AIS enable bit allows the alarm in signal defect to be ORed into the DS3/E3-AIS generation control to the D3E3MA. When the AISEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable DS3/E3-AIS generation control to the D3E3MA. When the AISEN bit is set low, the corresponding defect indication does not affect the DS3/E3-AIS generation control to the D3E3MA.

LOFEN

The LOF enable bit allows the loss of frame defect to be ORed into the DS3/E3-AIS generation control to the D3E3MA. When the LOFEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable DS3/E3-AIS generation control to the D3E3MA. When the LOFEN bit is set low, the corresponding defect indication does not affect the DS3/E3-AIS generation control to the D3E3MA.

AUXOOFEN

The Auxiliary OOF enable bit allows the auxiliary out of frame defect to be ORed into the DS3/E3-AIS generation control to the D3E3MA. When the AUXOOFEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable DS3/E3-AIS generation control to the D3E3MA. When the AUXOOFEN bit is set low, the corresponding defect indication does not affect the DS3/E3-AIS generation control to the D3E3MA.

AUXRBLEN

The Auxiliary RBL enable bit allows the auxiliary receive RED alarm (persistent out of frame) defect to be ORed into the DS3/E3-AIS generation control to the D3E3MA. When the AUXRBLEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable DS3/E3-AIS generation control to the D3E3MA. When the AUXRBLEN bit is set low, the corresponding defect indication does not affect the DS3/E3-AIS generation control to the D3E3MA.

AUXAISEN

The Auxiliary AIS enable bit allows the auxiliary alarm in signal defect to be ORed into the DS3/E3-AIS generation control to the D3E3MA. When the AUXAISEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable DS3/E3-AIS generation control to the D3E3MA. When the AUXAISEN bit is set low, the corresponding defect indication does not affect the DS3/E3-AIS generation control to the D3E3MA.

AUXLOFEN

The Auxiliary LOF enable bit allows the auxiliary loss of frame defect to be ORed into the DS3/E3-AIS generation control to the D3E3MA. When the AUXLOFEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable DS3/E3-AIS generation control to the D3E3MA. When the AUXLOFEN bit is set low, the corresponding defect indication does not affect the DS3/E3-AIS generation control to the D3E3MA.

ROOLEN

The ROOL enable bit allows the RJAT PLL reference out of lock signal defect to be ORed into the DS3/E3-AIS generation control to the D3E3MA. When the ROOLEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable DS3/E3-AIS generation control to the D3E3MA. When the ROOLEN bit is set low, the corresponding defect indication does not affect the DS3/E3-AIS generation control to the D3E3MA.

Register 0x118, 0x518, 0x1318, 0x1718: Channel FRMSTAT Control

Bit	Type	Function	Default
15	—	Unused	X
14	—	Unused	X
13	R/W	AUXLOFEN	0
12	—	Unused	X
11	R/W	AUXOOFEN	0
10	—	Unused	X
9	R/W	AUXAISEN	0
8	R/W	AUXLOSEN	0
7	R/W	AUXT3IDLEEN	0
6	R/W	LOFEN	0
5	R/W	PLCPLOFEN	0
4	R/W	OOFEN	0
3	R/W	PLCPOOFEN	0
2	R/W	AISEN	0
1	R/W	LOSEN	0
0	R/W	T3IDLEEN	0

T3IDLEEN

The T3 IDLE enable bit allows the T3 idle defect to be ORed into the FRMSTAT[x] output. When the T3IDLEEN bit is set high, the corresponding defect indication is ORed with other defect indications and output on FRMSTAT[x]. When the T3IDLEEN bit is set low, the corresponding defect indication does not affect the FRMSTAT[x] output.

LOSEN

The LOS enable bit allows the loss of signal defect to be ORed into the FRMSTAT[x] output. When the LOSEN bit is set high, the corresponding defect indication is ORed with other defect indications and output on FRMSTAT[x]. When the LOSEN bit is set low, the corresponding defect indication does not affect the FRMSTAT[x] output.

AISEN

The AIS enable bit allows the alarm in signal defect to be ORed into the FRMSTAT[x] output. When the AISEN bit is set high, the corresponding defect indication is ORed with other defect indications and output on FRMSTAT[x]. When the AISEN bit is set low, the corresponding defect indication does not affect the FRMSTAT[x] output.

PLCPOOFEN

The PLCP OOF enable bit allows the PLCP out of frame defect to be ORed into the FRMSTAT[x] output. When the PLCPOOFEN bit is set high, the corresponding defect indication is ORed with other defect indications and output on FRMSTAT[x]. When the PLCPOOFEN bit is set low, the corresponding defect indication does not affect the FRMSTAT[x] output.

OOFEN

The OOF enable bit allows the out of frame defect to be ORed into the FRMSTAT[x] output. When the OOFEN bit is set high, the corresponding defect indication is ORed with other defect indications and output on FRMSTAT[x]. When the OOFEN bit is set low, the corresponding defect indication does not affect the FRMSTAT[x] output.

PLCPLOFEN

The PLCP LOF enable bit allows the PLCP loss of frame defect to be ORed into the FRMSTAT[x] output. When the PLCPLOFEN bit is set high, the corresponding defect indication is ORed with other defect indications and output on FRMSTAT[x]. When the PLCPLOFEN bit is set low, the corresponding defect indication does not affect the FRMSTAT[x] output.

LOFEN

The LOF enable bit allows the loss of frame defect to be ORed into the FRMSTAT[x] output. When the LOFEN bit is set high, the corresponding defect indication is ORed with other defect indications and output on FRMSTAT[x]. When the LOFEN bit is set low, the corresponding defect indication does not affect the FRMSTAT[x] output.

AUXT3IDLEEN

The Auxiliary T3 IDLE enable bit allows the auxiliary T3 idle defect to be ORed into the FRMSTAT[x] output. When the AUXT3IDLEEN bit is set high, the corresponding defect indication is ORed with other defect indications and output on FRMSTAT[x]. When the AUXT3IDLEEN bit is set low, the corresponding defect indication does not affect the FRMSTAT[x] output.

AUXLOSEN

The Auxiliary LOS enable bit allows the auxiliary loss of signal defect to be ORed into the FRMSTAT[x] output. When the AUXLOSEN bit is set high, the corresponding defect indication is ORed with other defect indications and output on FRMSTAT[x]. When the AUXLOSEN bit is set low, the corresponding defect indication does not affect the FRMSTAT[x] output.

AUXAISEN

The Auxiliary AIS enable bit allows the auxiliary alarm in signal defect to be ORed into the FRMSTAT[x] output. When the AUXAISEN bit is set high, the corresponding defect indication is ORed with other defect indications and output on FRMSTAT[x]. When the AUXAISEN bit is set low, the corresponding defect indication does not affect the FRMSTAT[x] output.

AUXOOFEN

The Auxiliary OOF enable bit allows the out of frame defect to be ORed into the FRMSTAT[x] output. When the AUXOOFEN bit is set high, the corresponding defect indication is ORed with other defect indications and output on FRMSTAT[x]. When the AUXOOFEN bit is set low, the corresponding defect indication does not affect the FRMSTAT[x] output.

AUXLOFEN

The Auxiliary LOF enable bit allows the loss of frame defect to be ORed into the FRMSTAT[x] output. When the AUXLOFEN bit is set high, the corresponding defect indication is ORed with other defect indications and output on FRMSTAT[x]. When the AUXLOFEN bit is set low, the corresponding defect indication does not affect the FRMSTAT[x] output.

Register 0x119, 0x519, 0x1319, 0x1719: Channel Miscellaneous Configuration #2

Bit	Type	Function	Default
15	—	Unused	X
14	—	Unused	X
13	—	Unused	X
12	—	Unused	X
11	—	Unused	X
10	—	Unused	X
9	—	Unused	X
8	—	Unused	X
7	—	Unused	X
6	—	Unused	X
5	—	Unused	X
4	—	Unused	X
3	—	Unused	X
2	R/W	Reserved	0
1	R/W	Reserved	0
0	R/W	SQUELCHTIP	0

SQUELCHTIP

The Squelch TIP bit provisions the PMON/PMON AUX/PRGD blocks to assert TIP (address 0x1801) for the duration of the performance monitor registers update for the particular block.

When the SQUELCHTIP bit is set high, the corresponding blocks sets TIP high while the performance monitor registers are loading. When the SQUELCHTIP bit is set low, the corresponding blocks do not effect TIP.

Note that when configured for Cell/Packet direct mapped to SONET/SDH it is not a requirement to provide TICLK[x] and RCLK[x] since the serial interface is unused. To prevent TIP from getting stuck high when in this mode, need to set SQUELCHTIP to logic 1.

Register 0x120, 0x520, 0x1320, 0x1720: D3E3MD Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	AISV	X
Bit 6	R/W	AU3TUG3B	1
Bit 5	R/W	DS3E3B	1
Bit 4	R/W	FIFORST	0
Bit 3	R/W	PLLRST	0
Bit 2	R/W	LOOPBW[1]	1
Bit 1	R/W	LOOPBW[0]	0
Bit 0	R/W	AISGEN	0

AISGEN

The active high Alarm Indication Signal enable bit (AISGEN) configures the D3E3MD to override the demapped DS3/E3 data with a DS3/E3-AIS signal. Any DS3/E3 data contained within the incoming STS-1/STM-0 SPE is lost due to the assertion of AISGEN.

This register bit is logically ORed with the downstream AIS-P indication from the SARC (address 0x184A). When the OR of the two signals is logic 1, DS3/E3-AIS is generated downstream. When the OR of the two signals is logic 0, the DS3/E3 frame is demapped and presented downstream.

LOOPBW[1:0]

The LOOPBW[1:0] register bits are used to accelerate the time required to lock, and sets the corner frequency of D3E3MD. LOOPBW has no effect when the D3E3MD operates in 1x mode. The operation of the LOOPBW is summarized below:

Table 30 D3E3MD Loop Bandwidth Configurations

LOOPBW[1:0]	DPLL Loop Bandwidth
00	0.1 Hz
10	0.2 Hz
01	3.2 Hz
11	12.8 Hz

PLLRST

PLLRST is used to reset the DS3/E3 clock generator PLL circuit. When PLLRST is high, the PLL is held in reset. When PLLRST is set low, the PLL operates normally.

FIFORST

FIFORST is used to reset the elastic store FIFO. When FIFORST is high, the contents of the FIFO buffers are cleared and the elastic store read / write pointers are reset. When FIFORST is set low, normal operation of the elastic store FIFO resumes.

See the Operations Section in PMC-2021632 on resetting the receive and transmit FIFOs.

DS3E3B

The DS3E3B register bit specifies the mode of operation of the D3E3MD TSB. When DS3E3B is high, the D3E3MD operates in DS3 mode. When D3E3B is low, the D3E3MD operates in E3 mode.

AU3TUG3B

The AU3TUG3B register bit selects one of two possible demapping modes. The D3E3MD can demap the DS3/E3 frame from a STS-1/STM-0 via AU3 or TUG3.

When AU3TUG3B is high, the D3E3MD demaps the DS3/E3 frame from the STS-1/STM-0 via AU3 frame.

When AU3TUG3B is low, the D3E3MD demaps the DS3/E3 frame from the STS-1/STM-0 via TUG3 frame. In this mode of operation it is necessary to use three separate channels and D3E3MD's in order to demap a STS-3/STM-1 via TUG3 frame.

AISV

AISV is used to determine the status of the OR structure described for the AISGEN register bit. When the result of the OR is high, AISV is set high. When the result of the OR is low, the AISV bit is set low.

Register 0x121, 0x521, 0x1321, 0x1721: D3E3MD Status/Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	TU3PPJI	X
Bit 4	R	TU3NPJI	X
Bit 3	R	SPEPPJI	X
Bit 2	R	SPENPJI	X
Bit 1	R	FOVRI	X
Bit 0	R	FUDRI	X

FUDRI

FUDRI is the Elastic store FIFO underflow indication bit. FUDRI is set high when a FIFO underflow event occurs. This interrupt status bit is independent of the FUDRE interrupt enable bit. When WCIMODE is low (read mode), FUDRI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), FUDRI is cleared by writing a high value to bit 0 of the interrupt status register.

FOVRI

FOVRI is the Elastic Store FIFO overflow indication bit. FOVRI is set high when a FIFO overflow event occurs. This interrupt status bit is independent of the FOVRE interrupt enable bit. When WCIMODE is low (read mode), FOVRI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), FOVRI is cleared by writing a high value to bit 1 of the interrupt status register.

SPENPJI

SPENPJI is set high when a negative justification event has been detected in the incoming STS-1/STM-0 SPE. This interrupt status bit is independent of the SPENPJE interrupt enable bit. When WCIMODE is low (read mode), SPENPJI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), SPENPJI is cleared by writing a high value to bit 2 of the interrupt status register.

SPEPPJI

SPEPPJI is set high when a positive justification event has been detected in the incoming STS-1/STM-0 SPE. This interrupt status bit is independent of the SPEPPJE interrupt enable bit. When WCIMODE is low (read mode), SPEPPJI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), SPEPPI is cleared by writing a high value to bit 3 of the interrupt status register.

TU3NPJI

The TU3NPJI bit is set high when a negative TU3 pointer justification event is detected in the incoming SONET/SDH data stream. TU3NPJI is only valid when the D3E3MD is configured to operate in TU3 mode. This interrupt status bit is independent of the TU3NPJE interrupt enable bit. When WCIMODE is low (read mode), TU3NPJI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), TU3NPJI is cleared by writing a high value to bit 4 of the interrupt status register.

TU3PPJI

The TU3PPJI bit is set high when a positive TU3 pointer justification event is detected in the incoming SONET/SDH data stream. TU3PPJI is only valid when the D3E3MD is configured to operate in TU3 mode. This interrupt status bit is independent of the TU3PPJE interrupt enable bit. When WCIMODE is low (read mode), TU3PPJI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), TU3PPJI is cleared by writing a high value to bit 5 of the interrupt status register.

Register 0x122, 0x522, 0x1322, 0x1722: D3E3MD Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	TU3PPJE	0
Bit 4	R/W	TU3NPJE	0
Bit 3	R/W	SPEPPJE	0
Bit 2	R/W	SPENPJE	0
Bit 1	R/W	FOVRE	0
Bit 0	R/W	FUDRE	0

FUDRE

FUDRE controls the assertion of the INTB output pin when FIFO underrun events occur. When FUDRE is set high, the INTB output is deasserted when FUDRI is one. When FUDRE is set low, the FUDRI bit has no effect on the INTB output.

FOVRE

The FOVRE bit controls the assertion of the INTB output pin when FIFO overrun events occur. When FOVRE is set high, the INTB output is deasserted when FOVRI is one. When FOVRE is set low, the FOVRI bit has no effect on the INTB output.

SPENPJE

SPENPJE controls the assertion of the INTB output pin when negative pointer justification events are detected in the incoming STS-1/STM-0 SPE. When SPENPJE is set high, the INTB output is deasserted when the SPENPJ I register bit is one. When SPENPJE is set low, the SPENPJI bit has no effect on the INTB output.

SPEPPJE

The SPEPPJE bit controls the assertion of the INTB output pin when positive pointer justification events are detected in the incoming STS-1/STM-0 SPE. When SPEPPJE is set high, the INTB output is deasserted when the SPEPPJ I register bit is one. When SPEPPJE is set low, the PPJI bit has no effect on the INTB output.

TU3NPJE

TU3NPJE controls the assertion of the INTB output pin when negative TU3 pointer justification events occur. When TU3NPJE is set high, the INTB output is deasserted when the TU3NPJI register bit is one. When TU3NPJE is set low, TU3NPJI has no effect on the INTB output.

TU3PPJE

TU3PPJE controls the assertion of the INTB output pin when negative TU3 pointer justification events occur. When TU3PPJE is set high, the INTB output is deasserted when the TU3PPJI register bit is one. When TU3PPJE is set low, TU3PPJI has no effect on the INTB output.

Register 0x128, 0x528, 0x1328, 0x1728: D3E3MA Control

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	AISV	0
Bit 6	R/W	AU3TUG3B	1
Bit 5	R/W	DS3E3B	1
Bit 4	R/W	FIFORST	0
Bit 3	R/W	PLLRST	0
Bit 2	R/W	LOOPBW	0
Bit 1	R/W	RBSO	0
Bit 0	R/W	AISGEN	0

AISGEN

The active high Alarm Indication Signal enable bit (AISGEN) configures the D3E3MA to generate an AIS Signal.

The AISGEN bit is logically ORed with the LOS, OOF, RED, AIS, LOF, AUX OOF, AUX RED, AUX AIS, AUX LOF, and ROOL indications from the FRMR, AUX FRMR, and RJAT when the LOSEN, OOFEN, RBLEN, AISEN, LOFEN, AUXOOFEN, AUXRBLEN, AUXAISEN, AUXLOFEN, and ROOLEN register bits (in the Channel D3E3MA DS3/E3-AIS Enable register) are set to logic 1 respectively. When the OR of these two signals is logic 1, and D3E3B is logic 1, the D3E3MA generates DS3-AIS. When the OR of these two signals is logic 1, and D3E3B is logic 0, the D3E3MA generates E3-AIS.

RBSO

When RBSO is high, (fixed stuff) R bits are set to ‘1’s. If RBSO bit is low, R bits are set to ‘0’s. This bit is valid for both E3 and DS3 modes of operation.

LOOPBW

The LOOPBW bit is used to select one of two PLL loop bandwidths. When LOOPBW is high, the D3E3MA PLL is in fast lock mode. If LOOPBW is low, the D3E3MA PLL is in normal mode.

PLLRST

PLLRST is used to reset the PLL. When PLLRST is set high, the accumulator contents of the Phase Lock Loop are cleared. When PLLRST is set low, the Phase Lock Loop operates normally.

FIFORST

FIFORST is used to reset the elastic store FIFO. When FIFORST is set high, the contents of the FIFO buffers are cleared and the elastic store read / write pointers are set as far apart from each other as possible. When FIFORST is set low, normal operation of the elastic store FIFO resumes.

See the Operations Section in PMC-2021632 on resetting the receive and transmit FIFOs.

DS3E3B

The DS3E3B register bit specifies the mode of operation of the D3E3MA TSB. When DS3E3B is high, the D3E3MA operates in DS3 mode. When DS3E3B is low, the D3E3MA operates in E3 mode.

AU3TUG3B

The AU3TUG3B register bit selects one of two possible mapping modes. The D3E3MA can map the DS3/E3 frame to STS-1/STM-0 via AU3 or TUG3 framing.

When AU3TUG3B is low, the D3E3MA maps the incoming signal to an STS-1/STM-0 via the TUG3 format. In this mode of operation it is necessary to use three separate channels and D3E3MA's in order to construct a STS-3/STM-1 via TUG3 frame.

When AU3TUG3B is high, the D3E3MA maps the incoming signal to an STS-1/STM-0 via the AU3 format.

AISV

AISV is used to determine the status of the OR structure described for the AISGEN register bit. When the result of the OR is high, AISV is set high. When the result of the OR is low, the AISV bit is set low.

Register 0x129, 0x529, 0x1329, 0x1729: D3E3MA Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R	FOVRI	X
Bit 0	R	FUDRI	X

FUDRI

When set high, this bit indicates that an underflow condition has occurred in the elastic store. An underflow condition resets the elastic store FIFO read and write pointers as far apart from each other as possible. This interrupt status bit is independent of the FUDRE interrupt enable bit. When WCIMODE is low (read mode), FUDRI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), FUDRI is cleared by writing a high value to bit 0 of the interrupt status register.

FOVRI

When set high, this bit indicates that an overflow condition has occurred in the elastic store. An overflow condition resets the elastic store FIFO read and write pointers as far apart from each other as possible. This interrupt status bit is independent of the FOVRE interrupt enable bit. When WCIMODE is low (read mode), FOVRI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), FOVRI is cleared by writing a high value to bit 0 of the interrupt status register.

Register 0x12A, 0x52A, 0x132A, 0x172A: D3E3MA Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	FOVRE	0
Bit 0	R/W	FUDRE	0

FUDRE

FUDRE controls the assertion of the INTB output pin when FIFO underflow events occur. When FUDRE is set high, the INTB output is deasserted if FUDRI is one. When FUDRE is set low, the FUDRI bit has no effect on the INTB output.

FOVRE

The FOVRE bit controls the assertion of the INTB output pin when FIFO overflow events occur. When FOVRE is set high, the INTB output is deasserted if FOVRI is one. When FOVRE is set low, the FOVRI bit has no effect on the INTB output.

Register 0x130, 0x530, 0x1330, 0x1730: RDLC DEMAPPER Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	MEN	0
Bit 2	R/W	MM	0
Bit 1	R/W	TR	0
Bit 0	R/W	EN	0

The RDLC DEMAPPER block has been further illustrated in PMC-2021632 “SUNI 4xJET ASSP Telecom Standard Product Data Sheet.”

EN

The EN bit controls the overall operation of the RDLC DEMAPPER. When EN is set to logic 1, RDLC DEMAPPER is enabled. When set to logic 0, RDLC DEMAPPER is disabled. When RDLC DEMAPPER is disabled, the RDLC DEMAPPER FIFO buffer and interrupts are all cleared. When RDLC DEMAPPER is enabled, it will immediately begin looking for flags.

TR

Setting the terminate reception (TR) bit to logic 1 forces the RDLC DEMAPPER to immediately terminate the reception of the current data frame, empty the RDLC DEMAPPER FIFO buffer, clear the interrupts, and begin searching for a new flag sequence. The RDLC DEMAPPER handles a terminate reception event in the same manner as it would the toggling of the EN bit from logic 1 to logic 0 and back to logic 1. Thus, the RDLC DEMAPPER state machine will begin searching for flags. An interrupt will be generated when the first flag is detected. The TR bit will reset itself to logic 0 after the register write operation is completed and a rising and falling edge occurs on the internal datalink clock input. If the RDLC DEMAPPER Configuration Register is read after this time, the TR bit value returned will be logic 0.

MM

Setting the Match Mask (MM) bit to logic 1 ignores the PA[1:0] bits of the Primary Address Match Register, the SA[1:0] bits of the Secondary Address Match Register, and the two least significant bits of the universal all-ones address when performing the address comparison.

MEN

Setting the Match Enable (MEN) bit to logic 1 enables the detection and storage in the RDLC DEMAPPER FIFO of only those packets whose first data byte matches either of the bytes written to the Primary or Secondary Match Address Registers, or the universal all-ones address. When the MEN bit is logic 0, all packets received are written into the RDLC DEMAPPER FIFO.

Register 0x131, 0x531, 0x1331, 0x1731: RDLC DEMAPPER Interrupt Control

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	INTE	0
Bit 6	R/W	INTC[6]	0
Bit 5	R/W	INTC[5]	0
Bit 4	R/W	INTC[4]	0
Bit 3	R/W	INTC[3]	0
Bit 2	R/W	INTC[2]	0
Bit 1	R/W	INTC[1]	0
Bit 0	R/W	INTC[0]	0

The contents of the Interrupt Control Register should only be changed when the EN bit in the RDLC DEMAPPER Configuration Register is logic 0. This prevents any erroneous interrupt generation.

INTC[6:0]

The INTC[6:0] bits control the assertion of FIFO fill level set point interrupts. The value of INTC[6:0] = ‘b0000000 sets the interrupt FIFO fill level to 128.

INTE

The Interrupt Enable bit (INTE) must set to logic 1 to allow the internal interrupt status to be propagated to the INTB output. When the INTE bit is logic 0 the RDLC DEMAPPER will not assert INTB.

Register 0x132, 0x532, 0x1332, 0x1732: RDLC DEMAPPER Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	FE	X
Bit 6	R	OVR	X
Bit 5	R	COLS	X
Bit 4	R	PKIN	X
Bit 3	R	PBS[2]	X
Bit 2	R	PBS[1]	X
Bit 1	R	PBS[0]	X
Bit 0	R	INTR	X

Consecutive reads of the RDLC DEMAPPER Status and Data registers should not occur at rates greater than 1/120 that of the receive line clock ICLK.

INTR

The interrupt (INTR) bit reflects the status of the internal RDLC DEMAPPER interrupt. If the INTE bit in the RDLC DEMAPPER Interrupt Control Register is set to logic 1, a RDLC DEMAPPER interrupt (INTR is a logic 1) will cause INTB to be asserted low. The INTR register bit will be set to logic 1 when one of the following conditions occurs:

- The number of bytes specified in the RDLC DEMAPPER Interrupt Control register have been received on the data link and written into the FIFO.
- RDLC DEMAPPER FIFO buffer overrun has been detected.
- The last byte of a packet has been written into the RDLC DEMAPPER FIFO.
- The last byte of an aborted packet has been written into the RDLC DEMAPPER FIFO.
- Transition of receiving all-ones to receiving flags has been detected.

PBS[2:0]

The packet byte status (PBS[2:0]) bits indicate the status of the data last read from the FIFO as indicated in the following table:

Table 31 RDLC DEMAPPER PBS[2:0] Data Status

PBS[2:0]	Data Status
000	The data byte read from the FIFO is not special.
001	The data byte read from the FIFO is the dummy byte that was written into the FIFO when the first HDLC flag sequence (01111110) was detected. This indicates that the data link became active.
010	The data byte read from the FIFO is the dummy byte that was written into the FIFO when the HDLC abort sequence (01111111) was detected. This indicates that the data link became inactive.
011	Unused.
100	The data byte read from the FIFO is the last byte of a normally terminated packet with no CRC error and the packet received had an integer number of bytes.
101	The data byte read from the FIFO must be discarded because there was a non-integer number of bytes in the packet.
110	The data byte read from the FIFO is the last byte of a normally terminated packet with a CRC error. The packet was received in error.
111	The data byte read from the FIFO is the last byte of a normally terminated packet with a CRC error and a non-integer number of bytes. The packet was received in error.

PKIN

The Packet In (PKIN) bit is logic 1 when the last byte of a non-aborted packet is written into the FIFO. The PKIN bit is cleared to logic 0 after the RDLC DEMAPPER Status Register is read.

COLS

The Change of Link Status (COLS) bit is set to logic 1 if the RDLC DEMAPPER has detected the HDLC flag sequence (01111110) or HDLC abort sequence (01111111) in the data. This indicates that there has been a change in the data link status. The COLS bit is cleared to logic 0 by reading this register or by clearing the EN bit in the RDLC DEMAPPER Configuration Register. For each change in link status, a byte is written into the FIFO. If the COLS bit is found to be logic 1 then the RDLC DEMAPPER FIFO must be read until empty. The status of the data link is determined by the PBS[2:0] bits associated with the data read from the RDLC DEMAPPER FIFO.

OVR

The overrun (OVR) bit is set to logic 1 when data is written over unread data in the RDLC DEMAPPER FIFO buffer. This bit is not reset to logic 0 until after the Status Register is read. While the OVR bit is logic 1, the RDLC DEMAPPER and RDLC DEMAPPER FIFO buffer are held in the reset state, causing the COLS and PKIN bits to be reset to logic 0.

FE

The FIFO buffer empty (FE) bit is set to logic 1 when the last RDLC DEMAPPER FIFO buffer entry is read. The FE bit goes to logic 0 when the FIFO is loaded with new data.

Register 0x133, 0x533, 0x1333, 0x1733: RDLC DEMAPPER Data

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	RD[7]	X
Bit 6	R	RD[6]	X
Bit 5	R	RD[5]	X
Bit 4	R	RD[4]	X
Bit 3	R	RD[3]	X
Bit 2	R	RD[2]	X
Bit 1	R	RD[1]	X
Bit 0	R	RD[0]	X

Consecutive reads of the RDLC DEMAPPER Status and Data registers should not occur at rates greater than 1/120 that of the receive line clock ICLK.

RD[7:0]

RD[7:0] contains the received data link information. RD[0] corresponds to the first received bit of the data link message.

This register reads from the RDLC DEMAPPER 128-byte FIFO buffer. If data is available, the FE bit in the FIFO Input Status Register is logic 0.

When an overrun is detected, an interrupt is generated and the FIFO buffer is held cleared until the RDLC DEMAPPER Status Register is read.

Register 0x134, 0x534, 0x1334, 0x1734: RDLC DEMAPPER Primary Address Match

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	PA[7]	1
Bit 6	R/W	PA[6]	1
Bit 5	R/W	PA[5]	1
Bit 4	R/W	PA[4]	1
Bit 3	R/W	PA[3]	1
Bit 2	R/W	PA[2]	1
Bit 1	R/W	PA[1]	1
Bit 0	R/W	PA[0]	1

PA[7:0]

The first byte received after a flag character is compared against the contents of this register. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. PA[0] corresponds to the first received bit of the data link message. The MM bit in the Configuration Register is used mask off PA[1:0] during the address comparison.

Register 0x135, 0x535, 0x1335, 0x1735: RDLC DEMAPPER Secondary Address Match

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	SA[7]	1
Bit 6	R/W	SA[6]	1
Bit 5	R/W	SA[5]	1
Bit 4	R/W	SA[4]	1
Bit 3	R/W	SA[3]	1
Bit 2	R/W	SA[2]	1
Bit 1	R/W	SA[1]	1
Bit 0	R/W	SA[0]	1

SA[7:0]

The first byte received after a flag character is compared against the contents of this register. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. SA[0] corresponds to the first received bit data link message. The MM bit in the Configuration Register is used mask off SA[1:0] during the address comparison.

Register 0x138, 0x538, 0x1338, 0x1738: TDPR MAPPER Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	FLGSHARE	1
Bit 6	R/W	FIFOCLR	0
Bit 5	R/W	Reserved	0
Bit 4	—	Unused	X
Bit 3	R/W	EOM	0
Bit 2	R/W	ABT	0
Bit 1	R/W	CRC	1
Bit 0	R/W	EN	0

Consecutive writes to the TDPR MAPPER Configuration, TDPR MAPPER Interrupt Status/UDR Clear, and TDPR MAPPER Transmit Data register and reads of the TDPR MAPPER Interrupt Status/UDR Clear register should not occur at rates greater than 1/96 that of the transmit line clock OCLK.

The TDPR MAPPER block has been further illustrated in PMC-2021632 “SUNI 4xJET ASSP Telecom Standard Product Data Sheet.”

EN

The EN bit enables the TDPR MAPPER functions. When EN is set to logic 1, the TDPR MAPPER is enabled and flag sequences are sent until data is written into the TDPR MAPPER Transmit Data register. When the EN bit is set to logic 0, the TDPR MAPPER is disabled and an all 1's Idle sequence is transmitted on the datalink.

CRC

The CRC enable bit controls the generation of the CCITT_CRC frame check sequence (FCS). Setting the CRC bit to logic 1 enables the CCITT-CRC generator and appends the 16-bit FCS to the end of each message. When the CRC bit is set to logic 0, the FCS is not appended to the end of the message. The CRC type used is the CCITT-CRC with generator polynomial $x^{16} + x^{12} + x^{5} + 1$. The high order bit of the FCS word is transmitted first.

ABT

The Abort (ABT) bit controls the sending of the 7 consecutive ones HDLC abort code. Setting the ABT bit to a logic 1 causes the 01111111 code (the 0 is transmitted first) to be transmitted after the current byte from the TDPR MAPPER FIFO is transmitted. The TDPR MAPPER FIFO is then reset. All data in the TDPR MAPPER FIFO will be lost. Aborts are continuously sent and the FIFO is held in reset until this bit is reset to a logic 0. At least one Abort sequence will be sent when the ABT bit transitions from logic 0 to logic 1.

EOM

The EOM bit indicates that the last byte of data written in the Transmit Data register is the end of the present data packet. If the CRC bit is set then the 16-bit FCS word is appended to the last data byte transmitted and a continuous stream of flags is generated. The EOM bit is automatically cleared upon a write to the TDPR MAPPER Transmit Data register.

FIFOCLR

The FIFOCLR bit resets the TDPR MAPPER FIFO. When set to logic 1, FIFOCLR will cause the TDPR MAPPER FIFO to be cleared.

FLGSHARE

The FLGSHARE bit configures the TDPR MAPPER to share the opening and closing flags between successive frames. If FLGSHARE is logic 1, then the opening and closing flags between successive frames are shared. If FLGSHARE is logic 0, then separate closing and opening flags are inserted between successive frames.

Register 0x139, 0x539, 0x1339, 0x1739: TDPR MAPPER Upper Transmit Threshold

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	UTHR[6]	1
Bit 5	R/W	UTHR[5]	0
Bit 4	R/W	UTHR[4]	0
Bit 3	R/W	UTHR[3]	0
Bit 2	R/W	UTHR[2]	0
Bit 1	R/W	UTHR[1]	0
Bit 0	R/W	UTHR[0]	0

UTHR[6:0]

The UTHR[6:0] bits define the TDPR MAPPER FIFO fill level which will automatically cause the bytes stored in the TDPR MAPPER FIFO to be transmitted. Once the fill level exceeds the UTHR[6:0] value, transmission will begin. Transmission will not stop until the last complete packet is transmitted and the TDPR MAPPER FIFO fill level is below UTHR[6:0] + 1.

The value of UTHR[6:0] must always be greater than the value of LINT[6:0] unless both values are equal to 00H.

Register 0x13A, 0x53A, 0x133A, 0x173A: TDPR MAPPER Lower Interrupt Threshold

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	LINT[6]	0
Bit 5	R/W	LINT[5]	0
Bit 4	R/W	LINT[4]	0
Bit 3	R/W	LINT[3]	0
Bit 2	R/W	LINT[2]	1
Bit 1	R/W	LINT[1]	1
Bit 0	R/W	LINT[0]	1

LINT[6:0]

The LINT[6:0] bits define the TDPR MAPPER FIFO fill level which causes an internal interrupt (LFILLI) to be generated. Once the TDPR MAPPER FIFO level decrements to empty or to a value less than LINT[6:0], LFILLI and BLFILL register bits will be set to logic 1. LFILLI will cause an interrupt on INTB if LFILLE is set to logic 1.

The value of LINT[6:0] must always be less than the value of UTHR[6:0] unless both values are equal to 00H.

Register 0x13B, 0x53B, 0x133B, 0x173B: TDPR MAPPER Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	FULLE	0
Bit 2	R/W	OVRE	0
Bit 1	R/W	UDRE	0
Bit 0	R/W	LFILLE	0

LFILLE

The LFILLE enables a transition to logic 1 on LFILLI to generate an interrupt on INTB. If LFILLE is a logic 1, a transition to logic 1 on LFILLI will generate an interrupt on INTB. If LFILLE is a logic 0, a transition to logic 1 on LFILLI will not generate an interrupt on INTB.

UDRE

The UDRE enables a transition to logic 1 on UDRI to generate an interrupt on INTB. If UDRE is a logic 1, a transition to logic 1 on UDRI will generate an interrupt on INTB. If UDRE is a logic 0, a transition to logic 1 on UDRI will not generate an interrupt on INTB.

OVRE

The OVRE enables a transition to logic 1 on OVRI to generate an interrupt on INTB. If OVRE is a logic 1, a transition to logic 1 on OVRI will generate an interrupt on INTB. If OVRE is a logic 0, a transition to logic 1 on OVRI will not generate an interrupt on INTB.

FULLE

The FULLE enables a transition to logic 1 on FULLI to generate an interrupt on INTB. If FULLE is a logic 1, a transition to logic 1 on FULLI will generate an interrupt on INTB. If FULLE is a logic 0, a transition to logic 1 on FULLI will not generate an interrupt on INTB.

Register 0x13C, 0x53C, 0x133C, 0x173C: TDPR MAPPER Interrupt Status/UDR Clear

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R	FULL	X
Bit 5	R	BLFILL	X
Bit 4	R	Unused	X
Bit 3	R	FULLI	X
Bit 2	R	OVRI	X
Bit 1	R	UDRI	X
Bit 0	R	LFILLI	X

Consecutive writes to the TDPR MAPPER Configuration, TDPR MAPPER Interrupt Status/UDR Clear, and TDPR MAPPER Transmit Data register and reads of the TDPR MAPPER Interrupt Status/UDR Clear register should not occur at rates greater than 1/96 that of the transmit line clock OCLK.

LFILLI

The LFILLI bit will transition to logic 1 when the TDPR MAPPER FIFO level transitions to empty or falls below the value of LINT[6:0] programmed in the TDPR MAPPER Lower Interrupt Threshold register. LFILLI will assert INTB if it is a logic 1 and LFILLE is programmed to logic 1. LFILLI is cleared when this register is read.

UDRI

The UDRI bit will transition to 1 when the TDPR MAPPER FIFO underruns. That is, the TDPR MAPPER was in the process of transmitting a packet when it ran out of data to transmit. UDRI will assert INTB if it is a logic 1 and UDRE is programmed to logic 1. UDRI is cleared when this register is read.

OVRI

The OVRI bit will transition to 1 when the TDPR MAPPER FIFO overruns. That is, the TDPR MAPPER FIFO was already full when another data byte was written to the TDPR MAPPER Transmit Data register. OVRI will assert INTB if it is a logic 1 and OVRE is programmed to logic 1. OVRI is cleared when this register is read.

FULLI

The FULLI bit will transition to logic 1 when the TDPR MAPPER FIFO is full. FULLI will assert INTB if it is a logic 1 and FULLE is programmed to logic 1. FULLI is cleared when this register is read.

BLFILL

The BLFILL bit is set to logic 1 if the current FIFO fill level is below the LINT[7:0] level or is empty.

FULL

The FULL bit reflects the current condition of the TDPR MAPPER FIFO. If FULL is a logic 1, the TDPR MAPPER FIFO already contains 128-bytes of data and can accept no more.

Register 0x13D, 0x53D, 0x133D, 0x173D: TDPR MAPPER Transmit Data

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	TD[7]	X
Bit 6	R/W	TD[6]	X
Bit 5	R/W	TD[5]	X
Bit 4	R/W	TD[4]	X
Bit 3	R/W	TD[3]	X
Bit 2	R/W	TD[2]	X
Bit 1	R/W	TD[1]	X
Bit 0	R/W	TD[0]	X

Consecutive writes to the TDPR MAPPER Configuration, TDPR MAPPER Interrupt Status/UDR Clear, and TDPR MAPPER Transmit Data register and reads of the TDPR MAPPER Interrupt Status/UDR Clear register should not occur at rates greater than 1/96 that of the transmit line clock OCLK.

TD[7:0]

The TD[7:0] bits contain the data to be transmitted on the data link. Data written to this register is serialized and transmitted (TD[0] is transmitted first).

Register 0x140, 0x540, 0x1340, 0x1740: RXFP Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	FCSPASS	0
Bit 5	R/W	RPAINV	0
Bit 4	R/W	FCSSEL[1]	1
Bit 3	R/W	FCSSEL[0]	0
Bit 2	R/W	RXPTYP	0
Bit 1	R/W	DDSCR	1
Bit 0	R/W	FIFORST	0

FIFORST

The FIFORST bit is used to reset the channel 256-byte receive buffer. When FIFORST is set low, the channel buffer operates normally. When FIFORST is set high, the buffer is immediately emptied and ignores writes. The buffer remains empty and continues to ignore writes until a logic zero is written to FIFORST.

See the Operations Section in PMC-2021632 on resetting the receive and transmit FIFOs.

DDSCR

The DDSCR bit controls the descrambling of the frame payload with the polynomial $x^{43} + 1$. When DDSCR is set low, frame payload descrambling is disabled. When DDSCR is set high, payload descrambling is enabled.

DDSCR must be set low when operating in bit-HDLC mode of operation.

RXPTYP

The RXPTYP bit selects even or odd parity for output RPRTY for Level 2 operation. When set high, output RPRTY is the even parity bit for outputs RDAT[15:0]. When RXPTYP is set low, RPRTY is the odd parity bit for outputs RDAT[15:0].

RXPTYP must be set low when the system interface is configured for Level 3 operation.

FCSSEL[1:0]

The Frame Control Sequence select (FCSSEL[1:0]) bits allow to control the FCS calculation according to the table below. The FCS is calculated over the whole packet data, after byte destuffing and descrambling.

Table 32 RXFP FCS Configuration

FCSSEL[1:0]	FCS Operation
00	No FCS calculated
01	CRC-CCITT (2 bytes)
10	CRC-32 (4 bytes)
11	Reserved

RPAINV

The RPAINV bit inverts the polarity of the RPA output signal for Level 2 operation. When RPAINV is a logic one, the polarity of RPA is inverted (RPA at logic zero means there is a receive cell available to be read). When RPAINV is a logic zero, the polarity of RPA is not inverted.

RPAINV must be set low when the system interface is configured for Level 3 operation.

FCSPASS

FCSPASS determines if the FCS field will be passed through the system interface or stripped. When FCSPASS is set to logic one, the POS frame FCS field is written into the FIFO as part of the packet, and can thus be read through the system interface. When FCSPASS is set to logic zero, the FCS field is stripped from the POS frame.

Register 0x141, 0x541, 0x1341, 0x1741: RXFP Configuration/Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	MINLE	0
Bit 4	R/W	MAXLE	0
Bit 3	R/W	ABRTE	0
Bit 2	R/W	FCSE	0
Bit 1	R/W	FOVRE	0
Bit 0	R/W	Reserved	0

FOVRE

The FOVRE bit enables the generation of an interrupt due to a channel buffer overrun error condition. When FOVRE is set high, the pending interrupt in the Interrupt Status Register FOVRI, will deassert INTB. When FOVRE is set to logic 0, the pending interrupt will not deassert INTB.

FCSE

The FCSE bit enables the generation of an interrupt due to the detection of an FCS error. When FCSE is set high, the pending interrupt in the Interrupt Status Register FCSI, will deassert INTB. When FCSE is set to logic 0, the pending interrupt will not deassert INTB.

ABRTE

The Abort Packet Enable bit enables the generation of an interrupt due to the reception of an aborted packet. When ABRTE is set high, the pending interrupt in the Interrupt Status Register ABRTI, will deassert INTB. When ABRTE is set to logic 0, the pending interrupt will not deassert INTB.

MAXLE

The Maximum Length Packet Enable bit enables the generation of an interrupt due to the reception of a packet exceeding the programmable maximum packet length. When MAXLE is set high, the pending interrupt in the Interrupt Status Register MAXLI, will deassert INTB. When MAXLE is set to logic 0, the pending interrupt will not deassert INTB.

MINLE

The Minimum Length Packet Enable bit enables the generation of an interrupt due to the reception of a packet that is smaller than the programmable minimum packet length. When MINLE is set high, the pending interrupt in the Interrupt Status Register MINLI, will deassert INTB. When MINLE is set to logic 0, the pending interrupt will not deassert INTB.

Register 0x142, 0x542, 0x1342, 0x1742: RXFP Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	MINLI	X
Bit 4	R	MAXLI	X
Bit 3	R	ABRTI	X
Bit 2	R	FCSI	X
Bit 1	R	FOVRI	X
Bit 0	—	Unused	X

FOVRI

The FIFO overrun interrupt (FOVRI) bit is an event indicator set to logic 1 to indicate a FIFO overrun error condition. This interrupt status bit is independent of the FOVRE interrupt enable bit. FOVRI is cleared by reading the interrupt status register.

FCSI

The FCS error interrupt (FCSI) bit is an event indicator set to logic 1 to indicate a FCS error condition. This interrupt status bit is independent of the FCSE interrupt enable bit. FCSI is cleared by reading the interrupt status register.

ABRTI

The abort error interrupt (ABRTI) bit is an event indicator set to logic 1 to indicate an aborted packet error condition. This interrupt status bit is independent of the ABRTE interrupt enable bit. ABRTI is cleared by reading the interrupt status register.

MAXLI

The max length error interrupt (MAXLI) bit is an event indicator set to logic 1 to indicate the reception of a packet exceeding the programmable maximum packet length. This interrupt status bit is independent of the MAXLE interrupt enable bit. MAXLI is cleared by reading the interrupt status register.

MINLI

The minimum length error interrupt (MINLI) bit is an event indicator set to logic 1 to indicate the reception of a packet smaller than the programmable minimum packet length. This interrupt status bit is independent of the MINLE interrupt enable bit. MINLI is cleared by reading the interrupt status register.

Register 0x143, 0x543, 0x1343, 0x1743: RXFP Minimum Packet Length

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	MINPL[7]	0
Bit 6	R/W	MINPL[6]	0
Bit 5	R/W	MINPL[5]	0
Bit 4	R/W	MINPL[4]	0
Bit 3	R/W	MINPL[3]	0
Bit 2	R/W	MINPL[2]	1
Bit 1	R/W	MINPL[1]	0
Bit 0	R/W	MINPL[0]	0

MINPL[7:0]

The Minimum Packet Length (MINPL[7:0]) bits are used to set the minimum packet length. Packets smaller than this length are marked with an error. The packet length used here is defined as the number of bytes encapsulated into the POS frame, excluding byte stuffing and FCS bytes.

The minimum packet length supported by the RXFP is 3 bytes (0x03).

Register 0x144, 0x544, 0x1344, 0x1544, 0x1744: RXFP Maximum Packet Length LSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	MAXPL[7]	0
Bit 6	R/W	MAXPL[6]	0
Bit 5	R/W	MAXPL[5]	0
Bit 4	R/W	MAXPL[4]	0
Bit 3	R/W	MAXPL[3]	0
Bit 2	R/W	MAXPL[2]	0
Bit 1	R/W	MAXPL[1]	0
Bit 0	R/W	MAXPL[0]	0

Register 0x145, 0x545, 0x1345, 0x1745: RXFP Maximum Packet Length MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	MAXPL[15]	0
Bit 6	R/W	MAXPL[14]	0
Bit 5	R/W	MAXPL[13]	0
Bit 4	R/W	MAXPL[12]	0
Bit 3	R/W	MAXPL[11]	0
Bit 2	R/W	MAXPL[10]	1
Bit 1	R/W	MAXPL[9]	1
Bit 0	R/W	MAXPL[8]	0

MAXPL[15:0]

The Maximum Packet Length (MAXPL[15:0]) bits are used to set the maximum packet length. Packets larger than this length are marked with an error. The packet length used here is defined as the number of bytes encapsulated into the POS frame, including the FCS but excluding byte stuffing.

The maximum packet length supported by the RXFP is 65534 bytes (0xFFFE).

Register 0x146, 0x546, 0x1346, 0x1746: RXFP Receive Initiation Level

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	1
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	RIL[3]	1
Bit 2	R/W	RIL[2]	1
Bit 1	R/W	RIL[1]	0
Bit 0	R/W	RIL[0]	0

RIL[3:0]

The Reception Initiation Level (RIL[3:0]) bits are used to set the minimum number of bytes that must be available in the FIFO before received packets can be written into it. RIL[3:0] is only used after a FIFO overrun has been detected and FIFO writes have been suspended. This avoids restarting the reception of data too quickly after an overrun condition. If the system does not cause any FIFO overrun, then this register will not be used. RIL[3:0] breaks the FIFO in 16 Sections; for example a value of 0x4 correspond to a FIFO level of 64 bytes. The value of RIL must not be too large in order to prevent repetitive FIFO overruns and must not be programmed to zero.

Table 33 RXFP Receive Initiation Level Values

RIL[3:0]	FIFO Fill Level
0000	0
0001	16
0010	32
0011	48
0100	64
0101	80
0110	96
0111	112

RIL[3:0]	FIFO Fill Level
1000	128
1001	144
1010	160
1011	176
1100	192
1101	208
1110	224
1111	240

Reserved

All reserved bits must be programmed to default values for proper operation.

Register 0x147, 0x547, 0x1347, 0x1747: RXFP Receive Packet Available High Water Mark

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	RPAHWM[7]	0
Bit 6	R/W	RPAHWM[6]	1
Bit 5	R/W	RPAHWM[5]	0
Bit 4	R/W	RPAHWM[4]	0
Bit 3	R/W	RPAHWM[3]	0
Bit 2	R/W	RPAHWM[2]	0
Bit 1	R/W	RPAHWM[1]	0
Bit 0	R/W	RPAHWM[0]	0

RPAHWM[7:0]

The Receive FIFO High Water Mark (RPAHWM[7:0]) bits are used to generate the RPA output in POS-PHY interface. RPA is set to logic one when the number of bytes stored in the FIFO exceeds RPAHWM[7:0] or when there is at least one end of packet in the FIFO. The RPAHWM value is used to determine when data is transferred on the POS-PHY interface.

The programmed value for RPAHWM[7:0] must be less than 0xF0 and greater than 0x00 for proper operation.

When a packet with less than 6 bytes arrives (from the line side), the receive packet available signal (RPA) may assert before data is available. In this condition, RPA will assert between 1 to 3 RFCLK clock cycles before the data is available and will remain asserted for 1 to 3 RFCLK clock cycles. When the Link Layer device attempts to read the packet by asserting read enable (RENB), it may find that there is no valid data available (receive data valid signal (RVAL) remains deasserted). RPA will correctly assert again later when data is available. At this time the RVAL signal will be asserted indicating valid data.

With packets greater than 6 bytes, the RPA signal will assert, deassert and then reassert 1 to 3 RFCLK cycles later (same as the above case with packets less than 6 bytes). However, if the Link layer device attempts to read the packet on the basis of the first occurrence of RPA, it will read valid data (RVAL will be asserted), even if RPA may be deasserted.

This early assertion of RPA will not cause any data corruption if RVAL is used to qualify the data that is read. It is recommended that RVAL always be used to qualify receive data. The operation of RPA may cause a slight reduction of bandwidth on receive side of the POS-PHY interface. However, since there is ample bandwidth on the POS-PHY interface there will be no impact on performance of functionality.

Register 0x148, 0x548, 0x1348, 0x1748: RXFP Receive Byte Count LSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	RBYTE[7]	X
Bit 6	R	RBYTE[6]	X
Bit 5	R	RBYTE[5]	X
Bit 4	R	RBYTE[4]	X
Bit 3	R	RBYTE[3]	X
Bit 2	R	RBYTE[2]	X
Bit 1	R	RBYTE[1]	X
Bit 0	R	RBYTE[0]	X

Register 0x149, 0x549, 0x1349, 0x1749: RXFP Receive Byte Counter

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	RBYTE[15]	X
Bit 6	R	RBYTE[14]	X
Bit 5	R	RBYTE[13]	X
Bit 4	R	RBYTE[12]	X
Bit 3	R	RBYTE[11]	X
Bit 2	R	RBYTE[10]	X
Bit 1	R	RBYTE[9]	X
Bit 0	R	RBYTE[8]	X

Register 0x14A, 0x54A, 0x134A, 0x174A: RXFP Receive Byte Counter

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	RBYTE[23]	X
Bit 6	R	RBYTE[22]	X
Bit 5	R	RBYTE[21]	X
Bit 4	R	RBYTE[20]	X
Bit 3	R	RBYTE[19]	X
Bit 2	R	RBYTE[18]	X
Bit 1	R	RBYTE[17]	X
Bit 0	R	RBYTE[16]	X

Register 0x14B, 0x54B, 0x134B, 0x174B: RXFP Receive Byte Count MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	RBYTE[31]	X
Bit 6	R	RBYTE[30]	X
Bit 5	R	RBYTE[29]	X
Bit 4	R	RBYTE[28]	X
Bit 3	R	RBYTE[27]	X
Bit 2	R	RBYTE[26]	X
Bit 1	R	RBYTE[25]	X
Bit 0	R	RBYTE[24]	X

RBYTE[31:0]

The RBYTE[31:0] bits indicate the number of received bytes written into the receive FIFO during the last accumulation interval. This counter does not count any byte from errored and aborted frames. A write to any one of the RXFP Receive Byte Counter registers loads the registers with the current counter value and resets the internal counter to zero.

This counter (and all other counters in the RXFP) is polled by writing to any of the RXFP counter registers (channel address 0x148 to 0x156) or to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800). Such a write transfers the internally accumulated count to the RBYTE Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 0x14C, 0x54C, 0x134C, 0x174C: RXFP Receive Frame Count LSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	RFRAME[7]	X
Bit 6	R	RFRAME[6]	X
Bit 5	R	RFRAME[5]	X
Bit 4	R	RFRAME[4]	X
Bit 3	R	RFRAME[3]	X
Bit 2	R	RFRAME[2]	X
Bit 1	R	RFRAME[1]	X
Bit 0	R	RFRAME[0]	X

Register 0x14D, 0x54D, 0x134D, 0x174D: RXFP Receive Frame Count

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	RFRAME[15]	X
Bit 6	R	RFRAME[14]	X
Bit 5	R	RFRAME[13]	X
Bit 4	R	RFRAME[12]	X
Bit 3	R	RFRAME[11]	X
Bit 2	R	RFRAME[10]	X
Bit 1	R	RFRAME[9]	X
Bit 0	R	RFRAME[8]	X

Register 0x14E, 0x54E, 0x134E, 0x174E: RXFP Receive Frame Count MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	RFRAME[23]	X
Bit 6	R	RFRAME[22]	X
Bit 5	R	RFRAME[21]	X
Bit 4	R	RFRAME[20]	X
Bit 3	R	RFRAME[19]	X
Bit 2	R	RFRAME[18]	X
Bit 1	R	RFRAME[17]	X
Bit 0	R	RFRAME[16]	X

RFRAME[23:0]

The RFRAME[23:0] bits indicate the number of successfully received POS frames written into the receive FIFO after their extraction from the SONET/SDH stream during the last accumulation interval. This counter does not count any errored and aborted frames.

This counter (and all other counters in the RXFP) is polled by writing to any of the RXFP counter registers (channel address 0x148 to 0x156) or to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800). Such a write transfers the internally accumulated count to the RFRAME Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 0x14F, 0x54F, 0x134F, 0x174F: RXFP Receive Aborted Frame Count LSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	RABRF[7]	X
Bit 6	R	RABRF[6]	X
Bit 5	R	RABRF[5]	X
Bit 4	R	RABRF[4]	X
Bit 3	R	RABRF[3]	X
Bit 2	R	RABRF[2]	X
Bit 1	R	RABRF[1]	X
Bit 0	R	RABRF[0]	X

Register 0x150, 0x550, 0x1350, 0x1750: RXFP Receive Aborted Frame Count MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	RABRF[15]	X
Bit 6	R	RABRF[14]	X
Bit 5	R	RABRF[13]	X
Bit 4	R	RABRF[12]	X
Bit 3	R	RABRF[11]	X
Bit 2	R	RABRF[10]	X
Bit 1	R	RABRF[9]	X
Bit 0	R	RABRF[8]	X

RABRF[15:0]

The RABRF[15:0] bits indicate the number of aborted POS frames received and written into the receive FIFO during the last accumulation interval.

This counter (and all other counters in the RXFP) is polled by writing to any of the RXFP counter registers (channel address 0x148 to 0x156) or to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800). Such a write transfers the internally accumulated count to the RABRF Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 0x151, 0x551, 0x1351, 0x1751: RXFP Receive FCS Error Frame Count LSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	RFCSEF[7]	X
Bit 6	R	RFCSEF[6]	X
Bit 5	R	RFCSEF[5]	X
Bit 4	R	RFCSEF[4]	X
Bit 3	R	RFCSEF[3]	X
Bit 2	R	RFCSEF[2]	X
Bit 1	R	RFCSEF[1]	X
Bit 0	R	RFCSEF[0]	X

Register 0x152, 0x552, 0x1352, 0x1752: RXFP Receive FCS Error Frame Count MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	RFCSEF[15]	X
Bit 6	R	RFCSEF[14]	X
Bit 5	R	RFCSEF[13]	X
Bit 4	R	RFCSEF[12]	X
Bit 3	R	RFCSEF[11]	X
Bit 2	R	RFCSEF[10]	X
Bit 1	R	RFCSEF[9]	X
Bit 0	R	RFCSEF[8]	X

RFCSEF[15:0]

The RFCSEF[15:0] bits indicate the number of POS frames received with an FCS error and written into the receive FIFO during the last accumulation interval.

This counter (and all other counters in the RXFP) is polled by writing to any of the RXFP counter registers (channel address 0x148 to 0x156) or to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800). Such a write transfers the internally accumulated count to the RFCSEF Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 0x153, 0x553, 0x1353, 0x1753: RXFP Receive Minimum Length Error Frame Count LSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	RMINLF[7]	X
Bit 6	R	RMINLF[6]	X
Bit 5	R	RMINLF[5]	X
Bit 4	R	RMINLF[4]	X
Bit 3	R	RMINLF[3]	X
Bit 2	R	RMINLF[2]	X
Bit 1	R	RMINLF[1]	X
Bit 0	R	RMINLF[0]	X

Register 0x154, 0x554, 0x1354, 0x1754: RXFP Receive Minimum Length Error Frame Count MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	RMINLF[15]	X
Bit 6	R	RMINLF[14]	X
Bit 5	R	RMINLF[13]	X
Bit 4	R	RMINLF[12]	X
Bit 3	R	RMINLF[11]	X
Bit 2	R	RMINLF[10]	X
Bit 1	R	RMINLF[9]	X
Bit 0	R	RMINLF[8]	X

RMINLF[15:0]

The RMINLF[15:0] bits indicate the number of minimum packet length POS frames received and written into the receive FIFO during the last accumulation interval.

This counter (and all other counters in the RXFP) is polled by writing to any of the RXFP counter registers (channel address 0x148 to 0x156) or to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800). Such a write transfers the internally accumulated count to the RMINLF Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 0x155, 0x555, 0x1355, 0x1755: RXFP Receive Maximum Length Error Frame Count LSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	RMAXLF[7]	X
Bit 6	R	RMAXLF[6]	X
Bit 5	R	RMAXLF[5]	X
Bit 4	R	RMAXLF[4]	X
Bit 3	R	RMAXLF[3]	X
Bit 2	R	RMAXLF[2]	X
Bit 1	R	RMAXLF[1]	X
Bit 0	R	RMAXLF[0]	X

Register 0x156, 0x556, 0x1354, 0x1756: RXFP Receive Maximum Length Error Frame Count MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	RMAXLF[15]	X
Bit 6	R	RMAXLF[14]	X
Bit 5	R	RMAXLF[13]	X
Bit 4	R	RMAXLF[12]	X
Bit 3	R	RMAXLF[11]	X
Bit 2	R	RMAXLF[10]	X
Bit 1	R	RMAXLF[9]	X
Bit 0	R	RMAXLF[8]	X

RMAXLF[15:0]

The RMAXLF[15:0] bits indicate the number of POS frames exceeding the maximum packet length that were received and written into the receive FIFO during the last accumulation interval.

This counter (and all other counters in the RXFP) is polled by writing to any of the RXFP counter registers (channel address 0x148 to 0x156) or to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800). Such a write transfers the internally accumulated count to the RMAXLF Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 0x160, 0x560, 0x1360, 0x1760: TXFP Interrupt Enable/Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	—	Unused	X
Bit 5	R/W	FUDRE	0
Bit 4	R	FUDRI	X
Bit 3	R/W	FOVRE	0
Bit 2	R	FOVRI	X
Bit 1	R/W	TPRTYE	0
Bit 0	R	TPRTYIR	X

TPRTYI

The transmit parity error interrupt (TPRTYI) bit is an event indicator set to logic 1 to indicate a transmit parity error condition on the TDAT[15:0[system interface bus. Odd or even parity is selected using the TPTYP bit (channel address 0x161). This interrupt status bit is independent of the TPRTYE interrupt enable bit. TPRTYI is cleared by reading the interrupt status register.

TPRTYE

The transmit parity error enable bit enables the generation of an interrupt due to a transmit parity error condition on the TDAT[15:0] system interface bus. When set to logic one, the pending interrupt in the Interrupt Status Register TPRTYI, will deassert INTB. When TPRTYE is set to logic 0, the pending interrupt will not deassert INTB.

FOVRI

The FIFO overrun interrupt (FOVRI) bit is an event indicator set to logic 1 to indicate a FIFO overrun error condition. This interrupt status bit is independent of the FOVRE interrupt enable bit. FOVRI is cleared by reading the interrupt status register.

FOVRE

The FOVRE bit enables the generation of an interrupt due to a channel buffer overrun error condition. When FOVRE is set high, the pending interrupt in the Interrupt Status Register FOVRI, will deassert INTB. When FOVRE is set to logic 0, the pending interrupt will not deassert INTB.

FUDRI

The FIFO underrun interrupt (FUDRI) bit is an event indicator set to logic 1 to indicate a FIFO underrun error condition. This interrupt status bit is independent of the FUDRE interrupt enable bit. FUDRI is cleared by reading the interrupt status register.

When TXFP underruns, the programmed TIL[3:0] is not respected for back-to-back packet transfer (i.e. must transmit at least 4 flags before starting next packet). Hence it is recommended that upon detection of TXFP underrun the violating Level 2 and Level 3 channel FIFOs be reset.

FUDRE

The FUDRE bit enables the generation of an interrupt due to a channel buffer underrun error condition. When FUDRE is set high, the pending interrupt in the Interrupt Status Register FUDRI, will deassert INTB. When FUDRE is set to logic 0, the pending interrupt will not deassert INTB.

Register 0x161, 0x561, 0x1361, 0x1761: TXFP Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	XOFF	0
Bit 6	R/W	TPAINV	0
Bit 5	R/W	FCSERR	0
Bit 4	R/W	FCSSEL[1]	1
Bit 3	R/W	FCSSEL[0]	0
Bit 2	R/W	TPTYP	0
Bit 1	R/W	DSCR	1
Bit 0	R/W	FIFORST	0

FIFORST

The FIFORST bit is used to reset the 256-byte transmit channel buffer. When FIFORST is set to logic zero, the channel buffer operates normally. When FIFORST is set to logic one, the buffer is emptied of all octets (including the current packet being transmitted) and ignores writes. The buffer remains empty and continues to ignore writes until a logic zero is written to FIFORST. Flags are transmitted until a subsequent packet is written to the FIFO.

See the Operations Section in PMC-2021632 on resetting the receive and transmit FIFOs.

DSCR

The DSCR bit controls the scrambling of the POS frames. When DSCR is a logic one, scrambling is enabled. When DSCR is a logic zero, payload scrambling is disabled.

DSCR must be set low when configured for bit-HDLC mode of operation.

TPTYP

The TPTYP bit selects even or odd parity for input TPRTY for Level 2 operation. When set to logic one, the TPRTY input must report even parity for the TDAT[15:0] system interface bus. When set to logic zero, input TPRTY must report odd parity for the TDAT[15:0] bus.

TPTYP must be set low when the system interface is configured for Level 3 operation.

FCSSEL[1:0]

The Frame Control Sequence select (FCSSEL[1:0]) bits control the FCS calculation according to the table below. The FCS is calculated over the whole packet data, before byte stuffing and scrambling.

FCSSEL[1:0]	FCS Operation
00	No FCS inserted
01	CRC-CCITT (2 bytes)
10	CRC-32 (4 bytes)
11	Reserved

FCSERR

The FCSERR bit controls the insertion of FCS errors for diagnostic purposes. When FCSERR is set to logic one, if FCS insertion is enabled, the FCS octets are inverted prior to insertion in the POS frame. When FCSERR is set low, the FCS is inserted normally.

TPAINV

The TPAINV bit inverts the polarity of the TPA output signal for Level 2 operation. When TPAINV is a logic one, the polarity of TPA is inverted. When TPAINV is a logic zero, TPA operates normally.

TPAINV must be set low when the system interface is configured for Level 3 operation.

XOFF

The XOFF serves as a transmission enable bit. When XOFF is set to logic zero, POS frames are transmitted normally. When XOFF is set to logic one, the current frame being transmitted is completed and then POS frame transmission is suspended. When XOFF is asserted the FIFO still accepts data and can overflow. XOFF is provided to facilitate system debugging rather than flow control. This bit should not be changed on the fly for flow control purposes.

Register 0x162, 0x562, 0x1362, 0x1762: TXFP Control

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	IPGAP[3]	0
Bit 6	R/W	IPGAP[2]	0
Bit 5	R/W	IPGAP[1]	1
Bit 4	R/W	IPGAP[0]	0
Bit 3	R/W	TIL[3]	0
Bit 2	R/W	TIL[2]	1
Bit 1	R/W	TIL[1]	0
Bit 0	R/W	TIL[0]	0

TIL[3:0]

The Transmit Initiation Level (TIL[3:0]) bits are used to determine when to initiate a POS frame transmission. After the channel buffer is emptied, data transmission starts only when either there is a complete packet or when the number of bytes stored in the channel buffer exceeds the value of TIL[3:0] times 16.

Once initiated, the transmission will continue until the packet is transmitted or an underrun occurs. Before starting another packet, a complete packet must be in the channel buffer or the buffer fill level must exceed the level specified by TIL[3:0]. When TXFP underruns, the programmed TIL[3:0] is not respected for back-to-back packet transfer (i.e. must transmit at least 4 flags before starting next packet). Hence it is recommended that upon detection of TXFP underrun the violating Level 2 and Level 3 channel FIFOs be reset.

Table 34 TXFP Transmit Initiation Level Values

TIL[3:0]	FIFO Fill Level
0000	0
0001	16
0010	32
0011	48
0100	64
0101	80
0110	96
0111	112

TIL[3:0]	FIFO Fill Level
1000	128
1001	144
1010	160
1011	176
1100	192
1101	208
1110	224
1111	240

IPGAP[3:0]

The Inter Packet Gaping (IPGAP[3:0]) bits are used to program the number of Flag Sequence characters inserted between each POS Frame. These bits cannot be dynamically modified. The programmed value is encoded as indicated in Table 35.

Table 35 TXFP Inter Packet Gaping Values

IPGAP[3:0]	Number of Flags
0000	1
0001	2
0010	4
0011	8
0100	16
0101	32
0110	64
0111	128

IPGAP[3:0]	Number of Flags
1000	256
1001	512
1010	1024
1011	2048
1100	4096
1101	8192
1110	16384
1111	32768

Register 0x163, 0x563, 0x1363, 0x1763: TXFP Transmit Packet Available Low Water Mark

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	TPALWM[7]	0
Bit 6	R/W	TPALWM[6]	1
Bit 5	R/W	TPALWM[5]	0
Bit 4	R/W	TPALWM[4]	0
Bit 3	R/W	TPALWM[3]	0
Bit 2	R/W	TPALWM[2]	0
Bit 1	R/W	TPALWM[1]	0
Bit 0	R/W	TPALWM[0]	0

TPALWM[7:0]

The Transmit FIFO Low Water Mark (TPALWM[7:0]) bits are used to generate the TPA output in POS-PHY interface. Due to internal pipeline delay, the TPA output may not assert until the FIFO level has dropped a maximum of 16 bytes below the value specified by TPALWM.

The programmed value for TPALWM[7:0] must not be less than 0x0F for proper operation.

For Level 2 system interfaces, TPA is set to logic one when the number of bytes stored in the FIFO is lower than TPALWM[7:0].

For Level 3 system interfaces, TPA is set to logic one when the number of bytes sorted in the FIFO is lower than TPALWM[7:0] plus 2 bytes.

ENG: Register 0x164, 0x564, 0x1364, 0x1764: TXFP Transmit Packet Available High Water Mark

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	TPAHWM[7]	1
Bit 6	R/W	TPAHWM[6]	1
Bit 5	R/W	TPAHWM[5]	1
Bit 4	R/W	TPAHWM[4]	1
Bit 3	R/W	TPAHWM[3]	0
Bit 2	R/W	TPAHWM[2]	0
Bit 1	R/W	TPAHWM[1]	0
Bit 0	R/W	TPAHWM[0]	0

TPAHWM[7:0]

The Transmit FIFO High Water Mark (TPAHWM[7:0]) bits are used to generate the TPA output. Due to internal pipeline delay, the TPA output may not deassert until the FIFO level has raised a maximum of 8 bytes above the value specified by TPAHWM.

The programmed value for TPAHWM[7:0] must not be greater than 0xF0 for proper operation.

For Level 2 system interfaces, TPA is set to logic zero when the number of bytes stored in the FIFO exceeds TPAHWM[7:0].

For Level 3 system interfaces, TPA is set to logic zero when the number of bytes stored in the FIFO exceeds TPAHWM[7:0] less four bytes.

Register 0x165, 0x565, 0x1365, 0x1765: TXFP Transmit Byte Count LSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	TBYTE[7]	X
Bit 6	R	TBYTE[6]	X
Bit 5	R	TBYTE[5]	X
Bit 4	R	TBYTE[4]	X
Bit 3	R	TBYTE[3]	X
Bit 2	R	TBYTE[2]	X
Bit 1	R	TBYTE[1]	X
Bit 0	R	TBYTE[0]	X

Register 0x166, 0x566, 0x1366, 0x1766: TXFP Transmit Byte Count

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	TBYTE[15]	X
Bit 6	R	TBYTE[14]	X
Bit 5	R	TBYTE[13]	X
Bit 4	R	TBYTE[12]	X
Bit 3	R	TBYTE[11]	X
Bit 2	R	TBYTE[10]	X
Bit 1	R	TBYTE[9]	X
Bit 0	R	TBYTE[8]	X

Register 0x167, 0x567, 0x1367, 0x1767: TXFP Transmit Byte Count

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	TBYTE[23]	X
Bit 6	R	TBYTE[22]	X
Bit 5	R	TBYTE[21]	X
Bit 4	R	TBYTE[20]	X
Bit 3	R	TBYTE[19]	X
Bit 2	R	TBYTE[18]	X
Bit 1	R	TBYTE[17]	X
Bit 0	R	TBYTE[16]	X

Register 0x168, 0x568, 0x1368, 0x1768: TXFP Transmit Byte Count MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	TBYTE[31]	X
Bit 6	R	TBYTE[30]	X
Bit 5	R	TBYTE[29]	X
Bit 4	R	TBYTE[28]	X
Bit 3	R	TBYTE[27]	X
Bit 2	R	TBYTE[26]	X
Bit 1	R	TBYTE[25]	X
Bit 0	R	TBYTE[24]	X

TBYTE[31:0]

The TBYTE[31:0] bits indicate the number of bytes read from the transmit FIFO and transmitted during the last accumulation interval. This counter does not count bytes within aborted frames.

This counter (and all other counters in the TXFP) is polled by writing to any of the TXFP counter registers (channel addresses 0x166 to 0x16F) or to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800). Such a write transfers the internally accumulated count to the TBYTE Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 0x169, 0x569, 0x1369, 0x1769: TXFP Transmit Frame Count LSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	TFRAME[7]	X
Bit 6	R	TFRAME[6]	X
Bit 5	R	TFRAME[5]	X
Bit 4	R	TFRAME[4]	X
Bit 3	R	TFRAME[3]	X
Bit 2	R	TFRAME[2]	X
Bit 1	R	TFRAME[1]	X
Bit 0	R	TFRAME[0]	X

Register 0x16A, 0x56A, 0x136A, 0x176A: TXFP Transmit Frame Count

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	TFRAME[15]	X
Bit 6	R	TFRAME[14]	X
Bit 5	R	TFRAME[13]	X
Bit 4	R	TFRAME[12]	X
Bit 3	R	TFRAME[11]	X
Bit 2	R	TFRAME[10]	X
Bit 1	R	TFRAME[9]	X
Bit 0	R	TFRAME[8]	X

Register 0x16B, 0x56B, 0x136B, 0x176B: TXFP Transmit Frame Count MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	TFRAME[23]	X
Bit 6	R	TFRAME[22]	X
Bit 5	R	TFRAME[21]	X
Bit 4	R	TFRAME[20]	X
Bit 3	R	TFRAME[19]	X
Bit 2	R	TFRAME[18]	X
Bit 1	R	TFRAME[17]	X
Bit 0	R	TFRAME[16]	X

TFRAME[23:0]

The TFRAME[23:0] bits indicate the number of POS frames read from the transmit FIFO and inserted into the transmission stream during the last accumulation interval. This counter does not count aborted frames.

This counter (and all other counters in the TXFP) is polled by writing to any of the TXFP counter registers (channel addresses 0x166 to 0x16F) or to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800). Such a write transfers the internally accumulated count to the TFRAME Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 0x16C, 0x56C, 0x136C, 0x176C: TXFP Transmit User Aborted Frame Count LSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	TUSRABF[7]	X
Bit 6	R	TUSRABF[6]	X
Bit 5	R	TUSRABF[5]	X
Bit 4	R	TUSRABF[4]	X
Bit 3	R	TUSRABF[3]	X
Bit 2	R	TUSRABF[2]	X
Bit 1	R	TUSRABF[1]	X
Bit 0	R	TUSRABF[0]	X

Register 0x16D, 0x56D, 0x136D, 0x176D: TXFP Transmit User Aborted Frame Count MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	TUSRABF[15]	X
Bit 6	R	TUSRABF[14]	X
Bit 5	R	TUSRABF[13]	X
Bit 4	R	TUSRABF[12]	X
Bit 3	R	TUSRABF[11]	X
Bit 2	R	TUSRABF[10]	X
Bit 1	R	TUSRABF[9]	X
Bit 0	R	TUSRABF[8]	X

TUSRABF[15:0]

The TUSRABF[15:0] bits indicate the number of user aborted POS frames read from the transmit FIFO and inserted into the transmission stream during the last accumulation interval. User can abort frames by asserting TERR.

In level 3 operation, when the TUL3 FIFO is overrun, the corrupted packet is market as errored. When this errored packet is transmitted with the HDLC abort sequence, the TUSRABF count in the TXFP will be incremented. The TXFP cannot distinguish between a user aborted packet and a packet aborted by the TUL3.

This counter (and all other counters in the TXFP) is polled by writing to any of the TXFP counter registers (channel addresses 0x166 to 0x16F) or to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800). Such a write transfers the internally accumulated count to the TUSRABF Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 0x16E, 0x56E, 0x136E, 0x176E: TXFP Transmit Underrun/Error Aborted Frame Count LSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	TFERABF[7]	X
Bit 6	R	TFERABF[6]	X
Bit 5	R	TFERABF[5]	X
Bit 4	R	TFERABF[4]	X
Bit 3	R	TFERABF[3]	X
Bit 2	R	TFERABF[2]	X
Bit 1	R	TFERABF[1]	X
Bit 0	R	TFERABF[0]	X

Register 0x16F, 0x56F, 0x136F, 0x176F: TXFP Transmit Underrun/Error Aborted Frame Count MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	TFERABF[15]	X
Bit 6	R	TFERABF[14]	X
Bit 5	R	TFERABF[13]	X
Bit 4	R	TFERABF[12]	X
Bit 3	R	TFERABF[11]	X
Bit 2	R	TFERABF[10]	X
Bit 1	R	TFERABF[9]	X
Bit 0	R	TFERABF[8]	X

TFERABF[15:0]

The TFERABF[15:0] bits indicate the number of FIFO underrun error aborted POS frames read from the transmit FIFO and inserted into the transmission stream during the last accumulation interval. FIFO underruns errors are caused when the FIFO runs empty and the last byte read was not an end of packet or also when the FIFO overruns and corrupts the end of packet/start of packet sequence (example: when another RSOP is high when expecting an REOP). This is considered a system error and should not occur when the system works normally.

This counter (and all other counters in the TXFP) is polled by writing to any of the TXFP counter registers (channel addresses 0x166 to 0x16F) or to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800). Such a write transfers the internally accumulated count to the TFERABF Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 0x170, 0x570, 0x1370, 0x1770: PMON AUX Change of PMON AUX Performance Meters

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R	FERRCH	X
Bit 3	—	Unused	X
Bit 2	R	PERRCH	X
Bit 1	R	CPERRCH	X
Bit 0	R	FEBECH	X

FEBECH

The FEBECH bit is set to logic 1 if one or more FEBE events have occurred in FRMR AUX during the latest PMON AUX accumulation interval.

CPERRCH

The CPERRCH bit is set to logic 1 if one or more path parity error events (or E3 frame error events when E3 G. 832 framing format is selected) have occurred in FRMR AUX during the latest PMON AUX accumulation interval.

PERRCH

The PERRCH bit is set to logic 1 if one or more parity error events (or J2 CRC-5 errors) have occurred in FRMR AUX during the latest PMON AUX accumulation interval.

FERRCH

The FERRCH bit is set to logic 1 if one or more F-bit or M-bit error events have occurred in FRMR AUX during the latest PMON AUX accumulation interval.

Register 0x171, 0x571, 0x1371, 0x1771: PMON AUX Interrupt Enable/Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	INTE	0
Bit 1	R	INTR	X
Bit 0	R	OVR	X

OVR

The OVR bit indicates the overrun status of the PMON AUX holding registers. A logic 1 in this bit position indicates that a previous interrupt has not been cleared before the end of the next accumulation interval, and that the contents of the holding registers have been overwritten. A logic 0 indicates that no overrun has occurred. This bit is reset to logic 0 when this register is read.

INTR

The INTR bit indicates the current status of the interrupt signal. A logic 1 in this bit position indicates that a transfer of counter values to the holding registers has occurred; a logic 0 indicates that no transfer has occurred. The INTR bit is set to logic 0 when this register is read.

INTE

The INTE bit enables the generation of an interrupt when the PMON AUX counter values are transferred to the holding registers. When a logic 1 is written to INTE, the interrupt generation is enabled.

Register 0x176, 0x576, 0x1376, 0x1776: PMON AUX Framing Bit Error Event Count LSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	FERR[7]	X
Bit 6	R	FERR[6]	X
Bit 5	R	FERR[5]	X
Bit 4	R	FERR[4]	X
Bit 3	R	FERR[3]	X
Bit 2	R	FERR[2]	X
Bit 1	R	FERR[1]	X
Bit 0	R	FERR[0]	X

Register 0x177, 0x577, 0x1377, 0x1777: PMON AUX Framing Bit Error Event Count MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R	FERR[9]	X
Bit 0	R	FERR[8]	X

FERR[9:0]

FERR[9:0] represents the number of DS3 F-bit and M-bit errors, or E3 or J2 framing pattern errors, that have been detected by the FRMR AUX since the last time the framing error counter was polled. This counter is paused when the corresponding framer has lost frame alignment.

This counter (and all other counters in the PMON AUX) is polled by writing to any of the PMON AUX counter registers (channel addresses 0x174 to 0x17F) or to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800). Such a write transfers the internally accumulated count to the FERR Error Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 0x17A, 0x57A, 0x137A, 0x177A: PMON AUX Parity Error Event Count LSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	PERR[7]	X
Bit 6	R	PERR[6]	X
Bit 5	R	PERR[5]	X
Bit 4	R	PERR[4]	X
Bit 3	R	PERR[3]	X
Bit 2	R	PERR[2]	X
Bit 1	R	PERR[1]	X
Bit 0	R	PERR[0]	X

Register 0x17B, 0x57B, 0x137B, 0x177B: PMON AUX Parity Error Event Count MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	PERR[15]	X
Bit 6	R	PERR[14]	X
Bit 5	R	PERR[13]	X
Bit 4	R	PERR[12]	X
Bit 3	R	PERR[11]	X
Bit 2	R	PERR[10]	X
Bit 1	R	PERR[9]	X
Bit 0	R	PERR[8]	X

PERR[15:0]

PERR[15:0] represents the number of DS3 P-bit errors, the number of E3 G.832 BIP-8 errors or the number of J2 CRC-5 errors that have been detected by the FRMR AUX since the last time the parity error counter was polled.

This counter (and all other counters in the PMON AUX) is polled by writing to any of the PMON AUX counter registers (channel addresses 0x174 to 0x17F) or to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800). Such a write transfers the internally accumulated count to the PERR Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. This counter is paused when the corresponding framer has lost frame alignment.

Register 0x17C, 0x57C, 0x137C, 0x177C: PMON AUX Path Parity Error/E3-FRMERR Event Count LSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	CPERR/ FRMERR[7]	X
Bit 6	R	CPERR/ FRMERR[6]	X
Bit 5	R	CPERR/ FRMERR[5]	X
Bit 4	R	CPERR/ FRMERR[4]	X
Bit 3	R	CPERR/ FRMERR[3]	X
Bit 2	R	CPERR/ FRMERR[2]	X
Bit 1	R	CPERR/ FRMERR[1]	X
Bit 0	R	CPERR/ FRMERR[0]	X

Register 0x17D, 0x57D, 0x137D, 0x177D: PMON AUX Path Parity Error/E3-FRMERR Event Count MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	CPERR/ FRMERR[13]	X
Bit 4	R	CPERR/ FRMERR[12]	X
Bit 3	R	CPERR/ FRMERR[11]	X
Bit 2	R	CPERR/ FRMERR[10]	X
Bit 1	R	CPERR/ FRMERR[9]	X
Bit 0	R	CPERR/ FRMERR[8]	X

CPERR/FRMERR[13:0]

CPERR/FRMERR[13:0] represents the number of DS3 path parity errors, or E3 G.832 frame errors that have been detected by the FRMR AUX since the last time the parity/frame error counter was polled. This counter is forced to zero when configured for J2 applications. This counter is paused when the corresponding framer has lost frame alignment.

This counter (and all other counters in the PMON AUX) is polled by writing to any of the PMON AUX counter registers (channel addresses 0x174 to 0x17F) or to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800). Such a write transfers the internally accumulated count to the CPERR Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 0x17E, 0x57E, 0x137E, 0x177E: PMON AUX FEBE Event Count LSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register 0x17F, 0x57F, 0x137F, 0x177F: PMON AUX FEBE Event Count MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	FEBE[13]	X
Bit 4	R	FEBE[12]	X
Bit 3	R	FEBE[11]	X
Bit 2	R	FEBE[10]	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

FEBE[13:0]

FEBE[13:0] represents the number of DS3 or E3 G.832 far end block errors that have been detected by the FRMR AUX since the last time the FEBE error counter was polled. This counter is paused when the corresponding framer has lost frame alignment.

This counter (and all other counters in the PMON AUX) is polled by writing to any of the PMON AUX counter registers (channel addresses 0x174 to 0x17F) or to the Channel Reset and Performance Monitor Update register (channel address 0x006) or to the S/UNI 4xJET Master Reset and Identity register (address 0x1800). Such a write transfers the internally accumulated count to the FEBE Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 0x180, 0x580, 0x1380, 0x1780: DS3 FRMR AUX Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	AISPAT	1
Bit 6	R/W	FDET	0
Bit 5	R/W	MBDIS	0
Bit 4	R/W	M3O8	0
Bit 3	R/W	UNI	0
Bit 2	R/W	REFR	0
Bit 1	R/W	AISC	0
Bit 0	R/W	CBE	0

CBE

The CBE bit enables the DS3 C-bit parity application. When a logic 1 is written to CBE, C-bit parity mode is enabled. When a logic 0 is written to CBE, the DS3 M23 format is selected. While the C-bit parity application is enabled, C-bit parity error events, far end block errors are accumulated.

AISC

The AISC bit controls the algorithm used to detect the alarm indication signal (AIS). When a logic 1 is written to AISC, the algorithm checks that a framed DS3 signal with all C-bits set to logic 0 is observed for a period of time before declaring AIS. The payload contents are checked to the pattern selected by the AISPAT bit. When a logic 0 is written to AISC, the AIS detection algorithm is determined solely by the settings of AISPAT and AISONES register bits (see bit mapping table in the Additional Configuration Register description).

REFR

The REFR bit initiates a DS3 reframe. When a logic 1 is written to REFR, the DS3 FRMR AUX is forced out-of-frame, and a new search for frame alignment is initiated. Note that only a low to high transition of the REFR bit triggers reframing; multiple write operations are required to ensure such a transition.

UNI

UNI must be set to logic 1 for all modes of operation.

M3O8

The M3O8 bit controls the DS3 out of frame decision criteria. When a logic 1 is written to M3O8, DS3 out of frame is declared when 3 of 8 framing bits (F-bits) are in error. When a logic 0 is written to M3O8, the 3 of 16 framing bits in error criteria is used, as recommended in ANSI T1.107.

MBDIS

The MBDIS bit disables the use of M-bit errors as a criteria for losing frame alignment. When MBDIS is set to logic 1, M-bit errors are disabled from causing an OOF; the loss of frame criteria is based solely on the number of F-bit errors selected by the M3O8 bit. When MBDIS is set to logic 0, errors in either M-bits or F-bits are enabled to cause an OOF. When MBDIS is logic 0, an OOF can occur when one or more M-bit errors occur in 3 out of 4 consecutive M-frames, or when the F-bit error ratio selected by the M3O8 bit is exceeded.

FDET

The FDET bit selects the fast detection timing for AIS, IDLE and RED. When FDET is set to logic 1, the AIS, IDLE, and RED detection time is 2.23 ms; when FDET is set to logic 0, the detection time is 13.5 ms.

AISPAT

The AISPAT bit controls the pattern used to detect the alarm indication signal (AIS). When a logic 1 is written to AISPAT, the AIS detection algorithm checks that a framed DS3 signal containing the repeating pattern 1010... is present. The C-bits are checked for the value specified by the AISC bit setting. When a logic 0 is written to AISPAT, the AIS detection algorithm is determined solely by the settings of AISC and AISONES register bits (see bit mapping table in the Additional Configuration Register description).

Register 0x181, 0x581, 0x1381, 0x1781: DS3 FRMR AUX Interrupt Enable (ACE=0)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	COFAE	0
Bit 6	R/W	REDE	0
Bit 5	R/W	CBITE	0
Bit 4	R/W	FERFE	0
Bit 3	R/W	IDLE	0
Bit 2	R/W	AISE	0
Bit 1	R/W	OOFE	0
Bit 0	R/W	Reserved	0

The DS3 FRMR Interrupt Enable register is provided at channel address 181H when the ACE bit in channel address 183H is set to logic 0.

OOFE

The OOFE bit enables interrupt generation when a DS3 out of frame defect is declared or removed. The interrupt is enabled when a logic 1 is written.

AISE

The AISE bit enables interrupt generation when the DS3 AIS maintenance signal is detected or removed. The interrupt is enabled when a logic 1 is written.

IDLE

The IDLE bit enables interrupt generation when the DS3 IDLE maintenance signal is detected or removed. The interrupt is enabled when a logic 1 is written.

FERFE

The FERFE bit enables interrupt generation when a DS3 far end receive failure defect is declared or removed. The interrupt is enabled when a logic 1 is written.

CBITE

The CBITE bit enables interrupt generation when the DS3 FRMR AUX detects a change of state in the DS3 application identification channel. The interrupt is enabled when a logic 1 is written.

REDE

The REDE bit enables an interrupt to be generated when a change of state of the DS3 RED indication occurs. The DS3 RED indication is visible in the REDV bit location of the DS3 FRMR AUX Status register. When REDE is set to logic 1, the interrupt output, INTB, is set low when the state of the RED indication changes.

COFAE

The COFAE bit enables interrupt generation when the DS3 FRMR AUX detects a change of frame alignment. The interrupt is enabled when a logic 1 is written.

Register 0x181, 0x581, 0x1381, 0x1781: DS3 FRMR AUX Additional Configuration (ACE=1)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	AISONES	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The DS3 FRMR AUX Additional Configuration register is provided at channel address 181H when the ACE bit in channel address 183H is set to logic 1.

AISONES

The AISONES bit controls the pattern used to detect the alarm indication signal (AIS) when both AISPAT and AISC bits in DS3 FRMR AUX Configuration register are logic 0; if either AISPAT or AISC are logic 1, the AISONES bit is ignored. When a logic 0 is written to AISONES, the algorithm checks that a framed all-ones payload pattern (1111...) signal is observed for a period of time before declaring AIS. Only the payload bits are observed to follow an all-ones pattern, the overhead bits (X, P, M, F, C) are ignored. When a logic 1 is written to AISONES, the algorithm checks that an unframed all-ones pattern (1111...) signal is observed for a period of time before declaring AIS. In this case all the bits, including the overhead, are observed to follow an all-ones pattern. The valid combinations of AISPAT, AISC, and AISONES bits are summarized in Table 36.

Table 36 DS3 FRMR AUX AIS Configurations

AISPAT	AISC	AISONES	AIS Detected
1	0	X	Framed DS3 stream containing repeating 1010… pattern; overhead bits ignored.
0	1	X	Framed DS3 stream containing C-bits all logic 0; payload bits ignored.

AISPAT	AISC	AISONES	AIS Detected
1	1	X	Framed DS3 stream containing repeating 1010… pattern in the payload, C-bits all logic 0, and X-bits=1. This can be detected by setting both AISPAT and AISC high, and declaring AIS only when AISV=1 and FERFV=0 (Register x33).
0	0	0	Framed DS3 stream containing all-ones payload pattern; overhead bits ignored.
0	0	1	Unframed all-ones DS3 stream.

Register 0x182, 0x582, 0x1382, 0x1782: DS3 FRMR AUX Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	COFAI	X
Bit 6	R	REDI	X
Bit 5	R	CBITI	X
Bit 4	R	FERFI	X
Bit 3	R	IDLI	X
Bit 2	R	AISI	X
Bit 1	R	OOFI	X
Bit 0	—	Unused	X

OOFI

The OOFI bit is set to logic 1 when an out of frame defect is detected or removed. The OOFI bit position is set to logic 0 when this register is read.

AISI

The AISI bit is set to logic 1 when the DS3 AIS maintenance signal is detected or removed. The AISI bit position is set to logic 0 when this register is read.

IDLI

The IDLI bit is set to logic 1 when the DS3 IDLE maintenance signal is detected or removed. The IDLI bit position is set to logic 0 when this register is read.

FERFI

The FERFI bit is set to logic 1 when a FERF defect is detected or removed. The FERFI bit position is set to logic 0 when this register is read.

CBITI

The CBITI bit is set to logic 1 when a change of state is detected in the DS3 application identification channel. The CBITI bit position is set to logic 0 when this register is read.

REDI

The REDI bit indicates that a change of state of the DS3 RED indication has occurred. The DS3 RED indication is visible in the REDV bit location of the DS3 FRMR AUX Status register. When the REDI bit is a logic 1, a change in the RED state has occurred. When the REDI bit is logic 0, no change in the RED state has occurred.

COFAI

The COFAI bit is set to logic 1 when a change of frame alignment is detected. A COFA is generated when a new DS3 frame alignment is determined that differs from the last known frame alignment. The COFAI bit position is set to logic 0 when this register is read.

Register 0x183, 0x583, 0x1383, 0x1783: DS3 FRMR AUX Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	ACE	0
Bit 6	R	REDV	X
Bit 5	R	CBITV	X
Bit 4	R	FERFV	X
Bit 3	R	IDLV	X
Bit 2	R	AISV	X
Bit 1	R	OOFV	X
Bit 0	—	Unused	X

OOFV

The OOFV bit indicates the current DS3 out of frame defect state. When the DS3 FRMR AUX has lost frame alignment and is searching for the new alignment, OOFV is set to logic 1. When the DS3 FRMR AUX has found frame alignment, the OOFV bit is set to logic 0.

AISV

The AISV bit indicates the alarm indication signal state. When the DS3 FRMR AUX detects the AIS maintenance signal, AISV is set to logic 1.

IDLV

The IDLV bit indicates the IDLE signal state. When the DS3 FRMR AUX detects the IDLE maintenance signal, IDLV is set to logic 1.

FERFV

The FERFV bit indicates the current far end receive failure defect state. When the DS3 FRMR AUX detects an M-frame with the X1 and X2 bits both set to zero, FERFV is set to logic 1. When the DS3 FRMR AUX detects an M-frame with the X1 and X2 bits both set to one, FERFV is set to logic 0.

CBITV

The CBITV bit indicates the application identification channel (AIC) state. CBITV is set to logic 1 (indicating the presence of the C-bit parity application) when the AIC bit is set high for 63 consecutive M-frames. CBITV is set to logic 0 (indicating the presence of the M23 or SYNTRAN applications) when AIC is set low for 2 or more M-frames in the last 15.

REDV

The REDV bit indicates the current state of the DS3 RED indication. When the REDV bit is a logic 1, the DS3 FRMR AUX frame alignment acquisition circuitry has been out of frame for 2.23 ms (or for 13.5 ms when FDET is logic 0). When the REDV bit is logic 0, the frame alignment circuitry has found frame (i.e. OOFV=0) for 2.23 ms (or 13.5 ms if FDET=0).

ACE

The ACE bit selects the Additional Configuration register. This register is located at channel address 181H, and is only accessible when the ACE bit is set to logic 1. When ACE is set to logic 0, the Interrupt Enable register is accessible at channel address 181H.

Register 0x188, 0x588, 0x1388, 0x1788: E3 FRMR AUX Framing Options

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	UNI	0
Bit 3	R/W	FORMAT[1]	0
Bit 2	R/W	FORMAT[0]	0
Bit 1	R/W	REFRDIS	0
Bit 0	R/W	REFR	0

REFR

A transition from logic 0 to logic 1 in the REFR bit position forces the E3-FFRMR AUX to initiate a search for frame alignment. The bit must be cleared to logic 0, then set to logic 1 again to initiate subsequent searches for frame alignment.

REFRDIS

The REFRDIS bit disables reframing under the consecutive framing bit error condition once frame alignment has been found, leaving reframing to be initiated only by software via the REFR bit. A logic 1 in the REFRDIS bit position causes the FRMR to remain "locked in frame" once initial frame alignment has been found. A logic 0 allows reframing to occur when four consecutive framing patterns are received in error.

FORMAT[1:0]

The FORMAT[1:0] bits determine the framing mode used for pattern matching when finding frame alignment and for generating the output status signals. The FORMAT[1:0] bits select one of two framing formats:

Table 37 E3 FRMR AUX FORMAT[1:0] Configurations

FORMAT[1]	FORMAT[0]	Framing Format Selected
0	0	G.751 E3 format
0	1	G.832 E3 format
1	0	Reserved
1	1	Reserved

UNI

UNI must be set to logic 1 for all modes of operation.

Register 0x189, 0x589, 0x1389, 0x1789: E3 FRMR AUX Maintenance Options

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	WORDBIP	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	WORDERR	0
Bit 2	R/W	PYLD&JUST	0
Bit 1	R/W	FERFDET	0
Bit 0	R/W	TMARKDET	0

TMARKDET

The TMARKDET bit determines the persistency check performed on the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte). When TMARKDET is logic 1, the Timing Marker bit must be in the same state for 5 consecutive frames before the TIMEMK status is changed to that state. When TMARKDET is logic 0, the Timing Marker bit must be in the same state for 3 consecutive frames. When a framing mode other than G.832 is selected, the setting of the TMARKDET bit is ignored.

FERFDET

The FERFDET bit determines the persistency check performed on the Far End Receive Failure (FERF) bit (bit 1 of the G.832 Maintenance and Adaptation byte) or on the Remote Alarm indication (RAI) bit (bit 11 of the frame in G.751 mode). When FERFDET is logic 1, the FERF, or RAI, bit must be in the same state for 5 consecutive frames before the FERF/RAI status is changed to that state. When FERFDET is logic 0, the FERF, or RAI, bit must be in the same state for 3 consecutive frames.

PYLD&JUST

The PYLD&JUST bit selects whether the justification service bits and the tributary justification bits in framing mode G.751 is indicated as overhead or payload. When PYLD&JUST is logic 1, the justification service bits and the tributary justification bits are indicated as payload. When PYLD&JUST is logic 0, the justification service and tributary justification bits are indicated as overhead.

PYLD&JUST must be set to logic 1 when configured for E3 G.751 ATM applications.

WORDERR

The WORDERR bit selects whether the framing bit error indication pulses accumulated in PMON AUX indicate all bit errors in the framing pattern or only one error for one or more errors in the framing pattern. When WORDERR is logic 1, the FERR indication to PMON AUX pulses once per frame, accumulating one error for one or more framing bit errors occurred. When WORDERR is logic 0, the FERR indication to PMON AUX pulses for each and every framing bit error that occurs; PMON AUX accumulates all framing bit errors.

WORDBIP

The WORDBIP bit selects whether the parity bit error indication pulses to the E3-TRAN block indicate all bit errors in the BIP-8 pattern or only one error for one or more errors in the BIP-8 pattern. When WORDBIP is logic 1, the parity error indication to the E3-TRAN block pulses once per frame, indicating that one or more parity bit errors occurred. When WORDBIP is logic 0, the parity error indication to the E3-TRAN block pulses for each and every parity bit error that occurs. For G.832 applications, this bit should be set to logic 1.

Register 0x18A, 0x58A, 0x138A, 0x178A: E3 FRMR AUX Framing Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	COFAE	0
Bit 0	R/W	OOFE	0

OOFE

The OOFE bit is an interrupt enable. When OOFE is logic 1, a change of state of the OOF status generates an interrupt and sets the INTB output to logic 0. When OOFE is logic 0, changes of state of the OOF status are disabled from causing interrupts on the INTB output.

COFAE

The COFAE bit is an interrupt enable. When COFAE is logic 1, a change of frame alignment generates an interrupt and sets the INTB output to logic 0. When COFAE is logic 0, changes of frame alignment are disabled from causing interrupts on the INTB output.

Register 0x18B, 0x58B, 0x138B, 0x178B: E3 FRMR AUX Framing Interrupt Indication and Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	COFAI	X
Bit 2	R	OOFI	X
Bit 1	—	Unused	X
Bit 0	R	OOF	X

OOF

The OOF bit indicates the current state of the E3 FRMR AUX. When OOF is logic 1, the E3 FRMR AUX is out of frame alignment and actively searching for the new alignment. While OOF is high all status indications and overhead extraction continue with the previous known alignment. When OOF is logic 0, the E3 FRMR AUX has found a valid frame alignment and is operating in a maintenance mode, indicating framing bit errors, and extracting and processing overhead bits. During reset, OOF is set to logic 1, but the setting may change prior to the register being read.

OOFI

A logic 1 OOFI bit indicates a change in the OOF status. The OOFI bit is cleared to logic 0 upon the completion of the register read. When OOFI is logic 0, it indicates that no OOF state change has occurred since the last time this register was read.

COFAI

The COFAI bit indicates that a change of frame alignment between the previous alignment and the newly found alignment has occurred. When COFAI is logic 1, the last high-to-low transition on the OOF signal resulted in the new frame alignment differing from the previous one. The COFAI bit is cleared to logic 0 upon the completion of the register read. When COFAI is logic 0, it indicates that no change in frame alignment has occurred when OOF went low.

Register 0x18C, 0x58C, 0x138C, 0x178C: E3 FRMR AUX Maintenance Event Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	FERRE	0
Bit 6	R/W	PERRE	0
Bit 5	R/W	AISDE	0
Bit 4	R/W	FERFE	0
Bit 3	R/W	FEBEE	0
Bit 2	R/W	PTYPEE	0
Bit 1	R/W	TIMEMKE	0
Bit 0	R/W	NATUSEE	0

NATUSEE

The NATUSEE bit is an interrupt enable. When NATUSEE is logic 1, an interrupt is generated on the INTB output when the National Use bit (bit 12 of the frame in G.751 E3 mode) changes state. When NATUSEE is logic 0, changes in state of the National Use bit does not cause an interrupt on INTB.

TIMEMKE

The TIMEMKE bit is an interrupt enable. When TIMEMKE is logic 1, an interrupt is generated on the INTB output when the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte) changes state after the selected persistency check is applied. When TIMEMKE is logic 0, changes in state of the Timing Marker bit does not cause an interrupt on INTB.

PTYPEE

The PTYPEE bit is an interrupt enable. When PTYPEE is logic 1, an interrupt is generated on the INTB output when the Payload Type bits (bits 3,4,5 of the G.832 Maintenance and Adaptation byte) change state. When PTYPEE is logic 0, changes in state of the Payload Type bits does not cause an interrupt on INTB.

FEBEE

The FEBEE bit is an interrupt enable. When FEBEE is logic 1, an interrupt is generated on the INTB output when the Far End Block Error indication bit (bit 2 of the G.832 Maintenance and Adaptation byte) changes state. When FEBEE is logic 0, changes in state of the FEBE bit does not cause an interrupt on INTB.

FERFE

The FERFE bit is an interrupt enable. When FERFE is logic 1, an interrupt is generated on the INTB output when the Far End Receive Failure indication bit (bit 1 of the G.832 Maintenance and Adaptation byte), or when the Remote Alarm indication bit (bit 11 of the frame in G.751) changes state after the selected persistency check is applied. When FERFE is logic 0, changes in state of the FERF or RAI bit does not cause an interrupt on INTB.

AISDE

The AISDE bit is an interrupt enable. When AISDE is logic 1, an interrupt is generated on the INTB output when the AISD indication changes state. When AISDE is logic 0, changes in state of the AISD signal does not cause an interrupt on INTB.

PERRE

The PERRE bit is an interrupt enable. When PERRE is logic 1, an interrupt is generated on the INTB output when a BIP-8 error (in G.832 mode) is detected. When PERRE is logic 0, occurrences of BIP-8 errors do not cause an interrupt on INTB.

FERRE

The FERRE bit is an interrupt enable. When FERRE is logic 1, an interrupt is generated on the INTB output when a framing bit error is detected. When FERRE is logic 0, occurrences of framing bit errors do not cause an interrupt on INTB.

Register 0x18D, 0x58D, 0x138D, 0x178D: E3 FRMR AUX Maintenance Event Interrupt Indication

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	FERRI	0
Bit 6	R	PERRI	0
Bit 5	R	AISDI	0
Bit 4	R	FERFI	0
Bit 3	R	FEBEI	0
Bit 2	R	PTYPEI	0
Bit 1	R	TIMEMKI	0
Bit 0	R	NATUSEI	0

NATUSEI

The NATUSEI bit is a transition Indication. When NATUSEI is logic 1, a change of state of the National Use bit (bit 12 of the frame in G.751 E3 mode) has occurred. When NATUSEI is logic 0, no change of state of the National Use bit has occurred since the last time this register was read.

TIMEMKI

The TIMEMKI bit is a transition indication. When TIMEMKI is logic 1, a change in state of the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte) has occurred. When TIMEMKI is logic 0, no changes in the state of the Timing Marker bit occurred since the last time this register was read.

PTYPEI

The PTYPEI bit is a transition indication. When PTYPEI is logic 1, a change of state of the Payload Type bits (bits 3,4,5 of the G.832 Maintenance and Adaptation byte) has occurred. When PTYPEI is logic 0, no changes in the state of the Payload Type bits has occurred since the last time this register was read.

FEBEI

The FEBEI bit is a transition indication. When FEBEI is logic 1, a change of state of the Far End Block Error indication bit (bit 2 of the G.832 Maintenance and Adaptation byte) has occurred. When FEBEI is logic 0, no changes in the state of the FEBE bit has occurred since the last time this register was read.

FERFI

The FERFI bit is a transition indication. When FERFI is logic 1, a change of state of the Far End Receive Failure indication bit (bit 1 of the G.832 Maintenance and Adaptation byte), or when the Remote Alarm indication bit (bit 12 of the frame in G.751) has occurred. When FERFI is logic 0, no changes in the state of the FERF or RAI bit has occurred since the last time this register was read.

AISDI

The AISDI bit is a transition indication. When AISDI is logic 1, a change in state of the AISD indication has occurred. When AISDI is logic 0, no changes in the state of the AISD signal has occurred since the last time this register was read.

PERRI

The PERRI bit is an event indication. When PERRI is logic 1, the occurrence of one or more BIP-8 errors (in G.832 mode) has been detected. When PERRI is logic 0, no occurrences of BIP-8 errors have occurred since the last time this register was read.

FERRI

The FERRI bit is an event indication. When FERRI is logic 1, the occurrence of one or more framing bit error has been detected. When FERRI is logic 0, no occurrences of framing bit errors have occurred since the last time this register was read.

The transition/event interrupt indications within this register work independently from the interrupt enable bits, allowing the microprocessor to poll the register to determine the activity of the maintenance events. The contents of this register are cleared to logic 0 after the register is read; the INTB output is also cleared to logic 1 if the interrupt was generated by any of the Maintenance Event outputs.

Register 0x18E, 0x58E, 0x138E, 0x178E: E3 FRMR AUX Maintenance Event Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	AISD	X
Bit 6	R	FERF/RAI	X
Bit 5	R	FEBE	X
Bit 4	R	PTYPE[2]	X
Bit 3	R	PTYPE[1]	X
Bit 2	R	PTYPE[0]	X
Bit 1	R	TIMEMK	X
Bit 0	R	NATUSE	X

NATUSE

The NATUSE bit reflects the state of the extracted National Use bit (bit 12 of the frame in G.751 E3 mode).

TIMEMK

The TIMEMK bit reflects the state of the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte).

PTYPE[2:0]

The PTYPE[2:0] bits reflect the state of the Payload Type bits (bits 3,4,5 of the G.832 Maintenance and Adaptation byte). These bits are not latched and should be read 2 or 3 times in rapid succession to ensure a coherent binary value.

FEBE

The FEBE bit reflects the state of the Far End Block Error indication bit (bit 2 of the G.832 Maintenance and Adaptation byte).

FERF

The FERF bit reflects the value of the Far End Receive Failure indication bit (bit 1 of the G.832 Maintenance and Adaptation byte), or the value of the Remote Alarm indication bit (bit 11 of the frame in G.751) when the value has been the same for either 3 or 5 consecutive frames.

AISD

The AISD bit reflects the state of the AIS detection circuitry. When AISD is logic 1, less than 8 zeros (in G.832 mode), or less than 5 zeros (in G.751 mode), were detected during one complete frame period while the E3 FRMR AUX is out of frame alignment. When AISD is logic 0, 8 or more zeros (in G.832 mode), or 5 or more zeros (in G.751 mode), were detected during one complete frame period, or the E3 FRMR AUX has found frame alignment.

Register 0x190, 0x590, 0x1390, 0x1790: J2 FRMR AUX Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	UNI	0
Bit 5	R/W	REFRAME	0
Bit 4	R/W	FLOCK	0
Bit 3	R/W	CRC_REFR	0
Bit 2	R/W	SFRME	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

SFRME

When the Single Framing Bit Error (SFRME) bit is set to logic 1, then the J2 FRMR AUX will indicate (to the PMON AUX) a single framing error for every J2 multi-frame which contains one or more framing errors. When the SFRME bit is set to logic 0, the J2 FRMR AUX will identify every framing error to the PMON AUX.

CRC_REFR

When the CRC Reframe Enable bit is set to logic 1, an alternate framing algorithm is enabled, which uses the CRC-5 check to detect framing to a mimic pattern in the payload or signaling bits. The framer, once it has seen at least one correct framing pattern, begins looking for correct CRC-5s as well. If it observes three consecutive correct framing patterns, and two correct CRC-5 sequences, then frame is declared. Otherwise, a reframe is initiated. When CRC_REFR is set to logic 0, the framing algorithm simply searches for three consecutive correct framing patterns.

FLOCK

When the FLOCK bit is set to logic 1, the J2 FRMR AUX is prevented from declaring Loss of Frame and searching for a new frame alignment due to framing-pattern errors. In this case, the J2 FRMR AUX will only search for frame alignment when the REFRAME register bit transitions from logic 0 to logic 1.

REFRAME

Writing the REFRAME bit logic 1 forces the J2 FRMR AUX to declare loss of frame, and begin searching for a new alignment. In order to force another reframe, REFRAME must be written with logic 0, and then logic 1 again.

UNI

UNI must be set to logic 1 for all modes of operation.

Register 0x191, 0x591, 0x1391, 0x1791: J2 FRMR AUX Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R	LOF	X
Bit 5	—	Unused	X
Bit 4	R	RAI	X
Bit 3	R	RLOF	X
Bit 2	—	Unused	X
Bit 1	R	PHYAIS	X
Bit 0	R	PLDAIS	X

LOF, RAI, RLOF, PHYAIS, PLDAIS

These register bits reflect the current state of the Loss of Frame (LOF), Remote Alarm Indication (RAI), Remote Loss of Frame (RLOF, also known as the A-bit), Physical AIS (PHYAIS), and Payload AIS (PLDAIS) conditions.

Register 0x192, 0x592, 0x1392, 0x1792: J2 FRMR AUX Alarm Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	LOFE	0
Bit 5	R/W	COFAE	0
Bit 4	R/W	RAIE	0
Bit 3	R/W	RLOFE	0
Bit 2	R/W	RLOF_THR	1
Bit 1	R/W	PHYAISE	0
Bit 0	R/W	PLDAISE	0

PLDAISE

When PLDAISE is logic 1, the J2 FRMR AUX will generate an interrupt when a change is detected in the Payload AIS condition.

PHYAISE

When PHYAISE is logic 1, the J2 FRMR AUX will generate an interrupt when a change is detected in the Physical AIS condition.

RLOF_THR

The RLOF Threshold bit determines the number of consecutive A-bits that are required for the state of RLOF to change. When RLOF_THR is logic 0, RLOF is asserted when the A-bit has been logic 1 for three consecutive frames, and deasserted when the A-bit has been logic 0 for three consecutive frames. When RLOF_THR is logic 1, RLOF is asserted when the A-bit has been logic 1 for five consecutive frames, and deasserted when the A-bit has been logic 0 for five consecutive frames. The default setting is that five consecutive A-bits are required.

RLOFE

When RLOFE is logic 1, the J2 FRMR AUX will generate an interrupt when RLOF changes state.

RAIE

When RAIE is logic 1, the J2 FRMR AUX will generate an interrupt when RAI changes state.

COFAE

When COFAE is logic 1, the J2 FRMR AUX will generate an interrupt when a change of frame alignment occurs.

LOFE

When LOFE is logic 1, the J2 FRMR AUX will generate an interrupt when LOF changes state.

Register 0x193, 0x593, 0x1393, 0x1793: J2 FRMR AUX Alarm Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R	LOFI	X
Bit 5	R	COFAI	X
Bit 4	R	RAII	X
Bit 3	R	RLOFI	X
Bit 2	—	Unused	X
Bit 1	R	PHYAISI	X
Bit 0	R	PLDAISI	X

LOFI

The LOFI bit is set to logic 1 if a change occurs in the state of LOF. LOFI is cleared when this register is read.

COFAI

The COFAI bit is set to logic 1 if a change in frame alignment occurs. COFAI is cleared when this register is read.

RAII

The RAII bit is set to logic 1 if a change in the value of RAI occurs. RAII is cleared when this register is read.

RLOFI

The RLOFI bit is set to logic 1 if a change in the value of RLOF occurs. RLOFI is cleared when this register is read.

PHYAISI

The PHYAISI bit is set to logic 1 if a change in the condition of PHYAIS occurs. PHYAISI is cleared when this register is read.

PLDAISI

The PLDAISI bit is set to logic 1 if a change in the condition of PLDAIS occurs. PLDAISI is cleared when this register is read.

Register 0x194, 0x594, 0x1394, 0x1794: J2 FRMR AUX Error/Xbit Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	CRCEE	0
Bit 6	R/W	FRMEE	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	XBITE	0
Bit 2	—	Unused	X
Bit 1	R/W	XBIT_DEB	0
Bit 0	R/W	XBIT_THR	0

XBIT_THR

When XBIT_THR is set to logic 1, then XBIT_THR controls the debouncing threshold of the X-bit indications in the J2 FRMR AUX Error/Xbit Interrupt Status Register. When XBIT_THR is logic 0, the threshold is set to 3 consecutive multi-frames; when XBIT_THR is logic 1, the threshold is set to 5 consecutive multi-frames.

XBIT_DEB

When XBIT_DEB is set to logic 0, the X-bit indications in the J2 FRMR AUX Error/Xbit Interrupt Status Register reflect the most recent value of the X-bits. When XBIT_DEB is set to logic 1, the X-bit indications change value only when an X-bit has maintained its value for 3 or 5 consecutive multi-frames, depending on the setting of XBIT_THR.

XBITE

When XBITE is logic 1, the J2 FRMR AUX will generate an interrupt when any of the X-bits (X1, X2, X3) change state. Because the XBIT interrupt is generated when the X-bit indications change, the interrupt is debounced along with them via the XBIT_DEB and XBIT_THR bits.

FRMEE

When FRMEE is logic 1, the J2 FRMR AUX will generate an interrupt upon the reception of an errored framing bit.

CRCEE

When CRCEE is logic 1, the J2 FRMR AUX will generate an interrupt if a multi-frame fails its CRC-5 check.

Register 0x195, 0x595, 0x1395, 0x1795: J2 FRMR AUX Error/Xbit Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	CRCEI	X
Bit 6	R	FRMEI	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	XBITI	X
Bit 2	R	X3	X
Bit 1	R	X2	X
Bit 0	R	X1	X

X1, X2, X3

The X1, X2, and X3 bits reflect the most recent (debounced if XBIT_DEB is set to logic 1) value of bits 785, 786, and 787 respectively of frame 3 of each multi-frame. These bits are the spare or 'X-bits'

XBITI

The XBITI bit is set to logic 1 if a change in the debounced (if XBIT_DEB is set to logic 1) X-bits (X1, X2, and X3) is detected. XBITI is cleared when this register is read.

FRMEI

The FRMEI bit is set to logic 1 if an errored framing bit occurs. FRMEI is cleared when this register is read.

CRCEI

The CRCEI bit is set to logic 1 if a failed CRC-5 check occurs. CRCEI is cleared when this register is read.

Register 0x198, 0x598, 0x1398, 0x1798: RDLC AUX Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	MEN	0
Bit 2	R/W	MM	0
Bit 1	R/W	TR	0
Bit 0	R/W	EN	0

The RDLC block has been further illustrated in PMC-2021632 “SUNI 4xJET ASSP Telecom Standard Product Data Sheet.”

EN

The EN bit controls the overall operation of the RDLC AUX. When EN is set to logic 1, RDLC AUX is enabled. When set to logic 0, RDLC AUX is disabled. When RDLC AUX is disabled, the RDLC AUX FIFO buffer and interrupts are all cleared. When RDLC AUX is enabled, it will immediately begin looking for flags.

TR

Setting the terminate reception (TR) bit to logic 1 forces the RDLC AUX to immediately terminate the reception of the current data frame, empty the RDLC AUX FIFO buffer, clear the interrupts, and begin searching for a new flag sequence. The RDLC AUX handles a terminate reception event in the same manner as it would the toggling of the EN bit from logic 1 to logic 0 and back to logic 1. Thus, the RDLC AUX state machine will begin searching for flags. An interrupt will be generated when the first flag is detected. The TR bit will reset itself to logic 0 after the register write operation is completed and a rising and falling edge occurs on the internal datalink clock input. If the RDLC AUX Configuration Register is read after this time, the TR bit value returned will be logic 0.

MM

Setting the Match Mask (MM) bit to logic 1 ignores the PA[1:0] bits of the Primary Address Match Register, the SA[1:0] bits of the Secondary Address Match Register, and the two least significant bits of the universal all-ones address when performing the address comparison.

MEN

Setting the Match Enable (MEN) bit to logic 1 enables the detection and storage in the RDLC AUX FIFO of only those packets whose first data byte matches either of the bytes written to the Primary or Secondary Match Address Registers, or the universal all-ones address. When the MEN bit is logic 0, all packets received are written into the RDLC AUX FIFO.

Register 0x199, 0x599, 0x1399, 0x1799: RDLC AUX Interrupt Control

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	INTE	0
Bit 6	R/W	INTC[6]	0
Bit 5	R/W	INTC[5]	0
Bit 4	R/W	INTC[4]	0
Bit 3	R/W	INTC[3]	0
Bit 2	R/W	INTC[2]	0
Bit 1	R/W	INTC[1]	0
Bit 0	R/W	INTC[0]	0

INTC[6:0]

The INTC[6:0] bits control the assertion of FIFO fill level set point interrupts. The value of INTC[6:0] = ‘b0000000 sets the interrupt FIFO fill level to 128.

INTE

The Interrupt Enable bit (INTE) must set to logic 1 to allow the internal interrupt status to be propagated to the INTB output. When the INTE bit is logic 0 the RDLC AUX will not assert INTB.

The contents of the Interrupt Control Register should only be changed when the EN bit in the RDLC AUX Configuration Register is logic 0. This prevents any erroneous interrupt generation.

Register 0x19A, 0x59A, 0x139A, 0x179A: RDLC AUX Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	FE	X
Bit 6	R	OVR	X
Bit 5	R	COLS	X
Bit 4	R	PKIN	X
Bit 3	R	PBS[2]	X
Bit 2	R	PBS[1]	X
Bit 1	R	PBS[0]	X
Bit 0	R	INTR	X

Consecutive reads of the RDLC AUX Status and Data registers should not occur at rates greater than 1/10 that of the clock selected by the LINESYSCLK bit of the Channel Auxiliary Framer Configuration register (112, 312, 512, 712, 912, B12, D12, F12, 1112, 1312, 1512, 1712).

INTR

The interrupt (INTR) bit reflects the status of the internal RDLC AUX interrupt. If the INTE bit in the RDLC AUX Interrupt Control Register is set to logic 1, a RDLC AUX interrupt (INTR is a logic 1) will cause INTB to be asserted low. The INTR register bit will be set to logic 1 when one of the following conditions occurs:

- The number of bytes specified in the RDLC AUX Interrupt Control register have been received on the data link and written into the FIFO.
- RDLC AUX FIFO buffer overrun has been detected.
- The last byte of a packet has been written into the RDLC AUX FIFO.
- The last byte of an aborted packet has been written into the RDLC AUX FIFO.
- Transition of receiving all-ones to receiving flags has been detected.

PBS[2:0]

The packet byte status (PBS[2:0]) bits indicate the status of the data last read from the FIFO as indicated in Table 38.

Table 38 RDLC AUX PBS[2:0] Data Status

PBS[2:0]	Data Status
000	The data byte read from the FIFO is not special.
001	The data byte read from the FIFO is the dummy byte that was written into the FIFO when the first HDLC flag sequence (01111110) was detected. This indicates that the data link became active.
010	The data byte read from the FIFO is the dummy byte that was written into the FIFO when the HDLC abort sequence (01111111) was detected. This indicates that the data link became inactive.
011	Unused.
100	The data byte read from the FIFO is the last byte of a normally terminated packet with no CRC error and the packet received had an integer number of bytes.
101	The data byte read from the FIFO must be discarded because there was a non-integer number of bytes in the packet.
110	The data byte read from the FIFO is the last byte of a normally terminated packet with a CRC error. The packet was received in error.
111	The data byte read from the FIFO is the last byte of a normally terminated packet with a CRC error and a non-integer number of bytes. The packet was received in error.

PKIN

The Packet In (PKIN) bit is logic 1 when the last byte of a non-aborted packet is written into the FIFO. The PKIN bit is cleared to logic 0 after the RDLC AUX Status Register is read.

COLS

The Change of Link Status (COLS) bit is set to logic 1 if the RDLC AUX has detected the HDLC flag sequence (01111110) or HDLC abort sequence (01111111) in the data. This indicates that there has been a change in the data link status. The COLS bit is cleared to logic 0 by reading this register or by clearing the EN bit in the RDLC AUX Configuration Register. For each change in link status, a byte is written into the FIFO. If the COLS bit is found to be logic 1 then the RDLC AUX FIFO must be read until empty. The status of the data link is determined by the PBS[2:0] bits associated with the data read from the RDLC AUX FIFO.

OVR

The overrun (OVR) bit is set to logic 1 when data is written over unread data in the RDLC AUX FIFO buffer. This bit is not reset to logic 0 until after the Status Register is read. While the OVR bit is logic 1, the RDLC AUX and RDLC AUX FIFO buffer are held in the reset state, causing the COLS and PKIN bits to be reset to logic 0.

FE

The FIFO buffer empty (FE) bit is set to logic 1 when the last RDLC AUX FIFO buffer entry is read. The FE bit goes to logic 0 when the FIFO is loaded with new data.

Register 0x19B, 0x59B, 0x139B, 0x179B: RDLC AUX Data

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	RD[7]	X
Bit 6	R	RD[6]	X
Bit 5	R	RD[5]	X
Bit 4	R	RD[4]	X
Bit 3	R	RD[3]	X
Bit 2	R	RD[2]	X
Bit 1	R	RD[1]	X
Bit 0	R	RD[0]	X

Consecutive reads of the RDLC AUX Status and Data registers should not occur at rates greater than 1/10 that of the clock selected by the LINESYSCLK bit of the Channel Auxiliary Framer Configuration register (112, 312, 512, 712, 912, B12, D12, F12, 1112, 1312, 1512, 1712).

RD[7:0]

RD[7:0] contains the received data link information. RD[0] corresponds to the first received bit of the data link message.

This register reads from the RDLC AUX 128-byte FIFO buffer. If data is available, the FE bit in the FIFO Input Status Register is logic 0.

When an overrun is detected, an interrupt is generated and the FIFO buffer is held cleared until the RDLC AUX Status Register is read.

Register 0x19C, 0x59C, 0x139C, 0x179C: RDLC AUX Primary Address Match

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	PA[7]	1
Bit 6	R/W	PA[6]	1
Bit 5	R/W	PA[5]	1
Bit 4	R/W	PA[4]	1
Bit 3	R/W	PA[3]	1
Bit 2	R/W	PA[2]	1
Bit 1	R/W	PA[1]	1
Bit 0	R/W	PA[0]	1

PA[7:0]

The first byte received after a flag character is compared against the contents of this register. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. PA[0] corresponds to the first received bit of the data link message. The MM bit in the Configuration Register is used mask off PA[1:0] during the address comparison.

Register 0x19D, 0x59D, 0x139D, 0x179D: RDLC AUX Secondary Address Match

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	SA[7]	1
Bit 6	R/W	SA[6]	1
Bit 5	R/W	SA[5]	1
Bit 4	R/W	SA[4]	1
Bit 3	R/W	SA[3]	1
Bit 2	R/W	SA[2]	1
Bit 1	R/W	SA[1]	1
Bit 0	R/W	SA[0]	1

SA[7:0]

The first byte received after a flag character is compared against the contents of this register. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. SA[0] corresponds to the first received bit data link message. The MM bit in the Configuration Register is used mask off SA[1:0] during the address comparison.

Register 0x1A0, 0x5A0, 0x13A0, 0x17A0: TTB AUX Control

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	ZEROEN	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	RTIUIE	0
Bit 4	R/W	RTIMIE	0
Bit 3	R/W	PER5	0
Bit 2	R/W	TNULL	1
Bit 1	R/W	NOSYNC	0
Bit 0	R/W	Reserved	0

NOSYNC

The NOSYNC bit disables synchronization to the E3 G.832 Trail Trace message. When NOSYNC is set high, synchronization is disabled and the bytes of the Trail Trace message are captured by the TTB AUX in a circular buffer. When NOSYNC is set low, the TTB AUX synchronizes to the byte with the most significant bit set high and places that byte in the first location in the capture buffer page.

TNULL

The transmit null (TNULL) bit controls the insertion of all-zeros into the outgoing Trail Trace message. The null insertion should be used when microprocessor accesses that change the outgoing trail trace message are being performed. When TNULL is set high, an all-zeros byte is inserted to the transmit stream. When this bit is set low, the contents of the transmit trace buffer are sent.

PER5

The receive trace identifier persistency bit (PER5) controls the number of times that persistency check is made in order to accept the received message. When this bit is set high, five identical message required in order to accept the message. When this bit set low, three unchanged consecutive messages are required.

RTIMIE

The receive trace identifier mismatch interrupt enable (RTIMIE) controls the activation of INTB when comparison between the accepted identifier message and the expected identifier message changes state from match to mismatch and vice versa (RTIM). When RTIMIE is set high, changes in match state will activate the interrupt (INTB) output. When RTIMIE set low, path trace message match state changes will not affect INTB.

RTIUIE

The receive trace identifier unstable interrupt enable (RTIUIE) controls the activation of INTB when the receive identifier message changes state from stable to unstable and vice versa (RTIU). When RTIUIE is set high, changes in the receive path trace identifier stable/unstable (RTIU) state will activate the interrupt (INTB) output. When RTIUIE is set low, path trace identifier state changes will not affect INTB.

ZEROEN

The zero enable bit (ZEROEN) enables TIM assertion and removal based on an all-zeros path trace message string. When ZEROEN is set high, all-zeros path trace message strings are considered when entering and exiting TIM states (message is compare with the expected one and RTIM is set accordingly). When ZEROEN is set low, all-zeros path trace message strings are ignored (RTIM gets zero when message becomes persistent even if the message does not match the expected one). This register bit does not affect RTIU assertion or removal.

Register 0x1A1, 0x5A1, 0x13A1, 0x17A1: TTB AUX Trail Trace Identifier Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	RTIUI	X
Bit 2	R	RTIUV	X
Bit 1	R	RTIMI	X
Bit 0	R	RTIMV	X

RTIMV

The receive trace identifier mismatch value status bit (RTIMV) is set high when the accepted message differs from the expected message. The accepted message is the last message to have been received 5 times consecutively. RTIMV is set low when the accepted message is equal to the expected message. If the accepted trail trace message string is all-ZEROs, the mismatch is not declared unless the ZEROEN register bit in the Control register is set.

RTIMI

The receive trace identifier mismatch indication status bit (RTIMI) is set high when the trace identifier match/mismatch status (RTIMV) of the trace identifier framer changes state. This bit (and the interrupt) are cleared when this register is read.

RTIUV

The receive trace identifier unstable value bit is set high when 8 trace messages mismatching against their immediate predecessor message have been received without persistent message being detected. The unstable counter is incremented on each message that mismatches its predecessor and is cleared on the reception of a persistent message (3 or 5 consecutive matching messages). RTIUV is set high when the unstable counter reaches 8. RTIUV is set low and the unstable counter cleared once a persistent message has been received.

RTIUI

The receive trail trace identifier unstable interrupt status bit is set high when the path trace identifier unstable status (RTIUV) changes state. This bit and the interrupt are cleared when this register is read.

Register 0x1A2, 0x5A2, 0x13A2, 0x17A2: TTB AUX Indirect Address

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	A[7]	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

A[7:0]

The indirect read address bits (A[7:0]) indexes into the trail trace identifier buffers. Addresses 0 to 15 reference the transmit message buffer which contains the identifier message to be inserted into the TR byte of the E3 G.832 transmit stream. Addresses 64 to 79 reference the receive accepted message page. A receive message is accepted into this page when it is received unchanged three or five times consecutively as determined by the PER5 bit setting. Addresses 128 to 143 reference the receive capture page while addresses 192 to 207 reference the receive expected page. The receive capture page contains the identifier bytes extracted from the receive stream. The receive expected page contains the expected trace identifier message down-loaded from the microprocessor.

Table 39 TTB AUX RAM Contents

A[7:0]	RAM Contents
0-15	Transmit Trace Message
64-79	Receive Accepted Trace Message
128-143	Receive Captured Trace Message
192-207	Receive Expected Trace Message

Register 0x1A3, 0x5A3, 0x13A3, 0x17A3: TTB AUX Indirect Data

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	D[7]	X
Bit 6	R/W	D[6]	X
Bit 5	R/W	D[5]	X
Bit 4	R/W	D[4]	X
Bit 3	R/W	D[3]	X
Bit 2	R/W	D[2]	X
Bit 1	R/W	D[1]	X
Bit 0	R/W	D[0]	X

D[7:0]

The indirect data bits (D[7:0]) contain either the data read from a message buffer after an indirect read operation has completed, or the data to be written to the RAM for an indirect write operation. Note that the write data must be set up in this register before an indirect write is initiated. Data read from this register reflects the value written until the completion of a subsequent indirect read operation. The current and accepted message pages should be read at least twice and the result of the successive reads compared for consistency. The TTB AUX keeps overwriting these message pages and consequently the result of a read can be composed of multiple messages.

Register 0x1A4, 0x5A4, 0x13A4, 0x17A4: TTB AUX Expected Payload Type Label

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	EXPLD[2]	0
Bit 1	R/W	EXPLD[1]	0
Bit 0	R/W	EXPLD[0]	0

EXPLD[2:0]

The EXPLD[2:0] bits contain the expected payload type label bits of the G.832 E3 Maintenance and Adaptation (MA) byte. The EXPLD[2:0] bits are compared with the received payload type label extracted from the receive stream. A payload type label mismatch (PLDM) is declared if the received payload type bits differs from the expected payload type. If enabled, an interrupt is asserted upon declaration and removal of PLDM.

For compatibility with old equipment that inserts 000B for unequipped or 001B for equipped, regardless of the payload type, the receive payload type label mismatch mechanism is based on Table 40.

Table 40 TTB AUX Payload Type Match Configurations

Expected	Received	Action
000	000	Match
000	001	Mismatch
000	XXX	Mismatch
001	000	Mismatch
001	001	Match
001	XXX	Match
XXX	000	Mismatch
XXX	001	Match

Expected	Received	Action
XXX	XXX	Match
XXX	YYY	Mismatch

Note: XXX, YYY = anything except 000B or 001B, and XXX is not equal to YYY.

Register 0x1A5, 0x5A5, 0x13A5, 0x17A5: TTB AUX Payload Type Label Control/Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	RPLDUIE	0
Bit 6	R/W	RPLDMIE	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	PLDMODE	0
Bit 3	R	RPLDUI	X
Bit 2	R	RPLDUV	X
Bit 1	R	RPLDMI	X
Bit 0	R	RPLDMV	X

RPLDMV

The receive payload type label mismatch status bit (RPLDMV) is dependent on the PLD Mode. In Mode 1, this bit reports the match/mismatch status between the expected and the accepted payload type label. RPLDMV is set high when the accepted PLD differs from the expected PLD written by the microprocessor. RPLDMV is set low when the accepted PLD matches the expected PLD. In Mode 2, this bit reports the match/mismatch status between the expected and the received payload type label. RPLDMV is set high when the received PLD differs from the expected PLD written by the microprocessor. RPLDMV is set low when the accepted PLD matches the expected PLD.

RPLDMI

The receive payload type label mismatch interrupt status bit (RPLDMI) is set high when the match/mismatch (RPLDMV) status between the accepted and the expected payload type label changes state. The setting of this bit is dependent on the unstable status (RPLDMV) which is dependent on the PLD Mode. This bit (and the interrupt) is cleared when this register is read.

RPLDUV

The receive payload type label unstable status bit (RPLDUV) is independent on the PLD Mode. This bit reports the stable/unstable status of the payload type label in the receive stream. RPLDUV is set high when 5 labels that differ from its immediate predecessor is received. RPLDUV is set low and the unstable label count is reset when 5 consecutive identical labels are received.

RPLDUI

The receive payload type label unstable interrupt status bit (RPLDUI) is set high when the stable/unstable (RPLDUV) status of the payload type label changes state. This bit (and the interrupt) are cleared when this register is read.

PLDMODE

The PLD Mode is used to set the mode used for the payload type label alarm algorithms. Setting this bit to low sets the PLD Mode to Mode 1. Setting this bit to high sets the PLD Mode to Mode 2.

RPLDMIE

The receive payload type label mismatch interrupt enable bit (RPLDMIE) controls the activation of INTB when the comparison between accepted and the expected payload type label changes state from match to mismatch and vice versa. When RPLDMIE is set high, changes in match state (RPLDMI) activates the interrupt (INTB) output. When RPLDMIE is set low, payload type label state changes will not affect INTB.

RPLDUIE

The receive payload type label unstable interrupt enable bit (RPLDUIE) controls the activation of INTB when the received payload type label changes state from stable to unstable and vice versa. When RPLDUIE is set high, changes in stable state (RPLDUI)activates the interrupt (INTB) output. When RPLDUIE is set low, payload type label state changes will not affect INTB.

Register 0x1A6, 0x5A6, 0x13A6, 0x17A6: TTB AUX Indirect Access Trigger

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	BUSY	0
Bit 6	R/W	RWB	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

RWB

The access control bit (RWB) selects between an indirect read or write access to the static page of the trace message buffer. Writing to this register initiates an external microprocessor access to the static page of the trace message buffer. When RWB is set high, a read access is initiated. The data read can be found in the TTB AUX Indirect Data register. When RWB is set low, a write access is initiated. The data in the TTB AUX Indirect Data register will be written to the addressed location in the static page.

BUSY

The BUSY bit reports whether a previously initiated indirect read or write to the trace message RAM has been completed. BUSY is set high upon writing to the TTB AUX Indirect Access Trigger register, and stays high until the initiated access has completed. At this point, BUSY is set low. This register should be polled to determine when new data is available in the TTB AUX Indirect Data register. The maximum latency for the BUSY to return low is 10 µs.

Register 0x1A8, 0x5A8, 0x13A8, 0x17A8: RBOC AUX Configuration/Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	IDLE	0
Bit 1	R/W	AVC	0
Bit 0	R/W	FEACE	0

FEACE

The FEACE bit enables the generation of an interrupt when a valid far end alarm and control (FEAC) code is detected. When a logic 1 is written to FEACE, the interrupt generation is enabled.

AVC

The AVC bit position selects the validation criterion used in determining a valid FEAC code. When a logic 0 is written to AVC, a FEAC code is validated when 8 out of the last 10 received codes are identical. The FEAC code is removed when 2 out of the last 10 received code do not match the validated code.

When a logic 1 is written to AVC, a FEAC code is validated when 4 out of the last 5 received codes are identical. The FEAC code is removed when a single received FEACs does not match the validated code.

IDLE

The IDLE bit enables the generation of an interrupt when a validated FEAC is removed. When a logic 1 is written to IDLE, the interrupt generation is enabled.

Register 0x1A9, 0x5A9, 0x13A9, 0x17A9: RBOC AUX Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	IDLI	X
Bit 6	R	FEACI	X
Bit 5	R	FEAC[5]	X
Bit 4	R	FEAC[4]	X
Bit 3	R	FEAC[3]	X
Bit 2	R	FEAC[2]	X
Bit 1	R	FEAC[1]	X
Bit 0	R	FEAC[0]	X

FEAC[5:0]

The FEAC[5:0] bits contain the received far end alarm and control channel codes. The FEAC[5:0] bits are set to all-ones ("111111") when no code has been validated.

FEACI

The FEACI bit is set to logic 1 when a new FEAC code is validated. The FEAC code value is contained in the FEAC[5:0] bits. The FEACI bit position is set to logic 0 when this register is read.

IDLI

The IDLI bit is set to logic 1 when a validated FEAC code is removed. The FEAC[5:0] bits are set to all-ones when the code is removed. The IDLI bit position is set to logic 0 when this register is read.

Register 0x1B0, 0x5B0, 0x13B0, 0x17B0: RJAT PLL Configuration

Bit	Type	Function	Default
15	—	Unused	X
14	—	Unused	X
13	—	Unused	X
12	—	Unused	X
11	—	Unused	X
10	—	Unused	X
9	—	Unused	X
8	—	Unused	X
7	R/W	DIAG	0
6	R/W	BYPASS	1
5	R/W	INVERT	0
4	R/W	Reserved	0
3	R/W	FRAC[1]	1
2	R/W	FRAC[0]	1
1	R/W	MULTI[1]	1
0	R/W	MULTI[0]	1

MULTI[1:0]/FRAC[1:0]

The bandwidth control multiplier (MULTI[1:0]) and fractional bandwidth control (FRAC[1:0]) configures the RJAT bandwidth. The BW for typical operating modes (DS3 and E3) are illustrated in Table 41.

The RJAT DLL should be reset (write to channel address 0x1B3) whenever the value in MULTI[1:0] or FRAC[1:0] is changed.

Table 41 RJAT BW Configurations

MULT[1:0]	FRAC[1:0]	DS3 BW	E3 BW	BW Divisor
“00”	“00”	0.10	0.08	138412032π
“00”	“01”	0.21	0.16	469273600π
“00”	“10”	0.27	0.21	51887616π
“00”	“11”	0.55	0.42	25893136π
“01”	“00”	1.1	0.84	12976128π
“01”	“01”	1.9	1.4	7569408π
“01”	“10”	3.3	2.5	4325376π
“01”	“11”	6.6	5.1	2162688π
“10”	“00”	11	8.1	1351680π
“10”	“01”	21	16	675840π

MULT[1:0]	FRAC[1:0]	DS3 BW	E3 BW	BW Divisor
“10”	“10”	31	24	456192π
“10”	“11”	60	46	236544π
“11”	“00”	94	72	152064π
“11”	“01”	187	144	76032π
“11”	“10”	281	216	50688π
“11”	“11”	562	431	25344π

INVERT

The data invert (INVERT) controls the polarity of the serial inputs. When INVERT is high, the polarity of the received data on RPOS/RDATI[x] and RNEG/RLCV/ROHM[x] inputs are inverted. When INVERT is low, the polarity of the received data on the RPOS/RDATI[x] and RNEG/RLCV/ROHM[x] inputs are not inverted.

BYPASS

The RJAT bypass (BYPASS) controls the FIFO of the serial data stream.

When BYPASS is low, the incoming RPOS/RDATI[x] and RNEG/RLCV/ROHM[x] serial interface stream is buffered using the internal RJAT FIFO. The serial receive timing source is generated by the phase lock loop which uses the incoming line rate clock RCLK[x] as a reference.

When BYPASS is high, the incoming RPOS/RDATI[x] and RNEG/RLCV/ROHM[x] serial interface stream is retimed. The serial receive timing source is a phase delayed version of the incoming line rate clock RCLK[x].

When BYPASS is set high, the RJAT reduces power consumption by killing clocks internally.

DIAG

The RJAT diagnostic input enable (DIAG) controls the source clock and data used to perform the jitter attenuation function on and generate the serial interface stream to the FRMR. The jitter attenuation function can be disabled by setting BYPASS high.

When DIAG is low, the RJAT jitter attenuates the incoming RCLK[x], RPOS/RDATI[x] and RNEG/RLCV/ROHM[x] serial interface stream.

When DIAG is high, the RJAT jitter attenuates the serial interface stream driven by the TRAN. This loopback is commonly referred to as the serial diagnostic loopback and has been further illustrated in PMC-2021632 “SUNI 4xJET ASSP Telecom Standard Product Data Sheet.”

Register 0x1B1, 0x5B1, 0x13B1, 0x17B1: RJAT Interrupt Status

Bit	Type	Function	Default
15	—	Unused	X
14	—	Unused	X
13	—	Unused	X
12	—	Unused	X
11	—	Unused	X
10	—	Unused	X
9	—	Unused	X
8	—	Unused	X
7	R	ROOLI	X
6	R	ERRORI	X
5	R	OVERI	X
4	R	UNDRI	X
3	R/W	ROOLE	0
2	R/W	ERRORE	0
1	R/W	OVERE	0
0	R/W	UNDRE	0

UNDRE

The FIFO underrun error interrupt enable (UNDRE) bit enables the FIFO underrun error indication interrupt. When UNDRE is set high, an interrupt is generated when an attempt is made to read data from the FIFO when the FIFO is already empty. When UNDRE is set low, changes in the FIFO empty state do not generate an interrupt.

OVERE

The FIFO overrun error interrupt enable (OVERE) bit enables the FIFO error indication interrupt. When OVERE is set high, an interrupt is generated when an attempt is made to write data into the FIFO when the FIFO is already full. When OVERE is set low, changes in the FIFO full state do not generate an interrupt.

ERRORE

The ERROR interrupt enable (ERRORE) bit enables the error indication interrupt. When ERRORE is set high, an interrupt is generated upon assertion event of the ERROR register. When ERRORE is set low, changes in the ERROR register status does not generate an interrupt.

ROOLE

The PLL reference out of lock interrupt enable (ROOLE) bit enables the FIFO centering indication interrupt. When ROOLE is set high, an interrupt is generated upon assertion event of the ROOL register. When ROOLE is set low, changes in the ROOL status do not generate an interrupt.

UNDRI

The FIFO underrun error event register bit (UNDRI) indicates the FIFO has underrun. When an attempt is made to read data from the FIFO when the FIFO is already empty, the UNDRI register bit is set to logic one. If the UNDRE interrupt enable is high, the INTB output is also deasserted when UNDRI asserts.

When WCIMODE is low, the UNDRI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the UNDRI register bit is cleared immediately after a logic one is written to the UNDRI register, thus acknowledging the event has been recorded.

OVERI

The FIFO overrun error event register bit (OVERI) indicates the FIFO has overrun. When an attempt is made to write data into the FIFO when the FIFO is already full, the OVERI register bit is set to logic one. If the OVERE interrupt enable is high, the INTB output is also deasserted when OVERI asserts.

When WCIMODE is low, the OVERI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the OVERI register bit is cleared immediately after a logic one is written to the OVERI register, thus acknowledging the event has been recorded.

ERRORI

The delay line error event register bit (ERRORI) indicates the ERROR register bit has gone high. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. If the ERRORE interrupt enable is high, the INTB output is also deasserted when ERRORI asserts.

When WCIMODE is low, the ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the ERRORI register bit is cleared immediately after a logic one is written to the ERRORI register, thus acknowledging the event has been recorded.

ROOLI

The PLL reference out of lock register bit (ROOLI) indicates the ROOL register bit has changed state. When the ROOL register changes value, the ROOLI register bit is set to logic one. If the ROOLE interrupt enable is high, the INTB output is also deasserted when ROOLI asserts.

When WCIMODE is low, the ROOLI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the ROOLI register bit is cleared immediately after a logic one is written to the ROOLI register, thus acknowledging the event has been recorded.

Register 0x1B2, 0x5B2, 0x13B2, 0x17B2: RJAT Status and FIFO Control

Bit	Type	Function	Default
15	—	Unused	X
14	—	Unused	X
13	—	Unused	X
12	—	Unused	X
11	—	Unused	X
10	—	Unused	X
9	—	Unused	X
8	—	Unused	X
7	R/W	FRST	0
6	R/W	Reserved	0
5	R/W	Reserved	1
4	R/W	Reserved	1
3	R/W	Reserved	0
2	R	ROOL	X
1	R	ERROR	X
0	R	RUN	X

RUN

The DLL lock status register bit (RUN) indicates the DLL has found an initial lock condition. After system reset, RUN is logic zero until the phase detector indicates an initial lock condition. When the phase detector indicates lock, RUN is set high.

The RUN register bit is cleared only by a system reset or a software reset (writing to channel address 0x1B3), or when ERROR is asserted.

ERROR

The delay line error register bit (ERROR) indicates the DLL has run out of dynamic range. When the DLL attempts to move beyond the end of the delay line, ERROR is set high. When ERROR is high, the DLL cannot generate a recovered clock locked to the serial data stream. ERROR is set low one clock cycle after it is asserted, and RUN is de-asserted. At this time RJAT may again try to recover the data stream.

ROOL

The PLL reference out of look (ROOL) indicates the incoming reference clock is out of range. ROOL is high if the incoming reference clock (specified by DIAG in channel address 0x1B0) is not within the threshold specified by ROOLPPM[2:0] of the nominal line rate (specified by REFE3DS3B in channel address 0x113). ROOL is low when the PLL is able to lock to the reference clock.

FRST

The FIFO reset control (FRST) bit allows the RJAT FIFO to be set to a known state. When FRST is set high, the RJAT FIFO fill level is set to 64 bits (half full) and the outgoing streamline interface is held constant. When FRST is set low, the FIFO operates normally.

The FRST does not affect the serial line interface when the FIFO is not enabled (BYPASS set high).

Register 0x1B3, 0x5B3, 0x13B3, 0x17B3: RJAT DLL Reset

Bit	Type	Function	Default
15	—	Unused	X
14	—	Unused	X
13	—	Unused	X
12	—	Unused	X
11	—	Unused	X
10	—	Unused	X
9	—	Unused	X
8	—	Unused	X
7	R/W	Reserved	0
6	R/W	Reserved	0
5	R/W	Reserved	0
4	R/W	Reserved	0
3	R/W	Reserved	0
2	R/W	Reserved	0
1	R/W	Reserved	0
0	R/W	Reserved	0

Writing to this register with 0x00 set low performs a software reset of the RJAT. A software reset requires a maximum of 24*138*4 nominal line rate clock cycles (specified by REFE3DS3B in channel address 0x113) for the RJAT to regain lock.

Register 0x1B4, 0x5B4, 0x13B4, 0x17B4: RJAT ROOL Configuration

Bit	Type	Function	Default
15	—	Unused	X
14	—	Unused	X
13	—	Unused	X
12	—	Unused	X
11	—	Unused	X
10	—	Unused	X
9	—	Unused	X
8	—	Unused	X
7	—	Unused	X
6	—	Unused	X
5	—	Unused	X
4	R/W	Reserved	0
3	—	Unused	X
2	R/W	ROOLPPM[2]	0
1	R/W	ROOLPPM[1]	0
0	R/W	ROOLPPM[0]	0

ROOLPPM[2:0]

The reference out of lock threshold (ROOLPPM) controls when the RJAT ROOL alarm is declared. Changing this value may cause ROOL to monetarily assert while the frequency is being reacquired.

The threshold is only as accurate as the reference clock being used to measure the frequency. The thresholds listed below refer to the difference between the reference clock and the input clock. However, thresholds are approximate due to a number of factors.

Extremely large input jitter may cause the RJAT ROOL to falsely assert as the average frequency over a small time period actually exceeds the threshold. This effect can be seen as small vertical “bites” out of the JAT jitter tolerance curve.

Also, for small thresholds, wander between the reference clock and the input clock may prevent RJAT ROOL from asserting continuously. Specifically, for frequency differences between the threshold level and twice the threshold level, the RJAT ROOL alarm may periodically deassert depending on the relative phase between reference and input clocks.

Table 42 RJAT ROOL Threshold

ROOLPPM	ROOL Threshold
“111”	+/- 488 ppm
“110”	Reserved
“101”	Reserved
“100”	+/- 50 ppm
“011”	+/- 76 ppm
“010”	+/- 101 ppm
“001”	+/- 133 ppm
“000”	+/- 153 ppm

Register 0x1B8, 0x5B8, 0x13B8, 0x17B8: TJAT PLL Configuration

Bit	Type	Function	Default
15	—	Unused	X
14	—	Unused	X
13	—	Unused	X
12	—	Unused	X
11	—	Unused	X
10	—	Unused	X
9	—	Unused	X
8	—	Unused	X
7	R/W	DIAG	0
6	R/W	BYPASS	1
5	R/W	INVERT	0
4	R/W	REFEN	0
3	R/W	FRAC[1]	1
2	R/W	FRAC[0]	1
1	R/W	MULTI[1]	1
0	R/W	MULTI[0]	1

MULTI[1:0]/FRAC[1:0]

The bandwidth control multiplier (MULTI[1:0]) and fractional bandwidth control (FRAC[1:0]) configures the TJAT bandwidth. The BW for typical operating modes (DS3 and E3) are illustrated in Table 43.

The DLL should be reset (write to channel address 0x1BB) whenever the value in MULTI[1:0] or FRAC[1:0] is changed.

Table 43 TJAT BW Configurations

MULT[1:0]	FRAC[1:0]	DS3 BW	E3 BW	BW Divisor
“00”	“00”	0.10	0.08	138412032π
“00”	“01”	0.21	0.16	69273600π
“00”	“10”	0.27	0.21	51887616π
“00”	“11”	0.55	0.42	25893136π
“01”	“00”	1.1	0.84	12976128π
“01”	“01”	1.9	1.4	7569408π
“01”	“10”	3.3	2.5	4325376π
“01”	“11”	6.6	5.1	2162688π
“10”	“00”	11	8.1	1351680π
“10”	“01”	21	16	675840π

MULT[1:0]	FRAC[1:0]	DS3 BW	E3 BW	BW Divisor
“10”	“10”	31	24	456192π
“10”	“11”	60	46	236544π
“11”	“00”	94	72	152064π
“11”	“01”	187	144	76032π
“11”	“10”	281	216	50688π
“11”	“11”	562	431	25344π

REFEN

The arbitrary phase locked loop reference enable (REFEN) configures the reference clock used by the PLL.

When REFEN is low, the PLL is configured to use the reference clock specified by DIAG..

When REFEN is set high, the PLL is configured to use the reference clock specified by TJATREFSEL (channel address 0x113). In this mode, TCLK[x] is a smoothed version of the reference clock and can also be used in loop-timed operation in conjunction with TJATTICLKSEL (channel address 0x113).

INVERT

The data invert (INVERT) controls the polarity of the serial outputs. When INVERT is high, the polarity of the transmit data on TPOS/TDATO[x] and TNEG/TOHM[x] outputs are inverted. When INVERT is low, the polarity of the transmit data on the TPOS/TDATO[x] and TNEG/TOHM[x] outputs are not inverted.

BYPASS

The TJAT bypass (BYPASS) controls the FIFO of the serial data stream.

When BYPASS is low, the outgoing TPOS/TDATO[x] and TNEG/TOHM[x] serial interface stream is buffered using the internal TJAT FIFO. Incoming line rate clock is used as a reference for the phase lock loop which generates TCLK[x].

When BYPASS is high, the outgoing TPOS/TDATO[x] and TNEG/TOHM[x] serial interface stream is retimed. The outgoing clock TCLK[x] is a phase delayed version of the incoming line rate clock.

When BYPASS is set high, the TJAT reduces power consumption by killing clocks internally.

DIAG

The TJAT diagnostic input enable (DIAG) controls the source clock and data used to perform the jitter attenuation function on and generate TCLK[x], TPOS/TDATO[x], and TNEG/TOHM[x]. The jitter attenuation function can be disabled by setting BYPASS high.

When DIAG is low, the TJAT jitter attenuates the incoming serial interface stream from the TRAN.

When DIAG is high, the TJAT jitter attenuates the incoming RCLK[x], RPOS/RDATI[x], and RNEG/RLCV/ROHM[x] serial interface stream. This loopback is commonly referred to as the serial line loopback and has been further illustrated in PMC-2020632 “SUNI 4xJET ASSP Telecom Standard Product Data Sheet.”

Register 0x1B9, 0x5B9, 0x13B9, 0x17B9: TJAT Interrupt Status

Bit	Type	Function	Default
15	—	Unused	X
14	—	Unused	X
13	—	Unused	X
12	—	Unused	X
11	—	Unused	X
10	—	Unused	X
9	—	Unused	X
8	—	Unused	X
7	R	ROOLI	X
6	R	ERRORI	X
5	R	OVERI	X
4	R	UNDRI	X
3	R/W	ROOLE	0
2	R/W	ERRORE	0
1	R/W	OVERE	0
0	R/W	UNDRE	0

UNDRE

The FIFO underrun error interrupt enable (UNDRE) bit enables the FIFO underrun error indication interrupt. When UNDRE is set high, an interrupt is generated when an attempt is made to read data from the FIFO when the FIFO is already empty. When UNDRE is set low, changes in the FIFO empty state do not generate an interrupt.

OVERE

The FIFO overrun error interrupt enable (OVERE) bit enables the FIFO error indication interrupt. When OVERE is set high, an interrupt is generated when an attempt is made to write data into the FIFO when the FIFO is already full. When OVERE is set low, changes in the FIFO full state do not generate an interrupt.

ERRORE

The ERROR interrupt enable (ERRORE) bit enables the error indication interrupt. When ERRORE is set high, an interrupt is generated upon assertion event of the ERROR register. When ERRORE is set low, changes in the ERROR register status does not generate an interrupt.

ROOLE

The PLL reference out of lock interrupt enable (ROOLE) bit enables the FIFO centering indication interrupt. When ROOLE is set high, an interrupt is generated upon assertion event of the ROOL register. When ROOLE is set low, changes in the ROOL status do not generate an interrupt.

UNDRI

The FIFO underrun error event register bit (UNDRI) indicates the FIFO has underrun. When an attempt is made to read data from the FIFO when the FIFO is already empty, the UNDRI register bit is set to logic one. If the UNDRE interrupt enable is high, the INTB output is also deasserted when UNDRI asserts.

When WCIMODE is low, the UNDRI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the UNDRI register bit is cleared immediately after a logic one is written to the UNDRI register, thus acknowledging the event has been recorded.

OVERI

The FIFO overrun error event register bit (OVERI) indicates the FIFO has overrun. When an attempt is made to write data into the FIFO when the FIFO is already full, the OVERI register bit is set to logic one. If the OVERE interrupt enable is high, the INTB output is also deasserted when OVERI asserts.

When WCIMODE is low, the OVERI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the OVERI register bit is cleared immediately after a logic one is written to the OVERI register, thus acknowledging the event has been recorded.

ERRORI

The delay line error event register bit (ERRORI) indicates the ERROR register bit has gone high. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. If the ERRORE interrupt enable is high, the INTB output is also deasserted when ERRORI asserts.

When WCIMODE is low, the ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the ERRORI register bit is cleared immediately after a logic one is written to the ERRORI register, thus acknowledging the event has been recorded.

ROOLI

The PLL reference out of lock register bit (ROOLI) indicates the ROOL register bit has changed state. When the ROOL register changes value, the ROOLI register bit is set to logic one. If the ROOLE interrupt enable is high, the INTB output is also deasserted when ROOLI asserts.

When WCIMODE is low, the ROOLI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the ROOLI register bit is cleared immediately after a logic one is written to the ROOLI register, thus acknowledging the event has been recorded.

Register 0x1BA, 0x5BA, 0x13BA, 0x17BA: TJAT Status and FIFO Control

Bit	Type	Function	Default
15	—	Unused	X
14	—	Unused	X
13	—	Unused	X
12	—	Unused	X
11	—	Unused	X
10	—	Unused	X
9	—	Unused	X
8	—	Unused	X
7	R/W	FRST	0
6	R/W	Reserved	0
5	R/W	Reserved	1
4	R/W	Reserved	1
3	R/W	Reserved	0
2	R	ROOL	X
1	R	ERROR	X
0	R	RUN	X

RUN

The DLL lock status register bit (RUN) indicates the DLL has found an initial lock condition. After system reset, RUN is logic zero until the phase detector indicates an initial lock condition. When the phase detector indicates lock, RUN is set high.

The RUN register bit is cleared only by a system reset or a software reset (writing to channel address 0x1BD), or when ERROR is asserted.

ERROR

The delay line error register bit (ERROR) indicates the DLL has run out of dynamic range. When the DLL attempts to move beyond the end of the delay line, ERROR is set high. When ERROR is high, the DLL cannot generate a recovered clock locked to the serial data stream. ERROR is set low one clock cycle after it is asserted, and RUN is de-asserted. At this time, the TJAT may again try to recover the data stream.

ROOL

The PLL reference out of look (ROOL) indicates the incoming reference clock is out of range. ROOL is high if the incoming reference clock (specified by DIAG and REFEN in channel address 0x1B8) is not within the threshold specified by ROOLPPM[2:0] of the nominal line rate (specified by REFE3DS3B in channel address 0x113). ROOL is low when the PLL is able to lock to the reference clock.

FRST

The FIFO reset control (FRST) bit allows the TJAT FIFO to be set to a known state. When FRST is set high, the TJAT FIFO fill level is set to 64 bits (half full) and the outgoing stream line interface is held constant. When FRST is set low, the FIFO operates normally.

The FRST does not affect the serial line interface when the FIFO is not enabled (BYPASS set high).

Register 0x1BB, 0x5BB, 0x13BB, 0x17BB: TJAT DLL Reset

Bit	Type	Function	Default
15	—	Unused	X
14	—	Unused	X
13	—	Unused	X
12	—	Unused	X
11	—	Unused	X
10	—	Unused	X
9	—	Unused	X
8	—	Unused	X
7	R/W	Reserved	0
6	R/W	Reserved	0
5	R/W	Reserved	0
4	R/W	Reserved	0
3	R/W	Reserved	0
2	R/W	Reserved	0
1	R/W	Reserved	0
0	R/W	Reserved	0

Writing to this register performs a software reset of the TJAT. A software reset requires a maximum of 24*138*4 nominal line rate clock cycles (specified by REFE3DS3B in channel address 0x113) for the TJAT to regain lock.

Register 0x1BC, 0x5BC, 0x13BC, 0x17BC: TJAT ROOL Configuration

Bit	Type	Function	Default
15	—	Unused	X
14	—	Unused	X
13	—	Unused	X
12	—	Unused	X
11	—	Unused	X
10	—	Unused	X
9	—	Unused	X
8	—	Unused	X
7	—	Unused	X
6	—	Unused	X
5	—	Unused	X
4	R/W	UNIPOL	0
3	—	Unused	X
2	R/W	ROOLPPM[2]	0
1	R/W	ROOLPPM[1]	0
0	R/W	ROOLPPM[0]	0

ROOLPPM[2:0]

The reference out of lock threshold (ROOLPPM) controls when the TJAT ROOL alarm is declared. Changing this value may cause ROOL to monetarily assert while the frequency is being reacquired.

The threshold is only as accurate as the reference clock being used to measure the frequency. The thresholds listed below refer to the difference between the reference clock and the input clock. However, thresholds are approximate due to a number of factors.

Extremely large input jitter may cause the TJAT ROOL to falsely assert as the average frequency over a small time period actually exceeds the threshold. This effect can be seen as small vertical “bites” out of the JAT jitter tolerance curve.

Also, for small thresholds, wander between the reference clock and the input clock may prevent TJAT ROOL from asserting continuously. Specifically, for frequency differences between the threshold level and twice the threshold level, the TJAT ROOL alarm may periodically deassert depending on the relative phase between reference and input clocks.

Table 44 TJAT ROOL Threshold

ROOLPPM	ROOL Threshold
“111”	+/- 488 ppm
“110”	Reserved
“101”	Reserved
“100”	+/- 50 ppm
“011”	+/- 76 ppm
“010”	+/- 101 ppm
“001”	+/- 133 ppm
“000”	+/- 153 ppm

UNIPOL

The UNIPOL register controls the TJAT’s ability to process bipolar data. When UNIPOL is set high, the TNEG/TOHM[x] output is forced zero irrespective of the input data stream. When UNIPOL is set low, the TJAT operates normally.

The UNIPOL register must be set high when in serial diagnostic loopback and in unipolar mode so that the TOHM[x] signal is not looped around to the RLCV[x] input and generates line code violations.

Register 0x1800: S/UNI 4xJET Master Reset and Identity

Bit	Type	Function	Default
Bit 15	R/W	RESET	0
Bit 14	R	TYPE[10]	0
Bit 13	R	TYPE[9]	1
Bit 12	R	TYPE[8]	1
Bit 11	R	TYPE[7]	1
Bit 10	R	TYPE[6]	0
Bit 9	R	TYPE[5]	0
Bit 8	R	TYPE[4]	0
Bit 7	R	TYPE[3]	0
Bit 6	R	TYPE[2]	0
Bit 5	R	TYPE[1]	1
Bit 4	R	TYPE[0]	1
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	0
Bit 0	R	ID[0]	0

This register allows the revision number of the S/UNI 4xJET to be read by software permitting graceful migration to newer, feature-enhanced versions of the S/UNI 4xJET.

In addition, writing to this register simultaneously loads all the performance monitor registers in all channels. The TIP register (address 0x1801) is set high while the performance registers are loaded and clears when the transfer is done.

ID[3:0]

The ID bits can be read to provide a binary S/UNI 4xJET revision number.

TYPE[10:0]

The TYPE bits can be read to distinguish the S/UNI 4xJET from the other members of the S/UNI family of devices.

RESET

The RESET bit allows the S/UNI 4xJET to be reset under software control. If the RESET bit is a logic one, the entire S/UNI 4xJET is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the S/UNI 4xJET out of reset. Holding the S/UNI 4xJET in a reset state places it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus negating the software reset. Otherwise, the effect of a software reset is equivalent to that of a hardware reset.

Register 0x1801: S/UNI 4xJET Master Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	WCIMODE	0
Bit 0	R	TIP	X

TIP

The TIP bit is set to a logic one when the performance monitor registers are being loaded. Writing to the S/UNI 4xJET Master Reset and Identity register (address 0x1800) initiates an accumulation interval transfer and loads all the performance monitor registers in the PMON, PMON AUX, PRGD, RXCP, TXCP, RXFP, TXFP, PRGM Line, RHPP, RHPP TU3, .

TIP remains high while the transfer is in progress, and is set to a logic zero when the transfer is complete. TIP can be polled by a microprocessor to determine when the accumulation interval transfer is complete.

WCIMODE

The write on clear interrupt mode (WCIMODE) bit selects the clear interrupt mode. When a logic 1 is written to WCIMODE, the clear interrupt mode is clear on write. When a logic 0 is written to WCIMODE, the clear interrupt mode is clear on read.

Register 0x1803: S/UNI 4xJET Master Receive Configuration

Bit	Type	Function	Default
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	RHPP_TU3_DIS	0
Bit 5	R/W	RHPP_DIS	0
Bit 4	R/W	Reserved	0
Bit 3	—	Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

RHPP_DIS

The receive high order path processor disable (RHPP_DIS) bit disables the RHPP. When a logic 1 is written to RHPP_DIS, the RHPP is disabled. When a logic 0 is written to RHPP_DIS, the RHPP is enabled.

RHPP_TU3_DIS

The receive high order path processor TU3 disable (RHPP_TU3_DIS) bit disables the RHPP TU3. When a logic 1 is written to RHPP_TU3_DIS, the RHPP TU3 is disabled. When a logic 0 is written to RHPP_TU3_DIS, the RHPP TU3 is enabled.

Reserved (Bit 7)

This bit is default 0, and must be written to 1 after reset for proper operation.

Register 0x1804: S/UNI 4xJET Telecom Bus Parity

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	IPE	0
Bit 3	R/W	ODDPG	0
Bit 2	R/W	ODDPC	0
Bit 1	R/W	INCPL	0
Bit 0	R/W	INCJ0J1	0

INCJ0J1

The INCJ0J1 bit controls the whether the composite timing signals (IJ0J1, OJ0J1) in the Transmit and Receive Telecom Bus are used to calculate the corresponding parity signals (IDP, ODP). When INCJ0J1 is set logic 1, the parity signal set includes the IJ0J1 and OJ0J1 signal. When INCJ0J1 is logic 0, parity is calculated without regard to the state of the corresponding IJ0J1 or OJ0J1 signal on the buses.

INCPL

The INCPL bit controls the whether the payload active signal (IPL, OPL) in the Transmit and Receive Telecom Buses are used to calculate the corresponding parity signals (IDP and ODP respectively). When INCPL is set logic 1, the parity signal set includes the corresponding IPL or OPL signal. When INCPL is logic 0, parity is calculated without regard to the state of the corresponding IPL or OPL signal on the buses.

ODDPC

The ODDPC bit controls the parity checked on the Receive Telecom Bus parity signal (IDP). When logic 1, the ODDPC bit configures the bus parity including the corresponding parity signal to be odd. When logic 0, the ODDPC bit configures the bus parity to be even.

ODDPG

The ODDPG bit controls the parity generated on the Transmit Telecom Bus and parity signals (ODP). When logic 1, the ODDPG bit configures the bus parity including the corresponding parity signal to be odd. When logic 0, the ODDPG bit configures the bus parity to be even.

IPE

The IPE bit controls the assertion of interrupts when a parity error is detected on the Receive Telecom Bus. When IPE is logic 1, an interrupt will be asserted (INTB set logic 0) when a parity error has been detected in the Receive Telecom Bus. When IPE is logic 0, incoming bus parity errors will not affect INTB.

Register 0x1805:S/UNI 4xJET Transmit Telecom Bus Synchronization Delay

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	OJ0REFDLY[13]	0
Bit 12	R/W	OJ0REFDLY[12]	0
Bit 11	R/W	OJ0REFDLY[11]	0
Bit 10	R/W	OJ0REFDLY[10]	0
Bit 9	R/W	OJ0REFDLY[9]	0
Bit 8	R/W	OJ0REFDLY[8]	0
Bit 7	R/W	OJ0REFDLY[7]	0
Bit 6	R/W	OJ0REFDLY[6]	0
Bit 5	R/W	OJ0REFDLY[5]	0
Bit 4	R/W	OJ0REFDLY[4]	0
Bit 3	R/W	OJ0REFDLY[3]	0
Bit 2	R/W	OJ0REFDLY[2]	0
Bit 1	R/W	OJ0REFDLY[1]	0
Bit 0	R/W	OJ0REFDLY[0]	0

This register controls the delay from the OJ0REF input signal to the time when the S/UNI 4xJET produces the J0 pulse on the Transmit Telecom Bus interface.

OJ0REFDLY[13:0]

The transmit transport frame delay bits (OJ0REFDLY [13:0]) control the delay, in OCLK cycles, inserted by the S/UNI 4xJET between receiving a reference J0 frame pulse on OJ0REF, and presenting the outgoing J0 transmit frame pulse on OJ0J1.

The relationships of OJ0REF, OJ0REFDLY[13:0] has been further illustrated in PMC-2021632 “SUNI 4xJET ASSP Telecom Standard Product Data Sheet” Functional Timing Section.

Valid values of OJ0REFDLY [13:0] are 0000H to 25F7H.

Register 0x1807: S/UNI 4xJET Master Interrupt Status #1

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	CHNLI[3]	X
Bit 10	R	Reserved	X
Bit 9	R	CHNLI[1]	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	CHNLI[2]	X
Bit 1	R	Reserved	X
Bit 0	R	CHNLI[0]	X

When the interrupt output INTB goes low, this register allows the source of the active interrupt to be identified down to the channel level. Further register accesses are required for the channel in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

CHNLI[3:0]

A channel interrupt CHNLI[3:0] bit is a logic one when an interrupt request is active from the corresponding channel. Channel Interrupt Status #1 register (channel address 0x005) or Channel Interrupt Status #2 register (channel address 0x10A) must be read in order to determine the block with the active interrupt source.

Register 0x1808: S/UNI 4xJET Master Interrupt Status #2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	R	Reserved	X
Bit 13	R	Reserved	X
Bit 12	R	PRGMLI	X
Bit 11	R	RTTPPATHTU3I	X
Bit 10	R	RTTPPATHI	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	RHPPTU3I	X
Bit 6	R	RHPPI	X
Bit 5	R	Reserved	X
Bit 4	R	SARCI	X
Bit 3	R	TDLLI	X
Bit 2	R	RDLLI	X
Bit 1	R	TULI	X
Bit 0	R	RULI	X

When the interrupt output INTB goes low, this register allows the source of the active interrupt to be identified down to the block level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RULI

The RULI bit is a logic one when an interrupt request is active from the RUL3 block. The RUL3 interrupt sources are enabled in the RUL3 Interrupt Status/Enable register.

TULI

The TULI bit is a logic one when an interrupt request is active from the TUL3 block. The TUL3 interrupt sources are enabled in the TUL3 Interrupt Status/Enable registers.

RDLLI

The RDLLI bit is a logic one when an interrupt request is active from the RUL3 DLL block. The RUL3 DLL interrupt sources are enabled in the RUL3 DLL Configuration register.

TDLLI

The TDLLI bit is a logic one when an interrupt request is active from the TUL3 DLL block. The TUL3 DLL interrupt sources are enabled in the TUL3 DLL Configuration register.

SARCI

The SARCI bit is a logic one when an interrupt request is active from the SARC block. The SARC interrupt sources are enabled in the SARC Interrupt Enable registers.

RHPPI

The RHPPI bit is a logic one when an interrupt request is active from the RHPP block. The RHPP interrupt sources are enabled in the RHPP Interrupt Enable registers.

RHPPTU3I

The RHPPTU3I bit is a logic one when an interrupt request is active from the RHPP TU3 block. The RHPP TU3 interrupt sources are enabled in the RHPP TU3 Interrupt Enable registers.

RTTPPATHI

The RTTPPATHI bit is a logic one when an interrupt request is active from the RTTP PATH block. The RTTP PATH interrupt sources are enabled in the RTTP PATH Interrupt Enable registers.

RTTPPATHTU3I

The RTTPPATHTU3I bit is a logic one when an interrupt request is active from the RTTP PATH TU3 block. The RTTP PATH TU3 interrupt sources are enabled in the RTTP PATH TU3 Interrupt Enable registers.

PRGMLI

The PRGMLI bit is a logic one when an interrupt request is active from the PRGM Line block. The PRGM Line interrupt sources are enabled in the PRGM Line Interrupt Enable registers.

Register 0x1809: S/UNI 4xJET Master Interrupt Status #3

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	TTCOMDLLI	X
Bit 2	R	IPI	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

When the interrupt output INTB goes low, this register allows the source of the active interrupt to be identified down to the block level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

IPI

The Receive Telecom Bus parity interrupt status bit (IPI) reports the status of the incoming bus parity interrupt. IPI is logic 1 on detection of a parity error event on the incoming bus. This interrupt is cleared when this register is read.

The occurrence of parity error events is usually an indication of misconfigured parity generation/detection or an actual hardware problem at the incoming bus input.

TTCOMDLLI

The TTCOMDLLI bit is a logic one when an interrupt request is active from the transmit telecom DLL block. The transmit telecom DLL interrupt sources are enabled in the transmit telecom DLL Configuration register.

Register 0x180A: S/UNI 4xJET Master Clock Activity & Input Monitor

Bit	Type	Function	Default
Bit 15	R	Reserved	1
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	SMODE[2]	X
Bit 11	R	SMODE[1]	X
Bit 10	R	SMODE[0]	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	OHCLKA	X
Bit 4	R	OCLKA	X
Bit 3	R	ICLKA	X
Bit 2	R	REF8KICLKA	X
Bit 1	R	E3REFCLKA	X
Bit 0	R	DS3REFCLKA	X

This register provides activity monitoring of the S/UNI 4xJET clocks and mode pins. When a monitored clock signal makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is written, at which point, all the clock monitor bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read/written at periodic intervals to detect clock failures.

DS3REFCLKA

The DS3REFCLK active (DS3REFCLKA) bit monitors for low to high transition on the DS3_REFCLK reference clock input. DS3REFCLKA is set high on a rising edge of DS3_REFCLK and is set low when this register is written.

E3REFCLKA

The E3REFCLK active (E3REFCLKA) bit monitors for low to high transition on the E3_REFCLK reference clock input. E3REFCLKA is set high on a rising edge of E3_REFCLK and is set low when this register is written.

REF8KICLKA

The REF8KICLK active (REF8KICLKA) bit monitors for low to high transition on the REF8KI reference clock input. REF8KIA is set high on a rising edge of REF8KI and is set low when this register is written.

ICLKA

The ICLK active (ICLKA) bit monitors for low to high transition on the ICLK clock input. ICLKA is set high on a rising edge of ICLK and is set low when this register is written.

OCLKA

The OCLK active (OCLKA) bit monitors for low to high transition on the OCLK clock input. OCLKA is set high on a rising edge of OCLK and is set low when this register is written.

OHCLKA

The OHCLK active (OHCLKA) bit monitors for low to high transition on the OHCLK clock input. OHCLKA is set high on a rising edge of OHCLK and is set low when this register is written.

SMODE[2:0]

The SMODE[2:0] register bits are used to determine the value of the SMODE[2:0] inputs.

Register 0x180B: S/UNI 4xJET Master Loopback Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	TCOM_LLE	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	TCOM_DLE	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	TXSTI_DLE	0

These loopbacks have been further illustrated in PMC-2021632 “SUNI 4xJET ASSP Telecom Standard Product Data Sheet.”

TXSTI_DLE

The Transmit Time Slot Interchange Diagnostic Loop Back (TXSTI_DLE) bit enables the loop back of the STS-12/STM-4 data stream at the input of the PRGM Line to the STS-12/STM-4 data stream out of the RHPP_TU3. When a logic 1 is written to TXSTI_DLE, the loop back is active. When a logic 0 is written to TXSTI_DLE, the loop back is inactive.

TCOM_DLE

The Telecom Diagnostic Loop Back (TCOM_DLE) bit enables the loop back of the STS-12/STM-4 data stream at the output of the transmit telecom interface to the input of the receive telecom interface. When a logic 1 is written to TCOM_DLE, the loop back is active. When a logic 0 is written to TCOM_DLE, the loop back is inactive.

TCOM_LLE

The Telecom Line Loop Back (TCOM_LLE) bit enables the loop back of the STS-12/STM-4 data stream at the output of the receive telecom interface to the input of the transmit telecom interface. When a logic 1 is written to TCOM_LLE, the loop back is active. When a logic 0 is written to TCOM_LLE, the loop back is inactive.

Register 0x180D: S/UNI 4xJET Transmit Timeslot Enable

Bit	Type	Function	Default
15	—	Unused	X
14	—	Unused	X
13	—	Unused	X
12	R/W	TTBZ	0
11	R/W	STSEN[12]	1
10	R/W	STSEN[11]	1
9	R/W	STSEN[10]	1
8	R/W	STSEN[9]	1
7	R/W	STSEN[8]	1
6	R/W	STSEN[7]	1
5	R/W	STSEN[6]	1
4	R/W	STSEN[5]	1
3	R/W	STSEN[4]	1
2	R/W	STSEN[3]	1
1	R/W	STSEN[2]	1
0	R/W	STSEN[1]	1

STSEN[12:1]

The STSEN[12:1] bits are used in conjunction with the TTBZ bit to provide tristate control for the outgoing Telecom Bus signals (OD[7:0], OPL, ODP). In addition, STSEN[12:1] determines during which timeslots to assert OSTSEN irrespective of TTBZ.

When the specified timeslot is enabled (timeslot x, STSEN[x] = '1'), OD[7:0], OPL, and ODP are driven during the corresponding timeslot and OSTSEN is set high. When the specified timeslot is disabled (timeslot x, STSEN[x] = '0'), OD[7:0], OPL, and ODP are held in tristate during the corresponding timeslot and OSTSEN is set low.

When TTBZ is low, these bits have no effect on the tristate control of the outgoing Telecom Bus signals, and the signals are driven by the S/UNI 4xJET during all timeslots.

TTBZ

The TTBZ bit is used in conjunction with the STSEN[12:1] bits to provide tristate control for the outgoing Telecom Bus signals (OD[7:0], OPL, ODP). When TTBZ is low, OD[7:0], OPL, and ODP are always driven by the S/UNI 4xJET. When TTBZ is high, OD[7:0], OPL, and ODP are driven only when the specified timeslot is enabled (timeslot x, STSEN[x] = '1'), otherwise the pins are held in tristate during the corresponding timeslot.

Register 0x180E: S/UNI 4xJET 8kHz Output Reference Clock Select

Bit	Type	Function	Default
15	—	Unused	X
14	—	Unused	X
13	—	Unused	X
12	—	Unused	X
11	—	Unused	X
10	—	Unused	X
9	—	Unused	X
8	—	Unused	X
7	—	Unused	X
6	—	Unused	X
5	—	Unused	X
4	—	Unused	X
3	R/W	REF8KOSEL[3]	0
2	R/W	REF8KOSEL[2]	0
1	R/W	REF8KOSEL[1]	0
0	R/W	REF8KOSEL[0]	0

REF8KOSEL[3:0]

The REF8KOSEL[3:0] selects the source by which the 8kHz Output reference (REF8KO) is derived.

Table 45 REF8KO Source Select

REF8KOSEL[3:0]	REF8KO Source
0x0	RCLK[0]
0x9	RCLK[1]
0x2	RCLK[2]
0xB	RCLK[3]
0xD	ICLK input

Register 0x1810: RUL3 Interface Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	L3MODE	X
Bit 6	R/W	L3MODEINV	0
Bit 5	R/W	Reserved	0
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	RPRTYP	0
Bit 1	R/W	RCA_INV	0
Bit 0	R/W	FIFORST	1

FIFORST

The FIFORST bit is used to reset the system interface channel receive FIFOs. When FIFORST is set low, the channel receive FIFOs operate normally. When FIFORST is set high, the channel receive FIFOs are immediately emptied. The channel FIFOs remain empty and continue to ignore read operations until a logic zero is written to FIFORST.

The RCA output should be low when FIFORST is set high to prevent the Level 3 interface from falsely reporting data in the FIFOs.

When the system interface is configured for mixed mode (ATM and packets over Level 3 POSPHY) it is required that at least one channel is configured for ATM processing (PATM is set high) prior to toggling FIFORST.

RCA_INV

The RCA_INV bit is used to invert the polarity of the RCA output. When RCA_INV is set low, the RCA output operates normally. When RCA_INV is set high, the polarity of the control signals inverts. Therefore, when RCA_INV is set high, an empty channel FIFO is identified by RCA set high.

RPRTYP

The RPRTYP bit selects even or odd parity for the RPRTY output on the transmit Level 3 interface. When RPRTYP is set high, the RPRTY input is the even parity for inputs RDAT[31:0]. When RPRTYP is set low, the RPRTY input is the odd parity for inputs RDAT[31:0].

L3MODEINV

The L3MODE invert register bit provides a method to override the SMODE[0] input using software in the transmit direction. The value of the SMODE[0] input is logically XORed with the value of the L3MODEINV register bit to determine the mode of the receive Level 3 interface.

When L3MODEINV is high and SMODE[0] is low, the S/UNI 4xJET implements a receive POS-PHY Level 3 interface. When L3MODEINV is high and SMODE[0] is high, the S/UNI 4xJET implements a receive UTOPIA Level 3 interface. When L3MODEINV is low, the SMODE[0] input operates normally.

L3MODE

The L3MODE register bit reflects the polarity of the SMODE[0] input. When the SMODE[0] input is low, the L3MODE register bit is low. When the SMODE[0] input is high, the L3MODE register bit is high.

When L3MODE is low, the S/UNI 4xJET is configured for UTOPIA Level 3 operation. When L3MODE is high, the S/UNI 4xJET is configured for POS-PHY Level 3 operation.

Register 0x1811: RUL3 Interrupt Status/Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	FUNRE	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R	Reserved	X
Bit 2	R	FUNRI	0
Bit 1	R	Reserved	0
Bit 0	R	Reserved	0

FUNRI

The FIFO underrun interrupt is set high when a read from the FIFO is attempted while the FIFO is empty. The FUNRI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. This register bit is only valid during UTOPIA Level 3 operation.

In a single PHY UTOPIA operation, if RENB realignment happens on the same PHY, and this PHY is not empty, RUL3 FUNRI interrupt is reported. This re-alignment is a protocol violation that should be avoided by link layer device.

FUNRE

The FIFO underrun interrupt enable controls the assertion of the INTB output when FUNRI is high. When FUNRE is set high, an interrupt is generated upon assertion event of the FUNRI register. When FUNRE is set low, changes in the FUNRI status do not generate an interrupt.

Register 0x1812: RUL3 ATM Level 3 FIFO Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	CELLFORM	0
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

CELLFORM

The CELLFORM bits control the length of receive Level 3 interface ATM cell structure. When CELLFORM is low, the ATM cell structure is 56 bytes in size (14 RFCLK cycles) and contains the HCS (H5) and HCS Control bytes. When CELLFORM is high, the ATM cell structure is 52 bytes in size (13 RFCLK cycles) and does not contain the HCS and HCS Control bytes.

The value of CELLFORM should be changed only when FIFORST is set high.

Register 0x1813: RUL3 ATM Level 3 Signal Label

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	ATM[7]	0
Bit 6	R/W	ATM[6]	0
Bit 5	R/W	ATM[5]	0
Bit 4	R/W	ATM[4]	0
Bit 3	R/W	ATM[3]	0
Bit 2	R/W	ATM[2]	0
Bit 1	R/W	ATM[1]	0
Bit 0	R/W	ATM[0]	1

ATM[7:0]

The ATM[7:0] bits control the value of RDAT[31:24] when performing in-band addressing in POS-PHY Level 3 operation in the receive direction. When RSX is high and RVAL is low, the in-band address specifying the channel number is on RDAT[7:0]. In order to prevent confusion between ATM data and POS data, RDAT[31:24] is used to specify the data type for the channel.

For channels configured for packet data, RDAT[31:24] is set to the value specified by POS[7:0] during in-band addressing. For channels configured for ATM cell data, RDAT[31:24] is set to the value specified by ATM[7:0] during in-band addressing.

Register 0x1814: RUL3 POS Level 3 Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R/W	PAUSE[1]	0
Bit 0	R/W	PAUSE[0]	0

PAUSE[1:0]

The PAUSE[1:0] bits specify the minimum number of clock cycles the POS-PHY Level 3 interface will pause between transfer bursts. When PAUSE[1:0] is set to “00”, the POS-PHY Level 3 interface may select the next channel by immediately asserting RSX after ending a transfer. When PAUSE[1:0] is set to “11”, the POS-PHY Level 3 interface will wait for 3 RFCLK clock cycles before selecting the next channel and starting another transfer.

The PAUSE[1:0] register allows the user to configure the POS-PHY Level 3 interface to halt between burst transfers. By inserting dead time between bursts, the Layer device may cleanly pause the transfer of data between bursts by deasserting RENB.

Register 0x1815: RUL3 POS Level 3 Signal Label

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	POS[7]	0
Bit 6	R/W	POS[6]	0
Bit 5	R/W	POS[5]	0
Bit 4	R/W	POS[4]	0
Bit 3	R/W	POS[3]	0
Bit 2	R/W	POS[2]	0
Bit 1	R/W	POS[1]	0
Bit 0	R/W	POS[0]	0

POS[7:0]

The POS[7:0] bits control the value of RDAT[31:24] when performing in-band addressing in POS-PHY Level 3 operation in the receive direction. When RSX is high and RVAL is low, the in-band address specifying the channel number is on RDAT[7:0]. In order to prevent confusion between ATM data and POS data, RDAT[31:24] is used to specify the data type for the channel.

For channels configured for packet data, RDAT[31:24] is set to the value specified by POS[7:0] during in-band addressing. For channels configured for ATM cell data, RDAT[31:24] is set to the value specified by ATM[7:0] during in-band addressing.

Register 0x1816: RUL3 POS Level 3 Transfer Size

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	TRAN[6]	0
Bit 5	R/W	TRAN[5]	0
Bit 4	R/W	TRAN[4]	0
Bit 3	R/W	TRAN[3]	1
Bit 2	R/W	TRAN[2]	1
Bit 1	R/W	TRAN[1]	1
Bit 0	R/W	TRAN[0]	0

TRAN[6:0]

The TRAN[6:0] bits determine the maximum transfer length the POS-PHY Level 3 interface will service a PHY channel before servicing another PHY channel. TRAN[6:0] specifies the maximum number, plus 1, of RFCLK clock cycles the POS-PHY Level 3 interface will service on PHY channel. Therefore, the maximum number of bytes per transfer is 4*(TRAN[6:0]+1).

The actual transfer burst length is until an end-of-packet is transferred or until the burst length specified by TRAN[6:0]. Valid transfer burst length range from 1 to 84.

TRAN[6:0] and BURST[6:0] must be configured such that the sum of TRAN[6:0] in number of bytes and RUL3 BURST[6:0] in number of byte should be less than the 286 bytes (the size of the channel FIFO less the burst length from the slices). Last DWORD of an ATM cell is trapped in RUL3 FIFO for 52 bytes cell structure, if RUL3 TRAN is set to 4 , 8, 12, 16 or 24 bytes. For 56 bytes cell structure, the last DWORD of ATM cell will be trapped if RUL3 TRAN is set to 4 bytes.

Register 0x1818: RUL3 Channel #0 Mode Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	FIFORST[0]	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	PATM[0]	0

PATM[0]

The PATM registers configure channels #0 for ATM or packet operation during POS-PHY Level 3 operation in the receive direction. When SMODE[0] is high and PATM is low, the channel is configured for packet data over the POS-PHY Level 3 interface. When SMODE[0] is high and PATM is high, the channel is configured for ATM cells over the POS-PHY Level 3 interface.

When SMODE[0] is low, PATM must be set low.

When PATM[0] is updated it is required that the corresponding FIFORST[0] be toggled.

FIFORST[0]

The FIFORST registers are used to reset channels #0 four-cell/256 byte transmit FIFOs. When FIFORST is set to logic zero, the FIFO operates normally. When FIFORST is set to logic one, the FIFO is immediately emptied and ignores writes. The buffer remains empty and continues to ignore writes until a logic zero is written to FIFORST.

The channel FIFORST registers in the RXCP and RXFP must be set high before FIFORST is asserted. The channel FIFORST registers must be set low after FIFORST is deasserted.

Register 0x1819: RUL3 Level 2 Channel #1Mode Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	FIFORST[1]	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	PATM[1]	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

PATM[1]

The PATM registers configure channels #1 for ATM or packet operation during POS-PHY Level 3 operation in the receive direction. When SMODE[0] is high and PATM is low, the channel is configured for packet data over the POS-PHY Level 3 interface. When SMODE[0] is high and PATM is high, the channel is configured for ATM cells over the POS-PHY Level 3 interface.

When SMODE[0] is low, PATM must be set low.

When PATM[1] is updated it is required that the corresponding FIFORST[1] be toggled.

FIFORST[1]

The FIFORST registers are used to reset channels #1, #5, and #9 four-cell/256 byte transmit FIFOs. When FIFORST is set to logic zero, the FIFO operates normally. When FIFORST is set to logic one, the FIFO is immediately emptied and ignores writes. The buffer remains empty and continues to ignore writes until a logic zero is written to FIFORST.

The channel FIFORST registers in the RXCP and RXFP must be set high before FIFORST is asserted. The channel FIFORST registers must be set low after FIFORST is deasserted.

Register 0x181A: RUL3 Level 2 Channel #2 Mode Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	FIFORST[2]	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	PATM[2]	0

PATM[2]

The PATM registers configure channels #2 for ATM or packet operation during POS-PHY Level 3 operation in the receive direction. When SMODE[0] is high and PATM is low, the channel is configured for packet data over the POS-PHY Level 3 interface. When SMODE[0] is high and PATM is high, the channel is configured for ATM cells over the POS-PHY Level 3 interface.

When SMODE[0] is low, PATM must be set low.

When PATM[2] is updated it is required that the corresponding FIFORST[2] be toggled.

FIFORST[2]

The FIFORST registers are used to reset channels #2 four-cell/256 byte transmit FIFOs. When FIFORST is set to logic zero, the FIFO operates normally. When FIFORST is set to logic one, the FIFO is immediately emptied and ignores writes. The buffer remains empty and continues to ignore writes until a logic zero is written to FIFORST.

The channel FIFORST registers in the RXCP and RXFP must be set high before FIFORST is asserted. The channel FIFORST registers must be set low after FIFORST is deasserted.

Register 0x181B: RUL3 Level 2 Channel #3 Mode Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	FIFORST[3]	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	PATM[3]	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

PATM[3]

The PATM registers configure channels #3 for ATM or packet operation during POS-PHY Level 3 operation in the receive direction. When SMODE[0] is high and PATM is low, the channel is configured for packet data over the POS-PHY Level 3 interface. When SMODE[0] is high and PATM is high, the channel is configured for ATM cells over the POS-PHY Level 3 interface.

When SMODE[0] is low, PATM must be set low.

When PATM[3] is updated it is required that the corresponding FIFORST[3] be toggled.

FIFORST[3]

The FIFORST registers are used to reset channels #3 four-cell/256 byte transmit FIFOs. When FIFORST is set to logic zero, the FIFO operates normally. When FIFORST is set to logic one, the FIFO is immediately emptied and ignores writes. The buffer remains empty and continues to ignore writes until a logic zero is written to FIFORST.

The channel FIFORST registers in the RXCP and RXFP must be set high before FIFORST is asserted. The channel FIFORST registers must be set low after FIFORST is deasserted.

Register 0x1820: TUL3 Interface Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	L3MODE	X
Bit 6	R/W	L3MODEINV	0
Bit 5	R/W	Reserved	0
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	TPRTYP	0
Bit 1	R/W	TCA_TPA_INV	0
Bit 0	R/W	FIFORST	1

FIFORST

The FIFORST bit is used to reset the system interface channel transmit FIFOs. When FIFORST is set low, the channel transmit FIFOs operate normally. When FIFORST is set high, the channel transmit FIFOs are immediately emptied. The channel FIFOs remain empty and continue to ignore writes operations until a logic zero is written to FIFORST.

The TCA/PTPA and STPA outputs will be low when FIFORST is set high to prevent a Level 3 layer device from attempting to write data into the FIFOs.

When the system interface is configured for mixed mode (ATM and packets over Level 3 POSPHY), it is required that at least one channel be configured for ATM processing (PATM is set high) prior to toggling FIFORST.

TCA_TPA_INV

The TCA_TPA_INV bit is used to invert the polarity of the TCA/PTPA and STPA outputs. When TCA_TPA_INV is set low, the TCA_PTPA and STPA outputs operate normally. When TCA_TPA_INV is set high, the polarity of the control signals inverts. Therefore, when TCA_TPA_INV is set high, a full channel FIFO is identified by TCA_PTPA set high.

TPRTYP

The TPRTYP bit selects even or odd parity for the TPRTY output on the transmit Level 3 interface. When TPRTYP is set high, the TPRTY input is the even parity for inputs TDAT[31:0]. When TPRTYP is set low, the TPRTY input is the odd parity for inputs TDAT[31:0].

L3MODEINV

The L3MODE invert register bit provides a method to override the SMODE[0] input using software in the transmit direction. The value of the SMODE[0] input is logically XORed with the value of the L3MODEINV register bit to determine the mode of the transmit Level 3 interface.

When L3MODEINV is high and SMODE[0] is low, the S/UNI 4xJET implements a transmit POS-PHY Level 3 interface. When L3MODEINV is high and SMODE[0] is high, the S/UNI 4xJET implements a transmit UTOPIA Level 3 interface. When L3MODEINV is low, the SMODE[0] input operates normally.

L3MODE

The L3MODE register bit reflects the polarity of the SMODE[0] input. When the SMODE[0] input is set low, the L3MODE register bit is low. When the SMODE[0] input is set high, the L3MODE register bit is high.

When L3MODE is low, the S/UNI 4xJET is configured for UTOPIA Level 3 operation. When L3MODE is high, the S/UNI 4xJET is configured for POS-PHY Level 3 operation.

Register 0x1821: TUL3 Interrupt Status/Enable #1

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	CAME	0
Bit 6	R/W	FOVRE	0
Bit 5	R/W	TPRTYE	0
Bit 4	R/W	TSOCE	0
Bit 3	R	CAMI	X
Bit 2	R	FOVRI	X
Bit 1	R	TPRTYI	X
Bit 0	R	TSOCI	X

TSOCI

The TSOCI register functions as a start of cell re-alignment interrupt.

During Utopia level 3 operation, this interrupt is set high when the TSOC input is sampled high during any position other than the first word of the ATM cell structure on TDAT[31:0].

During POS-PHY Level 3 operation, this interrupt is set high when an ATM cell is shorter or longer than specified by CELLFORM. Any partial cell structure already written into the FIFO is discarded when a new cell structure alignment is detected. However, since TMOD is ignored during the last word of the ATM cell structure, invalid ATM cell structures 1, 2 or 3 bytes shorter than required will not cause TSOCI to assert.

If TENB is deasserted during a cell transfer (protocol violation) and then re-asserted during the same cell transfer, the current cell is dropped and TSOCI is asserted. However if TENB does not subsequently remain asserted until the next TSOC, no indication of dropped cell is raised. Only with back-to-back transfers to the same PHY will there be an indication of dropped cell raised. Although no TSOCI is asserted, cell counter values are updated correctly.

The TSOCI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

TPRTYI

The parity error interrupt indicates if a parity error was detected on the TDAT[31:0] input bus. TPRTYI is set high whenever a parity error occurs on the TDAT[31:0] bus. The TRPTYI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

FOVRI

The FIFO overflow interrupt is set high when a write into the channel FIFO is attempted while the FIFO is full. Overrunning the FIFO is considered a system error and should not occur. The FOVRI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

Due to the implemented recovery mechanism from FIFO overflow conditions, overflowing the TUL3 may cause continuous corrupted ATM cells to be transmitted by the device. However, resetting the level2 and level3 channel FIFOs will cause the FIFO to heal and operate properly. This problem occurs on channels configured for ATM cell traffic.

CAMI

The POS-PHY Level 3 channel address mismatch interrupt is set high when the value of TDAT[31:24] does not match the associated value of ATM[7:0] or POS[7:0] during in-band addressing. This interrupt allows the interface to detect when ATM data is being written to a channel configured for POS traffic or when POS data is being written to a channel configured for ATM traffic.

When TENB is asserted, TSX assertion is ignored. CAMI may assert when TENB is asserted and TSX is asserted, indicating that the TSX assertion is being ignored. CAMI will not assert if a valid channel address exists on the bus when TSX and TENB are both asserted.

The CAMI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

TSOCE

The start of cell re-alignment interrupt enable controls the assertion of the INTB output when TSOCI is high. When TSOCE is set high, an interrupt is generated upon assertion event of the TSOCI register. When TSOCE is set low, changes in the TSOCI status do not generate an interrupt.

TPRTYE

The parity error interrupt enable controls the assertion of the INTB output when TPRTYI is high. When TPRTYE is set high, an interrupt is generated upon assertion event of the TPRTYI register. When TPRTYE is set low, changes in the TPRTYI status do not generate an interrupt.

FOVRE

The FIFO overflow interrupt enable controls the assertion of the INTB output when FOVRI is high. When FOVRE is set high, an interrupt is generated upon assertion event of the FOVRI register. When FOVRE is set low, changes in the FOVRI status do not generate an interrupt.

CAME

The FIFO channel address mismatch interrupt enable controls the assertion of the INTB output when CAMI is high. When CAME is set high, an interrupt is generated upon assertion event of the CAMI register. When CAME is set low, changes in the CAMI status do not generate an interrupt.

Register 0x1822: TUL3 Interrupt Status/Enable #2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	UNPROVE	0
Bit 4	R/W	TXOPE	0
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R	UNPROVI	X
Bit 0	R	TXOPI	X

TXOPI

The start or end of packet interrupt is set high when either TSOP or TEOP is not asserted with the first or last word of a POS-PHY packet, respectively. The TXOPI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

UNPROVI

The POS-PHY Level3 unprovisioned address interrupt is set high when the value of TDAT[7:0] addresses a non-existent channel buffer during in-band addressing. This interrupt is asserted when this value is greater than 0x0F. The UNPROVI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. UNPROVI interrupt does not remain asserted even when there is a persistent in-band addressing error. A read of the UNPROVI will clear the interrupt. Hence, continuous in-band addressing error results in only one interrupt.

TXOPE

The start or end of packet interrupt enable controls the assertion of the INTB output when TXOPI is high. When TXOPE is set high, an interrupt is generated upon assertion event of the TXOPI register. When TXOPE is set low, changes in the TXOPI status do not generate an interrupt.

UNPROVE

The unprovisioned address interrupt enable controls the assertion of the INTB output when UNPROVI is high. When UNPROVE is set high, an interrupt is generated upon assertion event of the UNPROVI register. When UNPROVE is set low, changes in the UNPROVI status do not generate an interrupt.

Register 0x1823: TUL3 ATM Level 3 FIFO Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	CELLFORM	0
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	FIFODP[1]	1
Bit 0	R/W	FIFODP[0]	1

FIFODP[1:0]

The FIFODP[1:0] bits determine the channel FIFO level at which TCA deasserts in UTOPIA Level 3 operation. FIFO fill level control may be important in systems where the cell latency through the TUL3-32 must be minimized or when the layer device latency of deasserting TENB is large.

When the channel FIFO is filled to the specified depth, the transmit cell available signal TCA is deasserted. When the FIFO fill level is set below the maximum size of the channel FIFO, the channel FIFO will still accept writes. TCA is asserted when the FIFO depth falls below the level specified by FIFODP[1:0].

FIFODP[1:0] specifies the FIFO full level in number of ATM cells, plus one, in the channel FIFO. Therefore, the FIFO full level may be configured from 1 to 4 ATM cells.

CELLFORM

The CELLFORM bits control the length of transmit Level 3 interface ATM cell structure. When CELLFORM is low, the ATM cell structure is 56 bytes in size (14 TFCLK cycles) and contains the HCS (H5) and HCS Control bytes. When CELLFORM is high, the ATM cell structure is 52 bytes in size (13 TFCLK cycles) and does not contain the HCS and HCS Control bytes.

The value of CELLFORM should be changed only when FIFORST is set high.

Register 0x1824: TUL3 ATM Level 3 Signal Label

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	ATM[7]	0
Bit 6	R/W	ATM[6]	0
Bit 5	R/W	ATM[5]	0
Bit 4	R/W	ATM[4]	0
Bit 3	R/W	ATM[3]	0
Bit 2	R/W	ATM[2]	0
Bit 1	R/W	ATM[1]	0
Bit 0	R/W	ATM[0]	1

ATM[7:0]

The ATM[7:0] bits are used to check the value of TDAT[31:24] when performing in-band addressing in POS-PHY Level 3 operation in the transmit direction. When TSX and TENB are high, the in-band address specifying the channel number is on TDAT[7:0]. In order to prevent confusion between ATM and POS data, TDAT[31:24] may be used to specify the data type for the channel.

For channels configured for packet data, TDAT[31:24] may be set to the value specified by POS[7:0] during in-band addressing. For channels configured for ATM cell data, TDAT[31:24] may be set to the value specified by ATM[7:0] during in-band addressing.

If a channel is configured for ATM traffic and the value of TDAT[31:24] does not match the value of ATM[7:0] during in-band addressing, the CAMI bit is set.

Register 0x1825: TUL3 POS Level 3 FIFO Low Water Mark

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	LWM[6]	0
Bit 5	R/W	LWM[5]	0
Bit 4	R/W	LWM[4]	0
Bit 3	R/W	LWM[3]	0
Bit 2	R/W	LWM[2]	1
Bit 1	R/W	LWM[1]	0
Bit 0	R/W	LWM[0]	0

LWM[6:0]

The LWM[6:0] bits determine the channel FIF0 depth at which PTPA and STPA assert in POS-PHY Level 3 operation. FIFO fill level control may be important when the layer device latency is large.

When the channel FIFO empties to the specified depth, the transmit packet available signals PTPA and STPA are asserted. PTPA and STPA are deasserted based on the FIFO level specified by HWM[6:0]. Together with HWM[6:0], LWM[6:0] provides hysteresis in the toggling of the transmit packet available signal.

LWM[6:0] specifies the FIFO level in the number of double-words (4 bytes). Therefore, the low water mark may be configured from 0 bytes to 508 bytes. For proper operation, the high water mark level must be greater than the low water mark level.

When sending ATM cells over the POS-PHY Level 3 interface, HWM[6:0] together with LWM6:0] do not directly translate to the number of writeable locations in the FIFO as the ATM cells are internally stored at 64 byte entities in the FIFO. For proper operation when sending ATM cells over the POS-PHY Level 3 interface, LWM[6:0] must be configured to at least 52 or 56 bytes, as specified by CELLFORM. Failure to do this will result in a FIFO deadlock with a partial cell stuck in the FIFO and PTPA and STPA deasserted.

Register 0x1826: TUL3 POS Level 3 FIFO High Water Mark

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	HWM[6]	0
Bit 5	R/W	HWM[5]	1
Bit 4	R/W	HWM[4]	1
Bit 3	R/W	HWM[3]	1
Bit 2	R/W	HWM[2]	0
Bit 1	R/W	HWM[1]	0
Bit 0	R/W	HWM[0]	0

HWM[6:0]

The HWM[6:0] bits determine the channel FIF0 depth at which PTPA and STPA deassert in POS-PHY Level 3 operation. FIFO fill level control may be important when the layer device latency is large.

When the channel FIFO is filled to the specified depth, the transmit packet available signals PTPA and STPA are deasserted. TMOD[1:0] is ignored when calculating FIFO depth. Therefore, PTPA and STPA may deassert when end of a packet is within 4 bytes of HWM. PTPA and STPA are asserted based on the FIFO level specified by LWM[6:0]. Together with LWM[6:0], HWM[6:0] provides hysteresis in the toggling of the transmit packet available signal.

HWM[6:0] specifies the FIFO level in the number of double-words (4 bytes). Therefore, the high water mark may be configured from 0 bytes to 508 bytes and must be less than the maximum size of the FIFO. For proper operation, the high water mark level must be greater than the low water mark level.

When sending ATM cells over the POS-PHY Level 3 interface, HWM[6:0] together with LWM[6:0] do not directly translate to the number of writeable locations in the FIFO as the ATM cells are internally stored as 64 byte entities. In general, the HWM[6:0] should be programmed more than 240.

Register 0x1827: TUL3 POS Level 3 Signal Label

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	POS[7]	0
Bit 6	R/W	POS[6]	0
Bit 5	R/W	POS[5]	0
Bit 4	R/W	POS[4]	0
Bit 3	R/W	POS[3]	0
Bit 2	R/W	POS[2]	0
Bit 1	R/W	POS[1]	0
Bit 0	R/W	POS[0]	0

POS[7:0]

The POS[7:0] bits are used to check the value of TDAT[31:24] when performing in-band addressing in POS-PHY Level 3 operation. When TSX and TENB are high, the in-band address specifying the channel number is on TDAT[7:0]. In order to prevent confusion between ATM and POS data, TDAT[31:24] may be used to specify the data type for the channel.

For channels configured for packet data, TDAT[31:24] may be set to the value specified by POS[7:0] during in-band addressing. For channels configured for ATM cell data, TDAT[31:24] may be set to the value specified by ATM[7:0] during in-band addressing.

If a channel is configured for POS traffic and the value of TDAT[31:24] does not match the value of POS[7:0] during in-band addressing, the CAMI bit is set.

Register 0x1829: TUL3 Channel #0Mode Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	FIFORST[0]	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	PATM[0]	0

PATM[0]

The PATM registers configure channels #0 for ATM or packet operation during POS-PHY Level 3 operation in the transmit direction. When SMODE[0] is high and PATM is low, the channel is configured for packet data over the POS-PHY Level 3 interface. When SMODE[0] is high and PATM is high, the channel is configured for ATM cells over the POS-PHY Level 3 interface.

When SMODE[0] is low, PATM must be set low.

When PATM[0] is updated it is required that the corresponding FIFORST[0] be toggled.

FIFORST[0]

The FIFORST registers are used to reset channels #0 four cell/256 byte transmit FIFOs. When FIFORST is set to logic zero, the FIFO operates normally. When FIFORST is set to logic one, the FIFO is immediately emptied and ignores writes. The buffer remains empty and continues to ignore writes until a logic zero is written to FIFORST.

The channel FIFORST registers in the TXCP and TXFP must be set high before FIFORST is asserted. The channel FIFORST registers must be set low after FIFORST is deasserted.

Register 0x182A: TUL3 Channel #1, #5, #9 Mode Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	FIFORST[1]	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	PATM[1]	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

PATM[1]

The PATM registers configure channels #1 for ATM or packet operation during POS-PHY Level 3 operation. When SMODE[0] is high and PATM is low, the channel is configured for packet data over the POS-PHY Level 3 interface. When SMODE[0] is high and PATM is high, the channel is configured for ATM cells over the POS-PHY Level 3 interface.

When SMODE[0] is low, PATM must be set low.

When PATM[1] is updated it is required that the corresponding FIFORST[1] be toggled.

FIFORST[1]

The FIFORST registers are used to reset channels #1 four cell/256 byte transmit FIFOs. When FIFORST is set to logic zero, the FIFO operates normally. When FIFORST is set to logic one, the FIFO is immediately emptied and ignores writes. The buffer remains empty and continues to ignore writes until a logic zero is written to FIFORST.

The channel FIFORST registers in the TXCP and TXFP must be set high before FIFORST is asserted. The channel FIFORST registers must be set low after FIFORST is deasserted.

Register 0x182B: TUL3 Channel #2 Mode Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	FIFORST[2]	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	PATM[2]	0

PATM[2]

The PATM registers configure channels #2 for ATM or packet operation during POS-PHY Level 3 operation. When SMODE[0] is high and PATM is low, the channel is configured for packet data over the POS-PHY Level 3 interface. When SMODE[0] is high and PATM is high, the channel is configured for ATM cells over the POS-PHY Level 3 interface.

When SMODE[0] is low, PATM must be set low.

When PATM[2] is updated it is required that the corresponding FIFORST[2] be toggled.

FIFORST[2]

The FIFORST registers are used to reset channels #2 four cell/256 byte transmit FIFOs. When FIFORST is set to logic zero, the FIFO operates normally. When FIFORST is set to logic one, the FIFO is immediately emptied and ignores writes. The buffer remains empty and continues to ignore writes until a logic zero is written to FIFORST.

The channel FIFORST registers in the TXCP and TXFP must be set high before FIFORST is asserted. The channel FIFORST registers must be set low after FIFORST is deasserted.

Register 0x182C: TUL3 Channel #3 Mode Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	FIFORST[3]	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	PATM[3]	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

PATM[3]

The PATM register configures channel #3 for ATM or packet operation during POS-PHY Level 3 operation. When SMODE[0] is high and PATM is low, the channel is configured for packet data over the POS-PHY Level 3 interface. When SMODE[0] is high and PATM is high, the channel is configured for ATM cells over the POS-PHY Level 3 interface.

When SMODE[0] is low, PATM must be set low.

When PATM[3] is updated it is required that the corresponding FIFORST[3] be toggled.

FIFORST[3]

The FIFORST registers are used to reset channels #3 four cell/256 byte transmit FIFOs. When FIFORST is set to logic zero, the FIFO operates normally. When FIFORST is set to logic one, the FIFO is immediately emptied and ignores writes. The buffer remains empty and continues to ignore writes until a logic zero is written to FIFORST.

The channel FIFORST registers in the TXCP and TXFP must be set high before FIFORST is asserted. The channel FIFORST registers must be set low after FIFORST is deasserted.

Register 0x1830: DLL RUL3 Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	Reserved	0
Bit 3	—	Unused	X
Bit 2	R/W	ERRORE	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The DLL Configuration Register controls the basic operation of the DLL for the receive system interface clock RFCLK.

ERRORE

The DLL error interrupt enable controls the assertion of the INTB output when ERROR is high. When ERRORE is set high, an interrupt is generated upon assertion event of the ERROR register. When ERRORE is set low, changes in the ERROR status do not generate an interrupt.

Register 0x1832: DLL RUL3 Delay Tap Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

Writing to this register performs a software reset of the DLL. Any FIFOs associated with the RFCLK (RUL3, RXCP and RXFP) must be reset using FIFORST after the DLL is reset.

Register 0x1833: DLL RUL3 Control Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	RFCLKI	X
Bit 6	R	Reserved	X
Bit 5	R	ERRORI	X
Bit 4	R	Reserved	X
Bit 3	—	Unused	X
Bit 2	R	ERROR	X
Bit 1	R	Reserved	X
Bit 0	R	RUN	X

The DLL Control Status Register provides information of the DLL operation.

RUN

The DLL lock status register bit RUN indicates the DLL has found an initial lock condition. When the phase detector first indicates lock, RUN is set high. The RUN register bit is cleared only by a system reset or a software reset.

ERROR

The delay line error register ERROR indicates the DLL is currently at the end of the delay line. ERROR is set high when the DLL tries to move beyond the end of the delay line. Once DLL is in ERROR state, the only way to restore the DLL into normal operational state is to reset the DLL.

ERRORI

The error event register bit ERRORI indicates the ERROR register bit has been a logic one. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. The ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

RFCLKI

The clock event register bit RFCLKI provides a method to monitor activity on the RFCLK clock. When the RFCLK input changes from a logic zero to a logic one, the RFCLKI register bit is set to logic one. The RFCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

Register 0x1834: DLL TUL3 Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	Reserved	0
Bit 3	—	Unused	X
Bit 2	R/W	ERRORE	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The DLL Configuration Register controls the basic operation of the DLL for the transmit system interface clock TFCLK.

ERRORE

The DLL error interrupt enable controls the assertion of the INTB output when ERROR is high. When ERRORE is set high, an interrupt is generated upon assertion event of the ERROR register. When ERRORE is set low, changes in the ERROR status do not generate an interrupt.

Register 0x1836: DLL TUL3 Delay Tap Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

Writing to this register performs a software reset of the DLL. Any FIFOs associated with the TFCLK (TUL3, TXCP and TXFP) must be reset using FIFORST after the DLL is reset.

Register 0x1837: DLL TUL3 Control Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	TFCLKI	X
Bit 6	R	Reserved	X
Bit 5	R	ERRORI	X
Bit 4	R	Reserved	X
Bit 3	—	Unused	X
Bit 2	R	ERROR	X
Bit 1	R	Reserved	X
Bit 0	R	RUN	X

The DLL Control Status Register provides information of the DLL operation.

RUN

The DLL lock status register bit RUN indicates the DLL has found an initial lock condition. When the phase detector first indicates lock, RUN is set high. The RUN register bit is cleared only by a system reset or a software reset.

ERROR

The delay line error register ERROR indicates the DLL is currently at the end of the delay line. ERROR is set high when the DLL tries to move beyond the end of the delay line. Once DLL is in ERROR state, the only way to restore the DLL into normal operational state is to reset the DLL.

ERRORI

The error event register bit ERRORI indicates the ERROR register bit has been a logic one. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. The ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

TFCLKI

The clock event register bit TFCLKI provides a method to monitor activity on the TFCLK clock. When the TFCLK input changes from a logic zero to a logic one, the TFCLKI register bit is set to logic one. The TFCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

Register 0x1840: SARC Indirect Address

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM0 path and tributary path (TU3) is accessed by the current indirect transfer. SARC indirect address path (PATH[3:0]) bits must be written to a valid path value before a write access actually transfers data into indirect registers at address 1848H, 1849H, 184AH, 184CH, 184DH and 184EH.

PATH[3:0]	STS-1/STM-0 Path/Tributary Path #
0000	Invalid
0001-1100	Path/Tributary Path #1 to #12
1101-1111	Invalid

Register 0x1848: SARC Path Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	PRDIEN	0
Bit 6	R/W	PERDI20	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	PLOPTREND	0
Bit 3	R/W	PAISPTRCFG[1]	0
Bit 2	R/W	PAISPTRCFG[0]	0
Bit 1	R/W	PLOPTRCFG[1]	0
Bit 0	R/W	PLOPTRCFG[0]	0

PLOPTRCFG[1:0]

The path loss of pointer configuration (PLOPTRCFG[1:0]) bits in conjunction with the path loss of pointer removal (PLOPTREND) bit define the declaration and removal of the LOP-P defect.

Table 46 SARC Declaration and Removal of LOP-P

PLOPTRCFG[1:0]	LOP-P Declaration	LOP-P Removal
00	STS/AU Pointer in LOP state	STS/AU Pointer not in LOP state
01	STS/AU Pointer or concatenated pointer in LOP state	STS/AU Pointer and all concatenated pointers not in LOP state
10	STS/AU Pointer or concatenated pointer in LOP or AIS state	STS/AU Pointer and all concatenated pointers not in LOP or AIS state
11	Reserved	Reserved

PAISPTRCFG[1:0]

The path AIS pointer configuration (PAISPTRCFG[1:0]) bits define the declaration and removal of the AIS-P defect..

Table 47 SARC Declaration and Removal of AIS-P

PAISPTRCFG[1:0]	AIS-P Declaration	AIS-P Removal
00	STS/AU Pointer in AIS state	STS/AU Pointer not in AIS state
01	STS/AU Pointer or concatenated pointer in AIS state	STS/AU Pointer and all concatenated pointers not in AIS state
10	STS/AU Pointer and all concatenated pointers in AIS state	STS/AU Pointer or any concatenated pointer not in AIS state
11	Reserved	Reserved

PLOPTREND

The path loss of pointer removal (PLOPTREND) bit in conjunction with PLOPTRCFG[1:0] bits controls the removal of a LOP-P defect. When PLOPTREND is set to a logic 1, a LOP-P defect is terminated when an AIS-P defect is declared. When PLOPTREND is set to a logic 0, a LOP-P defect is not terminated when an AIS-P defect is declared.

PERDI20

The path enhanced remote defect indication control (PERDI20) bit selects the enhanced RDI-P persistence. When PERDI20 is set to logic 1, a new path enhanced RDI-P defect is transmitted for at least 20 frames. When PERDI20 is set to logic 0, a new path enhanced RDI-P defect is transmitted for at least 10 frames.

PRDIEN

The path remote defect indication enable (PRDIEN) bit selects between the 1 bit RDI-P code and the 3 bit enhanced RDI-P code. When PRDIEN is set to logic 1, the 1 bit RDI-P code is transmitted. When PRDIEN is set to logic 0, the 3 bit enhanced RDI-P code is transmitted.

Register 0x1849: SARC Path RALM Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	PPLMEN	0
Bit 12	R/W	PPLUEN	0
Bit 11	R/W	PTIMEN	0
Bit 10	R/W	PTIUEN	0
Bit 9	R/W	PERDIEN	0
Bit 8	R/W	PRDIEN	0
Bit 7	R/W	PPDIEN	0
Bit 6	R/W	PUNEQEN	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	LCDEN	0
Bit 3	R/W	PAISPTREN	0
Bit 2	R/W	PLOPTREN	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

PLOPTREN

The path loss of pointer enable (PLOPTREN) bit allows the LOP-P defect to be ORed into the RALM output. When the PLOPTREN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PLOPTREN bit is set low, the corresponding defect indication does not affect the RALM output.

PAISPTREN

The path alarm indication signal enable (PAISPTREN) bit allows the AIS-P defect to be ORed into the RALM output. When the PAISPTREN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PAISPTREN bit is set low, the corresponding defect indication does not affect the RALM output.

LCDEN

The loss of cell delineation enable (LCDEN) bit allows the LCD defect to be ORed into the RALM output. When the LCDEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the LCDEN bit is set low, the corresponding defect indication does not affect the RALM output.

PUNEQEN

The path payload unequipped enable (PUNEQEN) bit allows the UNUEQ-P defect to be ORed into the RALM output. When the PUNEQEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PUNEQEN bit is set low, the corresponding defect indication does not affect the RALM output.

PPDIEN

The path payload defect indication enable (PPDIEN) bit allows the PDI-P defect to be ORed into the RALM output. When the PPDIEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PPDIEN bit is set low, the corresponding defect indication does not affect the RALM output.

PRDIEN

The path remote defect indication enable (PRDIEN) bit allows the RDI-P defect indication defect to be ORed into the RALM output. When the PRDIEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PRDIEN bit is set low, the corresponding defect indication does not affect the RALM output.

PERDIEN

The path enhanced remote defect indication enable (PERDIEN) bit allows the enhanced RDI-P defect to be ORed into the RALM output. When the PERDIEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PERDIEN bit is set low, the corresponding defect indication does not affect the RALM output.

PTIUEN

The path trace identifier unstable enable (PTIUEN) bit allows the TIU-P defect to be ORed into the RALM output. When the PTIUEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PTIUEN bit is set low, the corresponding defect indication does not affect the RALM output.

PTIMEN

The path trace identifier mismatch enable (PTIMEN) bit allows the TIM-P defect to be ORed into the RALM output. When the PTIMEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PTIMEN bit is set low, the corresponding defect indication does not affect the RALM output.

PPLUEN

The path payload label unstable enable (PPLUEN) bit allows the PLU-P defect to be ORed into the RALM output. When the PPLUEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PPLUEN bit is set low, the corresponding defect indication does not affect the RALM output.

PPLMEN

The path payload label mismatch enable (PPLMEN) bit allows the PLM-P defect to be ORed into the RALM output. When the PPLMEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PPLMEN bit is set low, the corresponding defect indication does not affect the RALM output.

Register 0x184A: SARC Path Downstream AIS-P Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	PPLMEN	0
Bit 12	R/W	PPLUEN	0
Bit 11	R/W	PTIMEN	0
Bit 10	R/W	PTIUEN	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	PPDIEN	0
Bit 6	R/W	PUNEQEN	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	PAISPTREN	0
Bit 2	R/W	PLOPTREN	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

PLOPTREN

The path loss of pointer enable (PLOPTREN) bit allows the LOP-P defect to be ORed into the downstream AIS-P generation. When the PLOPTREN bit is set high, the corresponding defect indication is ORed with other defect indications to enable downstream AIS-P generation. When the PLOPTREN bit is set low, the corresponding defect indication does not enable downstream AIS-P generation.

PAISPTREN

The path alarm indication signal enable (PAISEN) bit allows the AIS-P defect to be ORed into the downstream AIS-P generation. When the PAISPTREN bit is set high, the corresponding defect indication is ORed with other defect indications to enable downstream AIS-P generation. When the PAISPTREN bit is set low, the corresponding defect indication does not enable downstream AIS-P generation.

PUNEQEN

The path payload unequipped enable (PUNEQEN) bit allows the UNEQ-P defect to be ORed into the downstream AIS-P generation. When the PUNEQEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable downstream AIS-P generation. When the PUNEQEN bit is set low, the corresponding defect indication does not enable downstream AIS-P generation.

PPDIEN

The payload defect indication enable (PPDIEN) bit allows the PDI-P defect indication defect to be ORed into the downstream AIS-P generation. When the PPDIEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable downstream AIS-P generation. When the PPDIEN bit is set low, the corresponding defect indication does not enable downstream AIS-P generation.

PTIUEN

The path trace identifier unstable enable (PTIUEN) bit allows the TIU-P defect to be ORed into the downstream AIS-P generation. When the PTIUEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable downstream AIS-P generation. When the PTIUEN bit is set low, the corresponding defect indication does not enable downstream AIS-P generation.

PTIMEN

The path trace identifier mismatch enable (PTIMEN) bit allows the TIM-P defect to be ORed into the downstream AIS-P generation. When the PTIMEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable downstream AIS-P generation. When the PTIMEN bit is set low, the corresponding defect indication does not enable downstream AIS-P generation.

PPLUEN

The path payload label unstable enable (PPLUEN) bit allows the PLU-P defect to be ORed into the downstream AIS-P generation. When the PPLUEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable downstream AIS-P generation. When the PPLUEN bit is set low, the corresponding defect indication does not enable downstream AIS-P generation.

PPLMEN

The path payload label mismatch enable (PPLMEN) bit allows the PLM-P defect to be ORed into the downstream AIS-P generation. When the PPLMEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable downstream AIS-P generation. When the PPLMEN bit is set low, the corresponding defect indication does not enable downstream AIS-P generation.

Register 0x184B: SARC TU3 Tributary Path Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	PRDIEN	0
Bit 6	R/W	PERDI20	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	PLOPTREND	0
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R/W	PLOPTRCFG	0
Bit 0	—	Unused	X

PLOPTRCFG

The tributary path loss of pointer configuration (PLOPTRCFG[1:0]) bits in conjunction with the tributary path loss of pointer removal (PLOPTREND) bit define the declaration and removal of the LOP-V defect.

Table 48 SARC Declaration and Removal of LOP-V

PLOPTRCFG	LOP-V Declaration	LOP-V Removal
0	TU Pointer in LOP state	TU Pointer not in LOP state
1	TU Pointer in LOP or AIS state	TU Pointer not in LOP or AIS state

PLOPTREND

The tributary path loss of pointer removal (PLOPTREND) bit in conjunction with the PLOPTRCFG bit controls the removal of a LOP-V defect. When PLOPTREND is set to a logic 1, a LOP-V defect is terminated when an AIS-V defect is declared. When PLOPTREND is set to a logic 0, a LOP-V defect is not terminated when an AIS-V defect is declared.

PERDI20

The tributary path enhanced remote defect indication control (PERDI20) bit selects the enhanced RDI-V persistence. When PERDI20 is set to logic 1, a new tributary path enhanced RDI-V defect is transmitted for at least 20 frames. When PERDI20 is set to logic 0, a new tributary path enhanced RDI-V defect is transmitted for at least 10 frames.

PRDIEN

The tributary path remote defect indication enable (PRDIEN) bit selects between the 1 bit RDI-V code and the 3 bit enhanced RDI-V code. When PRDIEN is set to logic 1, the 1 bit RDI-V code is transmitted. When PRDIEN is set to logic 0, the 3 bit enhanced RDI-V code is transmitted.

Register 0x184C: SARC TU3 Tributary Path RALM Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	PPLMEN	0
Bit 12	R/W	PPLUEN	0
Bit 11	R/W	PTIMEN	0
Bit 10	R/W	PTIUEN	0
Bit 9	R/W	PERDIEN	0
Bit 8	R/W	PRDIEN	0
Bit 7	R/W	PPDIEN	0
Bit 6	R/W	PUNEQEN	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	LCDEN	0
Bit 3	R/W	PAISPTREN	0
Bit 2	R/W	PLOPTREN	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

PLOPTREN

The tributary path loss of pointer enable (PLOPTREN) bit allows the LOP-V defect to be ORed into the RALM output. When the PLOPTREN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PLOPTREN bit is set low, the corresponding defect indication does not affect the RALM output.

PAISPTREN

The tributary path alarm indication signal enable (PAISPTREN) bit allows the AIS-V defect to be ORed into the RALM output. When the PAISPTREN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PAISPTREN bit is set low, the corresponding defect indication does not affect the RALM output.

LCDEN

The loss of cell delineation enable (LCDEN) bit allows the LCD defect to be ORed into the RALM output. When the LCDEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the LCDEN bit is set low, the corresponding defect indication does not affect the RALM output.

PUNEQEN

The tributary path payload unequipped enable (PUNEQEN) bit allows the UNUEQ-V defect to be ORed into the RALM output. When the PUNEQEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PUNEQEN bit is set low, the corresponding defect indication does not affect the RALM output.

PPDIEN

The tributary path payload defect indication enable (PPDIEN) bit allows the PDI-V defect to be ORed into the RALM output. When the PPDIEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PPDIEN bit is set low, the corresponding defect indication does not affect the RALM output.

PRDIEN

The tributary path remote defect indication enable (PRDIEN) bit allows the RDI-V defect indication defect to be ORed into the RALM output. When the PRDIEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PRDIEN bit is set low, the corresponding defect indication does not affect the RALM output.

PERDIEN

The tributary path enhanced remote defect indication enable (PERDIEN) bit allows the enhanced RDI-V defect to be ORed into the RALM output. When the PERDIEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PERDIEN bit is set low, the corresponding defect indication does not affect the RALM output.

PTIUEN

The tributary path trace identifier unstable enable (PTIUEN) bit allows the TIU-V defect to be ORed into the RALM output. When the PTIUEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PTIUEN bit is set low, the corresponding defect indication does not affect the RALM output.

PTIMEN

The tributary path trace identifier mismatch enable (PTIMEN) bit allows the TIM-V defect to be ORed into the RALM output. When the PTIMEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PTIMEN bit is set low, the corresponding defect indication does not affect the RALM output.

PPLUEN

The tributary path payload label unstable enable (PPLUEN) bit allows the PLU-V defect to be ORed into the RALM output. When the PPLUEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PPLUEN bit is set low, the corresponding defect indication does not affect the RALM output.

PPLMEN

The tributary path payload label mismatch enable (PPLMEN) bit allows the PLM-V defect to be ORed into the RALM output. When the PPLMEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PPLMEN bit is set low, the corresponding defect indication does not affect the RALM output.

Register 0x184D: SARC TU3 Tributary Path Downstream AIS-V Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	PPLMEN	0
Bit 12	R/W	PPLUEN	0
Bit 11	R/W	PTIMEN	0
Bit 10	R/W	PTIUEN	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	PPDIEN	0
Bit 6	R/W	PUNEQEN	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	PAISPTREN	0
Bit 2	R/W	PLOPTREN	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

PLOPTREN

The tributary path loss of pointer enable (PLOPTREN) bit allows the LOP-V defect to be ORed into the downstream AIS-V generation. When the PLOPTREN bit is set high, the corresponding defect indication is ORed with other defect indications to enable downstream AIS-V generation. When the PLOPTREN bit is set low, the corresponding defect indication does not enable downstream AIS-V generation.

PAISPTREN

The tributary path alarm indication signal enable (PAISEN) bit allows the AIS-V defect to be ORed into the downstream AIS-V generation. When the PAISPTREN bit is set high, the corresponding defect indication is ORed with other defect indications to enable downstream AIS-V generation. When the PAISPTREN bit is set low, the corresponding defect indication does not enable downstream AIS-V generation.

PUNEQEN

The tributary path payload unequipped enable (PUNEQEN) bit allows the UNEQ-V defect to be ORed into the downstream AIS-V generation. When the PUNEQEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable downstream AIS-V generation. When the PUNEQEN bit is set low, the corresponding defect indication does not enable downstream AIS-V generation.

PPDIEN

The payload defect indication enable (PPDIEN) bit allows the PDI-V defect indication defect to be ORed into the downstream AIS-V generation. When the PPDIEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable downstream AIS-V generation. When the PPDIEN bit is set low, the corresponding defect indication does not enable downstream AIS-V generation.

PTIUEN

The tributary path trace identifier unstable enable (PTIUEN) bit allows the TIU-V defect to be ORed into the downstream AIS-V generation. When the PTIUEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable downstream AIS-V generation. When the PTIUEN bit is set low, the corresponding defect indication does not enable downstream AIS-V generation.

PTIMEN

The tributary path trace identifier mismatch enable (PTIMEN) bit allows the TIM-V defect to be ORed into the downstream AIS-V generation. When the PTIMEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable downstream AIS-V generation. When the PTIMEN bit is set low, the corresponding defect indication does not enable downstream AIS-V generation.

PPLUEN

The tributary path payload label unstable enable (PPLUEN) bit allows the PLU-V defect to be ORed into the downstream AIS-V generation. When the PPLUEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable downstream AIS-V generation. When the PPLUEN bit is set low, the corresponding defect indication does not enable downstream AIS-V generation.

PPLMEN

The tributary path payload label mismatch enable (PPLMEN) bit allows the PLM-V defect to be ORed into the downstream AIS-V generation. When the PPLMEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable downstream AIS-V generation. When the PPLMEN bit is set low, the corresponding defect indication does not enable downstream AIS-V generation.

Register 0x1850: SARC Path LOP-P Pointer Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	PLOPTRV[12]	X
Bit 10	R	PLOPTRV[11]	X
Bit 9	R	PLOPTRV[10]	X
Bit 8	R	PLOPTRV[9]	X
Bit 7	R	PLOPTRV[8]	X
Bit 6	R	PLOPTRV[7]	X
Bit 5	R	PLOPTRV[6]	X
Bit 4	R	PLOPTRV[5]	X
Bit 3	R	PLOPTRV[4]	X
Bit 2	R	PLOPTRV[3]	X
Bit 1	R	PLOPTRV[2]	X
Bit 0	R	PLOPTRV[1]	X

PLOPTRV[12:1]

The path loss of pointer status (PLOPTRV[12:1]) bits indicate the current status of the LOP-P defect for STS-1/STM0 paths #1 to #12. PLOPTRV[x] is set to logic 1 when the LOP-P defect is declared. PLOPTRV[x] is set to logic zero when the LOP-P defect is removed.

The PLOPTRCFG[1:0] register bits (address 0x1848) in conjunction with the PLOPTREND register bit (address 0x1848) determine the declaration and removal of the LOP-P defect as illustrated in Table 46.

Register 0x1851: SARC Path LOP-P Pointer Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	PLOPTRE[12]	0
Bit 10	R/W	PLOPTRE[11]	0
Bit 9	R/W	PLOPTRE[10]	0
Bit 8	R/W	PLOPTRE[9]	0
Bit 7	R/W	PLOPTRE[8]	0
Bit 6	R/W	PLOPTRE[7]	0
Bit 5	R/W	PLOPTRE[6]	0
Bit 4	R/W	PLOPTRE[5]	0
Bit 3	R/W	PLOPTRE[4]	0
Bit 2	R/W	PLOPTRE[3]	0
Bit 1	R/W	PLOPTRE[2]	0
Bit 0	R/W	PLOPTRE[1]	0

PLOPTRE[12:1]

The path loss of pointer interrupt enable (PLOPTRE[12:1]) bits control the activation of INTB for STS-1/STM-0 paths #1 to #12. When PLOPTRE[x] is set to logic 1, the corresponding pending interrupt will deassert INTB. When PLOPTRE[x] is set to logic 0, the corresponding pending interrupt will not deassert INTB.

Register 0x1852: SARC Path LOP-P Pointer Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	PLOPTRI[12]	X
Bit 10	R	PLOPTRI[11]	X
Bit 9	R	PLOPTRI[10]	X
Bit 8	R	PLOPTRI[9]	X
Bit 7	R	PLOPTRI[8]	X
Bit 6	R	PLOPTRI[7]	X
Bit 5	R	PLOPTRI[6]	X
Bit 4	R	PLOPTRI[5]	X
Bit 3	R	PLOPTRI[4]	X
Bit 2	R	PLOPTRI[3]	X
Bit 1	R	PLOPTRI[2]	X
Bit 0	R	PLOPTRI[1]	X

PLOPTRI[12:1]

The path loss of pointer interrupt status (PLOPTRI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. PLOPTRI[x] is set to logic 1 to indicate any changes in the status of PLOPTRV[x]. These interrupt status bits are independent of the interrupt enable bits. When WCIMODE is low (read mode), PLOPTRI[x] is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PLOPTRI[x] is cleared by writing a high value to bit x of the interrupt status register.

Register 0x1853: SARC Path AIS-P Pointer Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	PAISPTRV[12]	X
Bit 10	R	PAISPTRV[11]	X
Bit 9	R	PAISPTRV[10]	X
Bit 8	R	PAISPTRV[9]	X
Bit 7	R	PAISPTRV[8]	X
Bit 6	R	PAISPTRV[7]	X
Bit 5	R	PAISPTRV[6]	X
Bit 4	R	PAISPTRV[5]	X
Bit 3	R	PAISPTRV[4]	X
Bit 2	R	PAISPTRV[3]	X
Bit 1	R	PAISPTRV[2]	X
Bit 0	R	PAISPTRV[1]	X

PAISPTRV[12:1]

The path alarm indication signal pointer status (PAISTRV[12:1]) bits indicate the current status of the AIS-P defect for STS-1/STM-0 paths #1 to #12. PAISPTRV[x] is set to logic 1 when the AIS-P defect is declared. PAISPTRV[x] is set to logic zero when the AIS-P defect is removed.

The PAISTRCFG[1:0] register bits (address 0x1848) determines the declaration and removal of the AIS-P defect as illustrated in Table 47.

Register 0x1854: SARC Path AIS-P Pointer Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	PAISPTRE[12]	0
Bit 10	R/W	PAISPTRE[11]	0
Bit 9	R/W	PAISPTRE[10]	0
Bit 8	R/W	PAISPTRE[9]	0
Bit 7	R/W	PAISPTRE[8]	0
Bit 6	R/W	PAISPTRE[7]	0
Bit 5	R/W	PAISPTRE[6]	0
Bit 4	R/W	PAISPTRE[5]	0
Bit 3	R/W	PAISPTRE[4]	0
Bit 2	R/W	PAISPTRE[3]	0
Bit 1	R/W	PAISPTRE[2]	0
Bit 0	R/W	PAISPTRE[1]	0

PAISPTRE[12:1]

The path alarm indication signal pointer interrupt enable (PAISPTRE[12:1]) bits control the activation of INTB for STS-1/STM-0 paths #1 to #12. When PAISPTRE[x] is set to logic 1, the corresponding pending interrupt will deassert INTB. When PAISPTRE[x] is set to logic 0, the corresponding pending interrupt will not deassert INTB.

Register 0x1855: SARC Path AIS-P Pointer Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	PAISPTRI[12]	X
Bit 10	R	PAISPTRI[11]	X
Bit 9	R	PAISPTRI[10]	X
Bit 8	R	PAISPTRI[9]	X
Bit 7	R	PAISPTRI[8]	X
Bit 6	R	PAISPTRI[7]	X
Bit 5	R	PAISPTRI[6]	X
Bit 4	R	PAISPTRI[5]	X
Bit 3	R	PAISPTRI[4]	X
Bit 2	R	PAISPTRI[3]	X
Bit 1	R	PAISPTRI[2]	X
Bit 0	R	PAISPTRI[1]	X

PAISPTRI[12:1]

The path alarm indication signal pointer interrupt status (PAISPTRI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. PAISPTRI[x] is set to logic 1 to indicate any changes in the status of PAISPTRV[x]. These interrupt status bits are independent of the interrupt enable bits. When WCIMODE is low (read mode), PAISPTRI[x] is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PAISPTRI[x] is cleared by writing a high value to bit x of the interrupt status register.

Register 0x1858: SARC TU3 Tributary Path LOP-V Pointer Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	PLOPTRV[12]	X
Bit 10	R	PLOPTRV[11]	X
Bit 9	R	PLOPTRV[10]	X
Bit 8	R	PLOPTRV[9]	X
Bit 7	R	PLOPTRV[8]	X
Bit 6	R	PLOPTRV[7]	X
Bit 5	R	PLOPTRV[6]	X
Bit 4	R	PLOPTRV[5]	X
Bit 3	R	PLOPTRV[4]	X
Bit 2	R	PLOPTRV[3]	X
Bit 1	R	PLOPTRV[2]	X
Bit 0	R	PLOPTRV[1]	X

PLOPTRV[12:1]

The tributary path loss of pointer status (PLOPTRV[12:1]) bits indicate the current status of the LOP-V defect for STS-1/STM-0 tributary paths #1 to #12. PLOPTRV[x] is set to logic 1 when the LOP-V defect is declared. PLOPTRV[x] is set to logic zero when the LOP-V defect is removed.

The PLOPTRCFG register bits (address 0x184B) in conjunction with the PLOPTREND register bit (address 0x184B) determine the declaration and removal of the LOP-V defect as illustrated in Table 48.

Register 0x1859: SARC TU3 Tributary Path LOP-V Pointer Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	PLOPTRE[12]	0
Bit 10	R/W	PLOPTRE[11]	0
Bit 9	R/W	PLOPTRE[10]	0
Bit 8	R/W	PLOPTRE[9]	0
Bit 7	R/W	PLOPTRE[8]	0
Bit 6	R/W	PLOPTRE[7]	0
Bit 5	R/W	PLOPTRE[6]	0
Bit 4	R/W	PLOPTRE[5]	0
Bit 3	R/W	PLOPTRE[4]	0
Bit 2	R/W	PLOPTRE[3]	0
Bit 1	R/W	PLOPTRE[2]	0
Bit 0	R/W	PLOPTRE[1]	0

PLOPTRE[12:1]

The tributary path loss of pointer interrupt enable (PLOPTRE[12:1]) bits control the activation of INTB for STS-1/STM-0 tributary paths #1 to #12. When PLOPTRE[x] is set to logic 1, the corresponding pending interrupt will deassert INTB. When PLOPTRE[x] is set to logic 0, the corresponding pending interrupt will not deassert INTB.

Register 0x185A: SARC TU3 Tributary Path LOP-V Pointer Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	PLOPTRI[12]	X
Bit 10	R	PLOPTRI[11]	X
Bit 9	R	PLOPTRI[10]	X
Bit 8	R	PLOPTRI[9]	X
Bit 7	R	PLOPTRI[8]	X
Bit 6	R	PLOPTRI[7]	X
Bit 5	R	PLOPTRI[6]	X
Bit 4	R	PLOPTRI[5]	X
Bit 3	R	PLOPTRI[4]	X
Bit 2	R	PLOPTRI[3]	X
Bit 1	R	PLOPTRI[2]	X
Bit 0	R	PLOPTRI[1]	X

PLOPTRI[12:1]

The tributary path loss of pointer interrupt status (PLOPTRI[12:1]) bits are event indicators for STS-1/STM-0 tributary paths #1 to #12. PLOPTRI[x] is set to logic 1 to indicate any changes in the status of PLOPTRV[x]. These interrupt status bits are independent of the interrupt enable bits. When WCIMODE is low (read mode), PLOPTRI[x] is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PLOPTRI[x] is cleared by writing a high value to bit x of the interrupt status register.

Register 0x185B: SARC TU3 Tributary Path AIS-V Pointer Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	PAISPTRV[12]	X
Bit 10	R	PAISPTRV[11]	X
Bit 9	R	PAISPTRV[10]	X
Bit 8	R	PAISPTRV[9]	X
Bit 7	R	PAISPTRV[8]	X
Bit 6	R	PAISPTRV[7]	X
Bit 5	R	PAISPTRV[6]	X
Bit 4	R	PAISPTRV[5]	X
Bit 3	R	PAISPTRV[4]	X
Bit 2	R	PAISPTRV[3]	X
Bit 1	R	PAISPTRV[2]	X
Bit 0	R	PAISPTRV[1]	X

PAISPTRV[12:1]

The tributary path alarm indication signal pointer status (PAISTRV[12:1]) bits indicate the current status of the AIS-V defect for STS-1/STM-0 tributary paths #1 to #12. PAISPTRV[x] is set to logic 1 when the AIS-V defect is declared. PAISPTRV[x] is set to logic zero when the AIS-V defect is removed.

Register 0x185C: SARC TU3 Tributary Path AIS-V Pointer Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	PAISPTRE[12]	0
Bit 10	R/W	PAISPTRE[11]	0
Bit 9	R/W	PAISPTRE[10]	0
Bit 8	R/W	PAISPTRE[9]	0
Bit 7	R/W	PAISPTRE[8]	0
Bit 6	R/W	PAISPTRE[7]	0
Bit 5	R/W	PAISPTRE[6]	0
Bit 4	R/W	PAISPTRE[5]	0
Bit 3	R/W	PAISPTRE[4]	0
Bit 2	R/W	PAISPTRE[3]	0
Bit 1	R/W	PAISPTRE[2]	0
Bit 0	R/W	PAISPTRE[1]	0

PAISPTRE[12:1]

The tributary path alarm indication signal pointer interrupt enable (PAISPTRE[12:1]) bits control the activation of INTB for STS-1/STM-0 tributary paths #1 to #12. When PAISPTRE[x] is set to logic 1, the corresponding pending interrupt will deassert INTB. When PAISPTRE[x] is set to logic 0, the corresponding pending interrupt will not deassert INTB.

Register 0x185D: SARC TU3 Tributary Path AIS-V Pointer Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	PAISPTRI[12]	X
Bit 10	R	PAISPTRI[11]	X
Bit 9	R	PAISPTRI[10]	X
Bit 8	R	PAISPTRI[9]	X
Bit 7	R	PAISPTRI[8]	X
Bit 6	R	PAISPTRI[7]	X
Bit 5	R	PAISPTRI[6]	X
Bit 4	R	PAISPTRI[5]	X
Bit 3	R	PAISPTRI[4]	X
Bit 2	R	PAISPTRI[3]	X
Bit 1	R	PAISPTRI[2]	X
Bit 0	R	PAISPTRI[1]	X

PAISPTRI[12:1]

The tributary path alarm indication signal pointer interrupt status (PAISPTRI[12:1]) bits are event indicators for STS-1/STM-0 tributary paths #1 to #12. PAISPTRI[x] is set to logic 1 to indicate any changes in the status of PAISPTRV[x]. These interrupt status bits are independent of the interrupt enable bits. When WCIMODE is low (read mode), PAISPTRI[x] is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PAISPTRI[x] is cleared by writing a high value to bit x of the interrupt status register.

Register 0x1880: RHPP Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The STS-1/STM0 path (PATH[3:0]) bits select which STS-1/STM0 path is accessed by the current indirect transfer.

PATH[3:0]	STS-1/STM-0 Path #
0000	Invalid
0001-1100	Path #1 to #12
1101-1111	Invalid

IADDR[3:0]

The indirect address location (IADDR[3:0]) bits select which address location is accessed by the current indirect transfer.

Indirect Address IADDR[3:0]	Indirect Data
0000	Pointer Interpreter Configuration
0001	Error Monitor Configuration
0010	Pointer Value and ERDI
0011	Captured and Accepted PSL
0100	Expected PSL and PDI
0101	Pointer Interpreter status
0110	Path BIP Error Counter

Indirect Address IADDR[3:0]	Indirect Data
0111	Path REI Error Counter
1000	Path Negative Justification Event Counter
1001	Path Positive Justification Event Counter
1010 to 1111	Unused

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

The maximum busy bit set time is 22 ICLK cycles.

Register 0x1881: RHPP Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Indirect Register 0x00: RHPP Pointer Interpreter Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	NDFCNT	0
Bit 4	R/W	INVCNT	0
Bit 3	R/W	RELAYPAIS	0
Bit 2	R/W	JUST3DIS	0
Bit 1	R/W	SSEN	0
Bit 0	—	Unused	X

SSEN

The SS bits enable (SSEN) bit selects whether or not the SS bits are taking into account in the pointer interpreter state machine. When SSEN is set to logic 1, the SS bits must be set to 10 for a valid NORM_POINT, NDF_ENABLE, INC_IND, DEC_IND or NEW_POINT indication. When SSEN is set to logic 0, the SS bits are ignored.

JUST3DIS

The “justification more than 3 frames ago disable” (JUST3DIS) bit selects whether or not the NDF_ENABLE, INC_IND or DEC_IND pointer justifications must be more than 3 frames apart to be considered valid. When JUST3DIS is set to logic 0, the previous NDF_ENABLE, INC_IND or DEC_IND indication must be more than 3 frames ago or the present NDF_ENABLE, INC_IND or DEC_IND indication is considered an INV_POINT indication. When JUST3DIS is set to logic 1, NDF_ENABLE, INC_IND or DEC_IND indication can be every frame.

RELAYPAIS

The relay path AIS (RELAYPAIS) bit selects the condition to enter the path AIS state in the pointer interpreter state machine. When RELAYPAIS is set to logic 1, the path AIS state is entered with 1 X AIS_ind indication. When RELAYPAIS is set to logic 0, the path AIS state is entered with 3 X AIS_ind indications. This configuration bit also affects the concatenation pointer interpreter state machine.

INVCNT

The invalid counter (INVCNT) bit selects the behavior of the consecutive INV_POINT event counter in the pointer interpreter state machine. When INVCNT is set to logic 1, the consecutive INV_POINT event counter is reset by 3 EQ_NEW_POINT indications. When INVCNT is set to logic 0, the counter is not reset by 3 EQ_NEW_POINT indications.

NDFCNT

The new data flag counter (NDFCNT) bit selects the behavior of the consecutive NDF_ENABLE event counter in the pointer interpreter state machine. When NDFCNT is set to logic 1, the NDF_ENABLE definition is enabled NDF + SS. When NDFCNT is set to logic 0, the NDF_ENABLE definition is enabled NDF + SS + offset value in the range 0 to 782 (764 in TU3 mode). This configuration bit only changes the NDF_ENABLE definition for the consecutive NDF_ENABLE even counter to count towards LOP-P defect when the pointer is out of range, this configuration bit does not change the NDF_ENABLE definition for pointer justification.

Indirect Register 0x01: RHPP Error Monitor Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	B3EONRPOH	0
Bit 10	R/W	IPREIBLK	0
Bit 9	R/W	IBER	0
Bit 8	R/W	PREIBLKACC	0
Bit 7	R/W	B3EBLK	0
Bit 6	R/W	PBIPEBLKREI	0
Bit 5	R/W	PBIPEBLKACC	0
Bit 4	R/W	FSBIPDIS	0
Bit 3	R/W	PRDI10	0
Bit 2	R/W	PLMEND	0
Bit 1	R/W	PSL5	0
Bit 0	R/W	ALGO2	0

ALGO2

The payload signal label algorithm 2 (ALGO2) bit selects the algorithm for the PSL monitoring. When ALGO2 is set to logic 1, the ITU compliant algorithm is (algorithm 2) is used to monitor the PSL. When ALGO2 is set to logic 0, the BELLCORE compliant algorithm (algorithm 1) is used to monitor the PSL. ALGO2 changes the PLU-P, PLM-P and PDI-P defect definitions but has no effect on UNEQ-P defect, accepted PSL and change of PSL definitions.

PSL5

The payload signal label detection (PSL5) bit selects the path PSL persistence. When PSL5 is set to logic 1, a new PSL is accepted when the same PSL value is detected in the C2 byte for five consecutive frames. When PSL5 is set to logic 0, a new PSL is accepted when the same PSL value is detected in the C2 byte for three consecutive frames.

PLMEND

The payload label mismatch removal (PLMEND) bit controls the removal of a PLM-P defect when an UNEQ-P defect is declared. When PLMEND is set to logic 1, a PLM-P defect is terminated when an UNEQ-P defect is declared. When PLMEND is set to logic 0, a PLM-P defect is not terminated when an UNEQ-P defect is declared.

PRDI10

The path remote defect indication detection (PRDI10) bit selects the RDI-P and enhanced RDI-P persistence. When PRDI10 is set to logic 1, RDI-P and enhanced RDI-P are accepted when the same pattern is detected in bits 5, 6, and 7 of the G1 byte for ten consecutive frames. When PRDI10 is set to logic 0, RDI-P and enhanced RDI-P are accepted when the same pattern is detected in bits 5, 6, and 7 of the G1 byte for five consecutive frames.

FSBIPDIS

The disable fixed stuff columns during BIP-8 calculation (FSBIPDIS) bit controls the path BIP-8 calculation for an STS-1 (VC-3) payload. When FSBIPDIS is set to logic 1, the fixed stuff columns are not part of the BIP-8 calculation when processing an STS-1 (VC-3) payload. When FSBIPDIS is set to logic 0, the fixed stuff columns are part of the BIP-8 calculation when processing an STS-1 (VC-3) payload.

PBIPEBLKACC

The path block BIP-8 errors accumulation (PBIPEBLKACC) bit controls the accumulation of path BIP-8 errors. When PBIPEBLKACC is set to logic 1, the path BIP-8 error accumulation represents block BIP-8 errors (a maximum of 1 error per frame). When PBIPEBLKACC is set to logic 0, the path BIP-8 error accumulation represents BIP-8 errors (a maximum of 8 errors per frame).

PBIPEBLKREI

The path block BIP-8 errors (PBIPEBLKREI) bit controls the path REI error returned to the THPP. When PBIPEBLKREI is set to logic 1, the path REI is updated with block BIP-8 errors (a maximum of 1 error per frame). When PBIPEBLKREI is set to logic 0, the path REI is updated with BIP-8 errors (a maximum of 8 errors per frame).

B3EBLK

The serial path block BIP-8 errors (B3EBLK) bit controls the indication of path BIP-8 errors on the B3E serial output. When B3EBLK is set to logic 1, B3E outputs block BIP-8 errors (a maximum of 1 error per frame). When B3EBLK is set to logic 0, B3E outputs BIP-8 errors (a maximum of 8 errors per frame).

PREIBLKACC

The path block REI errors accumulation (PREIBLKACC) bit controls the accumulation of path REI errors from the path status (G1) byte. When PREIBLK is set to logic 1, the extracted path REI errors are interpreted as block BIP-8 errors (a maximum of 1 error per frame). When PREIBLK is set to logic 0, the extracted path REI errors are interpret as BIP-8 errors (a maximum of 8 errors per frame).

IBER

The in-band error reporting (IBER) bit controls the in-band regeneration of the path status (G1) byte. When IBER is set to logic 1, the path status byte is updated with the REI-P and the enhanced RDI-P defects that must be returned to the far end. When IBER is set to logic 0, the path status byte is not altered.

IPREIBLK

The in-band path REI block errors (IPREIBLK) bit controls the regeneration of the path REI errors in the path status (G1) byte. When IPREIBLK is set to logic 1, the path REI is updated with block BIP-8 errors (a maximum of 1 error per frame). When IPREIBLK is set to logic 0, the path REI is updated with BIP-8 errors (a maximum of 8 errors per frame).

B3EONRPOH

The B3EONRPOH bit controls the data presented on RPOH. When set to logic 0, the received B3 byte is placed on RPOH. When set to logic 1, the B3 error count is placed on RPOH as well as B3E.

Indirect Register 0x02: RHPP Pointer value and ERDI

Bit	Type	Function	Default
Bit 15	R	PERDIV[2]	X
Bit 14	R	PERDIV[1]	X
Bit 13	R	PERDIV[0]	X
Bit 12	—	Unused	X
Bit 11	R	SSV[1]	X
Bit 10	R	SSV[0]	X
Bit 9	R	PTRV[9]	X
Bit 8	R	PTRV[8]	X
Bit 7	R	PTRV[7]	X
Bit 6	R	PTRV[6]	X
Bit 5	R	PTRV[5]	X
Bit 4	R	PTRV[4]	X
Bit 3	R	PTRV[3]	X
Bit 2	R	PTRV[2]	X
Bit 1	R	PTRV[1]	X
Bit 0	R	PTRV[0]	X

PTRV[9:0]

The path pointer value (PTRV[9:0]) bits represent the current STS/AU pointer being processed by the pointer interpreter state machine or by the concatenation pointer interpreter state machine.

SSV[1:0]

The SS value (SSV[1:0]) bits represent the current SS bits being processed by the pointer interpreter state machine or by the concatenation pointer interpreter state machine.

PERDIV[2:0]

The path enhanced remote defect indication value (PERDIV[2:0]) bits represent the filtered path enhanced remote defect indication value. PERDIV[2:0] is updated when the same enhanced RDI pattern is detected in bits 5, 6, and 7 of the G1 byte for five or ten consecutive frames (selectable with the PRDI10 register bit).

Indirect Register 0x03: RHPP captured and accepted PSL

Bit	Type	Function	Default
Bit 15	R	CPSLV[7]	X
Bit 14	R	CPSLV[6]	X
Bit 13	R	CPSLV[5]	X
Bit 12	R	CPSLV[4]	X
Bit 11	R	CPSLV[3]	X
Bit 10	R	CPSLV[2]	X
Bit 9	R	CPSLV[1]	X
Bit 8	R	CPSLV[0]	X
Bit 7	R	APSLV[7]	X
Bit 6	R	APSLV[6]	X
Bit 5	R	APSLV[5]	X
Bit 4	R	APSLV[4]	X
Bit 3	R	APSLV[3]	X
Bit 2	R	APSLV[2]	X
Bit 1	R	APSLV[1]	X
Bit 0	R	APSLV[0]	X

APSLV[7:0]

The accepted path signal label value (APSLV[7:0]) bits represent the last accepted path signal label value. A new PSL is accepted when the same PSL value is detected in the C2 byte for three or five consecutive frames. (selectable with the PSL5 register bit).

CPSLV[7:0]

The captured path signal label value (CPSLV[7:0]) bits represent the last captured path signal label value. A new PSL is captured every frame from the C2 byte.

Indirect Register 0x04: RHPP Expected PSL and PDI

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	PDIRANGE	0
Bit 12	R/W	PDI[4]	0
Bit 11	R/W	PDI[3]	0
Bit 10	R/W	PDI[2]	0
Bit 9	R/W	PDI[1]	0
Bit 8	R/W	PDI[0]	0
Bit 7	R/W	EPSL[7]	0
Bit 6	R/W	EPSL[6]	0
Bit 5	R/W	EPSL[5]	0
Bit 4	R/W	EPSL[4]	0
Bit 3	R/W	EPSL[3]	0
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

EPSL[7:0]

The expected path signal label (EPSL[7:0]) bits represent the expected path signal label. The expected PSL and the expected PDI validate the received or the accepted PSL to declare PLM-P, UNEQ-P and PDI-P defects.

See the Functional Description Section in the S/UNI 4xJET Data Sheet (PMC-2021632) for further explanation.

PDI[4:0], PDIRANGE

The payload defect indication (PDI[4:0]) bits and the payload defect indication range (PDIRANGE) bit determine the expected payload defect indication. When PDIRANGE is set to logic 1, the PDI range is enabled and the expected PDI range is from E1H to E0H+PDI[4:0]. When PDIRANGE is set to logic 0, the PDI range is disable and the expected PDI value is E0H+PDI[4:0]. The expected PSL and the expected PDI validate the received or the accepted PSL to declare PLM-P, UNEQ-P and PDI-P defects.

See the Functional Description Section in the S/UNI 4xJET Data Sheet (PMC-2021632) for further explanation.

Indirect Register 0x05: RHPP Pointer Interpreter Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R	NDF	X
Bit 5	R	ILLPTR	X
Bit 4	R	INVNDF	X
Bit 3	R	DISCOPA	X
Bit 2	R	CONCAT	X
Bit 1	R	ILLJREQ	X
Bit 0	—	Unused	X

The Pointer Interpreter Status bits are don't care for slave time slots. When WCIMODE is low (read mode) the Pointer Interpreter Status bits are cleared by reading the status register. When WCIMODE is high (write mode) the Pointer Interpreter Status bit x is cleared by a write high value to bit x of the status register.

ILLJREQ

The illegal pointer justification request (ILLJREQ) signal is set high when a positive and/or negative pointer adjustment is received within three frames of a pointer justification event (inc_ind, dec_ind) or an NDF triggered active offset adjustment (NDF_enable).

CONCAT

The CONCAT bit is set high if the H1 and H2 pointer bytes received matched the concatenation indication (one of the five NDF_enable patterns in the NDF field, don't care in the size field, and all-ones in the pointer offset field).

DISCOPA

The discontinuous change of pointer alignment (DISCOPA) signal is set high when there is a pointer adjustment due to receiving a pointer repeated three times.

INVNDF

The invalid new data flag (INVNDF) signal is set high when an invalid NDF code is received.

ILLPTR

The illegal pointer offset (ILLPTR) signal is set high when the pointer received is out of the range. Legal values are from 0 to 782. Pointer justification requests (inc_req, dec_req) and AIS indications (AIS_ind) are not considered illegal.

NDF

The new data flag (NDF) signal is set high when an enabled New Data Flag is received indicating a pointer adjustment (NDF_enabled indication).

Indirect Register 0x06: RHPP Path BIP Error Counter

Bit	Type	Function	Default
Bit 15	R	PBIPE[15]	X
Bit 14	R	PBIPE[14]	X
Bit 13	R	PBIPE[13]	X
Bit 12	R	PBIPE[12]	X
Bit 11	R	PBIPE[11]	X
Bit 10	R	PBIPE[10]	X
Bit 9	R	PBIPE[9]	X
Bit 8	R	PBIPE[8]	X
Bit 7	R	PBIPE[7]	X
Bit 6	R	PBIPE[6]	X
Bit 5	R	PBIPE[5]	X
Bit 4	R	PBIPE[4]	X
Bit 3	R	PBIPE[3]	X
Bit 2	R	PBIPE[2]	X
Bit 1	R	PBIPE[1]	X
Bit 0	R	PBIPE[0]	X

PBIPE[15:0]

The path BIP error (PBIPE[15:0]) bits represent the number of path BIP errors that have been detected in the B3 byte since the last accumulation interval.

Any write to the RHPP Counters Update Register (address 0x1883) or to the Master Reset and Identity Register (address 0x1800) will trigger the transfer of all counter values to their holding registers.

Indirect Register 0x07: RHPP Path REI Error Counter

Bit	Type	Function	Default
Bit 15	R	PREIE[15]	X
Bit 14	R	PREIE[14]	X
Bit 13	R	PREIE[13]	X
Bit 12	R	PREIE[12]	X
Bit 11	R	PREIE[11]	X
Bit 10	R	PREIE[10]	X
Bit 9	R	PREIE[9]	X
Bit 8	R	PREIE[8]	X
Bit 7	R	PREIE[7]	X
Bit 6	R	PREIE[6]	X
Bit 5	R	PREIE[5]	X
Bit 4	R	PREIE[4]	X
Bit 3	R	PREIE[3]	X
Bit 2	R	PREIE[2]	X
Bit 1	R	PREIE[1]	X
Bit 0	R	PREIE[0]	X

PREIE[15:0]

The path REI error (PREIE[15:0]) bits represent the number of path REI errors that have been extracted from the G1 byte since the last accumulation interval.

Any write to the RHPP Counters Update Register (address 0x1883) or to the Master Reset and Identity Register (address 0x1800) will trigger the transfer of all counter values to their holding registers.

Indirect Register 0x08: RHPP Path Negative Justification Event Counter

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R	PNJE[12]	X
Bit 11	R	PNJE[11]	X
Bit 10	R	PNJE[10]	X
Bit 9	R	PNJE[9]	X
Bit 8	R	PNJE[8]	X
Bit 7	R	PNJE[7]	X
Bit 6	R	PNJE[6]	X
Bit 5	R	PNJE[5]	X
Bit 4	R	PNJE[4]	X
Bit 3	R	PNJE[3]	X
Bit 2	R	PNJE[2]	X
Bit 1	R	PNJE[1]	X
Bit 0	R	PNJE[0]	X

PNJE[12:0]

The Path Negative Justification Event (PNJE[12:0]) bits represent the number of Path Negative Justification Events that have occurred since the last accumulation interval.

Any write to the RHPP Counters Update Register (address 0x1883) or to the Master Reset and Identity Register (address 0x1800) will trigger the transfer of all counter values to their holding registers.

Indirect Register 0x09: RHPP Path Positive Justification Event Counter

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R	PPJE[12]	X
Bit 11	R	PPJE[11]	X
Bit 10	R	PPJE[10]	X
Bit 9	R	PPJE[9]	X
Bit 8	R	PPJE[8]	X
Bit 7	R	PPJE[7]	X
Bit 6	R	PPJE[6]	X
Bit 5	R	PPJE[5]	X
Bit 4	R	PPJE[4]	X
Bit 3	R	PPJE[3]	X
Bit 2	R	PPJE[2]	X
Bit 1	R	PPJE[1]	X
Bit 0	R	PPJE[0]	X

PPJE[12:0]

The Path Positive Justification Event (PPJE[12:0]) bits represent the number of Path Positive Justification Events that have occurred since the last accumulation interval.

Any write to the RHPP Counters Update Register (address 0x1883) or to the Master Reset and Identity Register (address 0x1800) will trigger the transfer of all counter values to their holding registers.

Register 0x1882: RHPP Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	STS12C	0
Bit 13	R/W	Reserved	0
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	STS3C[4]	0
Bit 2	R/W	STS3C[3]	0
Bit 1	R/W	STS3C[2]	0
Bit 0	R/W	STS3C[1]	0

STS3C[1]

The STS-3c (VC-4) payload configuration (STS3C[1]) bit selects the payload configuration. When STS3C[1] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a STS-3c (VC-4) payload. When STS3C[1] is set to logic 0, the paths are STS-1 (VC-3) payloads. When STS12C is set to logic 1, STS3C[1] must be set to logic 0.

STS3C[2]

The STS-3c (VC-4) payload configuration (STS3C[2]) bit selects the payload configuration. When STS3C[2] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a STS-3c (VC-4) payload. When STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads. When STS12C is set to logic 1, STS3C[2] must be set to logic 0.

STS3C[3]

The STS-3c (VC-4) payload configuration (STS3C[3]) bit selects the payload configuration. When STS3C[3] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a STS-3c (VC-4) payload. When STS3C[3] is set to logic 0, the paths are STS-1 (VC-3) payloads. When STS12C is set to logic 1, STS3C[3] must be set to logic 0.

STS3C[4]

The STS-3c (VC-4) payload configuration (STS3C[4]) bit selects the payload configuration. When STS3C[4] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a STS-3c (VC-4) payload. When STS3C[4] is set to logic 0, the paths are STS-1 (VC-3) payloads. When STS12C is set to logic 1, STS3C[4] must be set to logic 0.

STS12C

The STS-12c (VC-4-4c) payload configuration (STS12C) bit selects the payload configuration. When STS12C is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of a STS-12c (VC-4-4c) payload. When STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the STS3C[1:4] register bit.

Register 0x1883: RHPP Counter Update

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

Any write to the RHPP Counters Update Register (address 0x1883) or to the Master Reset and Identity Register (address 0x1800) will trigger the transfer of all counter values to their holding registers.

Register 0x1884: RHPP Path Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	P_INT[12]	X
Bit 10	R	P_INT[11]	X
Bit 9	R	P_INT[10]	X
Bit 8	R	P_INT[9]	X
Bit 7	R	P_INT[8]	X
Bit 6	R	P_INT[7]	X
Bit 5	R	P_INT[6]	X
Bit 4	R	P_INT[5]	X
Bit 3	R	P_INT[4]	X
Bit 2	R	P_INT[3]	X
Bit 1	R	P_INT[2]	X
Bit 0	R	P_INT[1]	X

When the interrupt output INTB goes low, this register allows the source of the active interrupt to be identified down to the path level. Further register accesses are required for the path in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

P_INT[1:12]

A path interrupt P_INT[1:12] bit is a logic one when an interrupt request is active from the corresponding path. RHPP Pointer Interpreter Status register (RHPP Indirect Register 0x05) must be read in order to determine the source of the path interrupt.

Register 0x1885: RHPP Pointer Concatenation Processing Disable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	PTRCDIS[12]	0
Bit 10	R/W	PTRCDIS[11]	0
Bit 9	R/W	PTRCDIS[10]	0
Bit 8	R/W	PTRCDIS[9]	0
Bit 7	R/W	PTRCDIS[8]	0
Bit 6	R/W	PTRCDIS[7]	0
Bit 5	R/W	PTRCDIS[6]	0
Bit 4	R/W	PTRCDIS[5]	0
Bit 3	R/W	PTRCDIS[4]	0
Bit 2	R/W	PTRCDIS[3]	0
Bit 1	R/W	PTRCDIS[2]	0
Bit 0	R/W	PTRCDIS[1]	0

PTRCDIS[1:12]

The concatenation pointer processing disable (PTRCDIS[1:12]) bits disable the path concatenation pointer interpreter state machine. When PTRCDIS[n] is set to logic 1, the path concatenation pointer interpreter state-machine (for the path n) is disabled and excluded from the LOPC-P, AISC-P and ALLAISC-P defect declaration. When PTRCDIS is set to logic 0, the path concatenation pointer interpreter state-machine is enabled and included in the LOPC-P, AISC-P and ALLAISC-P defect declaration.

Register 0x1888: RHPP Pointer Interpreter Status(STS-1/STM-0 #1)
Register 0x1890: RHPP Pointer Interpreter Status (STS-1/STM-0 #2)
Register 0x1898: RHPP Pointer Interpreter Status (STS-1/STM-0 #3)
Register 0x18A0: RHPP Pointer Interpreter Status (STS-1/STM-0 #4)
Register 0x18A8: RHPP Pointer Interpreter Status (STS-1/STM-0 #5)
Register 0x18B0: RHPP Pointer Interpreter Status (STS-1/STM-0 #6)
Register 0x18B8: RHPP Pointer Interpreter Status (STS-1/STM-0 #7)
Register 0x18C0: RHPP Pointer Interpreter Status (STS-1/STM-0 #8)
Register 0x18C8: RHPP Pointer Interpreter Status (STS-1/STM-0 #9)
Register 0x18D0: RHPP Pointer Interpreter Status (STS-1/STM-0 #10)
Register 0x18D8: RHPP Pointer Interpreter Status (STS-1/STM-0 #11)
Register 0x18E0: RHPP Pointer Interpreter Status (STS-1/STM-0 #12)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	PAISCV	X
Bit 4	R	PLOPCV	X
Bit 3	R	PAISV	X
Bit 2	R	PLOPV	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

PLOPV

The path loss of pointer state (PLOPV) bit indicates the current status of the pointer interpreter state machine. PLOPV is set to logic 1 when the state machine is in the LOP_state. PLOPV is set to logic 0 when the state machine is not in the LOP_state.

PAISV

The path alarm indication signal state (PAISV) bit indicates the current status of the pointer interpreter state machine. PAISV is set to logic 1 when the state machine is in the AIS_state. PAISV is set to logic 0 when the state machine is not in the AIS_state.

PLOPCV

The path lost of pointer concatenation state (PLOPCV) bit indicates the current status of the concatenation pointer interpreter state machine. PLOPCV is set to logic 1 when the state machine is in the LOPC_state. PLOPCV is set to logic 0 when the state machine is not in the LOPC_state.

PAISCV

The path concatenation alarm indication signal state (PAISCV) bit indicates the current status of the concatenation pointer interpreter state machine. PAISCV is set to logic 1 when the state machine is in the AISC_state. PAISCV is set to logic 0 when the state machine is not in the AISC_state.

Register 0x1889: RHPP Pointer Interpreter Interrupt Enable (STS-1/STM-0 #1)
Register 0x1891: RHPP Pointer Interpreter Interrupt Enable (STS-1/STM-0 #2)
Register 0x1899: RHPP Pointer Interpreter Interrupt Enable (STS-1/STM-0 #3)
Register 0x18A1: RHPP Pointer Interpreter Interrupt Enable (STS-1/STM-0 #4)
Register 0x18A9: RHPP Pointer Interpreter Interrupt Enable (STS-1/STM-0 #5)
Register 0x18B1: RHPP Pointer Interpreter Interrupt Enable (STS-1/STM-0 #6)
Register 0x18B9: RHPP Pointer Interpreter Interrupt Enable (STS-1/STM-0 #7)
Register 0x18C1: RHPP Pointer Interpreter Interrupt Enable (STS-1/STM-0 #8)
Register 0x18C9: RHPP Pointer Interpreter Interrupt Enable (STS-1/STM-0 #9)
Register 0x18D1: RHPP Pointer Interpreter Interrupt Enable (STS-1/STM-0 #10)
Register 0x18D9: RHPP Pointer Interpreter Interrupt Enable (STS-1/STM-0 #11)
Register 0x18E1: RHPP Pointer Interpreter Interrupt Enable (STS-1/STM-0 #12)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	PAISCE	0
Bit 4	R/W	PLOPCE	0
Bit 3	R/W	PAISE	0
Bit 2	R/W	PLOPE	0
Bit 1	—	Unused	X
Bit 0	R/W	PTRJEE	0

PTRJEE

The pointer justification event interrupt enable (PTRJEE) bit control the activation of INTB. When PTRJEE is set to logic 1, the NJEI and PJEI pending interrupt will deassert INTB. When PTRJEE is set to logic 0, the NJEI and PJEI pending interrupt will not deassert INTB.

PLOPE

The path loss of pointer interrupt enable (PLOPE) bit controls the activation of INTB. When PLOPE is set to logic 1, the PLOPI pending interrupt will deassert INTB. When PLOPE is set to logic 0, the PLOPI pending interrupt will not assert INTB.

PAISE

The path alarm indication signal interrupt enable (PAISE) bit controls the activation of INTB. When PAISE is set to logic 1, the PAISI pending interrupt will deassert the INTB. When PAISE is set to logic 0, the PAISI pending interrupt will not deassert INTB.

PLOPCE

The path loss of pointer concatenation interrupt enable (PLOPCE) bit controls the activation of INTB. When PLOPCE is set to logic 1, the PLOPCI pending interrupt will deassert INTB. When PLOPCE is set to logic 0, the PLOPCI pending interrupt will not deassert INTB.

PAISCE

The path concatenation alarm indication signal interrupt enable (PAISCE) bit controls the activation of INTB. When PAISCE is set to logic 1, the PAISCI pending interrupt will deassert INTB. When PAISCE is set to logic 0, the PAISCI pending interrupt will not deassert INTB.

Register 0x188A: RHPP Pointer Interpreter Interrupt Status (STS-1/STM-0 #1)
Register 0x1892: RHPP Pointer Interpreter Interrupt Status (STS-1/STM-0 #2)
Register 0x189A: RHPP Pointer Interpreter Interrupt Status (STS-1/STM-0 #3)
Register 0x18A2: RHPP Pointer Interpreter Interrupt Status (STS-1/STM-0 #4)
Register 0x18AA: RHPP Pointer Interpreter Interrupt Status (STS-1/STM-0 #5)
Register 0x18B2: RHPP Pointer Interpreter Interrupt Status (STS-1/STM-0 #6)
Register 0x18BA: RHPP Pointer Interpreter Interrupt Status (STS-1/STM-0 #7)
Register 0x18C2: RHPP Pointer Interpreter Interrupt Status (STS-1/STM-0 #8)
Register 0x18CA: RHPP Pointer Interpreter Interrupt Status (STS-1/STM-0 #9)
Register 0x18D2: RHPP Pointer Interpreter Interrupt Status (STS-1/STM-0 #10)
Register 0x18DA: RHPP Pointer Interpreter Interrupt Status (STS-1/STM-0 #11)
Register 0x18E2: RHPP Pointer Interpreter Interrupt Status (STS-1/STM-0 #12)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	PAISCI	X
Bit 4	R	PLOPCI	X
Bit 3	R	PAISI	X
Bit 2	R	PLOPI	X
Bit 1	R	PJEI	X
Bit 0	R	NJEI	X

NJEI

The negative pointer justification event interrupt status (NJEI) bit is an event indicator. NJEI is set to logic 1 to indicate a negative pointer justification event. The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), NJEI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), NJEI is cleared by writing a high value to bit 0 of the interrupt status register.

PJEI

The positive pointer justification event interrupt status (PJEI) bit is an event indicator. PJEI is set to logic 1 to indicate a positive pointer justification event. The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), PJEI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PJEI is cleared by writing a high value to bit 1 of the interrupt status register.

PLOPI

The path loss of pointer interrupt status (PLOPI) bit is an event indicator. PLOPI is set to logic 1 to indicate any change in the status of PLOPV (entry to the LOP_state or exit from the LOP_state). The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), PLOPI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PLOPI is cleared by writing a high value to bit 2 of the interrupt status register.

PAISI

The path alarm indication signal interrupt status (PAISI) bit is an event indicator. PAISI is set to logic 1 to indicate any change in the status of PAISV (entry to the AIS_state or exit from the AIS_state). The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), PAISI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PAISI is cleared by writing a high value to bit 3 of the interrupt status register.

PLOPCI

The path loss of pointer concatenation interrupt status (PLOPCI) bit is an event indicator. PLOPCI is set to logic 1 to indicate any change in the status of PLOPCV (entry to the LOPC_state or exit from the LOPC_state). The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), PLOPCI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PLOPCI is cleared by writing a high value to bit 4 of the interrupt status register.

PAISCI

The path concatenation alarm indication signal interrupt status (PAISCI) bit is an event indicator. PAISCI is set to logic 1 to indicate any change in the status of PAISCV (entry to the AISC_state or exit from the AISC_state). The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), PAISCI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PAISCI is cleared by writing a high value to bit 5 of the interrupt status register.

Register 0x188B: RHPP Error Monitor Status (STS-1/STM-0 #1)
Register 0x1893: RHPP Error Monitor Status (STS-1/STM-0 #2)
Register 0x189B: RHPP Error Monitor Status (STS-1/STM-0 #3)
Register 0x18A3: RHPP Error Monitor Status (STS-1/STM-0 #4)
Register 0x18AB: RHPP Error Monitor Status (STS-1/STM-0 #5)
Register 0x18B3: RHPP Error Monitor Status (STS-1/STM-0 #6)
Register 0x18BB: RHPP Error Monitor Status (STS-1/STM-0 #7)
Register 0x18C3: RHPP Error Monitor Status (STS-1/STM-0 #8)
Register 0x18CB: RHPP Error Monitor Status (STS-1/STM-0 #9)
Register 0x18D3: RHPP Error Monitor Status (STS-1/STM-0 #10)
Register 0x18DB: RHPP Error Monitor Status (STS-1/STM-0 #11)
Register 0x18E3: RHPP Error Monitor Status (STS-1/STM-0 #12)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R	PERDIV	X
Bit 5	R	PRDIV	X
Bit 4	R	PPDIV	X
Bit 3	R	PUNEQV	X
Bit 2	R	PPLMV	X
Bit 1	R	PPLUV	X
Bit 0	—	Unused	X

The Error Monitor Status bits can be ignored for slave time slots.

PPLUV

The path payload label unstable status (PPLUV) bit indicates the current status of the PLU-P defect. The PLU-P defect is dependent on whether the ITU compliant algorithm (algorithm 2) or the BELLCORE compliant algorithm (algorithm 1) is used (selectable with the ALGO2 register bit).

Algorithm 1: PPLUV is set to logic 0.

Algorithm 2: PPLUV is set to logic 1 when a total of 5 received PSL differs from the previously accepted PSL without any persistent PSL in between. PPLUV is set to logic 0 when a persistent PSL is found. A persistent PSL is found when the same PSL is received for 3 or 5 consecutive frames.

PPLMV

The path payload label mismatch status (PPLMV) bit indicates the current status of the PLM-P defect. The PLM-P defect is dependent on whether the ITU compliant algorithm (algorithm 2) or the BELLCORE compliant algorithm (algorithm 1) is used (selectable with the ALGO2 register bit).

Algorithm 1: PPLMV is set to logic 1 when the received PSL does not match the expected PSL for 3 or 5 consecutive frames (selectable with the PSL5 register bit). PPLMV is set to logic 0 when the received PSL matches the expected PSL for 3 or 5 consecutive frames.

Algorithm 2: PPLMV is set to logic 1 when the accepted PSL does not match the expected PSL. PPLMV is set to logic 0 when the accepted PSL matches the expected PSL.

See the Functional Description Section in the S/UNI 4xJET Data Sheet (PMC-2021632) for further explanation on expected PSL.

PUNEQV

The path unequipped status (PUNEQV) bit indicates the current status of the UNEQ-P defect.

PUNEQV is set to logic 1 when the received PSL indicates unequipped for 3 or 5 consecutive frames (selectable with the PSL5 register bit). An PUNEQV is set to logic 0 when the received PSL indicates not unequipped for 3 or 5 consecutive frames.

See the Functional Description Section in the S/UNI 4xJET Data Sheet (PMC-2021632) for further explanation on expected PSL.

PPDIV

The path payload defect indication status (PPDIV) bit indicates the current status of the PDI-P defect. The PDI-P defect is dependent on whether the ITU compliant algorithm (algorithm 2) or the BELLCORE compliant algorithm (algorithm 1) is used (selectable with the ALGO2 register bit).

Algorithm 1: PPDIV is set to logic one when the received PSL is a defect for 3 or 5 consecutive frames (selectable with the PSL5 register bit). PPDIV is set to logic 0 when the received PSL is not a defect for 3 or 5 consecutive frames.

Algorithm 2: PPDIV is set to logic 1 when the accepted PSL is a defect. PPDI is set to logic 0 when the accepted PSL is not a defect.

See the Functional Description Section in the S/UNI 4xJET Data Sheet (PMC-2021632) for further explanation on defect PSL.

PRDIV

The path remote defect indication status (PRDIV) bit indicates the current status of the RDI-P defect. PRDIV is set to logic 1 when bit 5 of the G1 byte is set high for five or ten consecutive frames (selectable with the PRDI10 register bit). PRDIV is set to logic 0 when bit 5 of the G1 byte is set low for five or ten consecutive frames.

PERDIV

The path enhanced remote defect indication status (PERDIV) bit indicates the current status of the enhanced RDI-P defect. PERDIV is set to logic 1 when the same 010, 100, 101, 110, or 111 pattern is detected in bits 5, 6, and 7 of the G1 byte for five or ten consecutive frames (selectable with the PRDI10 register bit). PERDIV is set to logic 0 when the same 000, 001, or 011 pattern is detected in bits 5, 6, and 7 of the G1 byte for five or ten consecutive frames.

Register 0x188C: RHPP Error Monitor Interrupt Enable (STS-1/STM-0 #1)
Register 0x1894: RHPP Error Monitor Interrupt Enable (STS-1/STM-0 #2)
Register 0x189C: RHPP Error Monitor Interrupt Enable (STS-1/STM-0 #3)
Register 0x18A4: RHPP Error Monitor Interrupt Enable (STS-1/STM-0 #4)
Register 0x18AC: RHPP Error Monitor Interrupt Enable (STS-1/STM-0 #5)
Register 0x18B4: RHPP Error Monitor Interrupt Enable (STS-1/STM-0 #6)
Register 0x18BC: RHPP Error Monitor Interrupt Enable (STS-1/STM-0 #7)
Register 0x18C4: RHPP Error Monitor Interrupt Enable (STS-1/STM-0 #8)
Register 0x18CC: RHPP Error Monitor Interrupt Enable (STS-1/STM-0 #9)
Register 0x18D4: RHPP Error Monitor Interrupt Enable (STS-1/STM-0 #10)
Register 0x18DC: RHPP Error Monitor Interrupt Enable (STS-1/STM-0 #11)
Register 0x18E4: RHPP Error Monitor Interrupt Enable (STS-1/STM-0 #12)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	PREIEE	0
Bit 8	R/W	PBIPEE	0
Bit 7	R/W	COPERDIE	0
Bit 6	R/W	PERDIE	0
Bit 5	R/W	PRDIE	0
Bit 4	R/W	PPDIE	0
Bit 3	R/W	PUNEQE	0
Bit 2	R/W	PPLME	0
Bit 1	R/W	PPLUE	0
Bit 0	R/W	COPSLE	0

COPSLE

The change of path payload signal label interrupt enable (COPSLE) bit controls the activation of INTB. When COPSLE is set to logic 1, the COPSLI pending interrupt will deassert INTB. When COPSLE is set to logic 0, the COPSLI pending interrupt will not deassert INTB.

PPLUE

The path payload label unstable interrupt enable (PPLUE) bit controls the activation of INTB. When PPLUE is set to logic 1, the PPLUI pending interrupt will deassert INTB. When PPLUE is set to logic 0, the PPLUI pending interrupt will not deassert INTB.

PPLME

The path payload label mismatch interrupt enable (PPLME) bit controls the activation of INTB. When PPLME is set to logic 1, the PPLMI pending interrupt will deassert INTB. When PPLME is set to logic 0, the PPLMI pending interrupt will not deassert INTB.

PUNEQE

The path payload unequipped interrupt enable (PUNEQE) bit controls the activation of INTB. When PUNEQE is set to logic 1, the PUNEQI pending interrupt will deassert INTB. When PUNEQE is set to logic 0, the PUNEQI pending interrupt will not deassert INTB.

PPDIE

The path payload defect indication interrupt enable (PPDIE) bit controls the activation of INTB. When PPDIE is set to logic 1, the PPDI pending interrupt will deassert INTB. When PPDIE is set to logic 0, the PPDI pending interrupt will not deassert INTB.

PRDIE

The path remote defect indication interrupt enable (PRDIE) bit controls the activation of INTB. When PRDIE is set to logic 1, the PRDII pending interrupt will deassert INTB. When PRDIE is set to logic 0, the PRDII pending interrupt will not deassert INTB.

PERDIE

The path enhanced remote defect indication interrupt enable (PERDIE) bit controls the activation of INTB. When PERDIE is set to logic 1, the PERDII pending interrupt will deassert INTB. When PERDIE is set to logic 0, the PERDII pending interrupt will not deassert INTB.

COPERDIE

The change of path enhanced remote defect indication interrupt enable (COPERDIE) bit controls the activation of INTB. When COPERDIE is set to logic 1, the COPERDII pending interrupt will deassert INTB. When COPERDIE is set to logic 0, the COPERDII pending interrupt will not deassert INTB.

PBIPEE

The path BIP-8 error interrupt enable (PBIPEE) bit controls the activation of INTB. When PBIPEE is set to logic 1, the PBIPEI pending interrupt will deassert INTB. When PBIPEE is set to logic 0, the PBIPEI pending interrupt will not deassert INTB.

PREIEE

The path REI error interrupt enable (PREIEE) bit controls the activation of INTB. When PREIEE is set to logic 1, the PREIEI pending interrupt will deassert INTB. When PREIEE is set to logic 0, the PREIEI pending interrupt will not deassert INTB.

Register 0x188D: RHPP Error Monitor Interrupt Status (STS-1/STM-0 #1)
Register 0x1895: RHPP Error Monitor Interrupt Status (STS-1/STM-0 #2)
Register 0x189D: RHPP Error Monitor Interrupt Status (STS-1/STM-0 #3)
Register 0x18A5: RHPP Error Monitor Interrupt Status (STS-1/STM-0 #4)
Register 0x18AD: RHPP Error Monitor Interrupt Status (STS-1/STM-0 #5)
Register 0x18B5: RHPP Error Monitor Interrupt Status (STS-1/STM-0 #6)
Register 0x18BD: RHPP Error Monitor Interrupt Status (STS-1/STM-0 #7)
Register 0x18C5: RHPP Error Monitor Interrupt Status (STS-1/STM-0 #8)
Register 0x18CD: RHPP Error Monitor Interrupt Status (STS-1/STM-0 #9)
Register 0x18D5: RHPP Error Monitor Interrupt Status (STS-1/STM-0 #10)
Register 0x18DD: RHPP Error Monitor Interrupt Status (STS-1/STM-0 #11)
Register 0x18E5: RHPP Error Monitor Interrupt Status (STS-1/STM-0 #12)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R	PREIEI	X
Bit 8	R	PBIPEI	X
Bit 7	R	COPERDII	X
Bit 6	R	PERDII	X
Bit 5	R	PRDII	X
Bit 4	R	PPDII	X
Bit 3	R	PUNEQI	X
Bit 2	R	PPLMI	X
Bit 1	R	PPLUI	X
Bit 0	R	COPSLI	X

COPSLI

The change of path payload signal label interrupt status (COPSLI) bit is an event indicator. COPSLI is set to logic 1 to indicate a new PSL-P value. ALGO2 register bit has no effect on COPSLI. The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), COPSLI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), COPSLI is cleared by writing a high value to bit 0 of the interrupt status register.

PPLUI

The path payload label unstable interrupt status (PPLUI) bit is an event indicator. PPLUI is set to logic 1 to indicate any change in the status of PPLUV (stable to unstable or unstable to stable). The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), PPLUI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PPLUI is cleared by writing a high value to bit 1 of the interrupt status register.

PPLMI

The path payload label mismatch interrupt status (PPLMI) bit is an event indicator. PPLMI is set to logic 1 to indicate any change in the status of PPLMV (match to mismatch or mismatch to match). The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), PPLMI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PPLMI is cleared by writing a high value to bit 2 of the interrupt status register.

PUNEQI

The path payload unequipped interrupt status (PUNEQI) bit is an event indicator. PUNEQI is set to logic 1 to indicate any change in the status of PUNEQV (equipped to unequipped or unequipped to equipped). The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), PUNEQI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PUNEQI is cleared by writing a high value to bit 3 of the interrupt status register.

PPDII

The path payload defect indication interrupt status (PPDII) bit is an event indicator. PPDII is set to logic 1 to indicate any change in the status of PPDIV (no defect to payload defect or payload defect to no defect). The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), PPDII is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PPDII is cleared by writing a high value to bit 4 of the interrupt status register.

PRDII

The path remote defect indication interrupt status (PRDII) bit is an event indicator. PRDII is set to logic 1 to indicate any change in the status of PRDIV (no defect to RDI defect or RDI defect to no defect). The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), PRDII is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PRDII is cleared by writing a high value to bit 5 of the interrupt status register.

PERDII

The path enhanced remote defect indication interrupt status (PERDII) bit is an event indicator. PERDII is set to logic 1 to indicate any change in the status of PERDIV (no defect to enhanced RDI defect or enhanced RDI defect to no defect). The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), PERDII is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PERDII is cleared by writing a high value to bit 6 of the interrupt status register.

COPERDII

The change of path enhanced remote defect indication interrupt status (COPERDII) bit is an event indicator. COPERDII is set to logic 1 to indicate a new enhanced RDI-P value. The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), COPERDI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), COPERDI is cleared by writing a high value to bit 7 of the interrupt status register.

PBIPEI

The path BIP-8 error interrupt status (PBIPEI) bit is an event indicator. PBIPEI is set to logic 1 to indicate a path BIP-8 error. The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), PBIPEI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PBIPEI is cleared by writing a high value to bit 8 of the interrupt status register.

PREIEI

The path REI error interrupt status (PREIEI) bit is an event indicator. PREIEI is set to logic 1 to indicate a path REI error. The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), PREIEI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PREIEI is cleared by writing a high value to bit 9 of the interrupt status register.

Register 0x1900: RHPP TU3 Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The STS-1/STM-0 tributary path (PATH[3:0]) bits select which STS-1/STM-0 tributary path is accessed by the current indirect transfer.

PATH[3:0]	STS-1/STM-0 Tributary Path #
0000	Invalid path
0001-1100	Tributary Path #1 to #12
1101-1111	Invalid path

IADDR[3:0]

The indirect address location (IADDR[2:0]) bits select which address location is accessed by the current indirect transfer.

Indirect Address IADDR[3:0]	Indirect Data
0000	Pointer Interpreter Configuration
0001	Error Monitor Configuration
0010	Pointer Value and ERDI
0011	Captured and Accepted PSL
0100	Expected PSL and PDI
0101	Pointer Interpreter status
0110	Tributary Path BIP Error Counter

Indirect Address IADDR[3:0]	Indirect Data
0111	Tributary Path REI Error Counter
1000	Tributary Path Negative Justification Event Counter
1001	Tributary Path Positive Justification Event Counter
1010 to 1111	Unused

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

The maximum busy bit set time is 22 ICLK cycles.

Register 0x1901: RHPP TU3 Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Indirect Register 0x00: RHPP TU3 Pointer Interpreter Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	NDFCNT	0
Bit 4	R/W	INVCNT	0
Bit 3	R/W	RELAYPAIS	0
Bit 2	R/W	JUST3DIS	0
Bit 1	R/W	SSEN	0
Bit 0	—	Unused	X

SSEN

The SS bits enable (SSEN) bit selects whether or not the SS bits are taking into account in the pointer interpreter state machine. When SSEN is set to logic 1, the SS bits must be set to 10 for a valid NORM_POINT, NDF_ENABLE, INC_IND, DEC_IND or NEW_POINT indication. When SSEN is set to logic 0, the SS bits are ignored.

JUST3DIS

The “justification more than 3 frames ago disable” (JUST3DIS) bit selects whether or not the NDF_ENABLE, INC_IND or DEC_IND pointer justifications must be more than 3 frames apart to be considered valid. When JUST3DIS is set to logic 0, the previous NDF_ENABLE, INC_IND or DEC_IND indication must be more than 3 frames ago or the present NDF_ENABLE, INC_IND or DEC_IND indication is considered an INV_POINT indication. When JUST3DIS is set to logic 1, NDF_ENABLE, INC_IND or DEC_IND indication can be every frame.

RELAYPAIS

The relay tributary path AIS (RELAYPAIS) bit selects the condition to enter the tributary path AIS state in the pointer interpreter state machine. When RELAYPAIS is set to logic 1, the tributary path AIS state is entered with 1 X AIS_ind indication. When RELAYPAIS is set to logic 0, the tributary path AIS state is entered with 3 X AIS_ind indications. This configuration bit also affects the concatenation pointer interpreter state machine.

INVCNT

The invalid counter (INVCNT) bit selects the behavior of the consecutive INV_POINT event counter in the pointer interpreter state machine. When INVCNT is set to logic 1, the consecutive INV_POINT event counter is reset by 3 EQ_NEW_POINT indications. When INVCNT is set to logic 0, the counter is not reset by 3 EQ_NEW_POINT indications.

NDFCNT

The new data flag counter (NDFCNT) bit selects the behavior of the consecutive NDF_ENABLE event counter in the pointer interpreter state machine. When NDFCNT is set to logic 1, the NDF_ENABLE definition is enabled NDF + SS. When NDFCNT is set to logic 0, the NDF_ENABLE definition is enabled NDF + SS + offset value in the range 0 to 782 (764 in TU3 mode). This configuration bit only changes the NDF_ENABLE definition for the consecutive NDF_ENABLE even counter to count towards LOP-P defect when the pointer is out of range, this configuration bit does not change the NDF_ENABLE definition for pointer justification.

Indirect Register 0x01: RHPP TU3 Error Monitor Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	B3EONRPOH	0
Bit 10	R/W	IPREIBLK	0
Bit 9	R/W	IBER	0
Bit 8	R/W	PREIBLKACC	0
Bit 7	R/W	B3EBLK	0
Bit 6	R/W	PBIPEBLKREI	0
Bit 5	R/W	PBIPEBLKACC	0
Bit 4	R/W	FSBIPDIS	0
Bit 3	R/W	PRDI10	0
Bit 2	R/W	PLMEND	0
Bit 1	R/W	PSL5	0
Bit 0	R/W	ALGO2	0

ALGO2

The payload signal label algorithm 2 (ALGO2) bit selects the algorithm for the PSL monitoring. When ALGO2 is set to logic 1, the ITU compliant algorithm is (algorithm 2) is used to monitor the PSL. When ALGO2 is set to logic 0, the BELLCORE compliant algorithm (algorithm 1) is used to monitor the PSL. ALGO2 changes the PLU-V, PLM-V and PDI-V defect definitions but has no effect on UNEQ-V defect, accepted PSL and change of PSL definitions

PSL5

The payload signal label detection (PSL5) bit selects the tributary path PSL persistence. When PSL5 is set to logic 1, a new PSL is accepted when the same PSL value is detected in the C2 byte for five consecutive frames. When PSL5 is set to logic 0, a new PSL is accepted when the same PSL value is detected in the C2 byte for three consecutive frames.

PLMEND

The payload label mismatch removal (PLMEND) bit controls the removal of a PLM-V defect when an UNEQ-V defect is declared. When PLMEND is set to logic 1, a PLM-V defect is terminated when an UNEQ-V defect is declared. When PLMEND is set to logic 0, a PLM-V defect is not terminated when an UNEQ-V defect is declared.

PRDI10

The tributary path remote defect indication detection (PRDI10) bit selects the tributary path RDI-V and tributary path enhanced RDI-V persistence. When PRDI10 is set to logic 1, tributary path RDI-V and tributary path enhanced RDI-V are accepted when the same pattern is detected in bits 5, 6, and 7 of the G1 byte for ten consecutive frames. When PRDI10 is set to logic 0, tributary path RDI-V and tributary path enhanced RDI-V are accepted when the same pattern is detected in bits 5, 6, and 7 of the G1 byte for five consecutive frames.

FSBIPDIS

The disable fixed stuff columns during BIP-8 calculation (FSBIPDIS) bit controls the tributary path BIP-8 calculation for a VC-3 payload. When FSBIPDIS is set to logic 1, the fixed stuff columns are not part of the BIP-8 calculation when processing a VC-3 payload. When FSBIPDIS is set to logic 0, the fixed stuff columns are part of the BIP-8 calculation when processing a VC-3 payload.

PBIPEBLKACC

The tributary path block BIP-8 errors accumulation (PBIPEBLKACC) bit controls the accumulation of tributary path BIP-8 errors. When PBIPEBLKACC is set to logic 1, the tributary path BIP-8 error accumulation represents block BIP-8 errors (a maximum of 1 error per frame). When PBIPEBLKACC is set to logic 0, the tributary path BIP-8 error accumulation represents BIP-8 errors (a maximum of 8 errors per frame).

PBIPEBLKREI

The tributary path block BIP-8 errors (PBIPEBLKREI) bit controls the tributary path REI errors returned to the THPP-TU3. When PBIPEBLKREI is set to logic 1, the tributary path REI is updated with block BIP-8 errors (a maximum of 1 error per frame). When PBIPEBLKREI is set to logic 0, the tributary path REI is updated with BIP-8 errors (a maximum of 8 errors per frame).

B3EBLK

The serial tributary path block BIP-8 errors (B3EBLK) bit controls the indication of tributary path BIP-8 errors on the B3E serial output. When B3EBLK is set to logic 1, B3E outputs block BIP-8 errors (a maximum of 1 error per frame). When B3EBLK is set to logic 0, B3E outputs BIP-8 errors (a maximum of 8 errors per frame).

PREIBLKACC

The tributary path block REI errors accumulation (PREIBLKACC) bit controls the accumulation of tributary path REI errors from the tributary path status (G1) byte. When PREIBLK is set to logic 1, the extracted tributary path REI errors are interpreted as block BIP-8 errors (a maximum of 1 error per frame). When PREIBLK is set to logic 0, the extracted tributary path REI errors are interpret as BIP-8 errors (a maximum of 8 errors per frame).

IBER

The in-band error reporting (IBER) bit controls the in-band regeneration of the tributary path status (G1) byte. When IBER is set to logic 1, the tributary path status byte is updated with the REI-V and the enhanced RDI-V defects that must be returned to the far end. When IBER is set to logic 0, the tributary path status byte is not altered.

IPREIBLK

The in-band tributary path REI block errors (IPREIBLK) bit controls the regeneration of the tributary path REI errors in the tributary path status (G1) byte. When IPREIBLK is set to logic 1, the tributary path REI is updated with block BIP-8 errors (a maximum of 1 error per frame). When IPREIBLK is set to logic 0, the tributary path REI is updated with BIP-8 errors (a maximum of 8 errors per frame).

B3EONRPOH

The B3EONRPOH bit controls the data presented on RPOH. When set to logic 0, the received B3 byte is placed on RPOH. When set to logic 1, the B3 error count is placed on RPOH as well as B3E.

Indirect Register 0x02: RHPP TU3 Pointer value and ERDI

Bit	Type	Function	Default
Bit 15	R	PERDIV[2]	X
Bit 14	R	PERDIV[1]	X
Bit 13	R	PERDIV[0]	X
Bit 12	—	Unused	X
Bit 11	R	SSV[1]	X
Bit 10	R	SSV[0]	X
Bit 9	R	PTRV[9]	X
Bit 8	R	PTRV[8]	X
Bit 7	R	PTRV[7]	X
Bit 6	R	PTRV[6]	X
Bit 5	R	PTRV[5]	X
Bit 4	R	PTRV[4]	X
Bit 3	R	PTRV[3]	X
Bit 2	R	PTRV[2]	X
Bit 1	R	PTRV[1]	X
Bit 0	R	PTRV[0]	X

PTRV[9:0]

The tributary path pointer value (PTRV[9:0]) bits represent the current TU pointer being process by the pointer interpreter state machine or by the concatenation pointer interpreter state machine.

SSV[1:0]

The SS value (SSV[1:0]) bits represent the current SS bits being processed by the pointer interpreter state machine or by the concatenation pointer interpreter state machine.

PERDIV[2:0]

The tributary path enhanced remote defect indication value (PERDIV[2:0]) bits represent the filtered tributary path enhanced remote defect indication value. PERDIV[2:0] is updated when the same enhanced RDI pattern is detected in bits 5, 6, and 7 of the G1 byte for five or ten consecutive frames (selectable with the PRDI10 register bit).

Indirect Register 0x03: RHPP TU3 captured and accepted PSL

Bit	Type	Function	Default
Bit 15	R	CPSLV[7]	X
Bit 14	R	CPSLV[6]	X
Bit 13	R	CPSLV[5]	X
Bit 12	R	CPSLV[4]	X
Bit 11	R	CPSLV[3]	X
Bit 10	R	CPSLV[2]	X
Bit 9	R	CPSLV[1]	X
Bit 8	R	CPSLV[0]	X
Bit 7	R	APSLV[7]	X
Bit 6	R	APSLV[6]	X
Bit 5	R	APSLV[5]	X
Bit 4	R	APSLV[4]	X
Bit 3	R	APSLV[3]	X
Bit 2	R	APSLV[2]	X
Bit 1	R	APSLV[1]	X
Bit 0	R	APSLV[0]	X

APSLV[7:0]

The accepted tributary path signal label value (APSLV[7:0]) bits represent the last accepted tributary path signal label value. A new PSL is accepted when the same PSL value is detected in the C2 byte for three or five consecutive frames. (selectable with the PSL5 register bit).

CPSLV[7:0]

The captured tributary path signal label value (CPSLV[7:0]) bits represent the last captured tributary path signal label value. A new PSL is captured every frame from the C2 byte.

Indirect Register 0x04: RHPP TU3 Expected PSL and PDI

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	PDIRANGE	0
Bit 12	R/W	PDI[4]	0
Bit 11	R/W	PDI[3]	0
Bit 10	R/W	PDI[2]	0
Bit 9	R/W	PDI[1]	0
Bit 8	R/W	PDI[0]	0
Bit 7	R/W	EPSL[7]	0
Bit 6	R/W	EPSL[6]	0
Bit 5	R/W	EPSL[5]	0
Bit 4	R/W	EPSL[4]	0
Bit 3	R/W	EPSL[3]	0
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

EPSL[7:0]

The expected tributary path signal label (EPSL[7:0]) bits represent the expected tributary path signal label. The expected PSL and the expected PDI validate the received or the accepted PSL to declare PLM-V, UNEQ-V and PDI-V defects.

See the Functional Description Section in the S/UNI 4xJET Data Sheet (PMC-2021632) for further explanation on expected PSL.

PDI[4:0], PDIRANGE

The payload defect indication (PDI[4:0]) bits and the payload defect indication range (PDIRANGE) bit determine the expected payload defect indication. When PDIRANGE is set to logic 1, the PDI range is enabled and the expected PDI range is from E1H to E0H+PDI[4:0]. When PDIRANGE is set to logic 0, the PDI range is disable and the expected PDI value is E0H+PDI[4:0]. The expected PSL and the expected PDI validate the received or the accepted PSL to declare PLM-V, UNEQ-V and PDI-V defects.

See the Functional Description Section in the S/UNI 4xJET Data Sheet (PMC-2021632) for further explanation.

Indirect Register 0x05: RHPP TU3 Pointer Interpreter status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R	NDF	X
Bit 5	R	ILLPTR	X
Bit 4	R	INVNDF	X
Bit 3	R	DISCOPA	X
Bit 2	—	Unused	X
Bit 1	R	ILLJREQ	X
Bit 0		Unused	X

The Pointer Interpreter Status bits are don't care for slave time slots. When WCIMODE is low (read mode) the Pointer Interpreter Status bits are cleared by reading the status register. When WCIMODE is high (write mode) the Pointer Interpreter Status bit x is cleared by a write high value to bit x of the status register.

ILLJREQ

The illegal pointer justification request (ILLJREQ) signal is set high when a positive and/or negative pointer adjustment is received within three frames of a pointer justification event (inc_ind, dec_ind) or an NDF triggered active offset adjustment (NDF_enable).

DISCOPA

The discontinuous change of pointer alignment (DISCOPA) signal is set high when there is a pointer adjustment due to receiving a pointer repeated three times.

INVNDF

The invalid new data flag (INVNDF) signal is set high when an invalid NDF code is received.

ILLPTR

The illegal pointer offset (ILLPTR) signal is set high when the pointer received is out of the range. Legal values are from 0 to 764. Pointer justification requests (inc_req, dec_req) and AIS indications (AIS_ind) are not considered illegal.

NDF

The new data flag (NDF) signal is set high when an enabled New Data Flag is received indicating a pointer adjustment (NDF_enabled indication).

Indirect Register 0x06: RHPP TU3 Tributary Path BIP Error Counter

Bit	Type	Function	Default
Bit 15	R	PBIPE[15]	X
Bit 14	R	PBIPE[14]	X
Bit 13	R	PBIPE[13]	X
Bit 12	R	PBIPE[12]	X
Bit 11	R	PBIPE[11]	X
Bit 10	R	PBIPE[10]	X
Bit 9	R	PBIPE[9]	X
Bit 8	R	PBIPE[8]	X
Bit 7	R	PBIPE[7]	X
Bit 6	R	PBIPE[6]	X
Bit 5	R	PBIPE[5]	X
Bit 4	R	PBIPE[4]	X
Bit 3	R	PBIPE[3]	X
Bit 2	R	PBIPE[2]	X
Bit 1	R	PBIPE[1]	X
Bit 0	R	PBIPE[0]	X

PBIPE[15:0]

The tributary path BIP error (PBIPE[15:0]) bits represent the number of tributary path BIP errors that have been detected in the B3 byte since the last accumulation interval.

Any write to the RHPP TU3 Counters Update Register (address 0x1883) or to the Master Reset and Identity Register (address 0x1800) will trigger the transfer of all counter values to their holding registers.

Indirect Register 0x07: RHPP TU3 Tributary Path REI Error Counter

Bit	Type	Function	Default
Bit 15	R	PREIE[15]	X
Bit 14	R	PREIE[14]	X
Bit 13	R	PREIE[13]	X
Bit 12	R	PREIE[12]	X
Bit 11	R	PREIE[11]	X
Bit 10	R	PREIE[10]	X
Bit 9	R	PREIE[9]	X
Bit 8	R	PREIE[8]	X
Bit 7	R	PREIE[7]	X
Bit 6	R	PREIE[6]	X
Bit 5	R	PREIE[5]	X
Bit 4	R	PREIE[4]	X
Bit 3	R	PREIE[3]	X
Bit 2	R	PREIE[2]	X
Bit 1	R	PREIE[1]	X
Bit 0	R	PREIE[0]	X

PREIE[15:0]

The tributary path REI error (PREIE[15:0]) bits represent the number of tributary path REI errors that have been extracted from the G1 byte since the last accumulation interval.

Any write to the RHPP TU3 Counters Update Register (address 0x1883) or to the Master Reset and Identity Register (address 0x1800) will trigger the transfer of all counter values to their holding registers.

Indirect Register 0x08: RHPP TU3 Tributary Path Negative Justification Event Counter

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R	PNJE[12]	X
Bit 11	R	PNJE[11]	X
Bit 10	R	PNJE[10]	X
Bit 9	R	PNJE[9]	X
Bit 8	R	PNJE[8]	X
Bit 7	R	PNJE[7]	X
Bit 6	R	PNJE[6]	X
Bit 5	R	PNJE[5]	X
Bit 4	R	PNJE[4]	X
Bit 3	R	PNJE[3]	X
Bit 2	R	PNJE[2]	X
Bit 1	R	PNJE[1]	X
Bit 0	R	PNJE[0]	X

PNJE[12:0]

The Tributary path Negative Justification Event (PNJE[12:0]) bits represent the number of Tributary path Negative Justification Events that have occurred since the last accumulation interval.

Any write to the RHPP TU3 Counters Update Register (address 0x1883) or to the Master Reset and Identity Register (address 0x1800) will trigger the transfer of all counter values to their holding registers.

Indirect Register 0x09: RHPP TU3 Tributary Path Positive Justification Event Counter

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R	PPJE[12]	X
Bit 11	R	PPJE[11]	X
Bit 10	R	PPJE[10]	X
Bit 9	R	PPJE[9]	X
Bit 8	R	PPJE[8]	X
Bit 7	R	PPJE[7]	X
Bit 6	R	PPJE[6]	X
Bit 5	R	PPJE[5]	X
Bit 4	R	PPJE[4]	X
Bit 3	R	PPJE[3]	X
Bit 2	R	PPJE[2]	X
Bit 1	R	PPJE[1]	X
Bit 0	R	PPJE[0]	X

PPJE[12:0]

The Tributary path Positive Justification Event (PPJE[12:0]) bits represent the number of Tributary path Positive Justification Events that have occurred since the last accumulation interval.

Any write to the RHPP TU3 Counters Update Register (address 0x1883) or to the Master Reset and Identity Register (address 0x1800) will trigger the transfer of all counter values to their holding registers.

Register 0x1902: RHPP TU3 Payload Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	TUG3[4]	0
Bit 6	R/W	TUG3[3]	0
Bit 5	R/W	TUG3[2]	0
Bit 4	R/W	TUG3[1]	0
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

TUG3[1]

The TUG3 payload configuration (TUG3[1]) bit selects the payload configuration. When TUG3[1] is set to logic 1, the STS-1/STM-0 tributary paths #1, #5, and #9 are part of a VC-4 payload. When TUG3[1] is set to logic 0, the tributary paths are not part of a VC-4 payload.

TUG3[2]

The TUG3 payload configuration (TUG3[2]) bit selects the payload configuration. When TUG3[2] is set to logic 1, the STS-1/STM-0 tributary paths #2, #6, and #10 are part of a VC-4 payload. When TUG3[2] is set to logic 0, the tributary paths are not part of a VC-4 payload.

TUG3[3]

The TUG3 payload configuration (TUG3[3]) bit selects the payload configuration. When TUG3[3] is set to logic 1, the STS-1/STM-0 tributary paths #3, #7, and #11 are part of a VC-4 payload. When TUG3[3] is set to logic 0, the tributary paths are not part of a VC-4 payload.

TUG3[4]

The TUG3 payload configuration (TUG3[4]) bit selects the payload configuration. When TUG3[4] is set to logic 1, the STS-1/STM-0 tributary paths #4, #8, and #12 are part of a VC-4 payload. When TUG3[4] is set to logic 0, the tributary paths are not part of a VC-4 payload.

Register 0x1903: RHPP TU3 Counters update

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

Any write to the RHPP TU3 Counters Update Register (address 0x1903) or to the Master Reset and Identity Register (address 0x1800) will trigger the transfer of all counter values to their holding registers.

Register 0x1904: RHPP TU3 Tributary Path Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	P_INT[12]	X
Bit 10	R	P_INT[11]	X
Bit 9	R	P_INT[10]	X
Bit 8	R	P_INT[9]	X
Bit 7	R	P_INT[8]	X
Bit 6	R	P_INT[7]	X
Bit 5	R	P_INT[6]	X
Bit 4	R	P_INT[5]	X
Bit 3	R	P_INT[4]	X
Bit 2	R	P_INT[3]	X
Bit 1	R	P_INT[2]	X
Bit 0	R	P_INT[1]	X

When the interrupt output INTB goes low, this register allows the source of the active interrupt to be identified down to the tributary path level. Further register accesses are required for the tributary path in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

P_INT[1:12]

A tributary path interrupt P_INT[1:12] bit is a logic one when an interrupt request is active from the corresponding tributary path. RHPP TU3 Pointer Interpreter Status register (RHPP TU3 Indirect Register 0x05) must be read in order to determine the source of the tributary path interrupt.

Register 0x1908: RHPP TU3 Pointer Interpreter Status(STS-1/STM-0 #1)
Register 0x1910: RHPP TU3 Pointer Interpreter Status (STS-1/STM-0 #2)
Register 0x1918: RHPP TU3 Pointer Interpreter Status (STS-1/STM-0 #3)
Register 0x1920: RHPP TU3 Pointer Interpreter Status (STS-1/STM-0 #4)
Register 0x1928: RHPP TU3 Pointer Interpreter Status (STS-1/STM-0 #5)
Register 0x1930: RHPP TU3 Pointer Interpreter Status (STS-1/STM-0 #6)
Register 0x1938: RHPP TU3 Pointer Interpreter Status (STS-1/STM-0 #7)
Register 0x1940: RHPP TU3 Pointer Interpreter Status (STS-1/STM-0 #8)
Register 0x1948: RHPP TU3 Pointer Interpreter Status (STS-1/STM-0 #9)
Register 0x1950: RHPP TU3 Pointer Interpreter Status (STS-1/STM-0 #10)
Register 0x1958: RHPP TU3 Pointer Interpreter Status (STS-1/STM-0 #11)
Register 0x1960: RHPP TU3 Pointer Interpreter Status (STS-1/STM-0 #12)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	PAISV	X
Bit 2	R	PLOPV	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

PLOPV

The tributary path loss of pointer state (PLOPV) bit indicates the current status of the pointer interpreter state machine. PLOPV is set to logic 1 when the state machine is in the LOP_state. PLOPV is set to logic 0 when the state machine is not in the LOP_state.

PAISV

The tributary path alarm indication signal state (PAISV) bit indicates the current status of the pointer interpreter state machine. PAISV is set to logic 1 when the state machine is in the AIS_state. PAISV is set to logic 0 when the state machine is not in the AIS_state.

Register 0x1909: RHPP TU3 Interpreter Interrupt Enable (STS-1/STM-0 #1)
Register 0x1911: RHPP TU3 Interpreter Interrupt Enable (STS-1/STM-0 #2)
Register 0x1919: RHPP TU3 Interpreter Interrupt Enable (STS-1/STM-0 #3)
Register 0x1921: RHPP TU3 Interpreter Interrupt Enable (STS-1/STM-0 #4)
Register 0x1929: RHPP TU3 Interpreter Interrupt Enable (STS-1/STM-0 #5)
Register 0x1931: RHPP TU3 Interpreter Interrupt Enable (STS-1/STM-0 #6)
Register 0x1939: RHPP TU3 Interpreter Interrupt Enable (STS-1/STM-0 #7)
Register 0x1941: RHPP TU3 Interpreter Interrupt Enable (STS-1/STM-0 #8)
Register 0x1949: RHPP TU3 Interpreter Interrupt Enable (STS-1/STM-0 #9)
Register 0x1951: RHPP TU3 Interpreter Interrupt Enable (STS-1/STM-0 #10)
Register 0x1959: RHPP TU3 Interpreter Interrupt Enable (STS-1/STM-0 #11)
Register 0x1961: RHPP TU3 Interpreter Interrupt Enable (STS-1/STM-0 #12)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	PAISE	0
Bit 2	R/W	PLOPE	0
Bit 1	—	Unused	X
Bit 0	R/W	PTRJEE	0

PTRJEE

The pointer justification event interrupt enable (PTRJEE) bit control the activation of INTB. When PTRJEE is set to logic 1, the NJEI and PJEI pending interrupt will deassert INTB. When PTRJEE is set to logic 0, the NJEI and PJEI pending interrupt will not deassert INTB.

PLOPE

The tributary path loss of pointer interrupt enable (PLOPE) bit controls the activation of INTB. When PLOPE is set to logic 1, the PLOPI pending interrupt will deassert INTB. When PLOPE is set to logic 0, the PLOPI pending interrupt will not deassert INTB.

PAISE

The tributary path alarm indication signal interrupt enable (PAISE) bit controls the activation of INTB. When PAISE is set to logic 1, the PAISI pending interrupt will deassert INTB. When PAISE is set to logic 0, the PAISI pending interrupt will not deassert INTB.

Register 0x190A: RHPP TU3 Interpreter Interrupt Status (STS-1/STM-0 #1)
Register 0x1912: RHPP TU3 Interpreter Interrupt Status (STS-1/STM-0 #2)
Register 0x191A: RHPP TU3 Interpreter Interrupt Status (STS-1/STM-0 #3)
Register 0x1922: RHPP TU3 Interpreter Interrupt Status (STS-1/STM-0 #4)
Register 0x192A: RHPP TU3 Interpreter Interrupt Status (STS-1/STM-0 #5)
Register 0x1932: RHPP TU3 Interpreter Interrupt Status (STS-1/STM-0 #6)
Register 0x193A: RHPP TU3 Interpreter Interrupt Status (STS-1/STM-0 #7)
Register 0x1942: RHPP TU3 Interpreter Interrupt Status (STS-1/STM-0 #8)
Register 0x194A: RHPP TU3 Interpreter Interrupt Status (STS-1/STM-0 #9)
Register 0x1952: RHPP TU3 Interpreter Interrupt Status (STS-1/STM-0 #10)
Register 0x195A: RHPP TU3 Interpreter Interrupt Status (STS-1/STM-0 #11)
Register 0x1962: RHPP TU3 Interpreter Interrupt Status (STS-1/STM-0 #12)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	PAISI	X
Bit 2	R	PLOPI	X
Bit 1	R	PJEI	X
Bit 0	R	NJEI	X

NJEI

The negative pointer justification event interrupt status (NJEI) bit is an event indicator. NJEI is set to logic 1 to indicate a negative pointer justification event. The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), NJEI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), NJEI is cleared by writing a high value to bit 0 of the interrupt status register.

PJEI

The positive pointer justification event interrupt status (PJEI) bit is an event indicator. PJEI is set to logic 1 to indicate a positive pointer justification event. The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), PJEI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PJEI is cleared by writing a high value to bit 1 of the interrupt status register.

PLOPI

The tributary path loss of pointer interrupt status (PLOPI) bit is an event indicator. PLOPI is set to logic 1 to indicate any change in the status of PLOPV (entry to the LOP_state or exit from the LOP_state). The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), PLOPI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PLOPI is cleared by writing a high value to bit 2 of the interrupt status register.

PAISI

The tributary path alarm indication signal interrupt status (PAISI) bit is an event indicator. PAISI is set to logic 1 to indicate any change in the status of PAISV (entry to the AIS_state or exit from the AIS_state). The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), PAISI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PAISI is cleared by writing a high value to bit 3 of the interrupt status register.

Register 0x190B: RHPP TU3 Error Monitor Status (STS-1/STM-0 #1)
Register 0x1913: RHPP TU3 Error Monitor Status (STS-1/STM-0 #2)
Register 0x191B: RHPP TU3 Error Monitor Status (STS-1/STM-0 #3)
Register 0x1923: RHPP TU3 Error Monitor Status (STS-1/STM-0 #4)
Register 0x192B: RHPP TU3 Error Monitor Status (STS-1/STM-0 #5)
Register 0x1933: RHPP TU3 Error Monitor Status (STS-1/STM-0 #6)
Register 0x193B: RHPP TU3 Error Monitor Status (STS-1/STM-0 #7)
Register 0x1943: RHPP TU3 Error Monitor Status (STS-1/STM-0 #8)
Register 0x194B: RHPP TU3 Error Monitor Status (STS-1/STM-0 #9)
Register 0x1953: RHPP TU3 Error Monitor Status (STS-1/STM-0 #10)
Register 0x195B: RHPP TU3 Error Monitor Status (STS-1/STM-0 #11)
Register 0x1963: RHPP TU3 Error Monitor Status (STS-1/STM-0 #12)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R	PERDIV	X
Bit 5	R	PRDIV	X
Bit 4	R	PPDIV	X
Bit 3	R	PUNEQV	X
Bit 2	R	PPLMV	X
Bit 1	R	PPLUV	X
Bit 0	—	Unused	X

PPLUV

The tributary path payload label unstable status (PPLUV) bit indicates the current status of the PLU-V defect. The PLU-V defect is dependent on whether the ITU compliant algorithm (algorithm 2) or the BELLCORE compliant algorithm (algorithm 1) is used (selectable with the ALGO2 register bit).

Algorithm 1: PPLUV is set to logic 0.

Algorithm 2: PPLUV is set to logic 1 when a total of 5 received PSL differs from the previously accepted PSL without any persistent PSL in between. PPLUV is set to logic 0 when a persistent PSL is found. A persistent PSL is found when the same PSL is received for 3 or 5 consecutive frames.

PPLMV

The tributary path payload label mismatch status (PPLMV) bit indicates the current status of the PLM-V defect. The PLM-V defect is dependent on whether the ITU compliant algorithm (algorithm 2) or the BELLCORE compliant algorithm (algorithm 1) is used (selectable with the ALGO2 register bit).

Algorithm 1: PPLMV is set to logic 1 when the received PSL does not match the expected PSL for 3 or 5 consecutive frames (selectable with the PSL5 register bit). PPLMV is set to logic 0 when the received PSL matches the expected PSL for 3 or 5 consecutive frames.

Algorithm 2: PPLMV is set to logic 1 when the accepted PSL does not match the expected PSL. PPLMV is set to logic 0 when the accepted PSL matches the expected PSL.

See the Functional Description Section in the S/UNI 4xJET Data Sheet (PMC-2021632) for further explanation on expected PSL.

PUNEQV

The tributary path unequipped status (PUNEQV) bit indicates the current status of the UNEQ-V defect.

PUNEQV is set to logic 1 when the received PSL indicates unequipped for 3 or 5 consecutive frames (selectable with the PSL5 register bit). A PUNEQV is set to logic 0 when the received PSL indicates not unequipped for 3 or 5 consecutive frames.

See the Functional Description Section in the S/UNI 4xJET Data Sheet (PMC-2021632) for further explanation on expected PSL.

PPDIV

The tributary path payload defect indication status (PPDIV) bit indicates the current status of the PDI-V defect. The PDI-V defect is dependent on whether the ITU compliant algorithm (algorithm 2) or the BELLCORE compliant algorithm (algorithm 1) is used (selectable with the ALGO2 register bit).

Algorithm 1: PPDIV is set to logic one when the received PSL is a defect for 3 or 5 consecutive frames (selectable with the PSL5 register bit). PPDIV is set to logic 0 when the received PSL is not a defect for 3 or 5 consecutive frames.

Algorithm 2: PPDIV is set to logic 1 when the accepted PSL is a defect. PPDI is set to logic 0 when the accepted PSL is not a defect.

See the Functional Description Section in the S/UNI 4xJET Data Sheet (PMC-2021632) for further explanation on defect PSL.

PRDIV

The tributary path remote defect indication status (PRDIV) bit indicates the current status of the RDI-V defect. PRDIV is set to logic 1 when bit 5 of the G1 byte is set high for five or ten consecutive frames (selectable with the PRDI10 register bit). PRDIV is set to logic 0 when bit 5 of the G1 byte is set low for five or ten consecutive frames.

PERDIV

The tributary path enhanced remote defect indication status (PERDIV) bit indicates the current status of the enhanced RDI-V defect. PERDIV is set to logic 1 when the same 010, 100, 101, 110, or 111 pattern is detected in bits 5, 6, and 7 of the G1 byte for five or ten consecutive frames (selectable with the PRDI10 register bit). PERDIV is set to logic 0 when the same 000, 001, or 011 pattern is detected in bits 5, 6, and 7 of the G1 byte for five or ten consecutive frames.

Register 0x190C: RHPP TU3 Error Monitor Interrupt Enable (STS-1/STM-0 #1)
Register 0x1914: RHPP TU3 Error Monitor Interrupt Enable (STS-1/STM-0 #2)
Register 0x191C: RHPP TU3 Error Monitor Interrupt Enable (STS-1/STM-0 #3)
Register 0x1924: RHPP TU3 Error Monitor Interrupt Enable (STS-1/STM-0 #4)
Register 0x192C: RHPP TU3 Error Monitor Interrupt Enable (STS-1/STM-0 #5)
Register 0x1934: RHPP TU3 Error Monitor Interrupt Enable (STS-1/STM-0 #6)
Register 0x193C: RHPP TU3 Error Monitor Interrupt Enable (STS-1/STM-0 #7)
Register 0x1944: RHPP TU3 Error Monitor Interrupt Enable (STS-1/STM-0 #8)
Register 0x194C: RHPP TU3 Error Monitor Interrupt Enable (STS-1/STM-0 #9)
Register 0x1954: RHPP TU3 Error Monitor Interrupt Enable (STS-1/STM-0 #10)
Register 0x195C: RHPP TU3 Error Monitor Interrupt Enable (STS-1/STM-0 #11)
Register 0x1964: RHPP TU3 Error Monitor Interrupt Enable (STS-1/STM-0 #12)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	PREIEE	0
Bit 8	R/W	PBIPEE	0
Bit 7	R/W	COPERDIE	0
Bit 6	R/W	PERDIE	0
Bit 5	R/W	PRDIE	0
Bit 4	R/W	PPDIE	0
Bit 3	R/W	PUNEQE	0
Bit 2	R/W	PPLME	0
Bit 1	R/W	PPLUE	0
Bit 0	R/W	COPSLE	0

COPSLE

The change of tributary path payload signal label interrupt enable (COPSLE) bit controls the activation of INTB. When COPSLE is set to logic 1, the COPSLI pending interrupt will deassert INTB. When COPSLE is set to logic 0, the COPSLI pending interrupt will not deassert INTB.

PPLUE

The tributary path payload label unstable interrupt enable (PPLUE) bit controls the activation of INTB. When PPLUE is set to logic 1, the PPLUI pending interrupt will deassert INTB. When PPLUE is set to logic 0, the PPLUI pending interrupt will not deassert INTB.

PPLME

The tributary path payload label mismatch interrupt enable (PPLME) bit controls the activation of INTB. When PPLME is set to logic 1, the PPLMI pending interrupt will deassert INTB. When PPLME is set to logic 0, the PPLMI pending interrupt will not deassert INTB.

PUNEQE

The tributary path payload unequipped interrupt enable (PUNEQE) bit controls the activation of INTB. When PUNEQE is set to logic 1, the PUNEQI pending interrupt will deassert INTB. When PUNEQE is set to logic 0, the PUNEQI pending interrupt will not deassert INTB.

PPDIE

The tributary path payload defect indication interrupt enable (PPDIE) bit controls the activation of INTB. When PPDIE is set to logic 1, the PPDI pending interrupt will deassert INTB. When PPDIE is set to logic 0, the PPDI pending interrupt will not deassert INTB.

PRDIE

The tributary path remote defect indication interrupt enable (PRDIE) bit controls the activation of INTB. When PRDIE is set to logic 1, the PRDII pending interrupt will deassert INTB. When PRDIE is set to logic 0, the PRDII pending interrupt will not deassert INTB.

PERDIE

The tributary path enhanced remote defect indication interrupt enable (PERDIE) bit controls the activation of INTB. When PERDIE is set to logic 1, the PERDII pending interrupt will deassert INTB. When PERDIE is set to logic 0, the PERDII pending interrupt will not deassert INTB.

COPERDIE

The change of tributary path enhanced remote defect indication interrupt enable (COPERDIE) bit controls the activation of INTB. When COPERDIE is set to logic 1, the COPERDII pending interrupt will deassert INTB. When COPERDIE is set to logic 0, the COPERDII pending interrupt will not deassert INTB.

PBIPEE

The tributary path BIP-8 error interrupt enable (PBIPEE) bit controls the activation of INTB. When PBIPEE is set to logic 1, the PBIPEI pending interrupt will deassert INTB. When PBIPEE is set to logic 0, the PBIPEI pending interrupt will not deassert INTB.

PREIEE

The tributary path REI error interrupt enable (PREIEE) bit controls the activation of INTB. When PREIEE is set to logic 1, the PREIEI pending interrupt will deassert INTB. When PREIEE is set to logic 0, the PREIEI pending interrupt will not deassert INTB.

Register 0x190D: RHPP TU3 Error Monitor Interrupt Status (STS-1/STM-0 #1)
Register 0x1915: RHPP TU3 Error Monitor Interrupt Status (STS-1/STM-0 #2)
Register 0x191D: RHPP TU3 Error Monitor Interrupt Status (STS-1/STM-0 #3)
Register 0x1925: RHPP TU3 Error Monitor Interrupt Status (STS-1/STM-0 #4)
Register 0x192D: RHPP TU3 Error Monitor Interrupt Status (STS-1/STM-0 #5)
Register 0x1935: RHPP TU3 Error Monitor Interrupt Status (STS-1/STM-0 #6)
Register 0x193D: RHPP TU3 Error Monitor Interrupt Status (STS-1/STM-0 #7)
Register 0x1945: RHPP TU3 Error Monitor Interrupt Status (STS-1/STM-0 #8)
Register 0x194D: RHPP TU3 Error Monitor Interrupt Status (STS-1/STM-0 #9)
Register 0x1955: RHPP TU3 Error Monitor Interrupt Status (STS-1/STM-0 #10)
Register 0x195D: RHPP TU3 Error Monitor Interrupt Status (STS-1/STM-0 #11)
Register 0x1965: RHPP TU3 Error Monitor Interrupt Status (STS-1/STM-0 #12)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R	PREIEI	X
Bit 8	R	PBIPEI	X
Bit 7	R	COPERDII	X
Bit 6	R	PERDII	X
Bit 5	R	PRDII	X
Bit 4	R	PPDII	X
Bit 3	R	PUNEQI	X
Bit 2	R	PPLMI	X
Bit 1	R	PPLUI	X
Bit 0	R	COPSLI	X

COPSLI

The change of tributary path payload signal label interrupt status (COPSLI) bit is an event indicator. COPSLI is set to logic 1 to indicate a new PSL-V value. ALGO2 register bit has no effect on COPSLI. The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), COPSLI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), COPSLI is cleared by writing a high value to bit 0 of the interrupt status register.

PPLUI

The tributary path payload label unstable interrupt status (PPLUI) bit is an event indicator. PPLUI is set to logic 1 to indicate any change in the status of PPLUV (stable to unstable or unstable to stable). The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), PPLUI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PPLUI is cleared by writing a high value to bit 1 of the interrupt status register.

PPLMI

The tributary path payload label mismatch interrupt status (PPLMI) bit is an event indicator. PPLMI is set to logic 1 to indicate any change in the status of PPLMV (match to mismatch or mismatch to match). The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), PPLMI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PPLMI is cleared by writing a high value to bit 2 of the interrupt status register.

PUNEQI

The tributary path payload unequipped interrupt status (PUNEQI) bit is an event indicator. PUNEQI is set to logic 1 to indicate any change in the status of PUNEQV (equipped to unequipped or unequipped to equipped). The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), PUNEQI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PUNEQI is cleared by writing a high value to bit 3 of the interrupt status register.

PPDII

The tributary path payload defect indication interrupt status (PPDII) bit is an event indicator. PPDII is set to logic 1 to indicate any change in the status of PPDIV (no defect to payload defect or payload defect to no defect). The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), PPDII is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PPDII is cleared by writing a high value to bit 4 of the interrupt status register.

PRDII

The tributary path remote defect indication interrupt status (PRDII) bit is an event indicator. PRDII is set to logic 1 to indicate any change in the status of PRDIV (no defect to RDI defect or RDI defect to no defect). The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), PRDII is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PRDII is cleared by writing a high value to bit 5 of the interrupt status register.

PERDII

The tributary path enhanced remote defect indication interrupt status (PERDII) bit is an event indicator. PERDII is set to logic 1 to indicate any change in the status of PERDIV (no defect to enhanced RDI defect or enhanced RDI defect to no defect). The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), PERDII is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PERDII is cleared by writing a high value to bit 6 of the interrupt status register.

COPERDII

The change of tributary path enhanced remote defect indication interrupt status (COPERDII) bit is an event indicator. COPERDII is set to logic 1 to indicate a new enhanced RDI-P value. The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), COPERDI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), COPERDI is cleared by writing a high value to bit 7 of the interrupt status register.

PBIPEI

The tributary path BIP-8 error interrupt status (PBIPEI) bit is an event indicator. PBIPEI is set to logic 1 to indicate a tributary path BIP-8 error. The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), PBIPEI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PBIPEI is cleared by writing a high value to bit 8 of the interrupt status register.

PREIEI

The tributary path REI error interrupt status (PREIEI) bit is an event indicator. PREIEI is set to logic 1 to indicate a tributary path REI error. The interrupt status bit is independent of the interrupt enable bit. When WCIMODE is low (read mode), PREIEI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), PREIEI is cleared by writing a high value to bit 9 of the interrupt status register.

Register 0x1980: THPP Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer.

PATH[3:0]	STS-1/STM-0 Path #
0000	Invalid path
0001-1100	Path #1 to #12
1101-1111	Invalid path

IADDR[3:0]

The indirect address (IADDR[3:0]) bits select which address location is accessed by the current indirect transfer.

IADDR[3:0]	Indirect Register
0000	THPP Control Register
0001	THPP Source & Pointer Control
0010	Unused
0011	Unused
0100	THPP Fixed stuff byte and B3MASK
0101	THPP J1 and C2 POH
0110	THPP G1 POH and H4MASK
0111	THPP F2 and Z3 POH

IADDR[3:0]	Indirect Register
1000	THPP Z4 and Z5 POH
1001 to 1111	Unused

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The BUSY (BUSY) bit reports the status of an indirect read/write access to the time sliced ram. BUSY is set to logic 1 upon writing to the Indirect Addressing Register. BUSY is set to logic 0, upon completion of the RAM transfer. This register should be polled to determine when new data is available in the Indirect Data Register.

The maximum busy bit set time is 22 OCLK cycles.

Register 0x1981: THPP Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Indirect Register 0x00: THPP Control

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	TDIS	0
Bit 4	—	Unused	X
Bit 3	R/W	FSBEN	0
Bit 2	R/W	PREIEBLK	0
Bit 1	R/W	EXCFS	0
Bit 0	—	Unused	X

EXCFS

When EXCFS is logic high, the fixed stuff columns in the STS-1 (VC-3) format are excluded from BIP-8 calculations. When EXCFS is logic low, the fixed stuff columns in the STS-1 (VC-3) format are included in the BIP calculations.

PREIEBLK

When PREIEBLK is logic high, the REI-P value sourced from the RHPP represents BIP-8 block errors (i.e. the REI-P value allowed in G1 is either 0 or 1). When PREIEBLK is logic low, the REI-P value sourced from the RHPP represents BIP-8 errors (i.e. the REI-P value allowed in G1 is from 0 to 8).

FSBEN

When FSBEN is logic high, the THPP overwrites the fixed stuff bytes with the register value FSB[7:0]. When FSBEN is logic low, the fixed stuff bytes are passed through transparently from the TX_STI without being overwritten by the THPP.

TDIS

When TDIS is logic high, the path overhead bytes are passed through transparently from the TX_STI without being overwritten by the THPP. When TDIS is logic low, the THPP can insert path overhead bytes according to POH insertion priority.

Indirect Register 0x01: THPP Source and Pointer Control

Bit	Type	Function	Default
Bit 15	R/W	UNEQV	0
Bit 14	R/W	UNEQ	0
Bit 13	R/W	H4TPOHMASK	0
Bit 12	R/W	B3TPOHMASK	0
Bit 11	R/W	ENG1REC	1
Bit 10	R/W	H4REGMASK	0
Bit 9	R/W	PTBJ1	0
Bit 8	R/W	SRCZ5	0
Bit 7	R/W	SRCZ4	0
Bit 6	R/W	SRCZ3	0
Bit 5	R/W	SRCF2	0
Bit 4	R/W	SRCG1	0
Bit 3	R/W	SRCH4	0
Bit 2	R/W	SRCC2	0
Bit 1	R/W	SRCJ1	0
Bit 0	R/W	IBER	0

IBER

The IBER bit forces the G1 path overhead byte to be passed transparently through the THPP from the TX_STI. When IBER is logic high, the G1 byte is passed through the THPP transparently from the TX_STI interface. When IBER is logic low, the G1 byte is inserted according to POH insertion priority.

SRCJ1

The SRCJ1 bit selects the source for the J1 path overhead byte according to POH insertion priority. When SRCJ1 is logic high, the J1 byte can be sourced from the internal J1[7:0] register. When SRCJ1 is logic low, the J1 byte can be sourced from the TPOH port or the TTTP Path block.

SRCC2

The SRCC2 bit selects the source for the C2 path overhead byte according to POH insertion priority. When SRCC2 is logic high, the C2 byte can be sourced from the internal C2[7:0] register. When SRCC2 is logic low, the C2 byte can be sourced from the TPOH port.

SRCH4

The SRCH4 bit selects the source for the H4 path overhead byte according to POH insertion priority.

When SRCH4 is logic high, the H4 byte can be sourced directly from the internal H4[7:0] register, or the internal H4[7:0] register can be used as a mask (XOR) on the H4 byte sourced from the TX_STI (selected by H4REGMASK).

When SRCH4 is logic low, the H4 byte can be sourced directly from TPOH, or the H4 value from TPOH can be used as a mask (XOR) on the H4 byte sourced from the TX_STI (selected by H4TPOHMASK).

SRCG1

The SRCG1 bit selects the source for the G1 path overhead byte according to POH insertion priority. When SRCG1 is logic high, the G1 byte can be sourced from the internal G1[7:0] register. When SRCG1 is logic low, the G1 byte can be sourced from the TPOH port.

SRCF2

The SRCF2 bit selects the source for the F2 path overhead byte according to POH insertion priority. When SRCF2 is logic high, the F2 byte can be sourced from the internal F2[7:0] register. When SRCF2 is logic low, the F2 byte can be sourced from the TPOH port.

SRCZ3

The SRCZ3 bit selects the source for the Z3 path overhead byte according to POH insertion priority. When SRCZ3 is logic high, the Z3 byte can be sourced from the internal Z3[7:0] register. When SRCZ3 is logic low, the Z3 byte can be sourced from the TPOH port.

SRCZ4

The SRCZ4 bit selects the source for the Z4 path overhead byte according to POH insertion priority. When SRCZ4 is logic high, the Z4 byte can be sourced from the internal Z4[7:0] register. When SRCZ4 is logic low, the Z4 byte can be sourced from the TPOH port.

SRCZ5

The SRCZ5 bit selects the source for the Z5 path overhead byte according to POH insertion priority. When SRCZ5 is logic high, the Z5 byte can be sourced from the internal Z5[7:0] register. When SRCZ5 is logic low, the Z5 byte can be sourced from the TPOH port.

PTBJ1

The PTBJ1 bit selects the source for the J1 path overhead byte according to POH insertion priority. When PTBJ1 is logic high, the J1 byte can be sourced from the TTTP Path. When PTBJ1 is logic low, the J1 byte can be sourced from internal J1[7:0] register or from the TPOH port.

H4REGMASK

The H4REGMASK bit enables the internal H4[7:0] register to be used as a mask (XOR) on the H4 byte sourced from the TX_STI. When H4REGMASK is logic high, the internal H4[7:0] register is used as a mask (XOR) on the H4 byte sourced from the TX_STI. When H4REGMASK is logic low, the H4[7:0] register is used as the source of the H4 path overhead byte.

ENG1REC

The PTBJ1 bit selects the source for the J1 path overhead byte according to POH insertion priority. When PTBJ1 is logic high, the J1 byte can be sourced from the TTTP Path. When PTBJ1 is logic low, the J1 byte can be sourced from internal J1[7:0] register or from the TPOH port.

The ENG1REC bit allows the G1 byte to be modified by the RHPP according to POH insertion priority. When ENG1REC is logic high, the enhanced RDI-P and REI-P from the RHPP are inserted into the G1 byte sourced from the TX_STI. When ENG1REC is logic low, the G1 byte can be sourced from internal G1[7:0] register or from the TPOH port.

B3TPOHMASK

The B3TPOHMASK bit enables the B3 byte from TPOH to be used as a mask (XOR) on the calculated B3 byte. When B3TPOHMASK is logic high, the B3 byte from TPOH is used as a mask (XOR) on the calculated B3 byte. When B3TPOHMASK is logic low, the B3 byte from TPOH is used as the source of the B3 path overhead byte.

H4TPOHMASK

The H4TPOHMASK bit enables the H4 byte from TPOH to be used as a mask (XOR) on the H4 byte sourced from the TX_STI. When H4TPOHMASK is logic high, the H4 byte from TPOH is used as a mask (XOR) on the H4 byte sourced from the TX_STI. When H4TPOHMASK is logic low, the H4 byte from TPOH is used as the source of the H4 path overhead byte.

UNEQ

The unequipped bit (UNEQ) controls the insertion of an all-one or an all-zero pattern in the path overhead and in the payload. When UNEQ is logic high, the pattern specified by UNEQV is inserted in the path overhead and in the payload. When UNEQ is logic low, no pattern is inserted.

The fixed stuff bytes are excluded from the all-one or all-zero pattern insertion.

UNEQV

The unequipped value (UNEQV) bit controls the value inserted in the path overhead and in the payload when UNEQ is logic high. When UNEQV is logic high, an all-ones pattern is inserted in the path overhead and in the payload. When UNEQV is logic low, an all-zeros pattern is inserted in the path overhead and in the payload.

Indirect Register 0x04: THPP Fixed Stuff and B3 Mask

Bit	Type	Function	Default
Bit 15	R/W	B3MASK[7]	0
Bit 14	R/W	B3MASK[6]	0
Bit 13	R/W	B3MASK[5]	0
Bit 12	R/W	B3MASK[4]	0
Bit 11	R/W	B3MASK[3]	0
Bit 10	R/W	B3MASK[2]	0
Bit 9	R/W	B3MASK[1]	0
Bit 8	R/W	B3MASK[0]	0
Bit 7	R/W	FSB[7]	0
Bit 6	R/W	FSB[6]	0
Bit 5	R/W	FSB[5]	0
Bit 4	R/W	FSB[4]	0
Bit 3	R/W	FSB[3]	0
Bit 2	R/W	FSB[2]	0
Bit 1	R/W	FSB[1]	0
Bit 0	R/W	FSB[0]	0

FSB[7:0]

When FSBEN is logic high, the THPP replaces the fixed stuff bytes with the byte from this register. When FSBEN is logic low, this byte has no effect on the fixed stuff bytes.

B3MASK[7:0]

The calculated B3 byte to be inserted in the path overhead is XORed with this byte to allow the user to insert errors in B3.

Indirect Register 0x05: THPP J1 and C2

Bit	Type	Function	Default
Bit 15	R/W	C2[7]	0
Bit 14	R/W	C2[6]	0
Bit 13	R/W	C2[5]	0
Bit 12	R/W	C2[4]	0
Bit 11	R/W	C2[3]	0
Bit 10	R/W	C2[2]	0
Bit 9	R/W	C2[1]	0
Bit 8	R/W	C2[0]	0
Bit 7	R/W	J1[7]	0
Bit 6	R/W	J1[6]	0
Bit 5	R/W	J1[5]	0
Bit 4	R/W	J1[4]	0
Bit 3	R/W	J1[3]	0
Bit 2	R/W	J1[2]	0
Bit 1	R/W	J1[1]	0
Bit 0	R/W	J1[0]	0

J1[7:0]

When SRCJ1 is logic high, this byte is inserted in the J1 path overhead byte. When SRCJ1 is logic low, this byte has no effect on the J1 path overhead byte.

C2[7:0]

When SRCC2 is logic high, this byte is inserted in the C2 path overhead byte. When SRCC2 is logic low, this byte has no effect on the C2 path overhead byte.

Indirect Register 0x06: THPP G1 and H4 mask

Bit	Type	Function	Default
Bit 15	R/W	H4[7]	0
Bit 14	R/W	H4[6]	0
Bit 13	R/W	H4[5]	0
Bit 12	R/W	H4[4]	0
Bit 11	R/W	H4[3]	0
Bit 10	R/W	H4[2]	0
Bit 9	R/W	H4[1]	0
Bit 8	R/W	H4[0]	0
Bit 7	R/W	G1[7]	0
Bit 6	R/W	G1[6]	0
Bit 5	R/W	G1[5]	0
Bit 4	R/W	G1[4]	0
Bit 3	R/W	G1[3]	0
Bit 2	R/W	G1[2]	0
Bit 1	R/W	G1[1]	0
Bit 0	R/W	G1[0]	0

G1[7:0]

When SRCG1 is logic high, this byte is inserted in the G1 path overhead byte. When SRCG1 is logic low, this byte has no effect on the G1 path overhead byte.

H4[7:0]

When SRCH4 is logic high, this byte is either inserted in the H4 path overhead byte, or used as an XOR error mask (selected by H4REGMASK). When SRCH4 is logic low, this byte has no effect on the H4 path overhead byte.

Indirect Register 0x07: THPP F2 and Z3

Bit	Type	Function	Default
Bit 15	R/W	F2[7]	0
Bit 14	R/W	F2[6]	0
Bit 13	R/W	F2[5]	0
Bit 12	R/W	F2[4]	0
Bit 11	R/W	F2[3]	0
Bit 10	R/W	F2[2]	0
Bit 9	R/W	F2[1]	0
Bit 8	R/W	F2[0]	0
Bit 7	R/W	Z3[7]	0
Bit 6	R/W	Z3[6]	0
Bit 5	R/W	Z3[5]	0
Bit 4	R/W	Z3[4]	0
Bit 3	R/W	Z3[3]	0
Bit 2	R/W	Z3[2]	0
Bit 1	R/W	Z3[1]	0
Bit 0	R/W	Z3[0]	0

F2[7:0]

When SRCF2 is logic high, this byte is inserted in the F2 path overhead byte. When SRCF2 is logic low, this byte has no effect on the F2 path overhead byte.

Z3[7:0]

When SRCZ3 is logic high, this byte is inserted in the Z3 path overhead byte. When SRCZ3 is logic low, this byte has no effect on the Z3 path overhead byte.

Indirect Register 0x08: THPP Z4 and Z5

Bit	Type	Function	Default
Bit 15	R/W	Z4[7]	0
Bit 14	R/W	Z4[6]	0
Bit 13	R/W	Z4[5]	0
Bit 12	R/W	Z4[4]	0
Bit 11	R/W	Z4[3]	0
Bit 10	R/W	Z4[2]	0
Bit 9	R/W	Z4[1]	0
Bit 8	R/W	Z4[0]	0
Bit 7	R/W	Z5[7]	0
Bit 6	R/W	Z5[6]	0
Bit 5	R/W	Z5[5]	0
Bit 4	R/W	Z5[4]	0
Bit 3	R/W	Z5[3]	0
Bit 2	R/W	Z5[2]	0
Bit 1	R/W	Z5[1]	0
Bit 0	R/W	Z5[0]	0

Z4[7:0]

When SRCZ4 is logic high, this byte is inserted in the Z4 path overhead byte. When SRCZ4 is logic low, this byte has no effect on the Z4 path overhead byte.

Z5[7:0]

When SRCZ5 is logic high, this byte is inserted in the Z5 path overhead byte. When SRCZ5 is logic low, this byte has no effect on the Z5 path overhead byte.

Register 0x1982: THPP Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	STS12C	0
Bit 13	R/W	Reserved	0
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	STS3C[4]	0
Bit 2	R/W	STS3C[3]	0
Bit 1	R/W	STS3C[2]	0
Bit 0	R/W	STS3C[1]	0

STS3C[1]

The STS-3c (VC-4) payload configuration (STS3C[1]) bit selects the payload configuration. When STS3C[1] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a STS-3c (VC-4) payload. When STS3C[1] is set to logic 0, the paths are STS-1 (VC-3) payloads.

When STS12C is set to logic 1, STS3C[1] must be set to logic 0.

STS3C[2]

The STS-3c (VC-4) payload configuration (STS3C[2]) bit selects the payload configuration. When STS3C[2] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a STS-3c (VC-4) payload. When STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads.

When STS12C is set to logic 1, STS3C[2] must be set to logic 0.

STS3C[3]

The STS-3c (VC-4) payload configuration (STS3C[3]) bit selects the payload configuration. When STS3C[3] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a STS-3c (VC-4) payload. When STS3C[3] is set to logic 0, the paths are STS-1 (VC-3) payloads.

When STS12C is set to logic 1, STS3C[3] must be set to logic 0.

STS3C[4]

The STS-3c (VC-4) payload configuration (STS3C[4]) bit selects the payload configuration. When STS3C[4] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a STS-3c (VC-4) payload. When STS3C[4] is set to logic 0, the paths are STS-1 (VC-3) payloads.

When STS12C is set to logic 1, STS3C[4] must be set to logic 0.

STS12C

The STS-12c (VC-4-4c) payload configuration (STS12C) bit selects the payload configuration. When STS12C is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of an STS-12c (VC-4-4c) payload. When STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the STS3C[1:4] register bit.

Register 0x1988: THPP TU3 Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The STS-1/STM-0 tributary path (PATH[3:0]) bits select which STS-1/STM-0 tributary path is accessed by the current indirect transfer.

PATH[3:0]	STS-1/STM-0 Tributary Path #
0000	Invalid
0001-1100	Tributary Path #1 to #12
1101-1111	Invalid

IADDR[3:0]

The indirect address (IADDR[3:0]) bits select which address location is accessed by the current indirect transfer.

IADDR[3:0]	Indirect Register
0000	THPP TU3 Control Register
0001	THPP TU3 Source & Pointer Control
0010	Unused
0011	Unused
0100	THPP TU3 Fixed stuff byte and B3MASK
0101	THPP TU3 J1 and C2 POH
0110	THPP TU3 G1 POH and H4MASK
0111	THPP TU3 F2 and Z3 POH

IADDR[3:0]	Indirect Register
1000	THPP TU3 Z4 and Z5 POH
1001 to 1111	Unused

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The BUSY (BUSY) bit reports the status of an indirect read/write access to the time sliced ram. BUSY is set to logic 1 upon writing to the Indirect Addressing Register. BUSY is set to logic 0, upon completion of the RAM transfer. This register should be polled to determine when new data is available in the Indirect Data Register.

The maximum busy bit set time is 22 OCLK cycles.

Register 0x1989: THPP TU3 Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Indirect Register 0x00: THPP TU3 Control

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	TDIS	0
Bit 4	—	Unused	X
Bit 3	R/W	FSBEN	0
Bit 2	R/W	PREIEBLK	0
Bit 1	R/W	EXCFS	0
Bit 0	—	Unused	X

EXCFS

When EXCFS is logic high, the fixed stuff columns in the VC-3 format are excluded from BIP-8 calculations. When EXCFS is logic low, the fixed stuff columns in the VC-3 format are included in the BIP calculations.

PREIEBLK

When PREIEBLK is logic high, the REI-V value source from the RHPP represents BIP-8 block errors (i.e. the REI-V value allowed in G1 is either 0 or 1). When PREIEBLK is logic low, the REI-V value source from the RHPP represents BIP-8 errors (i.e. the REI-V value allowed in G1 is from 0 to 8).

FSBEN

When FSBEN is logic high, the THPP overwrites the fixed stuff bytes with the register value FSB[7:0]. When FSBEN is logic low, the fixed stuff bytes passed through transparently from the TX_STI without being overwritten by the THPP TU3.

TDIS

When TDIS is logic high, the path overhead bytes are passed through transparently from the TX_STI without being overwritten by the THPP. When TDIS is logic low, the THPP can insert tributary path overhead bytes according to POH insertion priority.

Indirect Register 0x01: THPP TU3 Source and Pointer Control

Bit	Type	Function	Default
Bit 15	R/W	UNEQV	0
Bit 14	R/W	UNEQ	0
Bit 13	R/W	H4MASK	0
Bit 12	R/W	B3MASK	0
Bit 11	R/W	ENG1REC	1
Bit 10	R/W	H4REGMASK	0
Bit 9	R/W	PTBJ1	0
Bit 8	R/W	SRCZ5	0
Bit 7	R/W	SRCZ4	0
Bit 6	R/W	SRCZ3	0
Bit 5	R/W	SRCF2	0
Bit 4	R/W	SRCG1	0
Bit 3	R/W	SRCH4	0
Bit 2	R/W	SRCC2	0
Bit 1	R/W	SRCJ1	0
Bit 0	R/W	IBER	0

IBER

The IBER bit forces the G1 tributary path overhead byte to be passed transparently through the THPP TU3 from the TX_STI. When IBER is logic high, the G1 byte is passed through the THPP TU3 transparently from the TX_STI interface. When IBER is logic low, the G1 byte is inserted according to POH insertion priority.

SRCJ1

The SRCJ1 bit selects the source for the J1 tributary path overhead byte according to POH insertion priority. When SRCJ1 is logic high, the J1 byte can be sourced from the internal J1[7:0] register. When SRCJ1 is logic low, the J1 byte can be sourced from the TPOH port or the TTTP TU3 Tributary Path block.

SRCC2

The SRCC2 bit selects the source for the C2 tributary path overhead byte according to POH insertion priority. When SRCC2 is logic high, the C2 byte can be sourced from the internal C2[7:0] register. When SRCC2 is logic low, the C2 byte can be sourced from the TPOH port.

SRCH4

The SRCH4 bit selects the source for the H4 tributary path overhead byte according to POH insertion priority.

When SRCH4 is logic high, the H4 byte can be sourced directly from the internal H4[7:0] register, or the internal H4[7:0] register can be used as a mask (XOR) on the H4 byte sourced from the TX_STI (selected by H4REGMASK).

When SRCH4 is logic low, the H4 byte can be sourced directly from TPOH, or the H4 value from TPOH can be used as a mask (XOR) on the H4 byte sourced from the TX_STI (selected by H4TPOHMASK).

SRCG1

The SRCG1 bit selects the source for the G1 tributary path overhead byte according to POH insertion priority. When SRCG1 is logic high, the G1 byte can be sourced from the internal G1[7:0] register. When SRCG1 is logic low, the G1 byte can be sourced from the TPOH port.

SRCF2

The SRCF2 bit selects the source for the F2 tributary path overhead byte according to POH insertion priority. When SRCF2 is logic high, the F2 byte can be sourced from the internal F2[7:0] register. When SRCF2 is logic low, the F2 byte can be sourced from the TPOH port.

SRCZ3

The SRCZ3 bit selects the source for the Z3 tributary path overhead byte according to POH insertion priority. When SRCZ3 is logic high, the Z3 byte can be sourced from the internal Z3[7:0] register. When SRCZ3 is logic low, the Z3 byte can be sourced from the TPOH port.

SRCZ4

The SRCZ4 bit selects the source for the Z4 tributary path overhead byte according to POH insertion priority. When SRCZ4 is logic high, the Z4 byte can be sourced from the internal Z4[7:0] register. When SRCZ4 is logic low, the Z4 byte can be sourced from the TPOH port.

SRCZ5

The SRCZ5 bit selects the source for the Z5 tributary path overhead byte according to POH insertion priority. When SRCZ5 is logic high, the Z5 byte can be sourced from the internal Z5[7:0] register. When SRCZ5 is logic low, the Z5 byte can be sourced from the TPOH port.

PTBJ1

The PTBJ1 bit selects the source for the J1 tributary path overhead byte according to POH insertion priority. When PTBJ1 is logic high, the J1 byte can be sourced from the TTTP Path. When PTBJ1 is logic low, the J1 byte can be sourced from internal J1[7:0] register or from the TPOH port.

H4REGMASK

The H4REGMASK bit enables the internal H4[7:0] register to be used as a mask (XOR) on the H4 byte sourced from the TX_STI. When H4REGMASK is logic high, the internal H4[7:0] register is used as a mask (XOR) on the H4 byte sourced from the TX_STI. When H4REGMASK is logic low, the H4[7:0] register is used as the source of the H4 tributary path overhead byte.

ENG1REC

The PTBJ1 bit selects the source for the J1 tributary path overhead byte according to POH insertion priority. When PTBJ1 is logic high, the J1 byte can be sourced from the TTTP Path. When PTBJ1 is logic low, the J1 byte can be sourced from internal J1[7:0] register or from the TPOH port.

The ENG1REC bit allows the G1 byte to be modified by the RHPP according to POH insertion priority. When ENG1REC is logic high, the enhanced RDI-P and REI-P from the RHPP are inserted into the G1 byte sourced from the TX_STI. When ENG1REC is logic low, the G1 byte can be sourced from internal G1[7:0] register or from the TPOH port.

B3TPOHMASK

The B3TPOHMASK bit enables the B3 byte from TPOH to be used as a mask (XOR) on the calculated B3 byte. When B3TPOHMASK is logic high, the B3 byte from TPOH is used as a mask (XOR) on the calculated B3 byte. When B3TPOHMASK is logic low, the B3 byte from TPOH is used as the source of the B3 tributary path overhead byte.

H4TPOHMASK

The H4TPOHMASK bit enables the H4 byte from TPOH to be used as a mask (XOR) on the H4 byte sourced from the TX_STI. When H4TPOHMASK is logic high, the H4 byte from TPOH is used as a mask (XOR) on the H4 byte sourced from the TX_STI. When H4TPOHMASK is logic low, the H4 byte from TPOH is used as the source of the H4 tributary path overhead byte.

UNEQ

The unequipped bit (UNEQ) controls the insertion of an all-one or an all-zero pattern in the tributary path overhead and in the payload. When UNEQ is logic high, the pattern specified by UNEQV is inserted in the tributary path overhead and in the payload. When UNEQ is logic low, no pattern is inserted.

The fixed stuff bytes are excluded from the all-one or all-zero pattern insertion.

UNEQV

The unequipped value (UNEQV) bit controls the value inserted in the tributary path overhead and in the payload when UNEQ is logic high. When UNEQV is logic high, an all-ones pattern is inserted in the tributary path overhead and in the payload. When UNEQV is logic low, an all-zeros pattern is inserted in the tributary path overhead and in the payload.

Indirect Register 0x04: THPP TU3 Fixed Stuff and B3 Mask

Bit	Type	Function	Default
Bit 15	R/W	B3MASK[7]	0
Bit 14	R/W	B3MASK[6]	0
Bit 13	R/W	B3MASK[5]	0
Bit 12	R/W	B3MASK[4]	0
Bit 11	R/W	B3MASK[3]	0
Bit 10	R/W	B3MASK[2]	0
Bit 9	R/W	B3MASK[1]	0
Bit 8	R/W	B3MASK[0]	0
Bit 7	R/W	FSB[7]	0
Bit 6	R/W	FSB[6]	0
Bit 5	R/W	FSB[5]	0
Bit 4	R/W	FSB[4]	0
Bit 3	R/W	FSB[3]	0
Bit 2	R/W	FSB[2]	0
Bit 1	R/W	FSB[1]	0
Bit 0	R/W	FSB[0]	0

FSB[7:0]

When FSBEN is logic high, the THPP-TU3 replaces the fixed stuff bytes with the byte from this register. When FSBEN is logic low, this byte has no effect on the fixed stuff bytes.

B3MASK[7:0]

The calculated B3 byte to be inserted in the tributary path overhead is XORed with this byte to allow the user to insert errors in B3.

Indirect Register 0x05: THPP TU3 J1 and C2

Bit	Type	Function	Default
Bit 15	R/W	C2[7]	0
Bit 14	R/W	C2[6]	0
Bit 13	R/W	C2[5]	0
Bit 12	R/W	C2[4]	0
Bit 11	R/W	C2[3]	0
Bit 10	R/W	C2[2]	0
Bit 9	R/W	C2[1]	0
Bit 8	R/W	C2[0]	0
Bit 7	R/W	J1[7]	0
Bit 6	R/W	J1[6]	0
Bit 5	R/W	J1[5]	0
Bit 4	R/W	J1[4]	0
Bit 3	R/W	J1[3]	0
Bit 2	R/W	J1[2]	0
Bit 1	R/W	J1[1]	0
Bit 0	R/W	J1[0]	0

J1[7:0]

When SRCJ1 is logic high, this byte is inserted in the J1 tributary path overhead byte. When SRCJ1 is logic low, this byte has no effect on the J1 tributary path overhead byte.

C2[7:0]

When SRCC2 is logic high, this byte is inserted in the C2 tributary path overhead byte. When SRCC2 is logic low, this byte has no effect on the C2 tributary path overhead byte.

Indirect Register 0x06: THPP TU3 G1 and H4 mask

Bit	Type	Function	Default
Bit 15	R/W	H4[7]	0
Bit 14	R/W	H4[6]	0
Bit 13	R/W	H4[5]	0
Bit 12	R/W	H4[4]	0
Bit 11	R/W	H4[3]	0
Bit 10	R/W	H4[2]	0
Bit 9	R/W	H4[1]	0
Bit 8	R/W	H4[0]	0
Bit 7	R/W	G1[7]	0
Bit 6	R/W	G1[6]	0
Bit 5	R/W	G1[5]	0
Bit 4	R/W	G1[4]	0
Bit 3	R/W	G1[3]	0
Bit 2	R/W	G1[2]	0
Bit 1	R/W	G1[1]	0
Bit 0	R/W	G1[0]	0

G1[7:0]

When SRCG1 is logic high, this byte is inserted in the G1 tributary path overhead byte. When SRCG1 is logic low, this byte has no effect on the G1 tributary path overhead byte.

H4[7:0]

When SRCH4 is logic high, this byte is either inserted in the H4 tributary path overhead byte, or used as an XOR error mask (selected by H4REGMASK). When SRCH4 is logic low, this byte has no effect on the H4 tributary path overhead byte.

Indirect Register 0x07: THPP TU3 F2 and Z3

Bit	Type	Function	Default
Bit 15	R/W	F2[7]	0
Bit 14	R/W	F2[6]	0
Bit 13	R/W	F2[5]	0
Bit 12	R/W	F2[4]	0
Bit 11	R/W	F2[3]	0
Bit 10	R/W	F2[2]	0
Bit 9	R/W	F2[1]	0
Bit 8	R/W	F2[0]	0
Bit 7	R/W	Z3[7]	0
Bit 6	R/W	Z3[6]	0
Bit 5	R/W	Z3[5]	0
Bit 4	R/W	Z3[4]	0
Bit 3	R/W	Z3[3]	0
Bit 2	R/W	Z3[2]	0
Bit 1	R/W	Z3[1]	0
Bit 0	R/W	Z3[0]	0

F2[7:0]

When SRCF2 is logic high, this byte is inserted in the F2 tributary path overhead byte. When SRCF2 is logic low, this byte has no effect on the F2 tributary path overhead byte.

Z3[7:0]

When SRCZ3 is logic high, this byte is inserted in the Z3 tributary path overhead byte. When SRCZ3 is logic low, this byte has no effect on the Z3 tributary path overhead byte.

Indirect Register 0x08: THPP TU3 Z4 and Z5

Bit	Type	Function	Default
Bit 15	R/W	Z4[7]	0
Bit 14	R/W	Z4[6]	0
Bit 13	R/W	Z4[5]	0
Bit 12	R/W	Z4[4]	0
Bit 11	R/W	Z4[3]	0
Bit 10	R/W	Z4[2]	0
Bit 9	R/W	Z4[1]	0
Bit 8	R/W	Z4[0]	0
Bit 7	R/W	Z5[7]	0
Bit 6	R/W	Z5[6]	0
Bit 5	R/W	Z5[5]	0
Bit 4	R/W	Z5[4]	0
Bit 3	R/W	Z5[3]	0
Bit 2	R/W	Z5[2]	0
Bit 1	R/W	Z5[1]	0
Bit 0	R/W	Z5[0]	0

Z4[7:0]

When SRCZ4 is logic high, this byte is inserted in the Z4 tributary path overhead byte.
When SRCZ4 is logic low, this byte has no effect on the Z4 tributary path overhead byte.

Z5[7:0]

When SRCZ5 is logic high, this byte is inserted in the Z5 tributary path overhead byte.
When SRCZ5 is logic low, this byte has no effect on the Z5 tributary path overhead byte.

Register 0x198A: THPP TU3 Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	TUG3[4]	0
Bit 6	R/W	TUG3[3]	0
Bit 5	R/W	TUG3[2]	0
Bit 4	R/W	TUG3[1]	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

TUG3[1]

The TUG3 payload configuration (TUG3[1]) bit selects the payload configuration. When TUG3[1] is set to logic 1, the STS-1/STM-0 tributary paths #1, #5 and #9 are part of a VC-4 payload. When TUG3[1] is set to logic 0, the tributary paths are not part of a VC-4 payload.

TUG3[2]

The TUG3 payload configuration (TUG3[2]) bit selects the payload configuration. When TUG3[2] is set to logic 1, the STS-1/STM-0 tributary paths #2, #6 and #10 are part of a VC-4 payload. When TUG3[2] is set to logic 0, the tributary paths are not part of a VC-4 payload.

TUG3[3]

The TUG3 payload configuration (TUG3[3]) bit selects the payload configuration. When TUG3[3] is set to logic 1, the STS-1/STM-0 tributary paths #3, #7 and #11 are part of a VC-4 payload. When TUG3[3] is set to logic 0, the tributary paths are not part of a VC-4 payload.

TUG3[4]

The TUG3 payload configuration (TUG3[4]) bit selects the payload configuration. When TUG3[4] is set to logic 1, the STS-1/STM-0 tributary paths #4, #8 and #12 are part of a VC-4 payload. When TUG3[4] is set to logic 0, the tributary paths are not part of a VC-4 payload.

Register 0x19B8: RTTP Path Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	R/W	IADDR[7]	0
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer. When the RTTP monitors path trace messages, paths #1 to #12 are valid.

PATH[3:0]	STS-1/STM-0 Path #
0000	Invalid
0001-1100	Path #1 to #12
1101-1111	Invalid

IADDR[7:0]

The indirect address location (IADDR[7:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[7:0]	Indirect Data
0000 0000	Configuration
0000 0001 to 0011 1111	Invalid address
0100 0000	First byte of the 1/16/64 byte captured trace

Indirect Address IADDR[7:0]	Indirect Data
0100 0001 to 0111 1111	Remaining bytes of the 16/64 byte captured trace
1000 0000	First byte of the 1/16/64 byte accepted trace
1000 0001 to 1011 1111	Remaining bytes of the 16/64 byte accepted trace
1100 0000	First byte of the 16/64 byte expected trace
1100 0001 to 1111 1111	Remaining bytes of the 16/64 byte expected trace

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

The maximum busy bit set time is 22 ICLK cycles.

Register 0x19B9: RTTP Path Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Indirect Register 0x00: RTTP Path Trace Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	SYNCCRLF	0
Bit 5	R/W	ZEROEN	0
Bit 4	R/W	PER5	0
Bit 3	R/W	NOSYNC	0
Bit 2	R/W	LENGTH16	0
Bit 1	R/W	ALGO[1]	0
Bit 0	R/W	ALGO[0]	0

ALGO[1:0]

The trail trace algorithm select (ALGO[1:0]) bits select the algorithm used to process the trail trace message.

ALGO[1:0]	Trail Trace Algorithm
00	Algorithm disable
01	Algorithm 1
10	Algorithm 2
11	Algorithm 3

When the trail trace algorithm is disabled the corresponding TIUV, TIMV status register bits and the corresponding TIU-P, TIM-P defects are suppressed.

LENGTH16

The message length (LENGTH16) bit selects the length of the trail trace message used by algorithm 1 and algorithm 2. When LENGTH16 is set to logic 1, the length of the trail trace message is 16 bytes. When LENGTH16 is set to logic 0, the length of the trail trace message is 64 bytes.

NOSYNC

The synchronization disable (NOSYNC) bit disables the synchronization of the trail trace message in algorithm 1 and algorithm 2. When NOSYNC is set to logic 1, no synchronization is done on the trail trace message. The bytes of the trail trace message are written in the captured page as in a circular buffer. When NOSYNC is set to logic 0, synchronization is done on the trail trace message. Refer to SYNCCRLF to determine how synchronization is handled when NOSYNC is set to logic 0.

PER5

The message persistency (PER5) bit selects the number of multi-frames a trail trace message must receive in order to be declared persistent in algorithm 2. When PER5 is set to logic 1, the same trail trace message must be received for 5 consecutive multi-frames to be declared persistent. When PER5 is set to logic 0, the same trail trace message must be received for 3 consecutive multi-frames to be declared persistent.

ZEROEN

The all-zero message enable (ZEROEN) bit selects if the all-zero messages are validated or not against the expected message in algorithm 1 and algorithm 2. When ZEROEN is set to logic 1, an all-zero captured message in algorithm 1 and an all-zero accepted message in algorithm 2 are validated against the expected message. A match is declared when both the captured/accepted message and the expected message are all-zero. When ZEROEN is set to logic 0, an all-zero captured message in algorithm 1 and an all-zero accepted message in algorithm 2 are not validated against the expected message but are considered match. A match is declared when the captured/accepted message is all-zero regardless of the expected message.

SYNCCRLF

The synchronization on CR/LF characters (SYNCCRLF) bit selects if the current algorithm (except algo3) synchronizes on the CR/LF ASCII characters or on the byte with its MSB set high. When SYNCCRLF is set to logic 1, the current algorithm synchronizes when it receives the ASCII character “CR” (carriage return) followed by “LF” (line feed) and the current active byte becomes the last byte of the message. When SYNCCRLF is set to 0, the current algorithm synchronizes when receiving a byte with its MSB set to logic 1. The current active byte then becomes the first byte of the message.

Indirect Register 0x40 to 0x7F: RTTP Path Trace Captured

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	CTRACE[7]	X
Bit 6	R	CTRACE[6]	X
Bit 5	R	CTRACE[5]	X
Bit 4	R	CTRACE[4]	X
Bit 3	R	CTRACE[3]	X
Bit 2	R	CTRACE[2]	X
Bit 1	R	CTRACE[1]	X
Bit 0	R	CTRACE[0]	X

CTRACE[7:0]

The captured trail trace message (CTRACE[7:0]) bits contain the currently received trail trace message.

When algorithm 1 or 2 is selected and LENGTH16 is set to logic 1, the captured message is stored between indirect address 40h and 4Fh. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 0, the captured message is stored between indirect address 40h and 7Fh. When NOSYNC is set to logic 1, the captured message is not synchronized. When NOSYNC is set to logic 0, the captured message is synchronized and the first byte of the message is stored at indirect address 40h.

When algorithm 3 is selected, the captured byte is stored at indirect address 40h.

Indirect Register 0x80 to 0xBF: RTTP Path Trace Accepted

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	ATRACE[7]	X
Bit 6	R	ATRACE[6]	X
Bit 5	R	ATRACE[5]	X
Bit 4	R	ATRACE[4]	X
Bit 3	R	ATRACE[3]	X
Bit 2	R	ATRACE[2]	X
Bit 1	R	ATRACE[1]	X
Bit 0	R	ATRACE[0]	X

ATRACE[7:0]

The accepted trail trace message (ATRACE[7:0]) bits contain the persistent trail trace message.

When algorithm 1 is selected, the accepted message will not be updated.

When algorithm 2 is selected and PER5 is set to logic 1, the accepted message is the same trail trace message received for 5 consecutive multi-frames. When algorithm 2 is selected and PER5 is set to logic 0, the accepted message is the same trail trace message received for 3 consecutive multi-frames. When algorithm 2 is selected and LENGTH16 is set to logic 1, the accepted message is stored between indirect address 80h and 8Fh. When algorithm 2 is selected and LENGTH16 is set to logic 0, the accepted message is stored between indirect address 80h and BFh.

When algorithm 3 is selected, the accepted byte is the same trail trace byte received for 48 frames. When algorithm 3 is selected, the accepted byte is stored at indirect address 80h.

Indirect Register 0xC0 to 0xFF: RTTP Path Trace Expected

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	ETRACE[7]	X
Bit 6	R/W	ETRACE[6]	X
Bit 5	R/W	ETRACE[5]	X
Bit 4	R/W	ETRACE[4]	X
Bit 3	R/W	ETRACE[3]	X
Bit 2	R/W	ETRACE[2]	X
Bit 1	R/W	ETRACE[1]	X
Bit 0	R/W	ETRACE[0]	X

ETRACE[7:0]

The expected trail trace message (ETRACE[7:0]) bits contain a static message written by an external microprocessor.

In algorithm 1 the expected message is used to validated the captured message.

In algorithm 2 the expected message is used to validate the accepted message. When LENGTH16 is set to logic 1, the expected message must be written between indirect address C0h and CFh. When LENGTH16 is set to logic 0, the accepted message must be written between indirect address C0h and FFh.

Register 0x19BA: RTTP Path Trace Unstable Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	TIUV[12]	X
Bit 10	R	TIUV[11]	X
Bit 9	R	TIUV[10]	X
Bit 8	R	TIUV[9]	X
Bit 7	R	TIUV[8]	X
Bit 6	R	TIUV[7]	X
Bit 5	R	TIUV[6]	X
Bit 4	R	TIUV[5]	X
Bit 3	R	TIUV[4]	X
Bit 2	R	TIUV[3]	X
Bit 1	R	TIUV[2]	X
Bit 0	R	TIUV[1]	X

TIUV[12:1]

The trace identifier unstable status (TIUV[12:1]) bits indicate the current status of the TIU-P defect for STS-1/STM-0 paths #1 to #12. The TIU-P defect is dependent on the trail trace algorithm used. The ALGO[1:0] bits in indirect address 00h selects the algorithm.

Algorithm 1: TIUV is set to logic 0.

Algorithm 2: TIUV is set to logic 1 when one or more erroneous bytes are detected between the current message and the previous message in a total of 8 trail trace messages without any persistent message in between. TIUV is set to logic 0 when a persistent message is found. A persistent message is found when the same message is receive for 3 or 5 consecutive multi-frames.

Algorithm 3: TIUV is set to logic 1 when one or more erroneous bytes are detected in three consecutive sixteen byte windows. The first window starts on the first erroneous trail trace byte. TIUV is set to logic 0 when the same trail trace byte is received for 48 consecutive frames.

Register 0x19BB: RTTP Path Trace Unstable Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	TIUE[12]	0
Bit 10	R/W	TIUE[11]	0
Bit 9	R/W	TIUE[10]	0
Bit 8	R/W	TIUE[9]	0
Bit 7	R/W	TIUE[8]	0
Bit 6	R/W	TIUE[7]	0
Bit 5	R/W	TIUE[6]	0
Bit 4	R/W	TIUE[5]	0
Bit 3	R/W	TIUE[4]	0
Bit 2	R/W	TIUE[3]	0
Bit 1	R/W	TIUE[2]	0
Bit 0	R/W	TIUE[1]	0

TIUE[12:1]

The trace identifier unstable interrupt enable (TIUE[12:1]) bits control the activation of INTB for STS-1/STM-0 paths #1 to #12. When any of these bit locations is set to logic 1, the corresponding pending interrupt will deassert INTB. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not deassert INTB.

Register 0x19BC: RTTP Path Trace Unstable Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	TIUI[12]	X
Bit 10	R	TIUI[11]	X
Bit 9	R	TIUI[10]	X
Bit 8	R	TIUI[9]	X
Bit 7	R	TIUI[8]	X
Bit 6	R	TIUI[7]	X
Bit 5	R	TIUI[6]	X
Bit 4	R	TIUI[5]	X
Bit 3	R	TIUI[4]	X
Bit 2	R	TIUI[3]	X
Bit 1	R	TIUI[2]	X
Bit 0	R	TIUI[1]	X

TIUI[12:1]

The trace identifier unstable interrupt status (TIUI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. TIUI[x] is set to logic 1 to indicate any changes in the status of TIUV[x] (stable to unstable, unstable to stable). These interrupt status bits are independent of the interrupt enable bits. When WCIMODE is low (read mode), TIUI[x] is cleared by reading the interrupt status register. When WCIMODE is high (write mode), TIUI[x] is cleared by writing a high value to bit x of the interrupt status register.

Register 0x19BD: RTTP Path Trace Mismatch Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	TIMV[12]	X
Bit 10	R	TIMV[11]	X
Bit 9	R	TIMV[10]	X
Bit 8	R	TIMV[9]	X
Bit 7	R	TIMV[8]	X
Bit 6	R	TIMV[7]	X
Bit 5	R	TIMV[6]	X
Bit 4	R	TIMV[5]	X
Bit 3	R	TIMV[4]	X
Bit 2	R	TIMV[3]	X
Bit 1	R	TIMV[2]	X
Bit 0	R	TIMV[1]	X

TIMV[12:1]

The trace identifier mismatch status (TIMV[12:1]) bit indicate the current status of the TIM-P defect for STS-1/STM-0 paths #1 to #12. The TIM-P defect is dependent on the trail trace algorithm used. The ALGO[1:0] bits in indirect address 00h selects the algorithm.

Algorithm 1: TIMV is set to logic 1 when none of the last 20 messages matches the expected message. TIMV is set to logic 0 when 16 of the last 20 messages match the expected message.

Algorithm 2: TIMV is set to logic 1 when the accepted message does not match the expected message. TIMV is set to logic 0 when the accepted message matches the expected message.

Algorithm 3: TIMV is set to logic 0.

Register 0x19BE: RTTP Path Trace Mismatch Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	TIME[12]	0
Bit 10	R/W	TIME[11]	0
Bit 9	R/W	TIME[10]	0
Bit 8	R/W	TIME[9]	0
Bit 7	R/W	TIME[8]	0
Bit 6	R/W	TIME[7]	0
Bit 5	R/W	TIME[6]	0
Bit 4	R/W	TIME[5]	0
Bit 3	R/W	TIME[4]	0
Bit 2	R/W	TIME[3]	0
Bit 1	R/W	TIME[2]	0
Bit 0	R/W	TIME[1]	0

TIME[12:1]

The trace identifier mismatch interrupt enable (TIME[12:1]) bits control the activation of INTB for STS-1/STM-0 paths #1 to #12. When any of these bit locations is set to logic 1, the corresponding pending interrupt will deassert INTB. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not deassert INTB.

Register 0x19BF: RTTP Path Trace Mismatch Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	TIMI[12]	X
Bit 10	R	TIMI[11]	X
Bit 9	R	TIMI[10]	X
Bit 8	R	TIMI[9]	X
Bit 7	R	TIMI[8]	X
Bit 6	R	TIMI[7]	X
Bit 5	R	TIMI[6]	X
Bit 4	R	TIMI[5]	X
Bit 3	R	TIMI[4]	X
Bit 2	R	TIMI[3]	X
Bit 1	R	TIMI[2]	X
Bit 0	R	TIMI[1]	X

TIMI[12:1]

The trace identifier mismatch interrupt status (TIMI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. TIMI[x] is set to logic 1 to indicate any changes in the status of TIMV[x] (match to mismatch, mismatch to match). These interrupt status bits are independent of the interrupt enable bits. When WCIMODE is low (read mode), TIMI[x] is cleared by reading the interrupt status register. When WCIMODE is high (write mode), TIMI[x] is cleared by writing a high value to bit x of the interrupt status register.

Register 0x19C0: RTTP TU3 Tributary Path Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	R/W	IADDR[7]	0
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The STS-1/STM-0 tributary path (PATH[3:0]) bits select which STS-1/STM-0 tributary path is accessed by the current indirect transfer. When the RTTP monitors tributary path trace messages, paths #1 to #12 are valid.

PATH[3:0]	STS-1/STM-0 Tributary Path #
0000	Invalid
0001-1100	Tributary Path #1 to #12
1101-1111	Invalid

IADDR[7:0]

The indirect address location (IADDR[7:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[7:0]	Indirect Data
0000 0000	Configuration
0000 0001 to 0011 1111	Invalid address
0100 0000	First byte of the 1/16/64 byte captured trace

Indirect Address IADDR[7:0]	Indirect Data
0100 0001 to 0111 1111	Remaining bytes of the 16/64 byte captured trace
1000 0000	First byte of the 1/16/64 byte accepted trace
1000 0001 to 1011 1111	Remaining bytes of the 16/64 byte accepted trace
1100 0000	First byte of the 16/64 byte expected trace
1100 0001 to 1111 1111	Remaining bytes of the 16/64 byte expected trace

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

The maximum busy bit set time is 22 ICLK cycles.

Register 0x19C1: RTTP TU3 Tributary Path Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Indirect Register 0x00: RTTP TU3 Tributary Path Trace Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	SYNCCRLF	0
Bit 5	R/W	ZEROEN	0
Bit 4	R/W	PER5	0
Bit 3	R/W	NOSYNC	0
Bit 2	R/W	LENGTH16	0
Bit 1	R/W	ALGO[1]	0
Bit 0	R/W	ALGO[0]	0

ALGO[1:0]

The trail trace algorithm select (ALGO[1:0]) bits select the algorithm used to process the trail trace message.

ALGO[1:0]	Trail Trace Algorithm
00	Algorithm disable
01	Algorithm 1
10	Algorithm 2
11	Algorithm 3

When the trail trace algorithm is disabled the corresponding TIUV, TIMV status register bits and the corresponding TIU-V, TIM-V defects are suppressed.

LENGTH16

The message length (LENGTH16) bit selects the length of the trail trace message used by algorithm 1 and algorithm 2. When LENGTH16 is set to logic 1, the length of the trail trace message is 16 bytes. When LENGTH16 is set to logic 0, the length of the trail trace message is 64 bytes.

NOSYNC

The synchronization disable (NOSYNC) bit disables the synchronization of the trail trace message in algorithm 1 and algorithm 2. When NOSYNC is set to logic 1, no synchronization is done on the trail trace message. The bytes of the trail trace message are written in the captured page as in a circular buffer. When NOSYNC is set to logic 0, synchronization is done on the trail trace message. Refer to SYNC_CRLF to determine how synchronization is handled when NOSYNC is set to logic 0.

PER5

The message persistency (PER5) bit selects the number of multi-frames a trail trace message must receive in order to be declared persistent in algorithm 2. When PER5 is set to logic 1, the same trail trace message must be received for 5 consecutive multi-frames to be declared persistent. When PER5 is set to logic 0, the same trail trace message must be received for 3 consecutive multi-frames to be declared persistent.

ZEROEN

The all-zero message enable (ZEROEN) bit selects if the all-zero messages are validated or not against the expected message in algorithm 1 and algorithm 2. When ZEROEN is set to logic 1, an all-zero captured message in algorithm 1 and an all-zero accepted message in algorithm 2 are validated against the expected message. A match is declared when both the captured/accepted message and the expected message are all-zero. When ZEROEN is set to logic 0, an all-zero captured message in algorithm 1 and an all-zero accepted message in algorithm 2 are not validated against the expected message but are considered match. A match is declared when the captured/accepted message is all-zero regardless of the expected message.

SYNCCRLF

The synchronization on CR/LF characters (SYNCCRLF) bit selects if the current algorithm (except algo3) synchronizes on the CR/LF ASCII characters or on the byte with its MSB set high. When SYNCCRLF is set to logic 1, the current algorithm synchronizes when it receives the ASCII character "CR" (carriage return) followed by "LF" (line feed) and the current active byte becomes the last byte of the message. When SYNCCRLF is set to 0, the current algorithm synchronizes when receiving a byte with its MSB set to logic 1. The current active byte then becomes the first byte of the message.

Indirect Register 0x40 to 0x7F: RTTP TU3 Tributary Path Trace Captured

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	CTRACE[7]	X
Bit 6	R	CTRACE[6]	X
Bit 5	R	CTRACE[5]	X
Bit 4	R	CTRACE[4]	X
Bit 3	R	CTRACE[3]	X
Bit 2	R	CTRACE[2]	X
Bit 1	R	CTRACE[1]	X
Bit 0	R	CTRACE[0]	X

CTRACE[7:0]

The captured trail trace message (CTRACE[7:0]) bits contain the currently received trail trace message.

When algorithm 1 or 2 is selected and LENGTH16 is set to logic 1, the captured message is stored between indirect address 40h and 4Fh. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 0, the captured message is stored between indirect address 40h and 7Fh. When NOSYNC is set to logic 1, the captured message is not synchronized. When NOSYNC is set to logic 0, the captured message is synchronized and the first byte of the message is stored at indirect address 40h.

When algorithm 3 is selected, the captured byte is stored at indirect address 40h.

Indirect Register 0x80 to 0xBF: RTTP TU3 Tributary Path Trace Accepted

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	ATRACE[7]	X
Bit 6	R/W	ATRACE[6]	X
Bit 5	R/W	ATRACE[5]	X
Bit 4	R/W	ATRACE[4]	X
Bit 3	R/W	ATRACE[3]	X
Bit 2	R/W	ATRACE[2]	X
Bit 1	R/W	ATRACE[1]	X
Bit 0	R/W	ATRACE[0]	X

ATRACE[7:0]

The accepted trail trace message (ATRACE[7:0]) bits contain the persistent trail trace message.

When algorithm 1 is selected, the accepted message will not be updated.

When algorithm 2 is selected and PER5 is set to logic 1, the accepted message is the same trail trace message received for 5 consecutive multi-frames. When algorithm 2 is selected and PER5 is set to logic 0, the accepted message is the same trail trace message received for 3 consecutive multi-frames. When algorithm 2 is selected and LENGTH16 is set to logic 1, the accepted message is stored between indirect address 80h and 8Fh. When algorithm 2 is selected and LENGTH16 is set to logic 0, the accepted message is stored between indirect address 80h and BFh.

When algorithm 3 is selected, the accepted byte is the same trail trace byte received for 48 frames. When algorithm 3 is selected, the accepted byte is stored at indirect address 80h.

Indirect Register 0xC0 to 0xFF: RTTP TU3 Tributary Path Trace Expected

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	ETRACE[7]	X
Bit 6	R/W	ETRACE[6]	X
Bit 5	R/W	ETRACE[5]	X
Bit 4	R/W	ETRACE[4]	X
Bit 3	R/W	ETRACE[3]	X
Bit 2	R/W	ETRACE[2]	X
Bit 1	R/W	ETRACE[1]	X
Bit 0	R/W	ETRACE[0]	X

ETRACE[7:0]

The expected trail trace message (ETRACE[7:0]) bits contain a static message written by an external microprocessor.

In algorithm 1 the expected message is used to validated the captured message.

In algorithm 2 the expected message is used to validate the accepted message. When LENGTH16 is set to logic 1, the expected message must be written between indirect address C0h and CFh. When LENGTH16 is set to logic 0, the accepted message must be written between indirect address C0h and FFh.

Register 0x19C2: RTTP TU3 Tributary Path Trace Unstable Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	TIUV[12]	X
Bit 10	R	TIUV[11]	X
Bit 9	R	TIUV[10]	X
Bit 8	R	TIUV[9]	X
Bit 7	R	TIUV[8]	X
Bit 6	R	TIUV[7]	X
Bit 5	R	TIUV[6]	X
Bit 4	R	TIUV[5]	X
Bit 3	R	TIUV[4]	X
Bit 2	R	TIUV[3]	X
Bit 1	R	TIUV[2]	X
Bit 0	R	TIUV[1]	X

TIUV[12:1]

The trace identifier unstable status (TIUV[12:1]) bits indicate the current status of the TIU-V defect for STS-1/STM-0 tributary paths #1 to #12. The TIU-V defect is dependent on the trail trace algorithm used. The ALGO[1:0] bits in indirect address 00h selects the algorithm.

Algorithm 1: TIUV is set to logic 0.

Algorithm 2: TIUV is set to logic 1 when one or more erroneous bytes are detected between the current message and the previous message in a total of 8 trail trace messages without any persistent message in between. TIUV is set to logic 0 when a persistent message is found. A persistent message is found when the same message is receive for 3 or 5 consecutive multi-frames.

Algorithm 3: TIUV is set to logic 1 when one or more erroneous bytes are detected in three consecutive sixteen byte windows. The first window starts on the first erroneous trail trace byte. TIUV is set to logic 0 when the same trail trace byte is received for 48 consecutive frames.

Register 0x19C3: RTTP TU3 Tributary Path Trace Unstable Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	TIUE[12]	0
Bit 10	R/W	TIUE[11]	0
Bit 9	R/W	TIUE[10]	0
Bit 8	R/W	TIUE[9]	0
Bit 7	R/W	TIUE[8]	0
Bit 6	R/W	TIUE[7]	0
Bit 5	R/W	TIUE[6]	0
Bit 4	R/W	TIUE[5]	0
Bit 3	R/W	TIUE[4]	0
Bit 2	R/W	TIUE[3]	0
Bit 1	R/W	TIUE[2]	0
Bit 0	R/W	TIUE[1]	0

TIUE[12:1]

The trace identifier unstable interrupt enable (TIUE[12:1]) bits control the activation of INTB for STS-1/STM-0 tributary paths #1 to #12. When any of these bit locations is set to logic 1, the corresponding pending interrupt will deassert INTB. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not deassert INTB.

Register 0x19C4: RTTP TU3 Tributary Path Trace Unstable Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	TIUI[12]	X
Bit 10	R	TIUI[11]	X
Bit 9	R	TIUI[10]	X
Bit 8	R	TIUI[9]	X
Bit 7	R	TIUI[8]	X
Bit 6	R	TIUI[7]	X
Bit 5	R	TIUI[6]	X
Bit 4	R	TIUI[5]	X
Bit 3	R	TIUI[4]	X
Bit 2	R	TIUI[3]	X
Bit 1	R	TIUI[2]	X
Bit 0	R	TIUI[1]	X

TIUI[12:1]

The trace identifier unstable interrupt status (TIUI[12:1]) bits are event indicators for STS-1/STM-0 tributary paths #1 to #12. TIUI[x] is set to logic 1 to indicate any changes in the status of TIUV[x] (stable to unstable, unstable to stable). These interrupt status bits are independent of the interrupt enable bits. When WCIMODE is low (read mode), TIUI[x] is cleared by reading the interrupt status register. When WCIMODE is high (write mode), TIUI[x] is cleared by writing a high value to bit x of the interrupt status register.

Register 0x19C5: RTTP TU3 Tributary Path Trace Mismatch Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	TIMV[12]	X
Bit 10	R	TIMV[11]	X
Bit 9	R	TIMV[10]	X
Bit 8	R	TIMV[9]	X
Bit 7	R	TIMV[8]	X
Bit 6	R	TIMV[7]	X
Bit 5	R	TIMV[6]	X
Bit 4	R	TIMV[5]	X
Bit 3	R	TIMV[4]	X
Bit 2	R	TIMV[3]	X
Bit 1	R	TIMV[2]	X
Bit 0	R	TIMV[1]	X

TIMV[12:1]

The trace identifier mismatch status (TIMV[12:1]) bit indicate the current status of the TIM-V defect for STS-1/STM-0 tributary paths #1 to #12. The TIM-V defect is dependent on the trail trace algorithm used. The ALGO[1:0] bits in indirect address 00h selects the algorithm.

Algorithm 1: TIMV is set to logic 1 when none of the last 20 messages matches the expected message. TIMV is set to logic 0 when 16 of the last 20 messages match the expected message.

Algorithm 2: TIMV is set to logic 1 when the accepted message does not match the expected message. TIMV is set to logic 0 when the accepted message matches the expected message.

Algorithm 3: TIMV is set to logic 0.

Register 0x19C6: RTTP TU3 Tributary Path Trace Mismatch Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	TIME[12]	0
Bit 10	R/W	TIME[11]	0
Bit 9	R/W	TIME[10]	0
Bit 8	R/W	TIME[9]	0
Bit 7	R/W	TIME[8]	0
Bit 6	R/W	TIME[7]	0
Bit 5	R/W	TIME[6]	0
Bit 4	R/W	TIME[5]	0
Bit 3	R/W	TIME[4]	0
Bit 2	R/W	TIME[3]	0
Bit 1	R/W	TIME[2]	0
Bit 0	R/W	TIME[1]	0

TIME[12:1]

The trace identifier mismatch interrupt enable (TIME[12:1]) bits control the activation of INTB for STS-1/STM-0 tributary paths #1 to #12. When any of these bit locations is set to logic 1, the corresponding pending interrupt will deassert INTB. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not deassert INTB.

Register 0x19C7: RTTP TU3 Tributary Path Trace Mismatch Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	TIMI[12]	X
Bit 10	R	TIMI[11]	X
Bit 9	R	TIMI[10]	X
Bit 8	R	TIMI[9]	X
Bit 7	R	TIMI[8]	X
Bit 6	R	TIMI[7]	X
Bit 5	R	TIMI[6]	X
Bit 4	R	TIMI[5]	X
Bit 3	R	TIMI[4]	X
Bit 2	R	TIMI[3]	X
Bit 1	R	TIMI[2]	X
Bit 0	R	TIMI[1]	X

TIMI[12:1]

The trace identifier mismatch interrupt status (TIMI[12:1]) bits are event indicators for STS-1/STM-0 tributary paths #1 to #12. TIMI[x] is set to logic 1 to indicate any changes in the status of TIMV[x] (match to mismatch, mismatch to match). These interrupt status bits are independent of the interrupt enable bits. When WCIMODE is low (read mode), TIMI[x] is cleared by reading the interrupt status register. When WCIMODE is high (write mode), TIMI[x] is cleared by writing a high value to bit x of the interrupt status registers.

Register 0x19D0: TTTP Path Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	—	Unused	X
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer. When the TTTP generates path trace messages, paths #1 to #12 are valid.

PATH[3:0]	STS-1/STM-0 Path #
0000	Invalid
0001-1100	Path #1 to #12
1101-1111	Invalid

IADDR[6:0]

The indirect address location (IADDR[6:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[6:0]	Indirect Data
000 0000	Configuration
000 0001 to 011 1111	Invalid address
100 0000	First byte of the 1/16/64 byte trace
100 0001 to 111 1111	Remaining bytes of the 16/64 byte trace

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

The maximum busy bit set time is 22 OCLK cycles.

Register 0x19D1: TTTP Path Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Indirect Register 0x00: TTTP Path Trace Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	ZEROEN	0
Bit 1	R/W	BYTEEN	0
Bit 0	R/W	LENGTH16	0

LENGTH16

The message length (LENGTH16) bit selects the length of the trail trace message to be transmitted. When LENGTH16 is set to logic 1, the length of the trail trace message is 16 bytes. When LENGTH16 is set to logic 0, the length of the trail trace message is 64 bytes.

BYTEEN

The single byte message enable (BYTEEN) bit enables the single byte trail trace message. When BYTEEN is set to logic 1, the length of the trail trace message is 1 byte. When BYTEEN is set to logic 0, the length of the trail trace message is determined by LENGTH16. BYTEEN has precedence over LENGTH16.

ZEROEN

The all-zero message enable (ZEROEN) bit enables the transmission of an all-zero trail trace message. When ZEROEN is set to logic 1, an all-zero message is transmitted. When ZEROEN is set to logic 0, the RAM message is transmitted. The enabling and disabling of the all-zero trail trace message is not done on message boundary since the receiver is required to perform filtering on the message.

Indirect Register 0x40 to 0x7F: TTTP Path Trace

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	TRACE[7]	X
Bit 6	R/W	TRACE[6]	X
Bit 5	R/W	TRACE[5]	X
Bit 4	R/W	TRACE[4]	X
Bit 3	R/W	TRACE[3]	X
Bit 2	R/W	TRACE[2]	X
Bit 1	R/W	TRACE[1]	X
Bit 0	R/W	TRACE[0]	X

TRACE[7:0]

The trail trace message (TRACE[7:0]) bits contain the trail trace message to be transmitted. When BYTEEN is set to logic 1, the message is stored at indirect address 40h. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 1, the message is stored between indirect address 40h and 4Fh. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 0, the message is stored between indirect address 40h and 7Fh.

Register 0x19D8: TTTP TU3 Tributary Path Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	—	Unused	X
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The STS-1/STM-0 tributary path (PATH[3:0]) bits select which STS-1/STM-0 tributary path is accessed by the current indirect transfer. When the TTTP generates tributary path trace messages, tributary paths #1 to #12 are valid.

PATH[3:0]	STS-1/STM-0 tributary Path #
0000	Invalid tributary path
0001-1100	Path #1 to Path #12
1101-1111	Invalid tributary path

IADDR[6:0]

The indirect address location (IADDR[6:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[6:0]	Indirect Data
000 0000	Configuration
000 0001 to 011 1111	Invalid address
100 0000	First byte of the 1/16/64 byte trace
100 0001 to 111 1111	Remaining bytes of the 16/64 byte trace

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

The maximum busy bit set time is 22 OCLK cycles.

Register 0x19D9: TTTP TU3 Tributary Path Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Indirect Register 0x00: TTTP TU3 Tributary Path Trace Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	ZEROEN	0
Bit 1	R/W	BYTEEN	0
Bit 0	R/W	LENGTH16	0

LENGTH16

The message length (LENGTH16) bit selects the length of the trail trace message to be transmitted. When LENGTH16 is set to logic 1, the length of the trail trace message is 16 bytes. When LENGTH16 is set to logic 0, the length of the trail trace message is 64 bytes.

BYTEEN

The single byte message enable (BYTEEN) bit enables the single byte trail trace message. When BYTEEN is set to logic 1, the length of the trail trace message is 1 byte. When BYTEEN is set to logic 0, the length of the trail trace message is determined by LENGTH16. BYTEEN has precedence over LENGTH16.

ZEROEN

The all-zero message enable (ZEROEN) bit enables the transmission of an all-zero trail trace message. When ZEROEN is set to logic 1, an all-zero message is transmitted. When ZEROEN is set to logic 0, the RAM message is transmitted. The enabling and disabling of the all-zero trail trace message is not done on message boundary since the receiver is required to perform filtering on the message.

Indirect Register 0x40 to 0x7F: TTTP TU3 Tributary Path Trace

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	TRACE[7]	X
Bit 6	R/W	TRACE[6]	X
Bit 5	R/W	TRACE[5]	X
Bit 4	R/W	TRACE[4]	X
Bit 3	R/W	TRACE[3]	X
Bit 2	R/W	TRACE[2]	X
Bit 1	R/W	TRACE[1]	X
Bit 0	R/W	TRACE[0]	X

TRACE[7:0]

The trail trace message (TRACE[7:0]) bits contain the trail trace message to be transmitted. When BYTEEN is set to logic 1, the message is stored at indirect address 40h. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 1, the message is stored between indirect address 40h and 4Fh. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 0, the message is stored between indirect address 40h and 7Fh.

Register 0x19E0: PRGM Line Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RDWRB	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The STS-1/STM-0 path PATH[3:0] bits select which STS-1/STM-0 path is accessed by the current indirect transfer.

PATH[3:0]	STS-1/STM-0 Path #
0000	Invalid
0001-1100	Path #1 to #12
1101-1111	Invalid

IADDR[3:0]

The indirect address select which indirect register is access by the current indirect transfer. Six indirect registers are defined for the monitor (IADDR[3] = '0') : the configuration, the PRBS[22:7], the PRBS[6:0], the B1/E1 value, the Monitor error count and the received B1/E1 byte.

IADDR[3:0]	RAM Page
0000	STS-1/STM-0 Path Configuration
0001	PRBS[22:7]
0010	PRBS[6:0]
0011	B1/E1 Value
0100	Monitor Error Count
0101	Received B1 and E1

Four indirect registers are defined for the generator (IADDR [3] = '1') : the configuration, the PRBS[22:7], the PRBS[6:0] and the B1/E1 value.

IADDR[3:0]	RAM Page
1000	STS-1/STM-0 Path Configuration
1001	PRBS[22:7]
1010	PRBS[6:0]
1011	B1/E1 value

RDWRB

The active high read and active low write (RDWRB) bit selects if the current access to the indirect register is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the indirect register. When RDWRB is set to logic 1, an indirect read access to the indirect register is initiated. The data from the addressed location will be transfer to the Indirect Data Register. When RDWRB is set to logic 0, an indirect write access to the indirect register is initiated. The data from the Indirect Data Register will be transfer to the addressed location.

BUSY

The active high busy (BUSY) bit reports if a previously initiated indirect access has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the access. This register should be polled to determine when new data is available in the Indirect Data Register.

The maximum busy bit set time is 22 OCLK cycles.

Register 0x19E1: PRGM Line Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from during indirect access. When RDWRB is set to logic 1 (indirect read), the data from the addressed location will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RDWRB is set to logic 0 (indirect write), the data from DATA[15:0] will be transfer to the addressed location. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which indirect register is being accessed.

Indirect Register 0x00: PRGM Line Monitor STS-1/STM-0 Path Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	SEQ_PRBSB	0
Bit 5	R/W	B1E1_ENA	0
Bit 4	—	Unused	X
Bit 3	W	RESYNC	0
Bit 2	R/W	INV_PRBS	0
Bit 1	—	Unused	X
Bit 0	R/W	MON_ENA	0

MON_ENA

The monitor enable (MON_ENA) bit enables the PRBS monitor. When MON_ENA is set to logic 1, a PRBS sequence is generated and compared to the incoming PRBS sequence contained in the payload of the SONET/SDH frame. When MON_ENA is logic 0, the incoming PRBS sequence is ignored.

INV_PRBS

The invert PRBS (INV_PRBS) bit configures the monitor to invert the incoming PRBS sequence. When INV_PRBS is a logic 1, the incoming PRBS sequence is inverted before comparing it to the internally generated PRBS sequence. When INV_PRBS is a logic 0, the incoming PRBS sequence is not inverted prior to comparing to the internally generated PRBS sequence.

RESYNC

The resync (RESYNC) bit configures the monitor to re-initialize the PRBS sequence. When RESYNC is a logic 1, the monitor's state machine will be forced in the Out Of Sync state and automatically try to resynchronize to the incoming stream.

B1E1_ENA

The B1E1 enable (B1E1_ENA) bit enables the monitoring of the B1 and E1 bytes in the SONET/SDH frame. When B1E1_ENA is a logic 1, the monitoring of the B1 and E1 bytes in the SONET/SDH frame is enabled. When B1E1_ENA is a logic 0, the monitoring of B1 and E1 bytes in the SONET/SDH frame is disabled.

The monitoring of the incoming B1 and E1 bytes when enabled is performed by comparing the B1 byte to a programmable register B1[7:0], and the E1 byte to the complement of the same value.

SEQ_PRBSB

The sequential or PRBS enable (SEQ_PRBSB) bit selects between the monitoring of a sequential pattern or a $X^{23}+X^{18}+1$ PRBS sequence. When SEQ_PRBSB is a logic 1, the monitor compares for a sequential pattern contained within the payload. When SEQ_PRBSB is a logic 0, the monitor compares for a PRBS sequence within the payload.

Indirect Register 0x01: PRGM Line Monitor PRBS[22:7] Accumulator

Bit	Type	Function	Default
Bit 15	R/W	PRBS[22]	0
Bit 14	R/W	PRBS[21]	0
Bit 13	R/W	PRBS[20]	0
Bit 12	R/W	PRBS[19]	0
Bit 11	R/W	PRBS[18]	0
Bit 10	R/W	PRBS[17]	0
Bit 9	R/W	PRBS[16]	0
Bit 8	R/W	PRBS[15]	0
Bit 7	R/W	PRBS[14]	0
Bit 6	R/W	PRBS[13]	0
Bit 5	R/W	PRBS[12]	0
Bit 4	R/W	PRBS[11]	0
Bit 3	R/W	PRBS[10]	0
Bit 2	R/W	PRBS[9]	0
Bit 1	R/W	PRBS[8]	0
Bit 0	R/W	PRBS[7]	0

PRBS[22:7]

The PRBS[22:7] register, are the 16 MSBs of the LFSR (linear feedback shift register) state of the STS-1/STM-0 path used to monitor the $X^{23}+X^{18}+1$ PRBS sequence. This register is used to change the initial state of the PRBS sequence.

Indirect Register 0x02: PRGM Line Monitor PRBS[6:0] Accumulator

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	PRBS[6]	0
Bit 5	R/W	PRBS[5]	0
Bit 4	R/W	PRBS[4]	0
Bit 3	R/W	PRBS[3]	0
Bit 2	R/W	PRBS[2]	0
Bit 1	R/W	PRBS[1]	0
Bit 0	R/W	PRBS[0]	0

PRBS[6:0]

The PRBS[6:0] register, are the 7 LSBs of the LFSR state of the STS-1/STM-0 path used to generate the $X^{23}+X^{18}+1$ PRBS sequence. This register is used to change the initial state of the PRBS sequence.

Indirect Register 0x03: PRGM Line Monitor B1/E1 value

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	B1[7]	0
Bit 6	R/W	B1[6]	0
Bit 5	R/W	B1[5]	0
Bit 4	R/W	B1[4]	0
Bit 3	R/W	B1[3]	0
Bit 2	R/W	B1[2]	0
Bit 1	R/W	B1[1]	0
Bit 0	R/W	B1[0]	0

B1[7:0]

The B1[7:0] register is used to compare against the B1/E1 bytes when B1E1_ENA (indirect address 0x00) is set to logic 1. The B1[7:0] register is directly used to compare against the B1 byte, and the compliment of the B1[7:0] register is used to compare against the E1 byte.

Indirect Register 0x04: PRGM Line Monitor Error count

Bit	Type	Function	Default
Bit 15	R	ERR_CNT[15]	X
Bit 14	R	ERR_CNT[14]	X
Bit 13	R	ERR_CNT[13]	X
Bit 12	R	ERR_CNT[12]	X
Bit 11	R	ERR_CNT[11]	X
Bit 10	R	ERR_CNT[10]	X
Bit 9	R	ERR_CNT[9]	X
Bit 8	R	ERR_CNT[8]	X
Bit 7	R	ERR_CNT[7]	X
Bit 6	R	ERR_CNT[6]	X
Bit 5	R	ERR_CNT[5]	X
Bit 4	R	ERR_CNT[4]	X
Bit 3	R	ERR_CNT[3]	X
Bit 2	R	ERR_CNT[2]	X
Bit 1	R	ERR_CNT[1]	X
Bit 0	R	ERR_CNT[0]	X

ERR_CNT[15:0]

The ERR_CNT[15:0] register, is the number of errors in the PRBS bytes detected during the last accumulation interval. Errors are accumulated only when the monitor is in the synchronized state. Even if there is multiple errors within one PRBS byte, only one error is counted. The error counter will not wrap around after reaching FFFFh, it will saturate at this value.

Any write to the PRGM Line Monitor Error Count Register (indirect address 0x04) or to the Master Reset and Identity Register (address 0x1800) will trigger the transfer of all counter values to their holding registers.

When losing synchronization the PRBS monitor may incorrectly count up to two additional byte errors.

Indirect Register 0x05: PRGM Line Monitor Received B1/E1 bytes

Bit	Type	Function	Default
Bit 15	R	REC_E1[7]	X
Bit 14	R	REC_E1[6]	X
Bit 13	R	REC_E1[5]	X
Bit 12	R	REC_E1[4]	X
Bit 11	R	REC_E1[3]	X
Bit 10	R	REC_E1[2]	X
Bit 9	R	REC_E1[1]	X
Bit 8	R	REC_E1[0]	X
Bit 7	R	REC_B1[7]	X
Bit 6	R	REC_B1[6]	X
Bit 5	R	REC_B1[5]	X
Bit 4	R	REC_B1[4]	X
Bit 3	R	REC_B1[3]	X
Bit 2	R	REC_B1[2]	X
Bit 1	R	REC_B1[1]	X
Bit 0	R	REC_B1[0]	X

REC_B1[7:0]

The Received B1 byte is the content of the B1 byte position in the SONET/SDH frame for this particular STS-1/STM-0 path. Every time a B1 byte is received, it is copied in this register.

REC_E1[7:0]

The Received E1 byte is the content of the E1 byte position in the SONET/SDH frame for this particular STS-1/STM-0 path. Every time a E1 byte is received, it is copied in this register.

Indirect Register 0x08: PRGM Line Generator STS-1/STM-0 Path Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R/W	GEN_ENA	0
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	SEQ_PRBSB	0
Bit 4	R/W	B1E1_ENA	0
Bit 3	W	FORCE_ERR	0
Bit 2	—	Unused	X
Bit 1	R/W	INV_PRBS	0
Bit 0	—	Unused	X

INV_PRBS

The invert PRBS (INV_PRBS) bit configures the generator to invert the PRBS sequence before insertion into the payload. When INV_PRBS is a logic 1, the PRBS sequence is inverted prior to insertion. When INV_PRBS is a logic 0, the PRBS sequence is not inverted prior to insertion.

FORCE_ERR

The Force Error (FORCE_ERR) bit is used for diagnostic purposes to force bit errors in the inserted pattern. When FORCE_ERR is a logic 1, the MSB of the next byte will be inverted and the register will clear itself when the operation is complete, thus inducing a single bit error. When FORCE_ERR is a logic 0, the PRBS sequence is inserted error free.

B1E1_ENA

This bit enables the replacement of the B1 bytes in the SONET/SDH frame, by inserting the B1[7:0] register value. The E1 byte is replaced by the inserting the complement of the B1[7:0] register value. When B1E1_ENA is set high, the B1/E1 bytes are inserted from the B1[7:0] register. When B1E1_ENA is logic 0, the monitoring of B1 and E1 bytes in the SONET/SDH frame is disabled.

The monitoring of the incoming B1 and E1 bytes when enabled is performed by comparing the B1 byte to a programmable register B1[7:0], and the E1 byte to the complement of the same value.

SEQ_PRBSB

The sequential or PRBS enable (SEQ_PRBSB) bit selects between the generation of a sequential pattern or a $X^{23}+X^{18}+1$ PRBS sequence. When SEQ_PRBSB is a logic 1, the generator inserts a sequential pattern contained within the payload. When SEQ_PRBSB is a logic 0, the generator inserts a PRBS sequence within the payload.

GEN_ENA

The generator enable (GEN_ENA) bit enables the insertion of sequential or PRBS data patterns. When GEN_ENA is a logic 1, patterns are generated and inserted. When GEN_ENA is a logic 0, no pattern is generated and the unmodified SONET/SDH input frame is passed transparently through the PRGM Line.

Indirect Register 0x09: PRGM Line Generator PRBS[22:7] Accumulator

Bit	Type	Function	Default
Bit 15	R/W	PRBS[22]	0
Bit 14	R/W	PRBS[21]	0
Bit 13	R/W	PRBS[20]	0
Bit 12	R/W	PRBS[19]	0
Bit 11	R/W	PRBS[18]	0
Bit 10	R/W	PRBS[17]	0
Bit 9	R/W	PRBS[16]	0
Bit 8	R/W	PRBS[15]	0
Bit 7	R/W	PRBS[14]	0
Bit 6	R/W	PRBS[13]	0
Bit 5	R/W	PRBS[12]	0
Bit 4	R/W	PRBS[11]	0
Bit 3	R/W	PRBS[10]	0
Bit 2	R/W	PRBS[9]	0
Bit 1	R/W	PRBS[8]	0
Bit 0	R/W	PRBS[7]	0

PRBS[22:7]

The PRBS[22:7] register, are the 16 MSBs of the LFSR state of the STS-1/STM-0 path used to generate the $X^{23}+X^{18}+1$ PRBS sequence. This register is used to change the initial state of the PRBS sequence.

Indirect Register 0x0A: PRGM Line Generator PRBS[6:0] Accumulator

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R/W	PRBS[6]	0
Bit 5	R/W	PRBS[5]	0
Bit 4	R/W	PRBS[4]	0
Bit 3	R/W	PRBS[3]	0
Bit 2	R/W	PRBS[2]	0
Bit 1	R/W	PRBS[1]	0
Bit 0	R/W	PRBS[0]	0

PRBS[6:0]

The PRBS[6:0] register, are the 7 LSBs of the LFSR state of the STS-1/STM-0 path used to generate the $X^{23}+X^{18}+1$ PRBS sequence. This register is used to change the initial state of the PRBS sequence.

Indirect Register 0x0B: PRGM Line Generator B1/E1 value

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	B1[7]	0
Bit 6	R/W	B1[6]	0
Bit 5	R/W	B1[5]	0
Bit 4	R/W	B1[4]	0
Bit 3	R/W	B1[3]	0
Bit 2	R/W	B1[2]	0
Bit 1	R/W	B1[1]	0
Bit 0	R/W	B1[0]	0

B1[7:0]

The B1[7:0] register is used to overwrite the B1/E1 bytes when B1E1_ENA (indirect address 0x08) is set to logic 1. The B1[7:0] register is directly used to overwrite the B1 byte, and the compliment of the B1[7:0] register is used to overwrite the E1 byte.

Register 0x19E2: PRGM Line Generator Payload Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	R/W	GEN_STS12C	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	GEN_STS3C[4]	0
Bit 2	R/W	GEN_STS3C[3]	0
Bit 1	R/W	GEN_STS3C[2]	0
Bit 0	R/W	GEN_STS3C[1]	0

GEN_STS3C[1]

The STS-3c (VC-4) payload configuration (GEN_STS3C[1]) bit selects the payload configuration. When GEN_STS3C[1] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a STS-3c (VC-4) payload. When GEN_STS3C[1] is set to logic 0, the paths are STS-1 (VC-3) payloads.

When GEN_STS12C is set to logic 1, GEN_STS3C[1] must be set to logic 0.

GEN_STS3C[2]

The STS-3c (VC-4) payload configuration (GEN_STS3C[2]) bit selects the payload configuration. When GEN_STS3C[2] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a STS-3c (VC-4) payload. When GEN_STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads.

When GEN_STS12C is set to logic 1, GEN_STS3C[2] must be set to logic 0.

GEN_STS3C[3]

The STS-3c (VC-4) payload configuration (GEN_STS3C[3]) bit selects the payload configuration. When GEN_STS3C[3] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a STS-3c (VC-4) payload. When GEN_STS3C[3] is set to logic 0, the paths are STS-1 (VC-3) payloads.

When GEN_STS12C is set to logic 1, GEN_STS3C[3] must be set to logic 0.

GEN_STS3C[4]

The STS-3c (VC-4) payload configuration (GEN_STS3C[4]) bit selects the payload configuration. When GEN_STS3C[4] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a STS-3c (VC-4) payload. When GEN_STS3C[4] is set to logic 0, the paths are STS-1 (VC-3) payloads.

When GEN_STS12C is set to logic 1, GEN_STS3C[4] must be set to logic 0.

GEN_STS12C

The STS-12c (VC-4-4c) payload configuration (GEN_STS12C) bit selects the payload configuration. When GEN_STS12C is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of the same concatenated payload defined by GEN_MSSLEN. When GEN_STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the GEN_STS3C[1:4] register bit.

Register 0x19E3: PRGM Line Monitor Payload Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	R/W	MON_STS12C	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	MON_STS3C[4]	0
Bit 2	R/W	MON_STS3C[3]	0
Bit 1	R/W	MON_STS3C[2]	0
Bit 0	R/W	MON_STS3C[1]	0

MON_STS3C[1]

The STS-3c (VC-4) payload configuration (MON_STS3C[1]) bit selects the payload configuration. When MON_STS3C[1] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a STS-3c (VC-4) payload. When MON_STS3C[1] is set to logic 0, the paths are STS-1 (VC-3) payloads.

When MON_STS12C is set to logic 1, MON_STS3C[1] must be set to logic 0.

MON_STS3C[2]

The STS-3c (VC-4) payload configuration (MON_STS3C[2]) bit selects the payload configuration. When MON_STS3C[2] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a STS-3c (VC-4) payload. When MON_STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads.

When MON_STS12C is set to logic 1, MON_STS3C[2] must be set to logic 0.

MON_STS3C[3]

The STS-3c (VC-4) payload configuration (MON_STS3C[3]) bit selects the payload configuration. When MON_STS3C[3] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a MON_STS-3c (VC-4) payload. When MON_STS3C[3] is set to logic 0, the paths are STS-1 (VC-3) payloads.

When MON_STS12C is set to logic 1, MON_STS3C[3] must be set to logic 0.

MON_STS3C[4]

The STS-3c (VC-4) payload configuration (MON_STS3C[4]) bit selects the payload configuration. When MON_STS3C[4] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a STS-3c (VC-4) payload. When MON_STS3C[4] is set to logic 0, the paths are STS-1 (VC-3) payloads.

When MON_STS12C is set to logic 1, MON_STS3C[4] must be set to logic 0.

MON_STS12C

The STS-12c (VC-4-4c) payload configuration (MON_STS12C) bit selects the payload configuration. When MON_STS12C is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of the same concatenated payload defined by MON_MSSLEN. When MON_STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the MON_STS3C[3:0] register bit.

Register 0x19E4: PRGM Line Monitor Byte Error Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	MON_ERRI[12]	X
Bit 10	R	MON_ERRI[11]	X
Bit 9	R	MON_ERRI[10]	X
Bit 8	R	MON_ERRI[9]	X
Bit 7	R	MON_ERRI[8]	X
Bit 6	R	MON_ERRI[7]	X
Bit 5	R	MON_ERRI[6]	X
Bit 4	R	MON_ERRI[5]	X
Bit 3	R	MON_ERRI[4]	X
Bit 2	R	MON_ERRI[3]	X
Bit 1	R	MON_ERRI[2]	X
Bit 0	R	MON_ERRI[1]	X

MON_ERRI[12:1]

The monitor byte error interrupt status (MONx_ERRI[12:1]) bits are event indicators. MON_ERRI[x] is set to logic 1 to indicate an error in a PRBS byte is detected in the corresponding STS-1/STM-0 path. These interrupt status bits are independent of the interrupt enable bits. When WCIMODE is low (read mode), MON_ERRI[12:1] is cleared by reading the interrupt status register. When WCIMODE is high (write mode), MON_ERRI[x] is cleared by writing a high value to bit x of the interrupt status register.

Register 0x19E5: PRGM Line Monitor Byte Error Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	MON_ERRE[12]	0
Bit 10	R/W	MON_ERRE[11]	0
Bit 9	R/W	MON_ERRE[10]	0
Bit 8	R/W	MON_ERRE[9]	0
Bit 7	R/W	MON_ERRE[8]	0
Bit 6	R/W	MON_ERRE[7]	0
Bit 5	R/W	MON_ERRE[6]	0
Bit 4	R/W	MON_ERRE[5]	0
Bit 3	R/W	MON_ERRE[4]	0
Bit 2	R/W	MON_ERRE[3]	0
Bit 1	R/W	MON_ERRE[2]	0
Bit 0	R/W	MON_ERRE[1]	0

MON_ERRE[12:1]

The monitor byte error interrupt enable (MON_ERRE[12:1]) bits control the activation of INTB. When MON_ERRE[x] is set to logic 1, the corresponding STS-1/STM-0 MON_ERRI[x] pending byte error interrupt will deassert INTB. When MON_ERRE[x] is set to logic 0, the MON_ERRI[x] pending byte error interrupt will not deassert INTB.

Register 0x19E6: PRGM Line Monitor B1/E1 Bytes Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	MON_B1E1I[12]	X
Bit 10	R	MON_B1E1I[11]	X
Bit 9	R	MON_B1E1I[10]	X
Bit 8	R	MON_B1E1I[9]	X
Bit 7	R	MON_B1E1I[8]	X
Bit 6	R	MON_B1E1I[7]	X
Bit 5	R	MON_B1E1I[6]	X
Bit 4	R	MON_B1E1I[5]	X
Bit 3	R	MON_B1E1I[4]	X
Bit 2	R	MON_B1E1I[3]	X
Bit 1	R	MON_B1E1I[2]	X
Bit 0	R	MON_B1E1I[1]	X

MON_B1E1I[12:1]

The monitor B1/E1 bytes interrupt status (MON_B1E1I[12:1]) bits are event indicators. MON_B1E1I[x] is set to logic 1 to indicate a change in the status of the comparison has been detected on the B1/E1 bytes for the corresponding STS-1/STM-0 path. These interrupt status bits are independent of the interrupt enable bits. When WCIMODE is low (read mode), MON_B1E1I[12:1] is cleared by reading the interrupt status register. When WCIMODE is high (write mode), MON_B1E1I[x] is cleared by writing a high value to bit x of the interrupt status register.

Register 0x19E7: PRGM Line Monitor B1/E1 Bytes Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	MON_B1E1E[12]	0
Bit 10	R/W	MON_B1E1E[11]	0
Bit 9	R/W	MON_B1E1E[10]	0
Bit 8	R/W	MON_B1E1E[9]	0
Bit 7	R/W	MON_B1E1E[8]	0
Bit 6	R/W	MON_B1E1E[7]	0
Bit 5	R/W	MON_B1E1E[6]	0
Bit 4	R/W	MON_B1E1E[5]	0
Bit 3	R/W	MON_B1E1E[4]	0
Bit 2	R/W	MON_B1E1E[3]	0
Bit 1	R/W	MON_B1E1E[2]	0
Bit 0	R/W	MON_B1E1E[1]	0

MON_B1E1E[12:1]

The monitor B1/E1 bytes interrupt enable (MON_B1E1E[12:1]) bits control the activation of INTB. When MON_B1E1E[x] is set to logic 1, the corresponding STS-1/STM-0 path MON_B1E1I[x] pending B1/E1 byte interrupt will deassert INTB. When MON_B1E1E[x] is set to logic 0, the MON_B1E1I[x] pending B1/E1 byte interrupt will not deassert INTB.

Register 0x19E9: PRGM Line Monitor Synchronization Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	MON_SYNCI[12]	X
Bit 10	R	MON_SYNCI[11]	X
Bit 9	R	MON_SYNCI[10]	X
Bit 8	R	MON_SYNCI[9]	X
Bit 7	R	MON_SYNCI[8]	X
Bit 6	R	MON_SYNCI[7]	X
Bit 5	R	MON_SYNCI[6]	X
Bit 4	R	MON_SYNCI[5]	X
Bit 3	R	MON_SYNCI[4]	X
Bit 2	R	MON_SYNCI[3]	X
Bit 1	R	MON_SYNCI[2]	X
Bit 0	R	MON_SYNCI[1]	X

MON_SYNCI[12:1]

The monitor synchronization interrupt status (MON_SYNCI[12:1]) bits are event indicators. MON_SYNCI[x] is set to logic 1 to indicate a change in the monitor's synchronization status for the corresponding STS-1/STM-0 path. These interrupt status bits are independent of the interrupt enable bits. When WCIMODE is low (read mode), MON_SYNCI[12:1] is cleared by reading the interrupt status register. When WCIMODE is high (write mode), MON_SYNCI[x] is cleared by writing a high value to bit x of the interrupt status register.

Register 0x19EA: PRGM Line Monitor Synchronization Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	MON12_SYNCE	0
Bit 10	R/W	MON11_SYNCE	0
Bit 9	R/W	MON10_SYNCE	0
Bit 8	R/W	MON9_SYNCE	0
Bit 7	R/W	MON8_SYNCE	0
Bit 6	R/W	MON7_SYNCE	0
Bit 5	R/W	MON6_SYNCE	0
Bit 4	R/W	MON5_SYNCE	0
Bit 3	R/W	MON4_SYNCE	0
Bit 2	R/W	MON3_SYNCE	0
Bit 1	R/W	MON2_SYNCE	0
Bit 0	R/W	MON1_SYNCE	0

MON_SYNCE[12:1]

The monitor synchronization interrupt enable (MON_SYNCE[12:1]) bits control the activation of INTB. When MON_SYNCE[x] is set to logic 1, the corresponding STS-1/STM-0 path MON_SYNCI[x] pending synchronization interrupt will deassert INTB. When MON_SYNCE[x] is set to logic 0, the MON_SYNCI[x] pending synchronization interrupt will not deassert INTB.

Register 0x19EB: PRGM Line Monitor Synchronization Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	MON_SYNCV[12]	X
Bit 10	R	MON_SYNCV[11]	X
Bit 9	R	MON_SYNCV[10]	X
Bit 8	R	MON_SYNCV[9]	X
Bit 7	R	MON_SYNCV[8]	X
Bit 6	R	MON_SYNCV[7]	X
Bit 5	R	MON_SYNCV[6]	X
Bit 4	R	MON_SYNCV[5]	X
Bit 3	R	MON_SYNCV[4]	X
Bit 2	R	MON_SYNCV[3]	X
Bit 1	R	MON_SYNCV[2]	X
Bit 0	R	MON_SYNCV[1]	X

MON_SYNCV[12:1]

The MON_SYNCV[x] bit reflects the current synchronization status of the monitor. The MON_SYNCV[x] is set high when the monitor is in synchronization for the corresponding STS-1/STM-0 path. The MON_SYNCV[x] is set low when the monitor is not in synchronization for the corresponding STS-1/STM-0 path.

The PRBS monitor will lock to an all 1s or all 0s pattern.

For concatenated payloads, only the first STS-1 path of the STS-Nc MON_SYNCV[x] bit is valid.

Register 0x19EC: PRGM Line Counter Update

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

A write to this register or to the Master Reset and Identity Register (address 0x1800) will trigger the transfer of the error counters to holding registers where they can be read. The value written in the register is not important.

Register 0x1AA0: Transmit Telecom DLL Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	—	Unused	X
Bit 2	R/W	ERRORE	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The DLL Configuration Register controls the basic operation of the DLL.

ERRORE

The ERROR interrupt enable (ERRORE) bit enables the error indication interrupt. When ERRORE is set high, an interrupt is generated upon assertion event of the ERR output and ERROR register. When ERRORE is set low, changes in the ERROR and ERR status do not generate an interrupt.

Register 0x1AA2: Transmit Telecom DLL

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

Writing to this register performs a software reset of the DLL. A software reset requires a maximum of 24*256 OCLK cycles for the DLL to regain lock. During this time the DLLCLK phase is adjusting from its current position to delay tap 0 and back to a lock position.

Register 0x1AA3: Transmit Telecom DLL Control Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	OCLKI	X
Bit 6	—	Unused	X
Bit 5	R	ERRORI	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R	ERROR	X
Bit 1	R	Reserved	0
Bit 0	R	RUN	0

The DLL Control Status Register provides information of the DLL operation.

RUN

The DLL lock status register bit RUN indicates the DLL has found an initial lock condition. When the phase detector first indicates lock, RUN is set high. The RUN register bit is cleared only by a system reset or a software reset.

ERROR

The delay line error register ERROR indicates the DLL is currently at the end of the delay line. ERROR is set high when the DLL tries to move beyond the end of the delay line. Once DLL is in ERROR state, the only way to restore the DLL into normal operational state is to reset DLLs.

ERRORI

The error event register bit ERRORI indicates the ERROR register bit has been a logic one. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. The ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

OCLKI

The clock event register bit OCLKI provides a method to monitor activity on the OCLK clock. When the OCLK input changes from a logic zero to a logic one, the OCLKI register bit is set to logic one. The OCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

Register 0x1FF0: S/UNI 4xJET Transmit L2 Tristate Control LSB

Bit	Type	Function	Default
Bit 15	R/W	TCNTRL[15]	1
Bit 14	R/W	TCNTRL[14]	1
Bit 13	R/W	TCNTRL[13]	1
Bit 12	R/W	TCNTRL[12]	1
Bit 11	R/W	TCNTRL[11]	1
Bit 10	R/W	TCNTRL[10]	1
Bit 9	R/W	TCNTRL[9]	1
Bit 8	R/W	TCNTRL[8]	1
Bit 7	R/W	TCNTRL[7]	1
Bit 6	R/W	TCNTRL[6]	1
Bit 5	R/W	TCNTRL[5]	1
Bit 4	R/W	TCNTRL[4]	1
Bit 3	R/W	TCNTRL[3]	1
Bit 2	R/W	TCNTRL[2]	1
Bit 1	R/W	TCNTRL[1]	1
Bit 0	R/W	TCNTRL[0]	1

Register 0x1FF1: S/UNI 4xJET Transmit L2 Tristate Control MSB

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14	R/W	TCNTRL[30]	1
Bit 13	R/W	TCNTRL[29]	1
Bit 12	R/W	TCNTRL[28]	1
Bit 11	R/W	TCNTRL[27]	1
Bit 10	R/W	TCNTRL[26]	1
Bit 9	R/W	TCNTRL[25]	1
Bit 8	R/W	TCNTRL[24]	1
Bit 7	R/W	TCNTRL[23]	1
Bit 6	R/W	TCNTRL[22]	1
Bit 5	R/W	TCNTRL[21]	1
Bit 4	R/W	TCNTRL[20]	1
Bit 3	R/W	TCNTRL[19]	1
Bit 2	R/W	TCNTRL[18]	1
Bit 1	R/W	TCNTRL[17]	1
Bit 0	R/W	TCNTRL[16]	1

TCNTRL[30:0]

The Transmit L2 Tristate Control (TCNTRL[30:0]) bits enable the S/UNI 4xJET to respond to a specified address on TADR[4:0] during L2 UTOPIA /L2 POSPHY operation. There are 31 valid addresses with the all-one's address being a null address. These 31 addresses correspond directly to the individual bits of TCNTRL[30:0] with TCNTRL[0] representing address 0, and TCNTRL[30] representing address 31.

When a logic 1 is written to TCNTRL[x], the transmit L2 outputs are driven by the S/UNI 4xJET in response to a valid address cycle specified by TADR[4:0] = address x. When a logic 0 is written to TCNTRL[x], the transmit L2 outputs are held in tristate in response to a valid address cycle specified by TADR[4:0] = address x. The transmit L2 outputs include TCA_PTPA, and STPA.

Register 0x1FF2: S/UNI 4xJET Receive L2 Tristate Control LSB

Bit	Type	Function	Default
Bit 15	R/W	RCNTRL[15]	1
Bit 14	R/W	RCNTRL[14]	1
Bit 13	R/W	RCNTRL[13]	1
Bit 12	R/W	RCNTRL[12]	1
Bit 11	R/W	RCNTRL[11]	1
Bit 10	R/W	RCNTRL[10]	1
Bit 9	R/W	RCNTRL[9]	1
Bit 8	R/W	RCNTRL[8]	1
Bit 7	R/W	RCNTRL[7]	1
Bit 6	R/W	RCNTRL[6]	1
Bit 5	R/W	RCNTRL[5]	1
Bit 4	R/W	RCNTRL[4]	1
Bit 3	R/W	RCNTRL[3]	1
Bit 2	R/W	RCNTRL[2]	1
Bit 1	R/W	RCNTRL[1]	1
Bit 0	R/W	RCNTRL[0]	1

Register 0x1FF3: S/UNI 4xJET Receive L2 Tristate Control MSB

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14	R/W	RCNTRL[30]	1
Bit 13	R/W	RCNTRL[29]	1
Bit 12	R/W	RCNTRL[28]	1
Bit 11	R/W	RCNTRL[27]	1
Bit 10	R/W	RCNTRL[26]	1
Bit 9	R/W	RCNTRL[25]	1
Bit 8	R/W	RCNTRL[24]	1
Bit 7	R/W	RCNTRL[23]	1
Bit 6	R/W	RCNTRL[22]	1
Bit 5	R/W	RCNTRL[21]	1
Bit 4	R/W	RCNTRL[20]	1
Bit 3	R/W	RCNTRL[19]	1
Bit 2	R/W	RCNTRL[18]	1
Bit 1	R/W	RCNTRL[17]	1
Bit 0	R/W	RCNTRL[16]	1

RCNTRL[30:0]

The Receive L2 Tristate Control (RCNTRL[30:0]) bits enable the S/UNI 4xJET to respond to a specified address on RADR[4:0] during L2 UTOPIA /L2 POSPHY operation. There are 31 valid addresses with the all-one's address being a null address. These 31 addresses correspond directly to the individual bits of RCNTRL[30:0] with RCNTRL[0] representing address 0, and RCNTRL[30] representing address 31.

When a logic 1 is written to RCNTRL[x], the receive L2 outputs are driven by the S/UNI 4xJET in response to a valid address cycle specified by RADR[4:0] = address x. When a logic 0 is written to RCNTRL[x], the receive L2 outputs are held in tristate in response to a valid address cycle specified by RADR[4:0] = address x. The receive L2 outputs include RDAT[15:0], RPRTY, RSOC_RSOP, REOP, RERR, RMOD, RVAL, and RCA_RPA.

4 Test Mode Register Description

Test mode registers are used to apply test vectors during production testing of the S/UNI 4xJET. Test mode registers (as opposed to normal mode registers) are selected when A[13] is high.

Test mode registers may also be used for board testing. When all of the TSBs within the S/UNI 4xJET are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface .

In addition, the S/UNI 4xJET also supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port.

Table 49 Test Mode Register Memory Map

Address	Register
0x000-0x1FFF	Normal Mode Registers
0x2000	Master Test Register
0x2000-0x2FFF	Reserved for Production Test

Notes on Test Mode Register Bits

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.
2. Writeable test mode register bits are not initialized upon reset unless otherwise noted.

Register 0x2000: S/UNI 4xJET Master Test

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	W	Reserved	X
Bit 6	—	Unused	X
Bit 5	W	Reserved	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	0
Bit 2	—	Unused	X
Bit 1	W	HIZDATA	0
Bit 0	W	HIZIO	0

This register is used to enable S/UNI 4xJET test features. All bits, except PMCTST are reset to zero by a hardware reset of the S/UNI 4xJET. The S/UNI 4xJET Master Test register is not affected by a software reset (via the S/UNI 4xJET Master Reset and Identity register address (address 0x1800)).

HIZIO, HIZDATA

The HIZIO and HIZDATA bits control the tri-state modes of the S/UNI 4xJET. While the HIZIO bit is a logic one, all output pins of the S/UNI 4xJET except the data bus and output TDO are held tri-state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles. The HIZDATA bit is overridden by the DBCTRL bit.

DBCTRL

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one and either IOTST or PMCTST are logic one, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the S/UNI 4xJET to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

PMCTST

The PMCTST bit is used to configure the S/UNI 4xJET for PMC's manufacturing tests. When PMCTST is set to logic one, the S/UNI 4xJET microprocessor port becomes the test access port used to run the PMC manufacturing test vectors. The PMCTST bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

Notes