▶UNDER DEVELOPMENT

BATTERY BACKUP IC

S-8423 Series

The S-8423 Series is a CMOS IC designed for use in the switching circuits of main and backup power supplies of 3-V operation microcomputers. It consists of two voltage regulators, three voltage detectors, a switchover circuit, and a control circuit. In addition to being able to switch from primary to backup power supplies, the S-8423 Series has three types of voltage detection output signal corresponding to the power supply voltage. The special sequence for switch control prevents unnecessary exhaustion of the backup power supply; this feature is suitable for structuring backup systems.

■ Features

- Low power consumption
  Normal operation: 43 μA max. (V_{IN} = 6 V)
  Backup: 2.1 μA max.
- Voltage regulator
  Small input/output voltage differences :
  0.35 V max. (I_{OUT} = 50mA)
  Output voltage tolerance : ±2%
- Three built-in voltage detectors (CS, $\overline{\text{PREEND}}$, $\overline{\text{RESET}}$)
  Detection voltage tolerance: ±2%
- Special sequence
  Backup voltage is not output, if the primary power supply voltage does not reach the $\overline{\text{RESET}}$ voltage that activates a CPU.

■ Applications

- Video camera recorder
- Still video camera
- Memory card
- SRAM backup equipment

■ Selection Guide

(Ta = 25°C)

Model No.	Output voltage*(V)			CS detection voltage(V)			CS release voltage(V)			$\overline{\text{RESET}}$ detection voltage(V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
S-8423AFT	3.23	3.30	3.37	3.919	4.000	4.081	4.003	4.100	4.197	2.253	2.300	2.347
S-8423BFT	3.332	3.400	3.468	3.185	3.250	3.315	3.264	3.348	3.432	2.449	2.500	2.551
	3.135	3.200	3.265									

*S-8423AFT : $V_{RO} = V_{OUT}$
S-8423BFT : Upper = V_{RO}, lower = V_{OUT}

■ Block Diagram

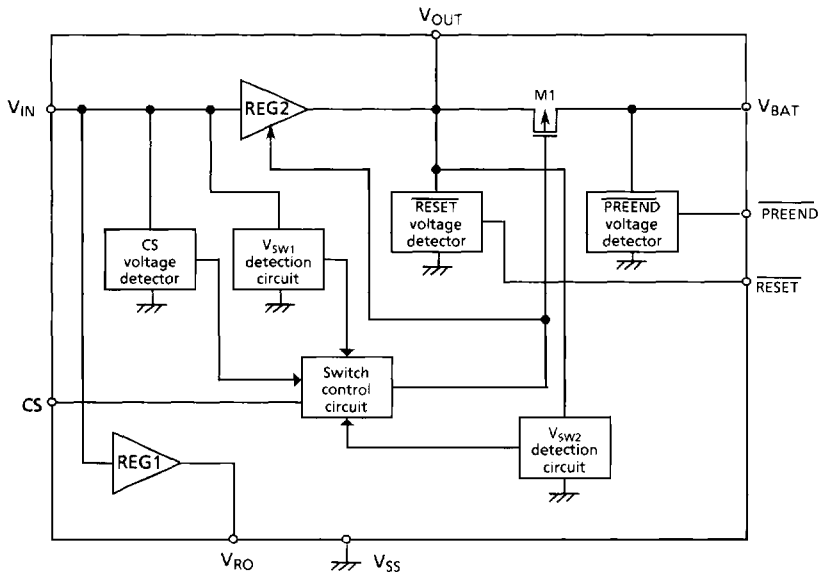
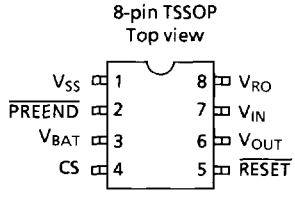


Figure 1

■ Pin Assignment



Pin name	Functions
CS	Output pin of CS voltage detector
RESET	Output pin of RESET voltage detector
PREEND	Output pin of PREEND voltage detector
V_{IN}*	Primary power supply input pin
V_{BAT}*	Backup power supply input pin
V_{OUT}*	Output pin of voltage regulator 2
V_{RO}*	Output pin of voltage regulator 1
V_{SS}	Ground

* Mount capacitors between V_{SS} (GND) and the V_{IN}, V_{BAT}, V_{OUT}, and V_{RO} pins. (See "Standard Circuit")

Figure 2

■ Absolute Maximum Ratings

Table 1

Ta = 25°C

Parameter	Symbol	Ratings	Unit
Primary power supply input voltage	V_{IN}	17	V
Backup power supply input voltage	V_{BAT}	17	V
Output voltage of voltage regulator	V_{RO}, V_{OUT}	V_{SS}-0.3 to V_{IN} + 0.3	V
Output voltage of CS, RESET, PREEND	V_{CS}, V_{RESET}, V_{PRE}	V_{SS}-0.3 to 17	V
Power dissipation	P_D	480	mW
Operating temperature	T_{opr}	-40 to + 85	°C
Storage temperature	T_{stg}	-40 to + 125	°C

■ Electrical Characteristics

1. S-8423AFT

Table 2

(Unless otherwise specified : Ta = 25°C)

	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test cir.
Voltage regulator	Output voltage1	V_{RO}	V_{IN} = 6 V, I_{RO} = 30 mA	3.23	3.30	3.37	V	1
	I/O voltage difference 1	V_{dif1}	I_{RO} = 30 mA	—	0.2	0.35	V	
	Load regulation 1	$\triangle V_{ROLO}$	V_{IN} = 6 V I_{RO} = 100 μA to 40 mA	—	40	100	mV	
	Line regulation 1	$\triangle V_{ROLI}$	V_{IN} = 6 to 16 V I_{RO} = 30 mA	—	38	100	mV	
	Temperature coefficient of V_{RO}	$\frac{\triangle V_{RO}}{\triangle Ta}$	Ta = -40°C to 85°C	—	± 0.47	—	mV/°C	
	Output voltage 2	V_{OUT}	V_{IN} = 6 V, I_{OUT} = 50 mA	3.23	3.30	3.37	V	
	I/O voltage difference 2	V_{dif2}	I_{OUT} = 50 mA	—	0.2	0.35	V	
	Load regulation 2	$\triangle V_{OUTLO}$	V_{IN} = 6 V I_{OUT} = 100 μA to 60 mA	—	50	110	mV	
	Line regulation 2	$\triangle V_{OUTLI}$	V_{IN} = 6 to 16 V I_{OUT} = 50 mA	—	50	110	mV	
	Temperature coefficient of V_{OUT}	$\frac{\triangle V_{OUT}}{\triangle Ta}$	Ta = -40°C to 85°C	—	± 0.47	—	mV/°C	
	Input voltage of primary power supply	V_{IN}		—	—	16	V	
Voltage detector	CS detection voltage	$-V_{DET1}$	Detects V_{IN}	3.919	4.000	4.081	V	2
	CS release voltage	$+V_{DET1}$		4.003	4.100	4.197	V	
	$\overline{\text{RESET}}$ detection voltage	$-V_{DET2}$	Detects V_{OUT}	2.253	2.300	2.347	V	
	$\overline{\text{RESET}}$ release voltage	$+V_{DET2}$		2.351	2.420	2.489	V	
	$\overline{\text{PREEND}}$ detection voltage	$-V_{DET3}$	Detects V_{BAT}	$-V_{DET2}$ + 0.15	$-V_{DET2}$ + 0.20	$-V_{DET2}$ + 0.25	V	
	$\overline{\text{PREEND}}$ release voltage	$+V_{DET3}$		$-V_{DET3}$ + 0.11	$-V_{DET3}$ + 0.14	$-V_{DET3}$ + 0.17	V	
	Operating voltage	V_{opr}	V_{IN} or V_{BAT}	2.0	—	16	V	
	Temperature coefficient of detection voltage	$\frac{\triangle -V_{DET1}}{\triangle Ta}$	Ta = -40°C to 85°C	—	± 0.57	—	mV/°C	
		$\frac{\triangle -V_{DET2}}{\triangle Ta}$	Ta = -40°C to 85°C	—	± 0.33	—	mV/°C	
		$\frac{\triangle -V_{DET3}}{\triangle Ta}$	Ta = -40°C to 85°C	—	± 0.36	—	mV/°C	
	Sink current	I_{SINK}	V_{DS} = 0.5 V, V_{IN} = V_{BAT} = 2.0 V; $\overline{\text{RESET}}$	1.50	2.30	—	mA	3
			$\overline{\text{PREEND}}$	1.50	2.30	—	mA	
			CS	1.50	2.30	—	mA	
	Leakage current	I_{LEAK}	V_{DS} = 16 V, V_{IN} = 16 V	—	—	0.1	μA	
Switch	Switchover voltage	V_{SW1}	V_{BAT} = 2.8 V Detects V_{IN}	+ V_{DET1} × 0.75	+ V_{DET1} × 0.77	+ V_{DET1} × 0.79	V	4
	CS output inhibit voltage	V_{SW2}	V_{BAT} = 3 V Detects V_{OUT}	V_{OUT} × 0.93	V_{OUT} × 0.95	V_{OUT} × 0.97	V	5
	M1 switch leakage current	I_{LEK}	V_{IN} = 6 V V_{BAT} = 0 V	—	—	1	μA	6
	M1 switch resistance value	R_{SW}	V_{IN} = open, V_{BAT} = 3 V I_{OUT} = 10 to 500 μA	—	—	100	Ω	7
	Temperature coefficient of V_{SW1}	$\frac{\triangle V_{SW1}}{\triangle Ta}$	Ta = − 40°C to 85°C	—	± 0.44	—	mV/°C	4
	Temperature coefficient of V_{SW2}	$\frac{\triangle V_{SW2}}{\triangle Ta}$	Ta = − 40°C to 85°C	—	± 0.45	—	mV/°C	5
Current consumption		I_{SS1}	V_{IN} = 6 V, Unloaded	—	28	43	μA	8
		I_{BAT1}	V_{BAT} = 3 V	—	0.26	0.50	μA	
		I_{BAT2}	V_{IN} = open, V_{BAT} = 3 V, Unloaded; Ta = 25°C	—	1.0	2.1	μA	
			Ta = 85°C	—	—	3.5	μA	
Input voltage of backup power supply		V_{BAT}		2.0	—	4.0	V	7

2. S-8423BFT

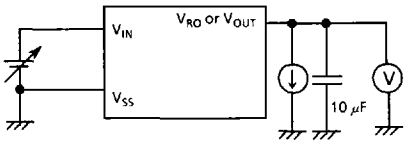
Table 3

(Unless otherwise specified : Ta = 25°C)

	Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test cir.
Voltage regulator	Output voltage1	V_{RO}	V_{IN} = 3.6 V, I_{RO} = 15 mA		3.332	3.400	3.468	V	1
	I/O voltage difference 1	V_{dif1}	I_{RO} = 15 mA		—	0.2	0.35	V	
	Load regulation 1	$\triangle V_{ROLO}$	V_{IN} = 3.6 V I_{RO} = 100 μA to 20 mA		—	40	100	mV	
	Line regulation 1	$\triangle V_{ROLI}$	V_{IN} = 3.6 to 16 V I_{RO} = 15 mA		—	38	100	mV	
	Temperature coefficient of V_{RO}	$\frac{\triangle V_{RO}}{\triangle Ta}$	Ta = -40°C to 85°C		—	± 0.47	—	mV/°C	
	Output voltage 2	V_{OUT}	V_{IN} = 3.6 V, I_{OUT} = 15 mA		3.135	3.200	3.265	V	
	I/O voltage difference 1	V_{dif2}	I_{OUT} = 15 mA		—	0.2	0.35	V	
	Load regulation 2	$\triangle V_{OUTLO}$	V_{IN} = 3.6 V I_{OUT} = 100 μA to 20 mA		—	50	110	mV	
	Line regulation 2	$\triangle V_{OUTLI}$	V_{IN} = 3.6 to 16 V I_{OUT} = 15 mA		—	50	110	mV	
	Temperature coefficient of V_{OUT}	$\frac{\triangle V_{OUT}}{\triangle Ta}$	Ta = -40°C to 85°C		—	± 0.47	—	mV/°C	
	Input voltage of primary power supply	V_{IN}			—	—	16	V	
Voltage detector	CS detection voltage	$-V_{DET1}$	Detects V_{IN}		3.185	3.250	3.315	V	2
	CS release voltage	$+V_{DET1}$			3.264	3.348	3.432	V	
	$\overline{\text{RESET}}$ detection voltage	$-V_{DET2}$	Detects V_{OUT}		2.449	2.500	2.551	V	
	$\overline{\text{RESET}}$ release voltage	$+V_{DET2}$			2.562	2.636	2.710	V	
	$\overline{\text{PREEND}}$ detection voltage	$-V_{DET3}$	Detects V_{BAT}		$-V_{DET2}$ + 0.15	$-V_{DET2}$ + 0.20	$-V_{DET2}$ + 0.25	V	
	$\overline{\text{PREEND}}$ release voltage	$+V_{DET3}$			$-V_{DET3}$ + 0.11	$-V_{DET3}$ + 0.14	$-V_{DET3}$ + 0.17	V	
	Operating voltage	V_{opr}	V_{IN} or V_{BAT}		2.0	—	16	V	
	Temperature coefficient of detection voltage	$\frac{\triangle -V_{DET1}}{\triangle Ta}$	Ta = -40°C to 85°C		—	± 0.47	—	mV/°C	
		$\frac{\triangle -V_{DET2}}{\triangle Ta}$	Ta = -40°C to 85°C		—	± 0.33	—	mV/°C	
		$\frac{\triangle -V_{DET3}}{\triangle Ta}$	Ta = -40°C to 85°C		—	± 0.36	—	mV/°C	
	Sink current	I_{SINK}	V_{DS} = 0.5 V, V_{IN} = V_{BAT} = 2.0 V	$\overline{\text{RESET}}$	1.50	2.30	—	mA	3
				$\overline{\text{PREEND}}$	1.50	2.30	—	mA	
				CS	1.50	2.30	—	mA	
	Leakage current	I_{LEAK}	V_{DS} = 16 V, V_{IN} = 16 V		—	—	0.1	μA	
Switch	Switchover voltage	V_{SW1}	V_{BAT} = 2.8 V Detects V_{IN}		+ V_{DET1} × 0.935	+ V_{DET1} × 0.955	+ V_{DET1} × 0.975	V	4
	CS output inhibit voltage	V_{SW2}	V_{BAT} = 3 V Detects V_{OUT}		V_{OUT} × 0.93	V_{OUT} × 0.95	V_{OUT} × 0.97	V	5
	M1 switch leakage current	I_{LEK}	V_{IN} = 3.6 V V_{BAT} = 0 V		—	—	1	μA	6
	M1 switch resistance value	R_{SW}	V_{IN} = open, V_{BAT} = 3 V		—	—	100	Ω	7
	Temperature coefficient of V_{SW1}	$\frac{\triangle V_{SW1}}{\triangle Ta}$	Ta = − 40°C to 85°C		—	± 0.44	—	mV/°C	4
	Temperature coefficient of V_{SW2}	$\frac{\triangle V_{SW2}}{\triangle Ta}$	Ta = − 40°C to 85°C		—	± 0.45	—	mV/°C	5
Current consumption		I_{SS1}	V_{IN} = 3.6 V, Unloaded		—	28	43	μA	8
		I_{BAT1}	V_{BAT} = 3 V		—	0.26	0.50	μA	
		I_{BAT2}	V_{IN} = open V_{BAT} = 3 V, Unloaded	Ta = 25°C	—	1.0	2.1	μA	
				Ta = 85°C	—	—	3.5	μA	
Input voltage of backup power supply		V_{BAT}			2.0	—	4.0	V	7

■ Test Circuit

1.



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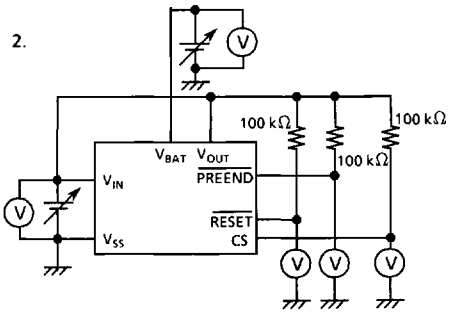
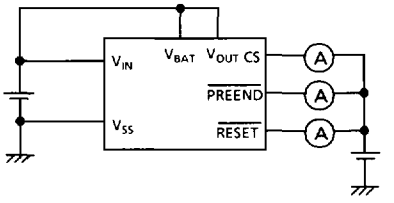


When measuring V_{DET3}, apply 6 V to V_{IN}

3.



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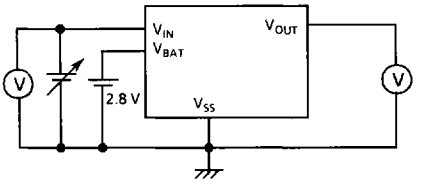
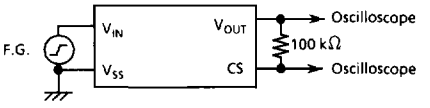


Measure the value after applying 5 V or more to V_{IN}

5.



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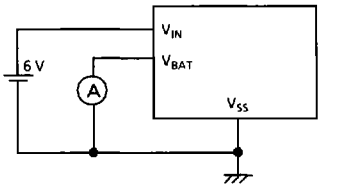

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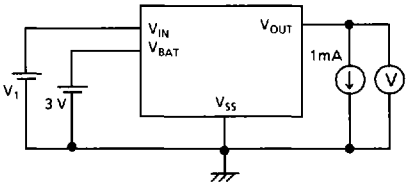
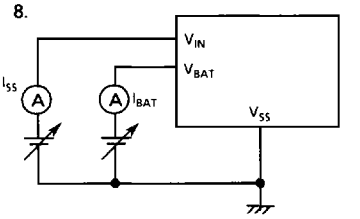


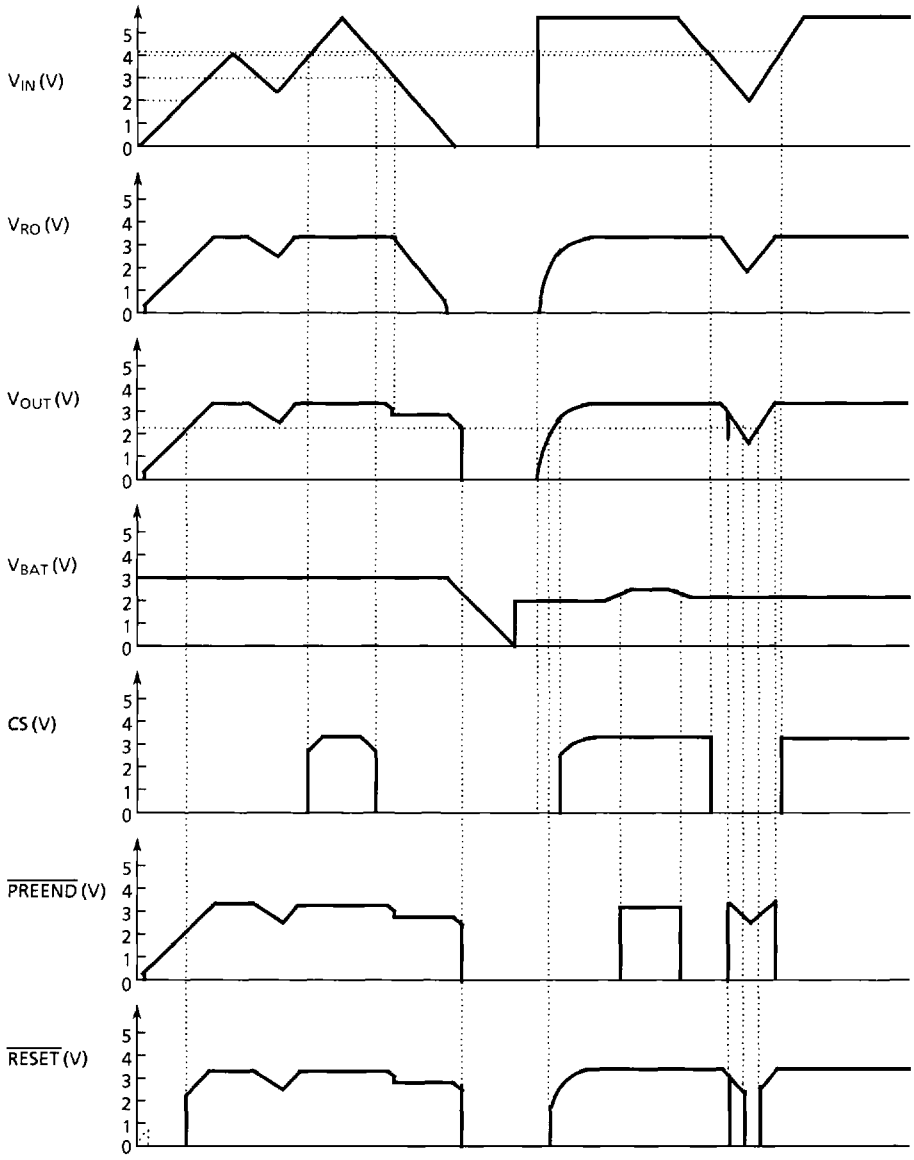
Open and measure the value after applying 6 V to V_1

8.



To measure I_{BAT2}, first apply 3 V to V_{BAT} and 6 V or more to V_{IN}. Then open V_{IN} and measure the current when V_{BAT} is 3 V.

■ Operation Timing Chart (S-8423AFT)



CS, and $\overline{PREEND}$ and $\overline{RESET}$ are pulled up to V_{OUT}.

■ Dimensions

8-pin TSSOP

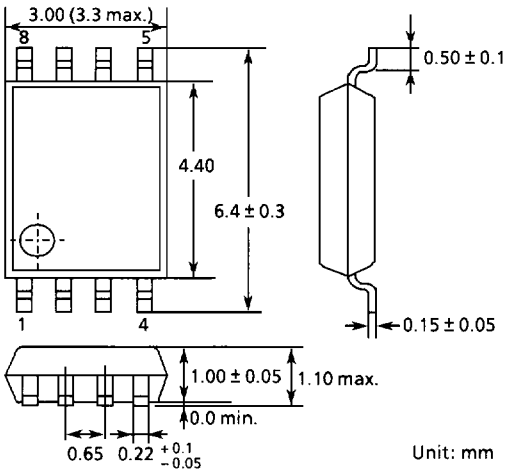
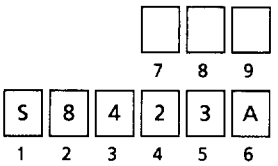


Figure 3

■ Markings



1 to 6 : Product name
7 : Assembly code
8 : Year of assembly (last digit)
9 : Month of assembly; Jan. = 1, Feb. = 2, Mar. = 3, Apr. = 4, May = 5, June = 6, July = 7, Aug. = 8, Sept. = 9, Oct. = X, Nov. = Y, Dec. = Z

Figure 4

■ Taping

1. Tape specifications

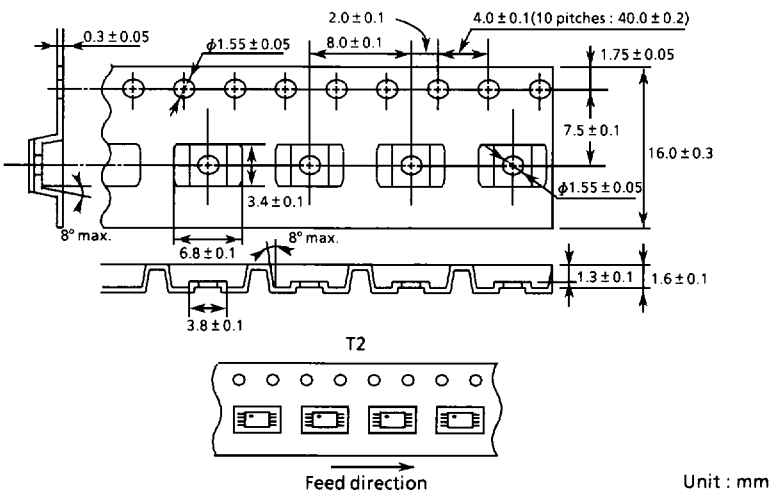


Figure 5

2. Reel specifications

1 reel holds 1500 ICs.

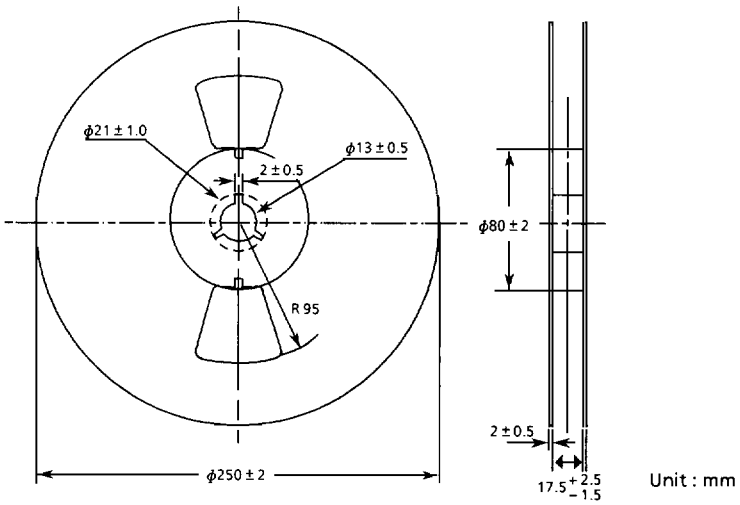


Figure 6

■ Operation

The S-8423 Series consists of two voltage regulators, and three voltage detectors. The voltage regulator 1 regulates input voltage V_{IN} and outputs to V_{RO}. The voltage regulator 2 outputs to V_{OUT}. This section describes the functions and operations of each part.

1. Voltage regulators 1 and 2

The built-in regulators have very small I/O voltage difference (V_{dif1} = 0.2 V typ. at I_{RO} = 30 mA). The output voltage of V_{RO} and V_{OUT} can be selected independently between 2.8 and 3.8 V by 0.1 V step.

I/O voltage difference V_{dif1} or V_{dif2}

Assume that the V_{RO} voltage when V_{IN} is 6 V and I_{RO} is 30 mA is Vinitial. When the amount voltage of I/O voltage difference V_{dif1} or V_{dif2} and Vinitial is applied to the V_{IN} pin, 95% of the Vinitial voltage is output at the V_{RO} pin.

2. Switch

The switch consists of the switch control circuit, V_{SW1} and V_{SW2} detection circuits, voltage regulator 2 and switch transistor M1.

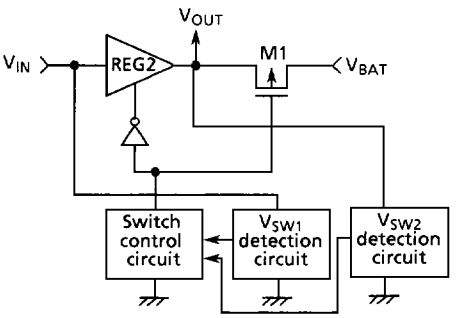


Figure 7 Switch

2.1 V_{SW1} detection circuit

The V_{SW1} detection circuit monitors the V_{IN} voltage and sends the results of detection to the switch control circuit. The detection voltage (V_{SW1}) is specified as 77 ± 2% of CS release voltage ($+V_{DET1}$).

2.2 V_{SW2} detection circuit

V_{SW2} voltage detector monitors V_{OUT} terminal voltage and keeps CS release voltage output low until V_{OUT} terminal voltage rises to V_{SW2}. Then CS output changes from low to high if V_{IN} terminal voltage is more than $+V_{DET1}$ (CS release voltage), when V_{OUT} terminal voltage rises to 95% of V_{OUT2} (output voltage of voltage regulator 2). CS output changes from high to low regardless of V_{SW2}, if V_{IN} terminal voltage falls down to less than $-V_{DET1}$ (CS detection voltage). CS output holds high if V_{IN} temrinal voltage keeps higher than $-V_{DET1}$, when V_{OUT} terminal voltage falls down to less than V_{SW2} because of undershoot.

2.3 Switch control circuit

The switch control circuit receives the signal from the V_{SW1} detection circuit and controls M1 and voltage regulator 2. The switch control circuit operates in two statuses: the special and normal sequences. In the special sequence status, the circuit does not receive nor control signals according to the V_{IN} (or V_{BAT}) voltage sequence. In the normal sequence status, the circuit receives and controls signals. Initially, the circuit is kept in the special sequence status. When V_{IN} increases until CS signal goes high, the circuit enters the normal sequence status.

(1) Special sequence status

When the V_{IN} (or V_{BAT}) voltage rises , the switch control circuit is kept in the special sequence status until CS signal goes high.

At that time, the switch control circuit turns voltage regulator 2 on and turns M1 off regardless of the status of the V_{SW1} detection circuit. The voltage regulator 2 has a switchover function.

(2) Normal sequence status

When V_{IN} voltage increases until CS signal, which monitors V_{OUT} terminal, goes high, the switch control circuit enters the normal sequence.

Once the circuit enters the normal sequence, it turns voltage regulator 2 and M1 on and off according to the V_{IN} voltage as shown in Table 3. It takes hundreds μs in the worst case until voltage regulator 2 goes ON from OFF. During this period, as both voltage regulator 2 and M1 are OFF, V_{OUT} voltage may drop. To protect this drop, do not fail to add 10 μF or more of capacitor to V_{OUT} terminal.

The circuit returns to the special sequence status, when $\overline{\text{RESET}}$ signal goes low.

Table 4

V_{IN} voltage	Voltage regulator 2	M1	V_{OUT}
$V_{IN}>V_{SW1}$	ON	OFF	V_{OUT2}
$V_{IN}<V_{SW1}$	OFF	ON	$V_{BAT}-V_{dif3}$

2.4 Switch transistor M1

Voltage regulator 2 is also used for switch from V_{IN} to V_{OUT}. Therefore, no reverse current flows from V_{OUT} to V_{IN}, when voltage regulator 2 is off.

The output voltage of voltage regulator 2 can be selected between 2.8 V and 3.8 V by 0.1 V step.

The ON resistance of M1 is 100 Ω or less when I_{OUT} is between 10 and 500 μA.

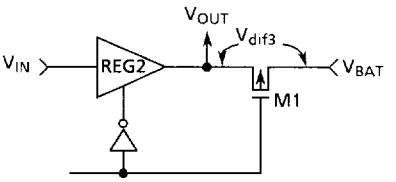


Figure 8 Definitions of V_{diff3}

Therefore, when M1 is turned on to connect V_{OUT} to V_{BAT}, the maximum voltage drop V_{dif3} due to M1 is 100 × I_{OUT} (output current). The minimum output at the V_{OUT} pin is $V_{BAT}-V_{dif3}$ (max.).

When voltage regulator 2 is on and M1 is off, the leakage current of M1 is kept below 1 μA (V_{IN} = 6 V, Ta = 25°C) with the V_{BAT} pin connected to the ground (V_{SS}).

3. Voltage detector

The S-8423 Series has three voltage detectors and V_{SW2} voltage detector. Three detectors feature high precision and low power consumption with hysteresis characteristics. And V_{SW2} voltage detector inhibit CS release output. The power of CS voltage detector is supplied from the V_{IN} and V_{BAT} pins. Therefore, the output is stable as long as the primary or backup power supplies are within the operating voltage range (2 to 16 V). All outputs are Nch open-drains, and need about 100 kΩ of pull-up resistors.

(1) CS voltage detector

CS monitors V_{IN} terminal voltage. The detection voltage can be selected between 3.0 and 5.0 V by 0.1 V step. The result of detection is output at the CS pin: "L" for lower voltages than the detection level and "H" for higher voltages than the release level.

(2) $\overline{\text{PREEND}}$ voltage detector

$\overline{\text{PREEND}}$ monitors the V_{BAT} pin. The detection voltage can be selected between 2.2 V and 2.7 V by 0.1 V step, and also higher than $\overline{\text{RESET}}$ voltage with any difference voltage, indicating that the backup power supply is running out. The result of detection is output at the $\overline{\text{PREEND}}$ pin: "L" for lower voltages than the detection level and "H" for higher voltages than the release level. The power of this detector is supplied from V_{IN} terminal, and its output is valid only when voltage ($\geq V_{SW1}$) is applied to V_{IN}.

(3) $\overline{\text{RESET}}$ voltage detector

$\overline{\text{RESET}}$ monitors the V_{OUT} pin. The detection voltage can be selected between 2.0 V and 2.7 V by 0.1 V step. The result of detection is output at the $\overline{\text{RESET}}$ pin: "L" for lower voltages than the detection level and "H" for higher voltages than the release level. $\overline{\text{RESET}}$ outputs normal logic when V_{OUT} terminal voltage is 1.0 V or more terminal.

NOTE $\overline{\text{PREEND}}$ and $\overline{\text{RESET}}$ are detected at different pins. In practice, current is taken from the V_{BAT} side, so consider the I/O voltage difference (V_{dif3}) of M1 when M1 is turned on.

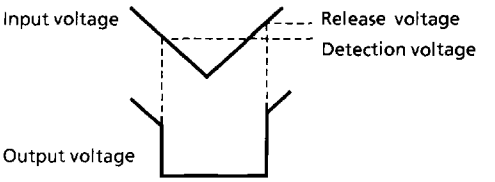


Figure 9 Detection potentials of voltage detectors

■ Standard Circuit

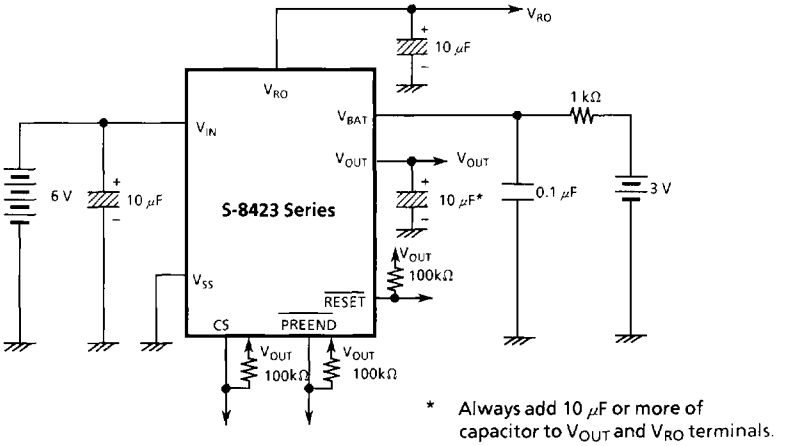


Figure 10

■ Application Circuits

1. Merits in designing

(1) A switching circuit for primary and backup power supplies is usually configured with discrete components. The S-8423 Series enables you to configure the circuit with a single chip.
Some microcomputers can enter standby mode (or low clock mode) from normal mode (or high clock mode) only, and need about 3 V each time they are used. If a low voltage (such as the backup voltage) is applied to these microcomputers initially, they may run away and vast current consumption may flow. The S-8423 Series is designed to have a *special sequence* that stops the backup voltage until the primary power supply voltage reaches the initial voltage that trips the switch.

(2) Systems can be structured easily.
Three types of built-in voltage detectors (CS, $\overline{\text{PREEND}}$, and $\overline{\text{RESET}}$) send three types of voltage detection signal to microcomputers.

(3) Battery service life are prolonged.

- The I/O voltage difference of the voltage regulator 2 switch is very small, and allows the primary power supply to be used until just before they are completely discharged.
- The current consumption during backup operation is very small (2.1 μA max.), and allows the backup power supply to have a long service life.

2. Design considerations

- In applications with small I_{RO} or I_{OUT}, output voltages (V_{RO} and V_{OUT}) may rise to cause the load stability to violate standards. Set I_{RO} and I_{OUT} to 10 μA or more.
- Attach the proper capacitor to the V_{OUT} pin to prevent the $\overline{\text{RESET}}$ voltage detector (which monitors the V_{OUT} pin) from being active due to undershoot.
- Watch for overshoot and ensure it does not exceed the ratings of the IC chips and/or capacitors attached to the V_{RO} and V_{OUT} pins.
- Power dissipation of TSSOP8 package is shown as Figure 11.

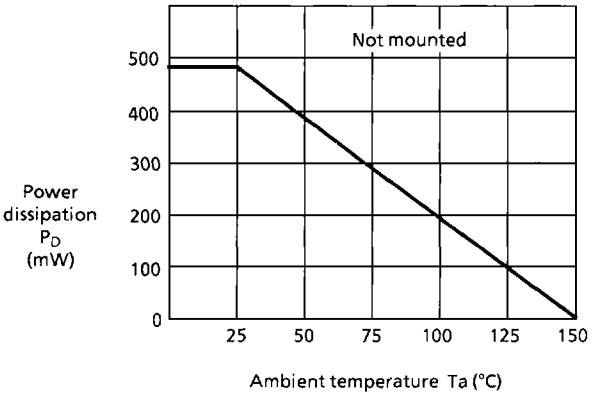
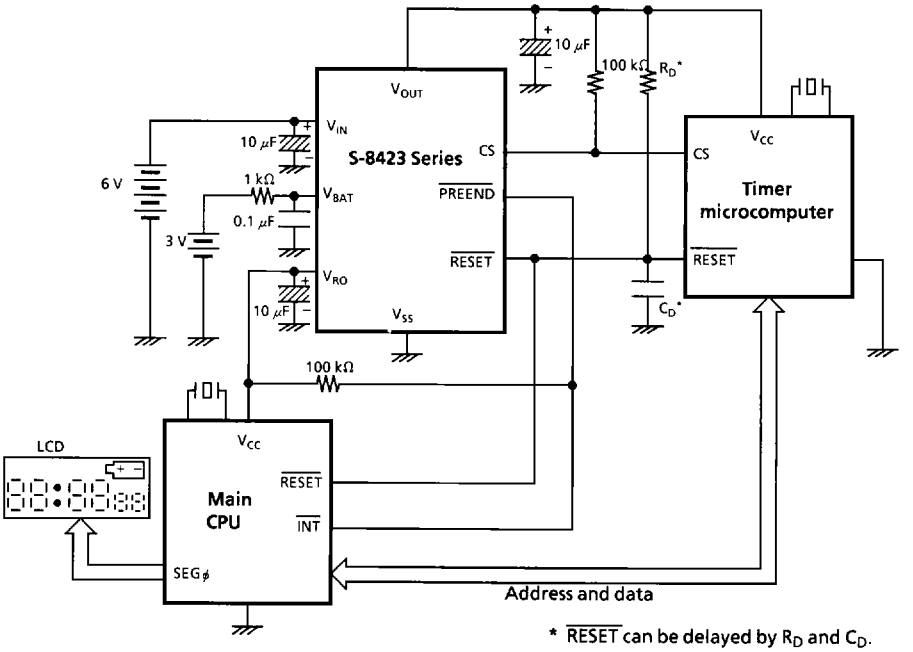


Figure 11 Power dissipation

3. Application examples

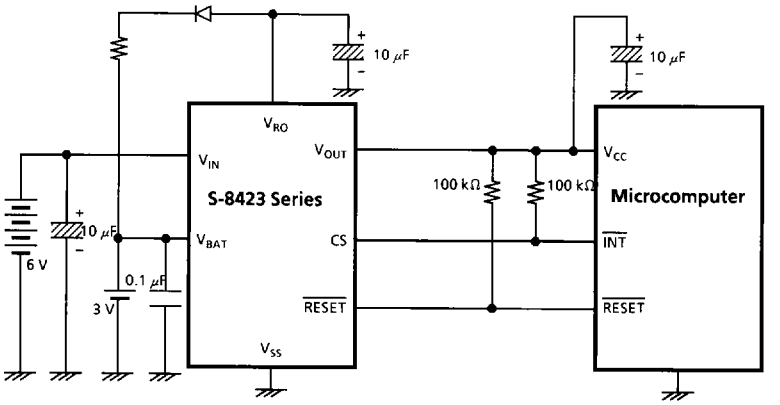
1. When using a timer microcomputer for backup and displaying $\overline{\text{PREEND}}$ on the main CPU



* $\overline{\text{RESET}}$ can be delayed by R_D and C_D.

Figure 12

2. When using rechargeable battery a sabackup battery



Backup battery can be floating-recharged by using voltage regulator1

Figure 13

3. Memory card

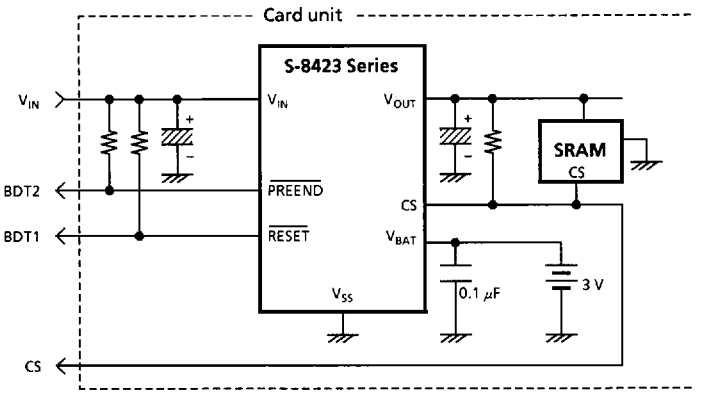


Figure 14