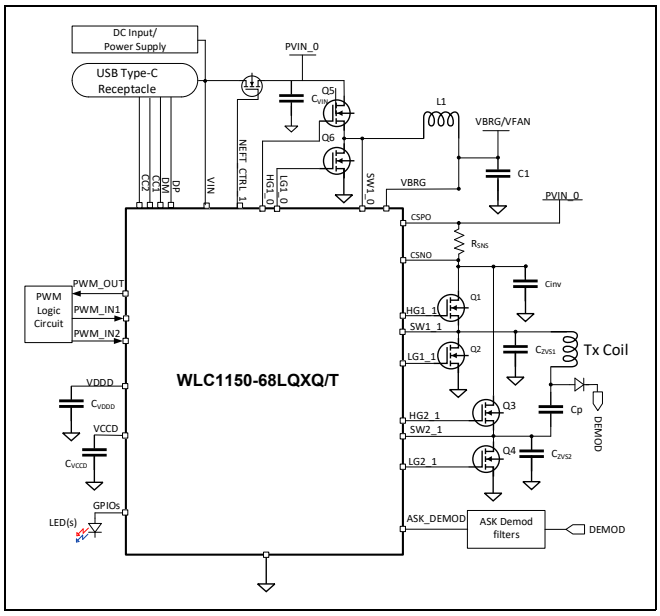
Wireless charging IC (WLC) - Transmitter 50W with integrated USB Type-C PD controller

General description

WLC1150 is a highly integrated wireless power transmitter, ideal for 50W charging applications. The IC works in Infineon high power proprietary protocol mode to deliver 50W power. WLC1150 offers a cost-effective solution for various applications up to 50W output power, by addressing critical system needs of high-power application, like thermal, EMI, foreign object detection (FOD), high efficiency and inverter control, and so on.

WLC1150 offers compatibility with various types of input configurations to address wide range of high-power applications. WLC1150 supports systems with input power supplied by either USB PD/PPS or fixed input from DC power supply. The IC supports these input configurations, without requiring a front-end DC-DC converter and this helps in achieving significant system efficiency gain, which is an important performance aspect of high-power system. WLC1150 offers many programmable features for creating distinct wireless transmitter solutions.

WLC1150 is a highly programmable wireless power transmitter with an on-chip 32-bit Arm® Cortex®-M0 processor, 128 KB flash, 16 KB RAM, and 32 KB ROM. The device also includes various analog and digital peripherals such as ADC, PWMs, and timers. The inclusion of a fully programmable MCU with analog and digital peripherals enable scalable wireless charging solutions.



Features

- 50W wireless power transfer using proprietary protocol
- Enables Qi v1.3.x compliant extended power profile (EPP) and basic power profile (BPP) transmitter (MP-A2 and similar)[1]
- Integrated gate drivers for inverter
- Inverter control using frequency, duty-cycle, and variable voltage
- Integrated buck controller for fan that enables cooling of interface surface during high power delivery.
- Integrated FOD
- Supports various input configuration i.e. USB PD/ PPS, fixed DC input of 20V without requiring an additional DC-DC converter.
- Integrated USB-PD controller
  - Supports latest USB-PD 3.1 version
  - Programmable power supply (PPS) mode
  - Support for USB PD legacy charging protocols like QC 2.0/ 3.0 and AFC
- Supports wide input voltage range: 4.5 V to 24 V with integrated buck-boost controller
- Communication ports: I2C, UART

Note

1. Customers might require a license to use the QC2.0/3.0, AFC and Qi protocols. For any other legacy charging protocol support, contact your local Infineon sales representative.

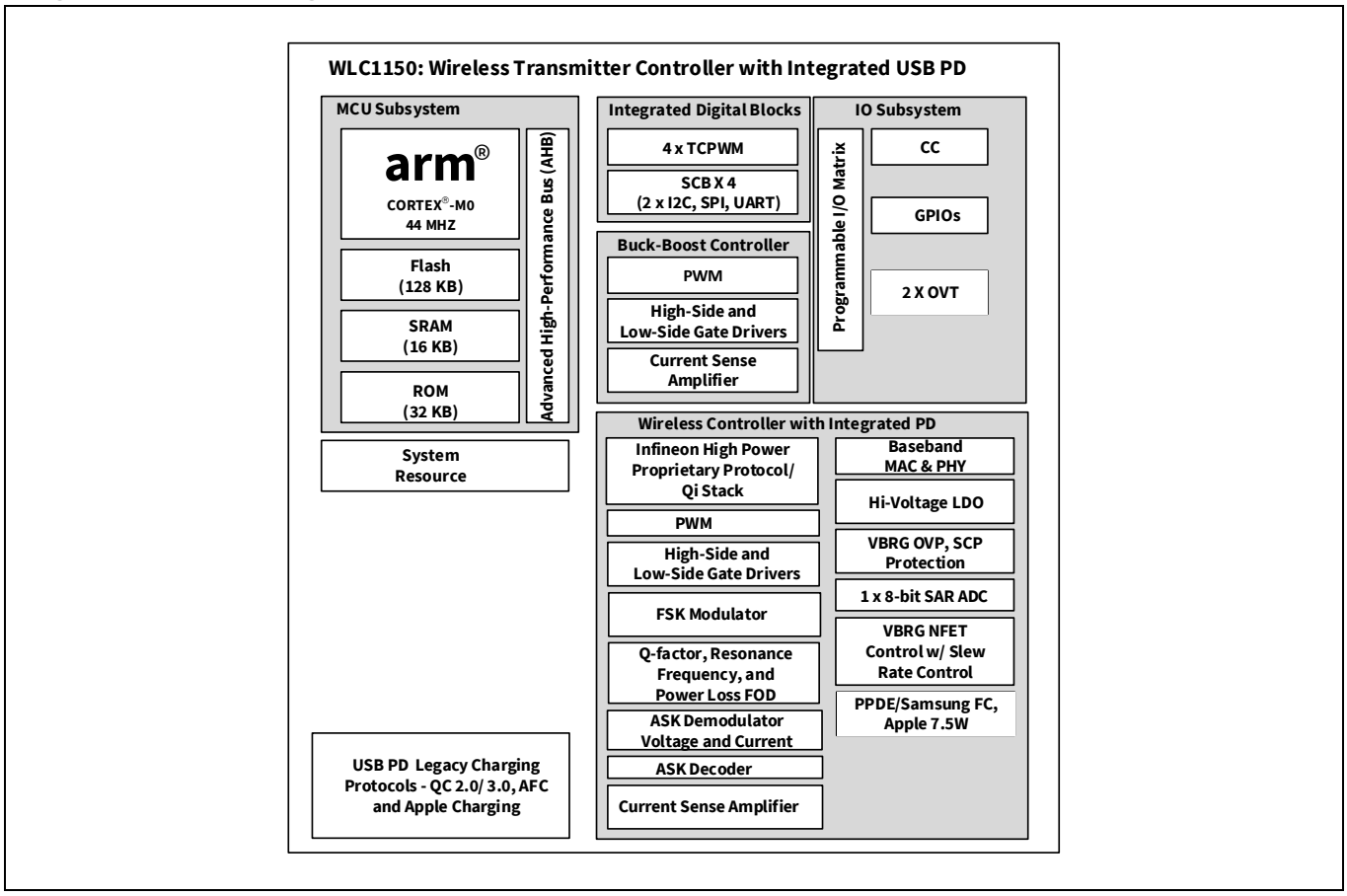
Features

- **Configurable protection**
  - Adaptive FOD
  - Overcurrent protection (OCP), overvoltage protection (OVP)
  - Supports over-temperature protection through integrated ADC circuit and internal temperature sensor
- **Temperature range**
  - Extended industrial temperature: -40°C to +105°C
- **Package**
  - 68 lead QFN 8.0 × 8.0 × 0.65 mm LD68B 5.7 × 5.7 mm EPAD

Potential applications

- Wireless charging pads with power proprietary protocol (50W)
- Industrial wireless charging applications
- Vacuum cleaner, robotics and drones
- Furniture and home goods
- Docking stations
- Smart phone charger with Qi EPP (up to 15W)

Logic block diagram



Note
2. Customers need to acquire their own licensing for Samsung FC.

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1 Single stage 50W transmitter solution with integrated buck controller for fan power supply

Figure 1 illustrates a typical application of WLC1150 for wireless power transmitter with frequency and duty cycle control based on MP-A2 transmitter coil. The input power to the system is through Type-C PD adapter or DC 20 V through power supply, powering the inverter, IC, and buck converter. The buck converter powers the fan and WLC1150. The WLC1150 controls the inverter frequency and duty to regulate the power flow to the transmitter coil powering the receiver. WLC1150 provides integrated voltage and current signal based amplitude shift key (ASK) demodulator and decoding feature with support of an external dual op amp. The OPTIGA™ Trust Security IC is interfaced over I2C for Qi authentication requirements.

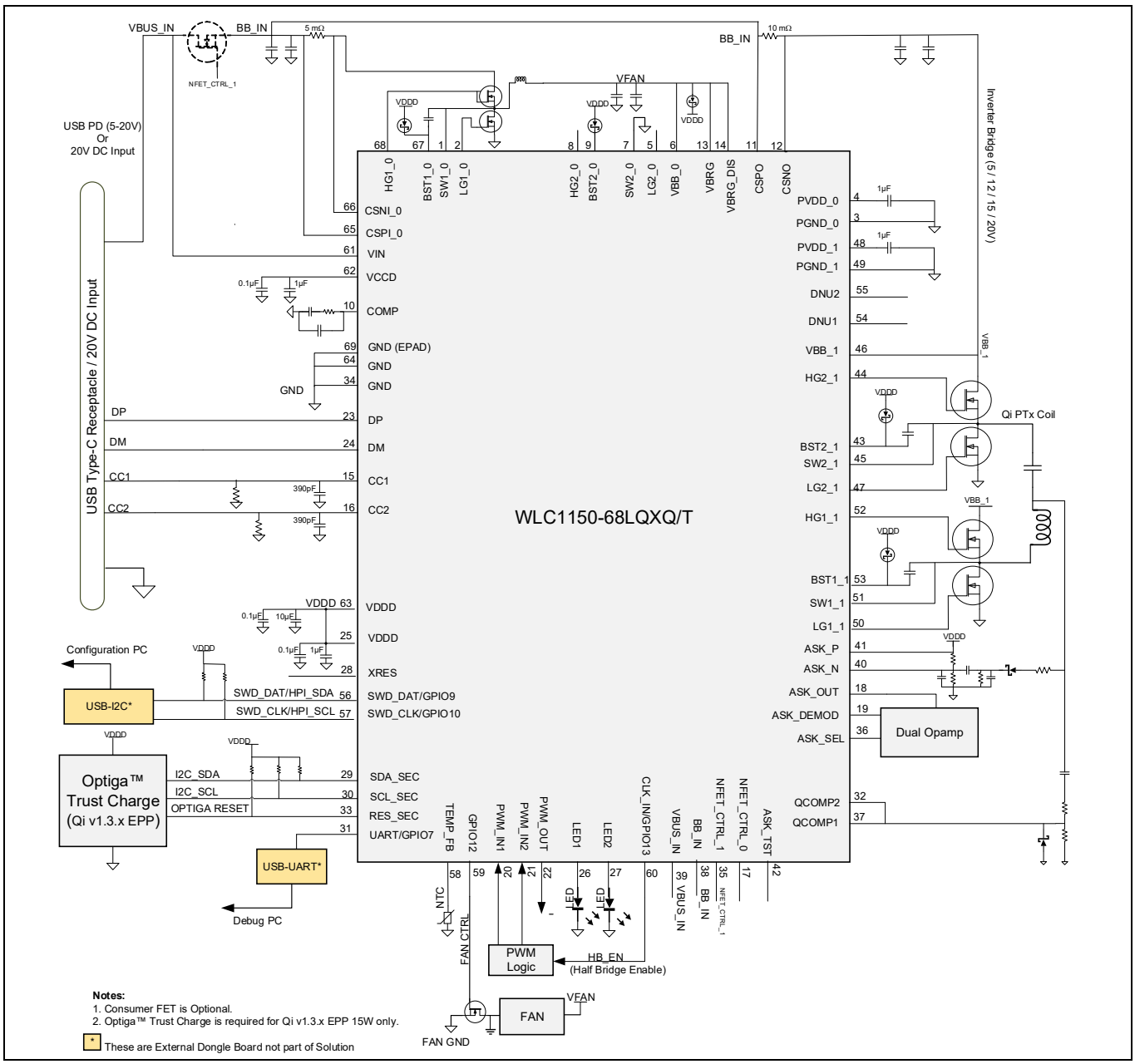


Figure 1 Application diagram for single stage 50W transmitter solution with integrated buck controller for fan power supply

2 Dual stage 50W transmitter solution with integrated buck-boost controller

Figure 2 illustrates a typical application of WLC1150 for 50W wireless power transmitter with wide input voltage range. The solution is based on MP-A2 transmitter coil. The input power to the system is through DC power supply with wide input voltage range (5 V to 20 V) powering the buck-boost converter, which in turn powers the inverter. The buck-boost converter powers regulates the VBRG to desired voltage. The WLCP1150 controls the inverter frequency and duty to regulate the power flow to the transmitter coil powering the receiver.

WLC1150 provides integrated voltage and current signal based amplitude shift key (ASK) demodulator and decoding feature with support of an external dual op amp. The OPTIGA™ Trust Security IC is interfaced over I2C for Qi authentication requirements.

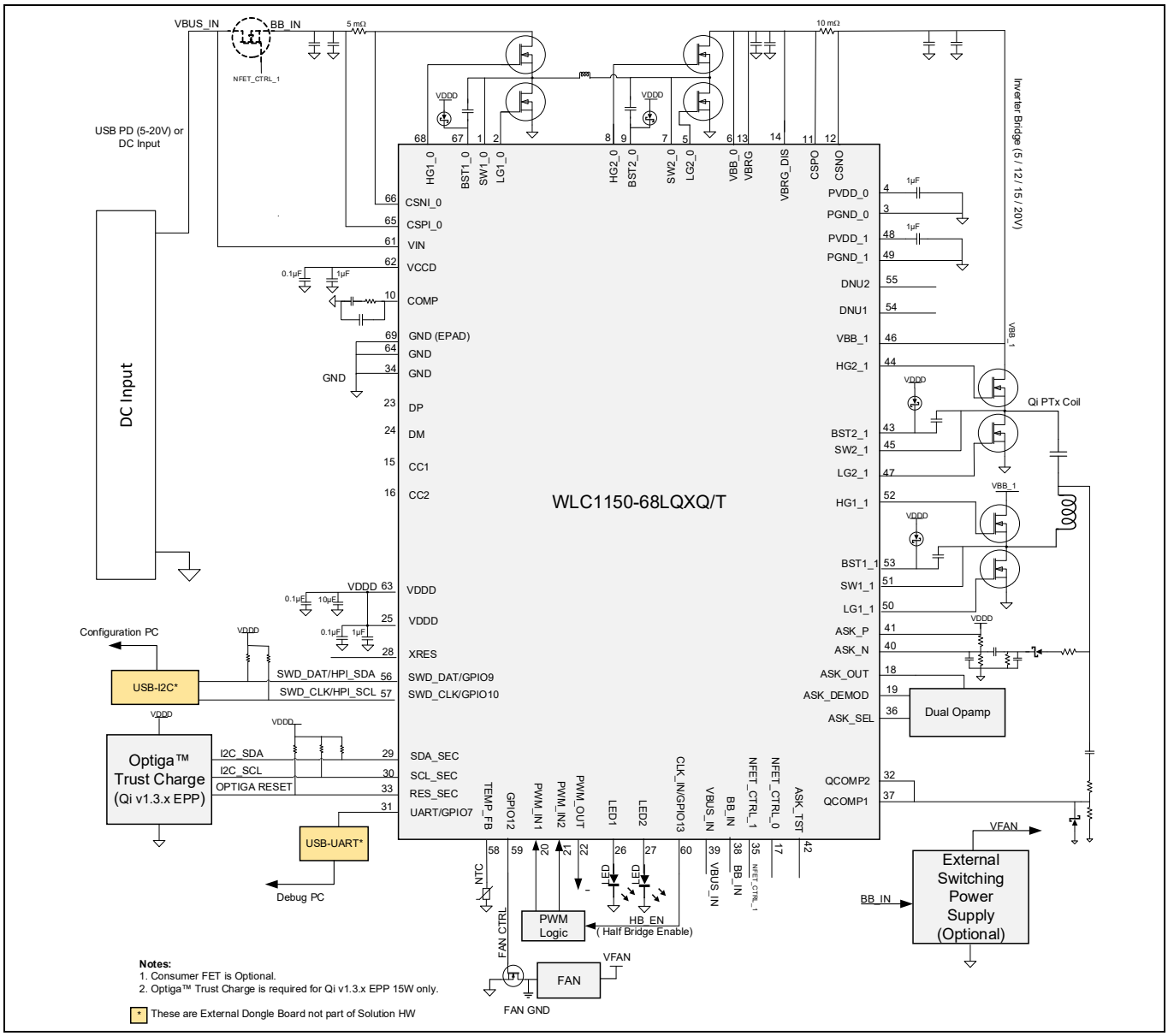


Figure 2 Application diagram for dual stage 50W transmitter solution with integrated buck-boost controller

3 Pin information

Table 1 WLC1150 pinouts

Pin #	Pin name	Pin function for 50W application firmware	Description
1	SW1_0		Switching node of buck/buck-boost converter (DC-DC bank 1) and input to zero current detector for low-side gate driver. **Single stage solution:** Connect this pin to switch node of buck with a short and wide trace. **Dual stage solution:** Connect this pin to switch node of buck-boost with a short and wide trace.
2	LG1_0		Low-side gate driver output for buck/buck-boost converter (DC-DC bank 1). **Single stage solution:** Connect to the buck low side FET gate. Use a wide trace to minimize inductance of this connection. **Dual stage solution:** Connect to the buck-boost low-side FET gate. Use a wide trace to minimize inductance of this connection.
3	PGND_0		Ground for gate driver (DC-DC). Connect all grounds (GND) and PGND pins (PNGD_0 and PGND_1) together. Connect directly PCB ground plane and EPAD.
4	PVDD_0		Connect to VDDD and to decoupling capacitors (1 µF and 0.1 µF), as close to the IC as possible.
5	LG2_0		Low-side gate driver output for DC-DC bank 2. **Single stage solution:** Float this pin. **Dual stage solution:** Connect this pin to low-side gate of buck-boost converter (DC-DC bank 2).
6	VBB_0		Output voltage of buck/buck-boost converter. **Single stage solution:** Connect this pin to output of buck converter. **Dual stage solution:** Input voltage of inverter. Connect this pin to the current sense resistor terminal which is connected to CSPO pin. Use a dedicated (Kelvin) trace for this connection.
7	SW2_0		Switching node (DC-DC bank 2). **Single stage solution:** Connect this pin directly to the EPAD. **Dual stage solution:** Connect this pin to switch node of buck-boost (DC-DC bank 2) with a short and wide trace.
8	HG2_0		High-side gate driver output of DC-DC bank 2. **Single stage solution:** Float this pin. **Dual stage solution:** Connect to the buck-boost (DC-DC bank 2) high-side FET gate. Use a wide trace to minimize inductance of this connection.
9	BST2_0		Bootstrap power supply for DC-DC bank 2. **Single stage solution:** Connect this pin to VDDD via a Schottky diode. **Dual stage solution:** Connect a capacitor (recommended value 0.1 µF) from this pin to SW2_0. Also, connect a Schottky diode from VDDD to BST2_0.
10	COMP		Error amplifier (EA) output for buck/buck-boost controller. Connect the RC compensation network to GND.
11	CSPO		Positive input of current sensing amplifier of inverter bridge input current. Connect to positive terminal of the output current sense resistor.
12	CSNO		Negative input of current sensing amplifier of inverter bridge input current. Connect to negative terminal of the current sense resistor.
13	VBRG		Feedback pin for buck/buck-boost output voltage. **Single stage solution:** Connect it to buck output. **Dual stage solution:** Connect it to buck-boost output.

Table 1 WLC1150 pinouts *(continued)*

Pin #	Pin name	Pin function for 50W application firmware	Description
14	VBRG_DIS		**Single stage solution:** Connect it to buck output. **Dual stage solution:** Connect this pin to current sense resistor terminal which is connected to CSPO pin.
15	CC1		Type-C connector configuration channel 1. Connect directly to the CC1 pin on the port's Type-C connector and to a capacitor (recommended value 390 pF) to ground. Float this pin for power supply (non USB PD) input.
16	CC2		Type-C connector configuration channel 2. Connect directly to the CC2 pin on the port's Type-C connector and to a capacitor (recommended value 390 pF) to ground. Float this pin for power supply (non USB PD) input.
17	NFET_CTRL_0		NFET gate driver output of provider FET for buck or buck-boost (DC-DC). Float this pin if it is not used.
18	ASK_OUT		ASK voltage/current sensing path. IC output for ASK signal processing.
19	ASK_DEMOD		Input for ASK signal decoding. Connect external ASK comparator output to this pin. Short this pin to pin-36 (ASK_SEL).
20	GD_OVR_HB_1	PWM_IN1	Inverter gate driver input signal for inverter bank 1. Connect output of PWM logic signal to this pin for 50W application.
21	GD_OVR_HB_2	PWM_IN2	Inverter gate driver input signal for inverter bank 2. Connect output of PWM logic signal to this pin for 50W application.
22	PWM_OUT		Input for PWM logic circuit. Connect to input of PWM logic circuit.
23	DP/GPIO1	DP	Default USB D+ / configurable GPIO. For support of legacy charging BC 1.2, AFC, QC or Apple. IC does not support USB data transmission on this pin.
24	DM/GPIO2	DM	Default USB D- / configurable GPIO. For support of legacy charging BC 1.2, AFC, QC or Apple. IC does not support USB data transmission on this pin.
25, 63	VDDD		VDDD 5V LDO output from VIN. Connect a ceramic bypass capacitor (recommended value 1 µF) from this pin to GND close to the IC. Connect all VDDD and PVDD pins together.
26	GPIO3	LED1	Default LED1 50W application/configurable GPIO. Float this pin if it is not used.
27	GPIO4	LED2	Default LED2 for 50W application/configurable GPIO. Float this pin if it is not used.
28	XRES		External reset – active low, internally pulled-up (~6 kΩ). Float this pin if it is not used.
29	GPIO5/SCB0	SDA_SEC	Used for interfacing as master, with OPTIGA™ Trust I2C SDA. The pin is configured for open drain connection, connect an external pull-up resistor. Float this pin if it is not used.
30	GPIO6/SCB0	SCL_SEC	Used for interfacing with OPTIGA™ Trust I2C SCL. The pin is configured for open drain connection, connect an external pull-up resistor. Float this pin if it is not used.
31	GPIO7/SCB1	UART/GPIO7	Default UART Tx for debug/configurable GPIO. Float this pin if it is not used.
32	QCOMP2	QCOMP2	Q-factor based foreign object detection (FOD) pre-charge measurement input for frequency counting. Connect this pin to pin 37 (QCOMP1).
33	GPIO8	RES_SEC	RESET for OPTIGA™ Trust IC. Configured for using OPTIGA™ Trust in low power mode. Float this pin if it is not used.
34, 64	GND		Ground. Connect directly to the E-PAD and to ground plane.
35	NFET_CTRL_1		NFET gate driver output for consumer FET, if used. Float this pin if not used (consumer FET is required to meet USB PD specification).

Table 1 WLC1150 pinouts *(continued)*

Pin #	Pin name	Pin function for 50W application firmware	Description
36	ASK_SEL		Input for ASK signal decoding. Connect this pin to pin-19 (ASK_DEMOD).
37	QCOMP1		Q-factor based FOD pre-charge measurement input for peak voltage detect. Short this pin to pin 32 (QCOMP2).
38	BB_IN		**Single stage solution:** Input voltage to buck (DC-DC) and inverter. Connect to USB Type-C connector's VBUS pin. If EMI filter/choke and consumer FET is used after Type-C connector, then connect it to output of the EMI filter/choke and consumer FET. **Dual stage solution:** Input voltage to buck-boost (DC-DC). Connect to USB Type-C connector's VBUS pin. If EMI filter/choke and consumer FET is used after Type-C connector, then connect it to output of the EMI filter/choke and consumer FET.
39	VBUS_IN		Input voltage feedback of buck (DC-DC). Connect to USB Type-C connector's VBUS pin. If EMI filter/choke and consumer FET is used after Type-C connector, then connect it to output of the EMI filter/choke and at the input of consumer FET.
40	ASK_N		Negative input of ASK voltage sensing signal input to internal amplifier.
41	ASK_P		Positive input of ASK voltage sensing signal input to internal amplifier.
42	ASK_TST		Float this pin if it is not used.
43	BST2_1		Bootstrap power supply for (inverter bank 2) inverter high side gate driver. Connect a capacitor (recommended value 0.1 µF) from this pin to SW2_1. Also, connect a Schottky diode from VDDD to BST2_1.
44	HG2_1		High-side gate driver for inverter FET (inverter bank 2). Connect to the inverter bank 2, high-side FET gate. Use a wide trace to minimize inductance of this connection.
45	SW2_1		Inverter switching node for inverter bank 2. Connect this pin to the inverter bank 2 switching node with a short and wide trace.
46	VBB_1		Inverter input voltage sense. Connect to inverter input voltage, after the current sense resistor. Use a dedicated (Kelvin) trace for this connection.
47	LG2_1		Low-side gate driver for inverter FET (inverter bank 2). Connect to the inverter bank 2 low side FET gate.
48	PVDD_1		Connect to VDDD pin. Connect bypass capacitors (recommended values 1 µF and 0.1 µF) as close to the IC as possible.
49	PGND_1		Ground for inverter gate driver. Connect directly to PCB ground plane and E-PAD. Connect all GND and PGND pins together.
50	LG1_1		Low-side gate driver for inverter FET (inverter bank 1). Connect to the inverter bank 1 low-side FET gate.
51	SW1_1		Inverter switching node for inverter bank 1. Connect this pin to the Inverter bank 1 switching node with a short and wide trace.
52	HG1_1		High-side gate driver for inverter FET (inverter bank 1). Connect to the inverter bank 1 high side FET gate.
53	BST1_1		Bootstrap power supply for (inverter bank 1) inverter high side gate driver. Connect a capacitor (recommended values 0.1 µF) from this pin to SW1_1. Also, connect a Schottky diode from VDDD to BST1_1.
54	DUN1/CSNI_1		Negative input of input current sense amplifier (CSA) for inverter. Float this pin if it is not used.
55	DNU2/CSPI_1		Positive input of input CSA for inverter. Float this pin if it is not used.

Table 1 WLC1150 pinouts *(continued)*

Pin #	Pin name	Pin function for 50W application firmware	Description
56	GPIO9/SCB3/SWD_DAT	SWD_DAT/GPIO9	Used for I2C/SWD register access or programming/configurable GPIO.
57	GPIO10/SCB3/SWD_CLK	SWD_CLK/GPIO10	Used for I2C/SCL register access or programming/configurable GPIO.
58	GPIO11/SCB3	TEMP_FB	Tx coil temperature measurement via thermistor monitoring for 50W application/configurable GPIO. Float this pin if it is not used.
59	GPIO12/SCB3	GPIO12	Configurable GPIO. Configure for FAN PWM or float this pin if it is not used.
60	GPIO13		Default used as input to external PWM logic circuit to enable/disable inverter half bridge operation. Float this pin if it is not used.
61	VIN		4.5 to 24 V input supply. Connect a decoupling capacitor (recommended value 0.1 µF) from this pin to GND close to this pin.
62	VCCD		1.8 V LDO output for Arm®-M0 power and 1.8 V references. Connect a decoupling capacitor (recommended value 0.1 µF) from this pin to ground. Not for external use or loading.
65	CSPI_0		Positive input of USB input CSA (DC-DC). Connect to the positive terminal of the input current sense resistor. Use a dedicated (Kelvin) connection.
66	CSNI_0		Negative input of USB input CSA (DC-DC). Connect to the negative terminal of the input current sense resistor. Use a dedicated (Kelvin) connection.
67	BST1_0		Bootstrap power supply for buck/buck-boost (DC-DC) high-side gate driver. Connect a capacitor (recommended value 0.1 µF) from this pin to SW1_0. Also, connect a Schottky diode from VDDD to BST1_0.
68	HG1_0		High-side gate driver output of buck/buck-boost converter (DC-DC bank 1). Connect to the buck high side FET gate. Use a wide trace to minimize inductance of this connection.
	EPAD		Exposed ground pad. Connect directly to ground plane and pins 34 and 64.

Refer **Figure 8** for single stage converter and **Figure 9** for double stage converter key pin mapping.

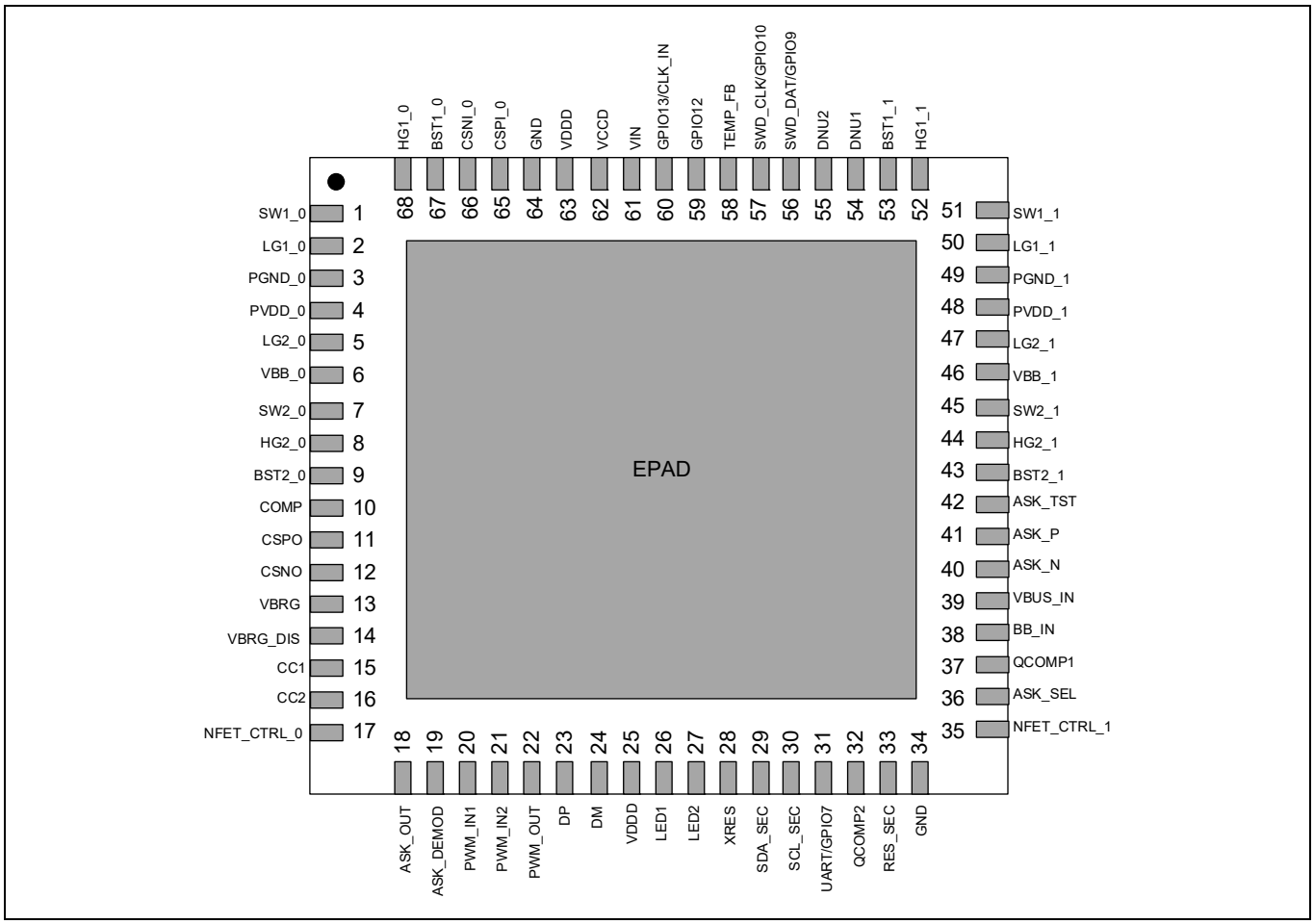


Figure 3 WLC1150 68-QFN pinout

4 Electrical specifications

4.1 Absolute maximum ratings

Table 2 Absolute maximum ratings[3]

Exceeding maximum ratings may shorten the useful life of the device.

All specifications are valid for -40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

Parameter	Description	Min	Typ	Max	Unit	Description
VIN	Maximum input supply voltage	–	–	40	V	–
VDDD, PVDD	Maximum supply voltage relative to VSS			6		
VBUS	Max VBRG_DIS (P0/P1) voltage relative to GND			24		
CC_0, ASK_SEL	Max voltage on CC and ASK_SEL pins			24		
QCOMP1	Max voltage on QCOMP1 pins	–0.7		24		Current limited to 1mA for -0.7V minimum specification.
QCOMP2	Input to QCOMP2	–0.7		VDDD + 0.5		
GPIO	Inputs to GPIO	–0.5		VDDD + 0.5		–
IGPIO	Maximum current per GPIO	–25		25	mA	
IGPIO_INJECTION	GPIO injection current, Max for VIH > VDDD, and Min for VIL < GND	–0.5		0.5		Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge (ESD) human body model (HBM)	2000		–	V	Applicable for all pins except CC1_0, CC2_0, ASK_SEL, QCOMP1 pins.
ESD_HBM_CC	ESDHBM for CC1 and CC2 pins for both ports	1100				Only applicable to CC1_0, CC2_0, ASK_SEL, QCOMP1 pins
ESD_CDM	ESD charged device model	500				Charged device model ESD
LU	Pin current for latch-up	–100		100	mA	–
TJ	Junction temperature	–40		125	°C	

Note

3. Usage above the absolute maximum conditions listed in **Table 2** may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, high temperature storage life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 3 Pin based absolute maximum ratings

Pin#	Pin name	Pin function for 50W application firmware	Absolute minimum (V)	Absolute maximum (V)
1	SW1_0		-0.7	35
2	LG1_0[4]		-0.5	PVDD+0.5
3	PGND_0		-0.3	0.3
4	PVDD_0			VDD
5	LG2_0[4]		-0.5	PVDD+0.5
6	VBB_0		-0.3	24
7	SW2_0			
8	HG2_0 (w.r.t SW2_0)[4, 5]		-0.5	PVDD+0.5
9	BST2_0 (w.r.t SW2_0)[4, 5, 6]		0	
10	COMP[4]		-0.5	
11	CSPO		-0.3	24
12	CSNO			
13	VBRG			
14	VBRG_DIS			
15	CC1		-0.5	
16	CC2			
17	NFET_CTRL_0			32
18	ASK_OUT[4]			PVDD+0.5
19	ASK_DEMOD[4]			
20	GD_OVR_HB_1[4]	PWM_IN1		
21	GD_OVR_HB_2[4]	PWM_IN2		
22	PWM_OUT[4]			
23	DP/GPIO1[4]	DP		
24	DM/GPIO2[4]	DM		
25, 63	VDDD		-0.3	6
26	GPIO3[4]	LED1	-0.5	PVDD+0.5
27	GPIO4[4]	LED2		
28	XRES[4]			
29	GPIO5/SCB0[4]	SDA_SEC		
30	GPIO6/SCB0[4]	SCL_SEC		
31	GPIO7/SCB1[4]	UART/GPIO7		
32	QCOMP2[4, 7]		-0.7	
33	GPIO8[4]	RES_SEC	-0.5	
34,64	GND		-0.3	0.3
35	NFET_CTRL_1		-0.5	32
36	ASK_SEL			24
37	QCOMP1[7]		-0.7	

Notes
4. Maximum voltage cannot exceed 6 V.
5. Maximum absolute voltage w.r.t GND must not exceed 40 V.
6. Minimum absolute voltage w.r.t GND must not be lower than -0.3 V.
7. Current limited to 1 mA for -0.7 V minimum specification only.

Table 3 Pin based absolute maximum ratings *(continued)*

Pin#	Pin name	Pin function for 50W application firmware	Absolute minimum (V)	Absolute maximum (V)
38	BB_IN		-0.3	24
39	VBUS_IN			
40	ASK_N			
41	ASK_P			
42	ASK_TST[4]		-0.5	PVDD+0.5
43	BST2_1 (w.r.t SW2_1)[4, 5, 6]		0	
44	HG2_1 (w.r.t SW2_1)[4, 5]		-0.5	
45	SW2_1		-0.7	24
46	VBB_1		-0.3	24
47	LG2_1[4]		-0.5	PVDD+0.5
48	PVDD_1		-0.3	VDDD
49	PGND_1		-0.3	0.3
50	LG1_1[4]		-0.5	PVDD+0.5
51	SW1_1		-0.7	35
52	HG1_1 (w.r.t SW1_1)[4, 5]		-0.5	PVDD+0.5
53	BST1_1 (w.r.t SW1_1)[4, 5, 6]		0	
54	CSNI_1	DNU1	-0.3	40
55	CSPI_1	DNU2		
56	GPIO9/SCB3/SWD_DAT[4]	SWD_DAT/GPIO9	-0.5	PVDD+0.5
57	GPIO10/SCB3/SWD_CLK[4]	SWD_CLK/GPIO10		
58	GPIO11/SCB3[4]	TEMP_FB		
59	GPIO12/SCB3[4]	GPIO12		
60	GPIO13/CLK_IN[4]	GPIO13/CLK_IN		
61	VIN		-0.3	40
62	VCCD			2
65	CSPI_0			40
66	CSNI_0			
67	BST1_0 (w.r.t SW1_0)[4, 5, 6]		0	PVDD+0.5
68	HG1_0 (w.r.t SW1_0)[4, 5]		-0.5	
	EPAD		-0.3	0.3

Notes
4. Maximum voltage cannot exceed 6 V.
5. Maximum absolute voltage w.r.t GND must not exceed 40 V.
6. Minimum absolute voltage w.r.t GND must not be lower than -0.3 V.
7. Current limited to 1 mA for -0.7 V minimum specification only.

4.2 Device-level specifications

All specifications are valid for -40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

4.3 DC specifications

Table 4 DC specifications (Operating conditions)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR#1	VIN	Input supply voltage	4.5	20	24	V	With fixed PD supply
SID.PWR#2	VDDD	VDDD output voltage range	4.6	–	5.5		5.5 V < VINS < 24 V; Max load = 150 mA
SID.PWR#3	VDDD_MIN	VDDD dropout voltage	VIN - 0.2	–	–		4.5 V < VIN < 5.5 V; Max load = 20 mA
SID.PWR#20	VBRG	VBRG_0 output range	3.3	5	21.5		VIN > VBRG
SID.PWR#5	VCCD	VCCD output voltage	–	1.8	–		–
SID.PWR#25	IDD_ACT48M	Operating quiescent current at 0.4 MHz switching frequency	–	87	–	mA	TA = 25°C, VIN = 12 V. CC IO in Transmit or Receive, no I/O sourcing current, No VCONN load current, CPU at 48 MHz, buck and inverter ON, 3-nF gate driver capacitance.

4.3.1 CPU

Table 5 CPU specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CLK#4	FCPU	CPU input frequency	–	44	48	MHz	–
SYS.XRES#5	TXRES	External reset pulse width	5	–	–	µs	
SYS.FES#1	T_PWR_RDY	Power-up to “Ready to accept I^2C/CC command”	–	5	25	ms	

4.3.2 GPIO

All specifications are valid for -40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

Table 6 GPIO specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
GPIO DC specifications							
SID.GIO#9	V_{IH_CMOS}	Input voltage HIGH threshold	0.7 × VDDD	–	–	V	CMOS input
SID.GIO#10	V_{IL_CMOS}	Input voltage LOW threshold	–		0.3 × VDDD		
SID.GIO#7	V_{OH}	Output voltage HIGH level	VDDD – 0.6		–		IOH = –4 mA
SID.GIO#8	V_{OL}	Output voltage LOW level	–		0.6		IOL = 10 mA
SID.GIO#2	Rpu	Pull-up resistor when enabled	3.5	5.6	8.5	kΩ	–
SID.GIO#3	Rpd	Pull-down resistor when enabled	3.5	5.6	8.5		
SID.GIO#4	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	TA = 25°C, VDDD = 3 V
SID.GIO#5	C_{PIN_A}	Max pin capacitance			22	pF	Capacitance on DP, DM pins
SID.GIO#6	C_{PIN}	Max pin capacitance		3	7		–40°C < TA < +105°C, All VDDD, all other I/Os
SID.GIO#13	V_{HYSTTL}	Input hysteresis, LVTTL, VDDD > 2.7V	100	–	–	mV	VDDD > 2.7 V
SID.GIO#14	$V_{HYSCMOS}$	Input hysteresis CMOS	0.1 × VDDD				–
GPIO AC specifications							
SID.GIO#16	T_{RISEF}	Rise time in Fast Strong mode	2	–	12	ns	Cload = 25 pF
SID.GIO#17	T_{FALLF}	Fall time in Fast Strong mode	2		12		
SID.GIO#18	T_{RISES}	Rise time in Slow Strong mode	10		60		
SID.GIO#19	T_{FALLS}	Fall time in Slow Strong mode	10		60		
SID.GIO#20	F_{GPIO_OUT1}	GPIO FOUT; 3.0 V ≤ VDDD ≤ 5.5 V. Fast Strong mode.	–		16	MHz	
SID.GIO#21	F_{GPIO_OUT2}	GPIO FOUT; 3.0 V ≤ VDDD ≤ 5.5 V. Slow Strong mode.			7		
SID.GIO#22	F_{GPIO_IN}	GPIO input operating frequency; 3.0 V ≤ VDDD ≤ 5.5 V.		44	48		-40°C ≤ TA ≤ +105°C
GPIO OVT DC specifications							
SID.GPIO_20VT_GIO#4	GPIO_20VT_I_LU	GPIO_20VT latch up current limits	–140	–	140	mA	Max / min current in to any input or output, pin-to-pin, pin-to-supply

Table 6 GPIO specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.GPIO_20VT_ GIO#5	GPIO_20VT_RPU	GPIO_20VT pull-up resistor value	3.5		8.5	kΩ	–40°C ≤ TA ≤ +105°C, All VDDD
SID.GPIO_20VT_ GIO#6	GPIO_20VT_RPD	GPIO_20VT pull-down resistor value	3.5		8.5		–40°C ≤ TA ≤ +105°C, All VDDD
SID.GPIO_20VT _GIO#16	GPIO_20VT_IIL	GPIO_20VT input leakage current (absolute value)	–		2	nA	+25°C TA, 3 V VDDD
SID.GPIO_20VT _GIO#17	GPIO_20VT_CPIN	GPIO_20VT pin capacitance			10	pF	–40°C ≤ TA ≤ +105°C, All VDDD
SID.GPIO_20VT _GIO#33	GPIO_20VT_Voh	GPIO_20VT output voltage high level	VDDD - 0.6	–	–	V	IOH = -4 mA
SID.GPIO_20VT _GIO#36	GPIO_20VT_Vol	GPIO_20VT output voltage low level	–		0.6		IOL = 8 mA
SID.GPIO_20VT _GIO#41	GPIO_20VT_Vih_ LV TTL	GPIO_20VT LVTTL input	2		–		–40°C ≤ TA ≤ +105°C, All VDDD
SID.GPIO_20VT _GIO#42	GPIO_20VT_Vil_ LV TTL	GPIO_20VT LVTTL input	–		0.8		–40°C ≤ TA ≤ +105°C, All VDDD
SID.GPIO_20VT _GIO#43	GPIO_20VT_ Vhysttl	GPIO_20VT input hysteresis LVTTL	100		–	mV	–40°C ≤ TA ≤ +105°C, All VDDD
SID.GPIO_20VT _GIO#45	GPIO_20VT_ ITOT_G PIO	GPIO_20VT maximum total sink pin current to ground	–		95	mA	V (GPIO_20VT Pin) > VDDDs
GPIO OVT AC specifications							
SID.GPIO_20VT_70	GPIO_20VT_TriseF	GPIO_20VT Rise time in Fast Strong Mode	1	–	15	ns	All VDDD, Cload = 25 pF
SID.GPIO_20VT_71	GPIO_20VT_TfallF	GPIO_20VT Fall time in Fast Strong Mode	1		15		
SID.GPIO_20VT_ GIO#46	GPIO_20VT_ TriseS	GPIO_20VT Rise time in Slow Strong Mode	10		70		
SID.GPIO_20VT_ GIO#47	GPIO_20VT_TfallS	GPIO_20VT Fall time in Slow Strong Mode	10		70		
SID.GPIO_20VT_ GIO#48	GPIO_20VT_FGPIO _OUT1	GPIO_20VT GPIO Fout; 3 V ≤ VDDD ≤ 5.5 V. Fast Strong mode.	–		33	MHz	
SID.GPIO_20VT_ GIO #50	GPIO_20VT_FGPIO _OUT3	GPIO_20VT GPIO Fout; 3 V ≤ VDDD ≤ 5.5 V. Slow Strong mode.			7		
SID.GPIO_20VT_ GIO #52	GPIO_20VT_FGPIO _IN	GPIO_20VT GPIO input operating frequency; 3 V ≤ VDDD ≤ 5.5 V			8		All VDDD

4.3.3 XRES and POR

All specifications are valid for -40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

Table 7 XRES specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
XRES DC specifications							
SID.XRES#1	V_{IH_XRES}	Input voltage HIGH threshold on XRES pin	0.7 × VDDD	–	–	V	CMOS input
SID.XRES#2	V_{IL_XRES}	Input voltage LOW threshold on XRES pin	–		0.3 × VDDD		
SID.XRES#3	C_{IN_XRES}	Input capacitance on XRES pin			7	pF	–
SID.XRES#4	$V_{HYSXRES}$	Input voltage hysteresis on XRES pin		0.05 × VDDD	–	mV	
Imprecise POR (IPOR) specifications							
SID185	$V_{RISEIPOR}$	POR rising trip voltage	0.80	–	1.50	V	-40°C < TA < +105°C, all VDDD
SID186	$V_{FALLIPOR}$	POR falling trip voltage	0.70		1.4		
Precise POR (POR) specifications							
SID190	$V_{FALLPPOR}$	Brown-out detect (BOD) trip voltage in active/sleep modes	1.48	–	1.62	V	-40°C < TA < +105°C, all VDDD
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep mode	1.1		1.5		

4.4 Digital peripherals

All specifications are valid for -40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

The following specifications apply to the Timer/counter/PWM peripherals in the Timer mode.

4.4.1 Inverter pulse-width modulation (PWM) for GPIO pins

Table 8 PWM AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.TCPWM.1	PWM_OUT	Operating frequency	170	–	300	kHz	PWM_OUT pin[8]
SID.TCPWM.3	T_{PWMEXT}	Output trigger pulse width	2/Fc		–	ns	Minimum possible width of overflow, underflow, and CC (counter equals compare value) outputs. Fc = System clock.

Note

8. PWM_OUT signal is of double the inverter switching frequency. Refer **"Inverter and duty cycle control"** on page 32.

4.4.2 I²C, UART, SWD interface

Table 9 Communication interface specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
Fixed I²C AC specifications							
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–
Fixed UART AC specifications							
SID16	F_{UART}	Bit rate	–	–	1	Mbps	–
SWD interface specifications							
SID.SWD#1	F_SWDCLK1	3.0 V ≤ VDDIO ≤ 5.5 V	–	–	14	MHz	–
SID.SWD#2	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
SID.SWD#3	T_SWDI_HOLD		0.25 × T		–		
SID.SWD#4	T_SWDO_VALID		–		0.50 × T		
SID.SWD#5	T_SWDO_HOLD		1		–		

4.4.3 Memory

Table 10 Flash AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.MEM#2	FLASH_WRITE	Row (block) write time (erase and program)	–	–	20	ms	–
SID.MEM#1	FLASH_ERASE	Row erase time			15.5		
SID.MEM#5	FLASH_ROW_PGM	Row program time after erase			7		
SID178	$T_{BULKERASE}$	Bulk erase time (32 KB)			35		
SID180	$T_{DEVPROG}$	Total device program time			7.5	s	
SID.MEM#6	$FLASH_{ENPB}$	Flash write endurance	100k		–	cycles	25°C < T_A < 55°C
SID182	F_{RET1}	Flash retention, T_A < 55°C, 100K P/E cycles	20			years	–
SID182A	F_{RET2}	Flash retention, T_A < 85°C, 10K P/E cycles	10				

4.5 System resources

All specifications are valid for -40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

4.5.1 Internal main oscillator clock

Table 11 IMO AC, clock specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
IMO AC specifications							
SID.CLK#13	F_{IMOTOL}	Frequency variation at 44 MHz (trimmed)	–2	–	+2	%	3.0 V < VDDD < 5.5 V
SID226	$T_{STARTIMO}$	IMO start-up time	–		7	µs	–
SID.CLK#1	F_{IMO}	IMO frequency		44	–	MHz	

4.5.2 USB PD

Table 12 USB PD DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.DC.cc_shvt.1	vSwing	Transmitter output high voltage	1.05	–	1.2	V	–
SID.DC.cc_shvt.2	vSwing_low	Transmitter output low voltage	–		0.075		
SID.DC.cc_shvt.3	zDriver	Transmitter output impedance	33		75	Ω	
SID.DC.cc_shvt.4	zBmcRx	Receiver input impedance	10		–	MΩ	
SID.DC.cc_shvt.8	Rd	Pull down termination resistance when acting as UFP	4.59		5.61	kΩ	
SID.DC.cc_shvt.10	zOPEN	CC impedance to ground when disabled	108		–		
SID.DC.cc_shvt.15	UFP_default_0 p66	CC voltages on UFP side-standard USB	0.61		0.7	V	
SID.DC.cc_shvt.16	UFP_1.5A_1p23	CC voltages on UFP side-1.5A	1.16		1.31		
SID.DC.cc_shvt.17	Vattach_ds	Deep Sleep attach threshold	0.3		0.6	%	
SID.DC.cc_shvt.18	Rattach_ds	Deep Sleep pull-up resistor	10		50	kΩ	
SID.DC.cc_shvt.19	VTX_step	TX drive voltage step size	80		120	mV	

4.5.3 ADC

All specifications are valid for -40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

Table 13 ADC DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	Bits	–
SID.ADC.2	INL	Integral non-linearity	-1.5	–	1.5	LSB	Reference voltage generated from bandgap
SID.ADC.3	DNL	Differential non-linearity	-2.5		2.5		Reference voltage generated from VDDD
SID.ADC.4	Gain Error	Gain error	-1.5		1.5		Reference voltage generated from bandgap
SID.ADC.5	VREF_ADC1	Reference voltage of ADC	VDDDmin		VDDDmax	V	Reference voltage generated from VDDD
SID.ADC.6	VREF_ADC2	Reference voltage of ADC	1.96	2.0	2.04		Reference voltage generated from deep sleep reference

4.5.4 Current sense amplifier (CSA) / ASK amplifier (ASK_P and ASK_N)

Table 14 CSA/ASK amplifier specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
HS CSA DC specifications							
SID.HSCSA.7	Csa_SCP_Acc1	CSA short circuit protection (SCP) at 6A with 5/10mΩ sense resistor	-10	–	10	%	Active mode
SID.HSCSA.8	Csa_SCP_Acc2	CSA SCP at 10A with 5/10mΩ sense resistor	-10		10		
SID.HSCSA.9	Csa_OCP_1A	CSA OCP at 1A with 5/10mΩ sense resistor	104	130	156		
SID.HSCSA.10	Csa_OCP_5A	CSA OCP for 5A with 5/10mΩ sense resistor	117	130	143		
SID.HSCSA.13	Csa_CBL_MON_Acc2	Vsense > 10mV	–	±3.5	–		CSA sense accuracy. Active mode. 3.0 V < VDDD < 5.5 V. T_A = 25°C.
CSA AC specifications							
SID.HSCSA.AC.1	T_{SCP_GATE}	Delay from SCP threshold trip to external NFET power gate turn off	–	3.5	–	µs	1 nF NFET gate
SID.HSCSA.AC.2	$T_{SCP\_GATE\_1}$	Delay from SCP threshold trip to external NFET power gate turn off		8			3 nF NFET gate

4.5.5 VIN UV/OV

All specifications are valid for -40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

Table 15 VIN UV/OV specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.UVOV.1	VTHOV1	Overvoltage threshold accuracy, 4 V - 11 V	-3	–	3	%	Active mode
SID.UVOV.2	VTHOV2	Overvoltage threshold accuracy, 11 V - 21.5 V	-3.2		3.2		
SID.UVOV.3	VTHUV1	Undervoltage threshold accuracy, 3 V - 3.3 V	-4		4		
SID.UVOV.4	VTHUV2	Undervoltage threshold accuracy, 3.3 V - 4.0 V	-3.5		3.5		
SID.UVOV.5	VTHUV3	Undervoltage threshold accuracy, 4.0 V - 21.5 V	-3		3		

4.5.6 Voltage regulation - VBRG

Table 16 VBRG specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
VBRG discharge specifications							
SID.VBUS.DISC.1	R_DIS1	20V NMOS ON resistance for DS = 1	500	–	2000	Ω	Measured at 0.5V
SID. VBUS.DISC.2	R_DIS 2	20V NMOS ON resistance for DS = 2	250		1000		
SID. VBUS.DISC.3	R_DIS 4	20V NMOS ON resistance for DS = 4	125		500		
SID. VBUS.DISC.4	R_DIS 8	20V NMOS ON resistance for DS = 8	62.5		250		
SID. VBUS DISC.5	R_DIS 16	20V NMOS ON resistance for DS = 16	31.25		125		
SID. VBUS.DISC.6	VBRG_stop_error	Error percentage of final VBRG value from setting	–		10	%	When VBRG is discharged to 5V
Voltage regulation DC specifications							
SID.DC.VR.1	VBB	VBB output voltage range	3.3	–	21.5	V	–
SID.DC.VR.3	VIN_UVLO	VIN supply below which chip will get reset	1.7	–	3.0		
SID.VREG.1	TSTART	Total startup time for the regulator supply outputs	–		200	µs	Specification for VDDD LDO

4.5.7 NFET gate driver specifications

All specifications are valid for -40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

Table 17 NFET gate driver specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
NFET gate driver DC specifications							
SID.GD.1	GD_VGS	Gate to source overdrive during ON condition	4.5	5	10	V	NFET driver is ON
SID.GD.2	GD_RPD	Resistance when pull-down enabled	–	–	2	kΩ	Applicable on NFET_CTRL to turn off external NFET.
NFET gate driver AC specifications							
SID.GD.3	T_{ON}	NFET_CTRL Low to High (1 V to VBUS + 1 V) with 3 nF external capacitance.	2	5	10	ms	VBUS = 5V
SID.GD.4	T_{OFF}	NFET_CTRL High to Low (90% to 10%) with 3 nF external capacitance.	–	7	–	µs	VBUS = 21.5V

4.5.8 PWM controller

Table 18 PWM controller specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
PWM controller specifications							
PWM.1	FSW	Buck/buck-boost switching frequency	150	–	600	kHz	–
GD1	Fsw Gd Ovr	Inverter switching frequency	85	–	150		Pins PWM_IN1 and PWM_IN2 are connected to pin PWM_OUT.
PWM.2	FSS	Spread spectrum frequency dithering span-buck/buck-boost	–	10	–	%	–
Buck gate driver specifications							
DR.1	R_HS_PU	Top-side gate driver on-resistance - gate pull-up	–	2	–	Ω	–
DR.2	R_HS_PD	Top-side gate driver on-resistance - gate pull-down		1.5			
DR.3	R_LS_PU	Bottom-side gate driver on-resistance - gate pull-up		2			
DR.4	R_LS_PD	Bottom-side gate driver on-resistance - gate pull-down		1.5			
DR.5	Dead_HS	Dead time before high-side rising edge		30		ns	
DR.6	Dead_LS	Dead time before low-side rising edge		30			
DR.7	Tr_HS	Top-side gate driver rise time		25			
DR.8	Tf_HS	Top-side gate driver fall time		20			
NFET gate driver specifications							
DR.9	Tr_LS	Bottom-side gate driver rise time	–	25	–	ns	–
DR.10	Tf_LS	Bottom-side gate driver fall time		20			

4.5.9 Thermal

All specifications are valid for -40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

Table 19 Thermal specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.OTP.1	OTP	Thermal shutdown	120	125	130	°C	–

5 Functional overview

5.1 Wireless power transmitter

WLC1150 supports wireless power transfer between power transmitter (TX) and power receiver (RX), based on inductive power transfer technology (IPT). The Tx runs an alternating electrical current through the Tx coil(s) to generate an alternating magnetic field in accordance with Faraday's law. This magnetic field is mutually coupled to the Rx coil inside the power receiver and is transformed back into an alternating electrical current that is rectified and stored on a Vrect capacitor bank to power the Rx load.

Before the power transfer begins, the Rx and Tx communicate with each other to establish that a valid Rx device has been placed and they negotiate the level of power to be transferred during the charging cycle. The digital communication used by Tx and Rx is in-band communication. The communication from Tx to Rx is frequency shift key (FSK) modulation and from Rx to Tx is amplitude shift key (ASK) modulation. The WLC1150 solution is for 50W charging application and compatible with Qi v1.3.x standard up to 15W. The WLC1150 operates with the Infineon high power proprietary protocol for wireless power transfer of more than 15W and up to 50W. This includes ready to use firmware stack with a robust demodulation scheme for continuous power transfer and reliable FOD to ensure safety. WLC1150 firmware stack comes with a high level of configurable options to enable IC configuration based on application using the configuration utility tool.

5.2 Infineon high power proprietary protocol operation and protocol

The WLC1150 supports up to 50W power levels using the Infineon high power proprietary protocol enabled Rx and 15W and 5W with Qi EPP and BPP enabled Rx respectively. When using the Infineon high power proprietary protocol, the USB PD adapter needs to have sufficient power delivery capabilities to overcome any system losses caused by operation or misalignment and the Rx power requirements. To enable 50W power transfer, both Tx and Rx must support the Infineon high power proprietary protocol.

The Tx will connect to the Rx (BPP or EPP) in the identical method prescribed by the WPC specification. The Infineon high power proprietary protocol is Infineon’s proprietary extension of WPC Qi protocol. In the configuration of WPC operation, Tx detects the Infineon high power proprietary protocol enabled Rx continues with negotiation phase, where Tx and Rx enters in high power contract and delivers up to 50W. If Tx does not detect the Infineon high power proprietary protocol enabled Rx in configuration phase, Tx enters into Qi defined mode and limits the power accordingly.

5.3 Wireless charging system control

WLC1150 supports up to 50W power levels using the Infineon high power proprietary protocol and 15W power as per Qi v1.3.x. The section describes the Qi 1.3.x system operation.

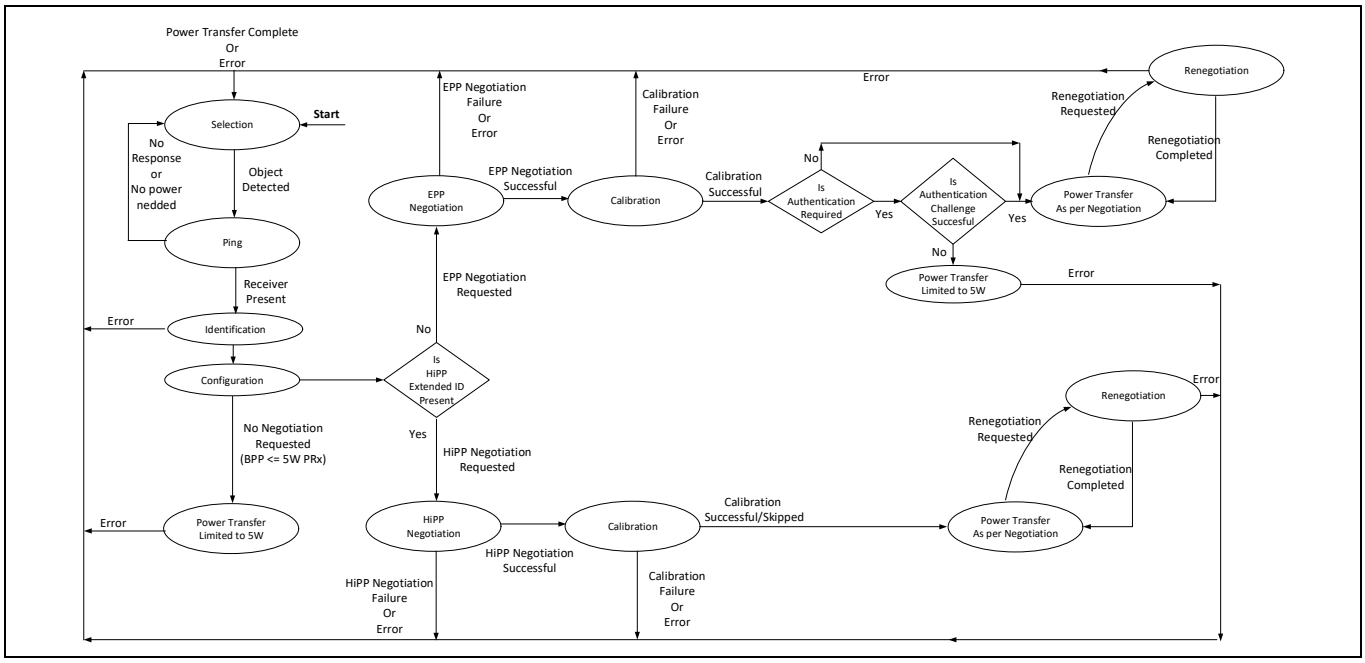


Figure 4 Tx system control flow chart with Qi and the Infineon high power proprietary protocol Rx[9]

5.3.1 Selection phase

The Tx monitors the interface surface using low energy signals (analog ping or Q-factor) to detect objects' placement and removal. The Analog Ping energy is limited such that impedance changes above the Tx coil may be detected without powering or waking up the receiver. The WLC1150 contract PD with 5 V and powering the inverter as half-bridge to generate sufficient energy to measure for any interface impedance changes without transferring any power during the selection phase.

5.3.2 Digital ping phase

In this phase, the Tx sends a power signal that is sufficient to power the receiver and prompt a response. This signal is called Digital Ping and the magnitude and length of time are predefined by the WPC Tx specifications. The Digital Ping phase ends when no response is detected or the Rx responds with a signal strength packet (SSP). When the Tx receives a valid SSP, the Digital Ping is extended and the system proceeds to the Identification and Configuration phase.

Note

9. The **Functional overview** section only describes the Qi specification. However, IC can support wireless charging proprietary power delivery extensions (PPDE)/Samsung FC.

5.3.3 Identification and configuration phase

In this phase, the Tx identifies whether the Rx belongs to BPP, EPP, or the Infineon high power proprietary protocol profile. Additionally, in this phase, the Tx obtains configuration information such as the maximum amount of power that the Rx may require at its output. The power transmitter uses this information to create a Power Transfer Contract.

If the receiver is a BPP type then the power transmitter enters into the power transfer phase at the completion of the identification and configuration phase as shown in **Figure 4**, or with EPP/Infineon high power proprietary protocol receivers it proceeds to the negotiation phase if requested by the Rx.

5.3.4 Negotiation

In this phase, the EPP and the Infineon high power proprietary protocol power receiver negotiates with the power transmitter to fine-tune the power transfer contract. For this purpose, the power receiver sends negotiation requests to the power transmitter, which the power transmitter can grant or deny.

In compliance with Q-factor FOD, the Tx will compare the Q-factor and resonance frequency reported by the Rx with its own measurement to determine if the Q-factor and resonance frequency of the coil is appropriate for the Rx that has been placed (EPP/Infineon high power proprietary protocol only). If the Tx Q-factor reading is too low it will flag a QFOD alarm and return to the selection phase.

5.3.5 Calibration

When this phase is requested, the Tx will ACK the request and commence with the EPP/Infineon high power proprietary protocol Rx to enable and enter the calibration phase to calibrate for transmitter power losses at two fixed receiver loads i.e., light load and connected load. This system's power loss information will be used by the Tx to detect the presence of foreign objects on the interface surface during the power delivery phase. In Infineon high power prosperity protocol, the calibration might be skipped if the light and connected are of similar values.

5.3.6 Authentication

Post successful calibration, Tx enters into power transfer mode limited to 5W. In this mode, Rx can request and challenge Tx for authentication. In case of successful authentication, Tx proceeds with negotiated power delivery. If authentication challenge is not successful then Tx continues to be in power transfer mode, limited to 5W. WLC1150 provides an I^2C port for interfacing with OPTGA™ Trust Charge IC to enable authentication.

5.3.7 Renegotiation phase

In this phase, the EPP/Infineon high power proprietary protocol Rx can request to adjust the power transfer contract. This phase may be aborted prematurely without changing the power transfer contract.

5.3.8 Power transfer phase

In this phase, the Tx transfers power to the Rx and the power level is determined by the control error packets (CEP) and limited by the guaranteed power contract. Power loss FOD is also enabled and utilized to prevent excessive power loss which could result in FO heating.

1. CEP: These packets are used by the Tx to adjust the amount of power being sent. The CEP may be positive, negative, or 0. The Tx adjusts its operating point based on the value of the CEP. The CEP packet must be received every 1.8s (configurable) or power will be withdrawn along with other constraints that specify when a CEP may be sent by the Rx as defined in the WPC specifications.
2. Received power packet (RPP): The packet (8 bits for BPP and 24 bits for EPP and the Infineon high power proprietary protocol) contains power received by receiver. The RPP is used by the Tx to determine if the power loss is safe or excessive based on the FOD thresholds contained in the FW.
3. End power transmit (EPT): The Rx may send an EPT packet anytime to inform Tx to withdraw/terminate the power delivery. The Tx will end the power transfer immediately if an EPT packet is received.

The Rx and Tx communicate with each other by modulating the carrier wave used to transfer power. The following sections describe the communication layer used and defined by the WPC.

5.3.9 Bidirectional in-band communication interface

The Qi standard requires bi-directional in-band communication between Tx and Rx. The communication from Tx to Rx is FSK and is implemented by the Tx alternating the carrier wave frequency. The communication from Rx to Tx is ASK and is created by modulating the load on the Rx side causing a reflection to appear on the Tx which is filtered and decoded.

5.4 Communication from Tx to Rx - FSK

The power transmitter communicates to the power receiver using frequency shift keying, in which the power transmitter modulates the operating frequency of the power signal.

In FSK, the Tx changes its operating frequency between the current operating frequency (f_{OP}) to an alternate frequency (f_{MOD}) in the modulated state. The difference between these two frequencies is characterized by two parameters that are determined during the initial ID and config stage of the wireless power connection:

- Polarity: This parameter determines whether the difference between f_{MOD} and f_{OP} is positive or negative.
- Depth: This parameter determines the magnitude of the difference between f_{OP} and f_{MOD} in Hertz (Hz).

The Tx uses a differential bi-phase encoding scheme to modulate data bits to the carrier wave. For this purpose, the Tx aligns each data bit to segments of 512 cycles of the carrier wave frequency.

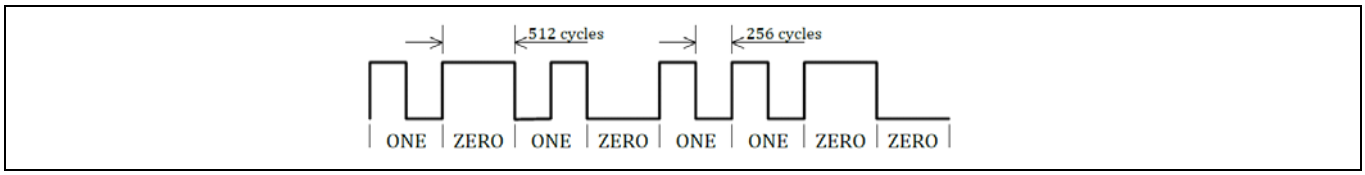


Figure 5 Example of differential bi-phase encoding - FSK

5.5 Communication from Rx to Tx - ASK

In the ASK communication scheme, the Rx modulates the amount of power that it draws from the Tx power signal. The Tx detects this through as a modulation of the Tx current and/or voltage and uses a demodulation scheme to convert the modulated signal into a binary signal.

The Rx shall use a differential bi-phase encoding scheme to modulate data bits onto the power signal. For this purpose, the power receiver shall align each data bit to a full period t_{CLK} of an internal clock signal, such that the start of a data bit coincides with the rising edge of the clock signal. This internal clock (INTCLK) signal shall have a frequency fCLK = 2 kHz ±4%. tCLK is time period of the INTCLK clock.

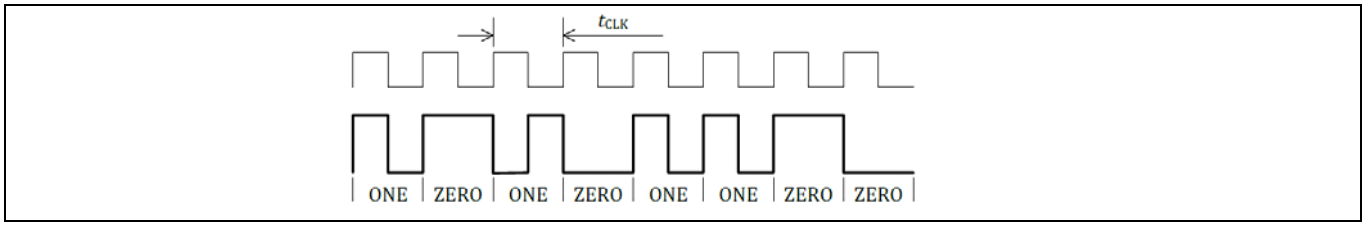


Figure 6 Example of differential bi-phase encoding - ASK

When the Tx receives a modulated signal from the Rx the information is decoded and the Tx will react to the packet according to the type and the WPC specification.

5.6 Demodulation

The WLC1150 ASK demodulating and decoding scheme works by detecting voltage and current variations in the Tx coil caused by the Rx modulation signal. The voltage path for ASK uses an external band pass filter to filter the demod signal out of the carrier wave. The current sense uses the bridge current sense resistor and an integrated differential amplifier to sense the ASK variations. Both ASK sensing paths can be multiplexed to the external Opamp filter and comparator to improve communication in low signal-to-noise environments or conditions.

Figure 7 shows the demodulation path used for current and voltage sensing of the modulation signal for packet decoding.

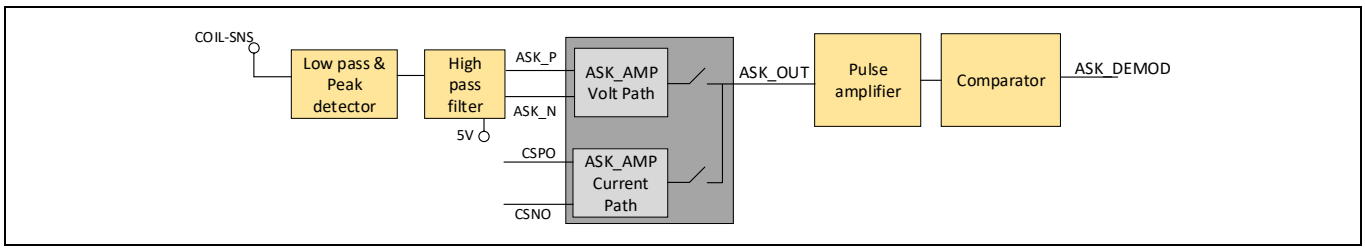


Figure 7 WLC1150 voltage and current demodulation path for ASK

5.7 Input power

The WLC1150 supports three different types of input power. **Table 20** suggests a typical solution configuration which can be used with each input power type.

Table 20 Input power type vs solution configuration

Input power type	Typical configuration
Type-C USB PD	Single stage solution
DC input voltage 20 V	Single stage solution
Variable DC input voltage	Double stage solution

The WLC1150 works with Type-C USB PD and DC 20V input without requiring a front-end converter, i.e system input power, providing power to inverter. Since, this configuration eliminates front end converter, this configuration offers higher efficiency and lower BOM count. The power train diagram below shows these to configuration. **Figure 8** describes the system diagram for PD and 20 V input.

For application, with variable DC input voltage, requires a front-end converter to regulate the VBRG voltage of the system. The WLC1150 offers integrated buck-boost controller and gate driver to enable the front converter as buck-boost converter which can work with input voltage from 5 V to 20 V. The buck-boost converter is followed by inverter, powering the wireless transmitter coil. **Figure 9** describes the system diagram for DC input voltage.

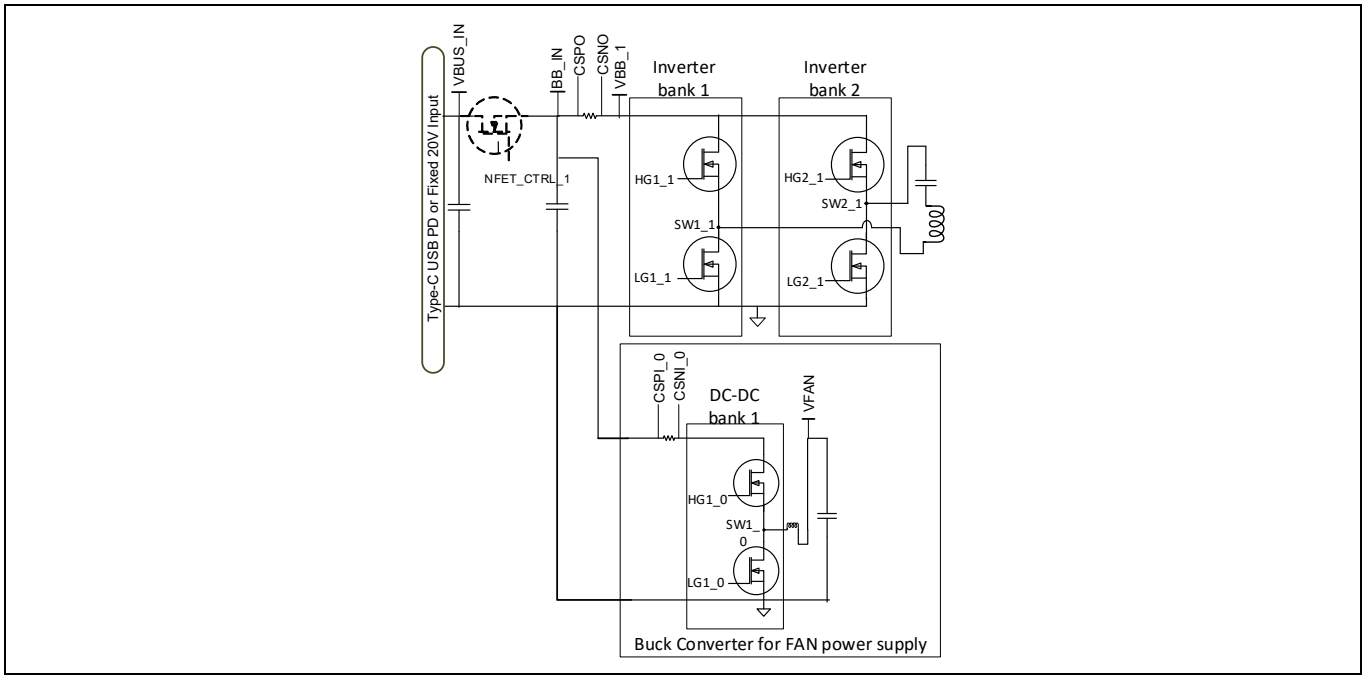


Figure 8 WLC1150 system diagram for PD and 20 V input (single stage solution)

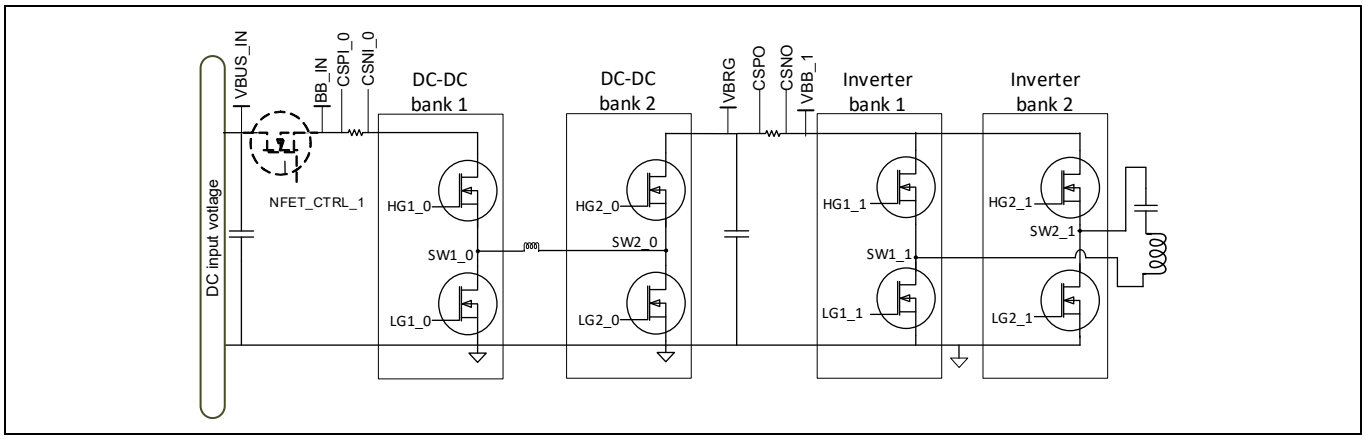


Figure 9 WLC1150 system diagram for DC input voltage (dual stage solution)

5.8 Inverter and duty cycle control

The WLC1150 contract with PD as 5 V / 9 V /15 V /20 V depending on receiver type (BPP, EPP, or the Infineon high power proprietary protocol) to power the full-bridge inverter that powers the Tx resonance tank to deliver power to the Rx. The integrated gate drivers of the WLC1150 are designed to control a full bridge or half-bridge inverter depending on the WPC specification type and operating scenario.

The inverter typically operates at switching frequencies between 110 to 148 kHz. During the power transfer phase, the inverter responds to Rx CEP packets by adjusting the operating frequency or duty cycle.

The WLC1150 requires an external logic circuit to enable duty cycle control. The PMW_OUT pin of the IC is input signal to the logic circuit. The logic circuit detects the edge (rising and falling edge) of PWM_OUT signal to derive the PWM signals, PWM_IN1 and PWM_IN2, which is input to the WLC1150. These signal are used by IC for generating the gate signals LG1_1, HG1_1, LG2_1, HG2_1 for full bridge inverter and LG1_1 and HG1_1 for half bridge inverter.

The duty cycle of PWM_OUT governs the phase difference (θ) between HG1_1 and HG2_1 and thus governs the duty cycle for the full bridge inverter control.

The logic circuit requires additional input to enable duty cycle control for the half bridge inverter i.e HB_EN. This signal is active HIGH and enable LG1_1 and HG1_1 as gate driver for half bridge inverter. The duty cycle of PWM_OUT governs the duty cycle of the inverter. The output of logic circuit PMW_IN1 follows the PWM_OUT. The WLC1150 uses PWM_IN1 for generating LG1_1 and HG1_1 gate driver signals for half bridge inverter.

The input and output waveforms for logic circuit along with high side gate driver signals (HG1_1 and H2_1) are described in **Figure 10**. The low side gate driver signals (LG1_1 and LG2_1) will be complementary of corresponding leg high side gate driver signals.

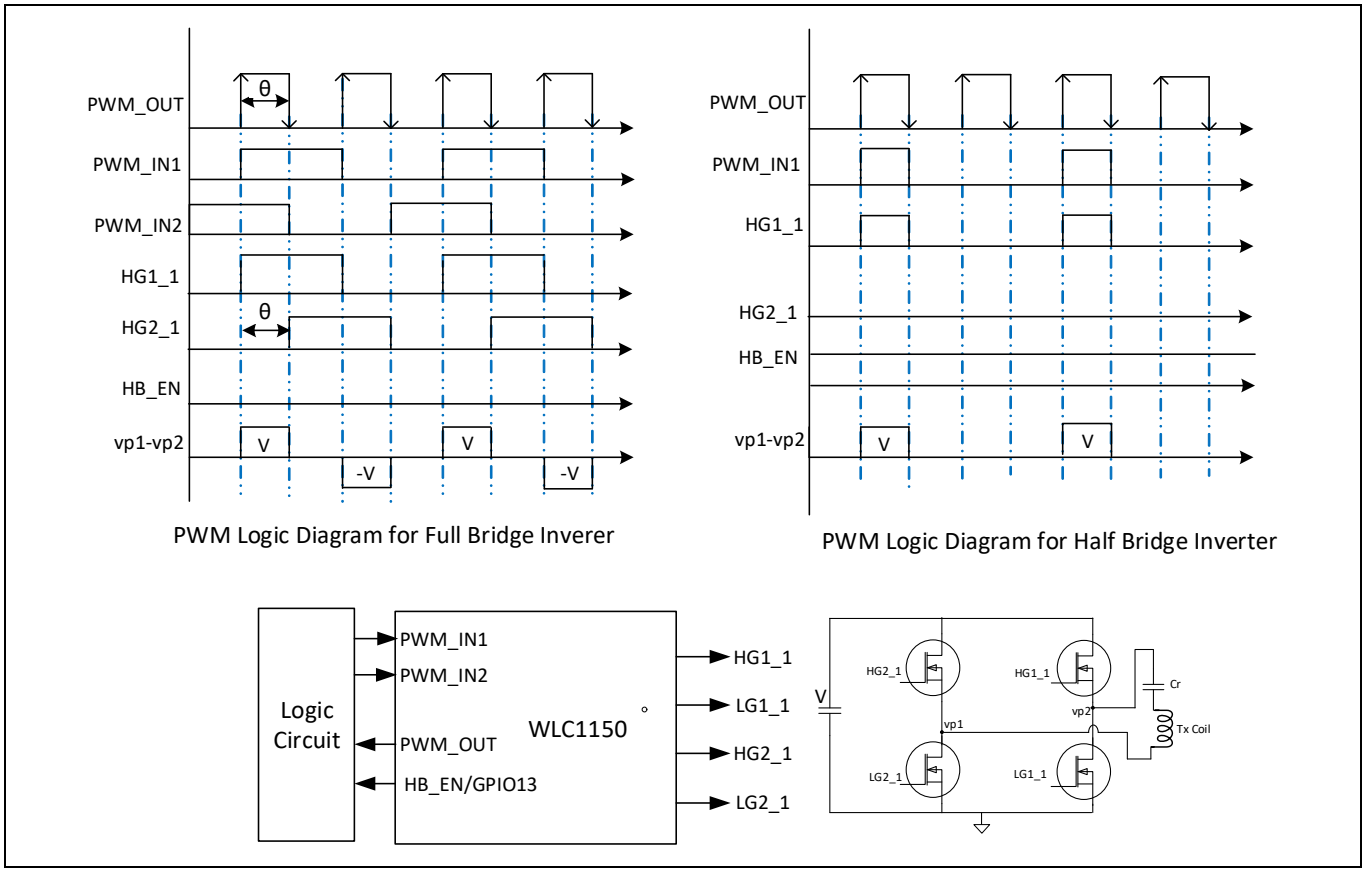


Figure 10 Duty cycle control for inverter

5.9 Rx detection

During the selection phase, the Tx will periodically poll the interface to detect impedance changes in order to quickly send a Digital Ping within 0.5s of a user placing an Rx. During this phase, the WLC1150 is able to distinguish between large ferrous objects (such as keys or coins) and regular Rx devices using Q factor or shifts in resonance frequency to attempt FOD before power transfer. In case of marginally change in Q factor, the Tx will commence to Digital Ping in order to guarantee a connection with a valid Rx is made in a timely manner.

Figure 11 describes the process used during the selection phase for quick Rx detection and connection.

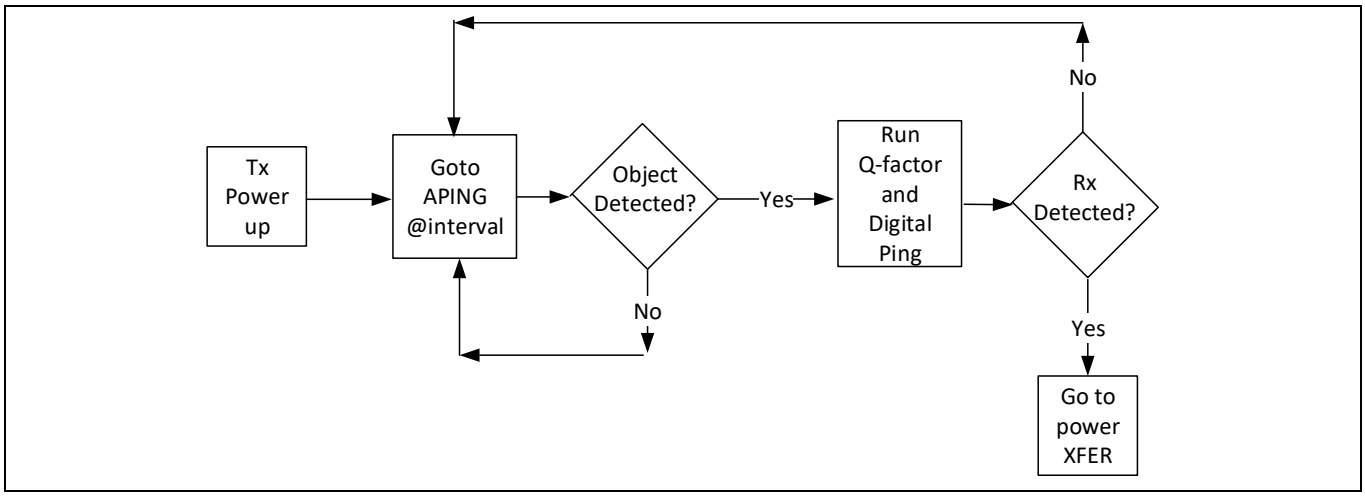


Figure 11 Typical selection phase flow chart for Rx detection and connection

The Rx detection in **Figure 11** also covers foreign object detection. The foreign object is identified by using Q factor. In case of foreign object detection, the process flow proceeds to analog ping (APNG). Further details about foreign object detection is covered in **"Foreign object detection (FOD)"** on page 33.

5.9.1 Foreign object detection (FOD)

WLC1150 supports enhanced FOD as per Qi v1.3.x standard. This includes FOD based on Q factor, resonance frequency, power loss, and over temperature (if a thermistor is used).

5.9.2 Q factor FOD and resonance frequency FOD

WLC1150 offers integrated Q factor and resonance frequency measurements for QFOD pre-power delivery. The measurements are made using the internal comparators QCOMP1 and QCOMP2 and the simple external components to charge the resonance capacitor and then discharge by shorting the LC tank and observing the resulting oscillation and voltage decay. The measurement of the Q factor is performed directly before every digital ping. Alternatively, to save quiescent system power, digital ping can be performed only when objected by Q factor measurement. The number of cycle count 'N' between two coil voltages V1 and V2 and period between corresponding rising edge pulses are used for Q factor and resonance frequency measurement as shown in **Figure 12**.

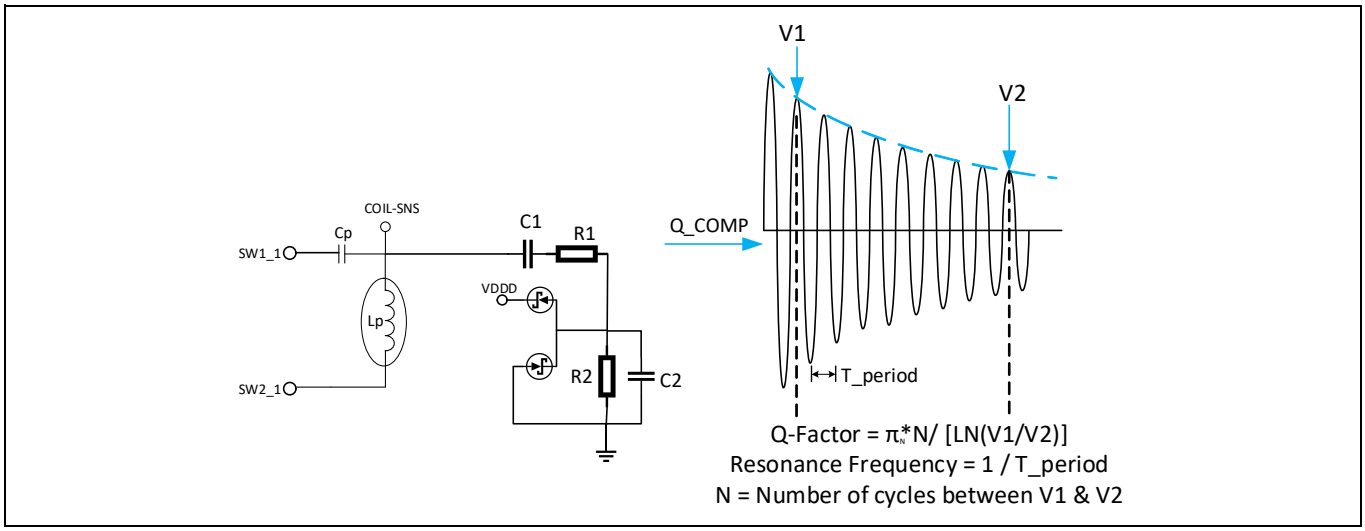


Figure 12 WLC1150 Q factor measurement schematic and signal

5.9.3 Power loss FOD

WLC1150 supports power loss FOD during power transfer. The power loss FOD uses the Tx power measured at the input and is the product of the inverter input voltage and the inverter current (current is sensed at inputs CSPO_0 and CSNO_0). This result for Tx power is further adjusted by tuning FOD coefficients to account for inverter losses and friendly metal losses. After computing the calibrated Tx power the result is compared against the latest RPP value sent by the Rx. If the difference between Tx_Power_Calibrated and RPP exceeds the Ploss threshold then an FOD event is logged. To prevent erroneous disconnects and improve user experience the WLC1150 will only disconnect the power for Ploss FOD in the event that three consecutive Ploss threshold breaches occur. The FOD coefficients and the Ploss thresholds are configurable to adapt to the system design. The calibration feature when utilized with two-point loading of the Rx will be used to further enhance and improve the accuracy of FO detection.

5.9.4 Over temperature FOD

The WLC1150 is able to monitor interface temperature if an external NTC thermistor is connected and placed in contact with the Tx coil. This can be enabled to disconnect the Tx from the Rx in the event that the Tx coil temperature exceeds a configurable threshold.

5.10 Buck/buck-boost regulators

5.10.1 Buck regulator

WLC1150 offers integrated controller for buck/buck-boost converter. Based on the need of application either buck or buck-boost configuration can be used.

The buck converter, powered from Tx input (PD or DC input of 20 V) can be used for fan power supply and for powering and WLC1150. Thus, it eliminates the need for an external switching power supply for fan.

The buck-boost converter can be used as front end converter for application where input to wireless transmitter is power supply with wide variation i.e 5V to 20V. The buck boost converter provides a desired stable input voltage to inverter.

The WLC1150's buck controller provides two N-channel MOSFET gate drivers: complete with a floating high-side gate driver via HG1_0 and a ground-referenced low-side driver via LG1_0 pins. Similarly for buck-boost controller provides 4 N-channel MOSFET gate drivers, including two floating high side gate driver via HG1_0 and HG2_0.

The gate drivers are powered by VDDD and are a nominal voltage of 5 V. The buck/buck-boost controller switching frequency is programmable and can be set between 150 and 600 kHz. In order to prevent EMI related issue's gate drivers, have programmable drive strength, dead-time, and can be run in a dithering mode to spread the radiated spectrum energy levels. An external capacitor and Schottky diode from the BST1_0 pin & BST2_0 (only for buck-boost controller) are used for the high-side gate drive power supply.

Furthermore, the high- and low-side gate driver blocks include zero-crossing detector (ZCD) to implement discontinuous-conduction mode (DCM) mode with diode emulation.

The WLC1150 buck/buck-boost controller uses an integrated error amplifier for output voltage regulation. The error amplifier is a trans-conductance type amplifier with a single compensation pin (COMP_0) which requires the RC filter shown in the reference schematic to be connected from this pin to GND.

The WLC1150 supports high-voltage (22 V) VBRG discharge circuitry and upon detection of device disconnection, faults, or hard resets, the chip may discharge the VBRG node.

Maintain equivalent amount of capacitance on input and output as shown in **Figure 13** in order to maintain stable operation based on compensation values.

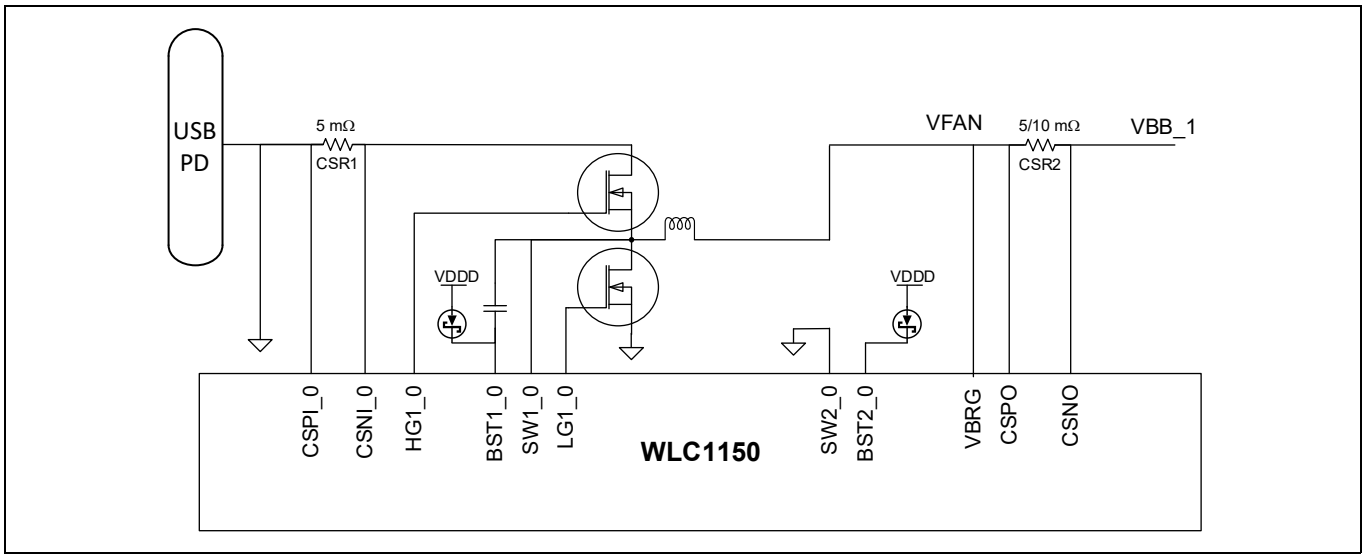


Figure 13 WLC1150 typical buck regulator schematic

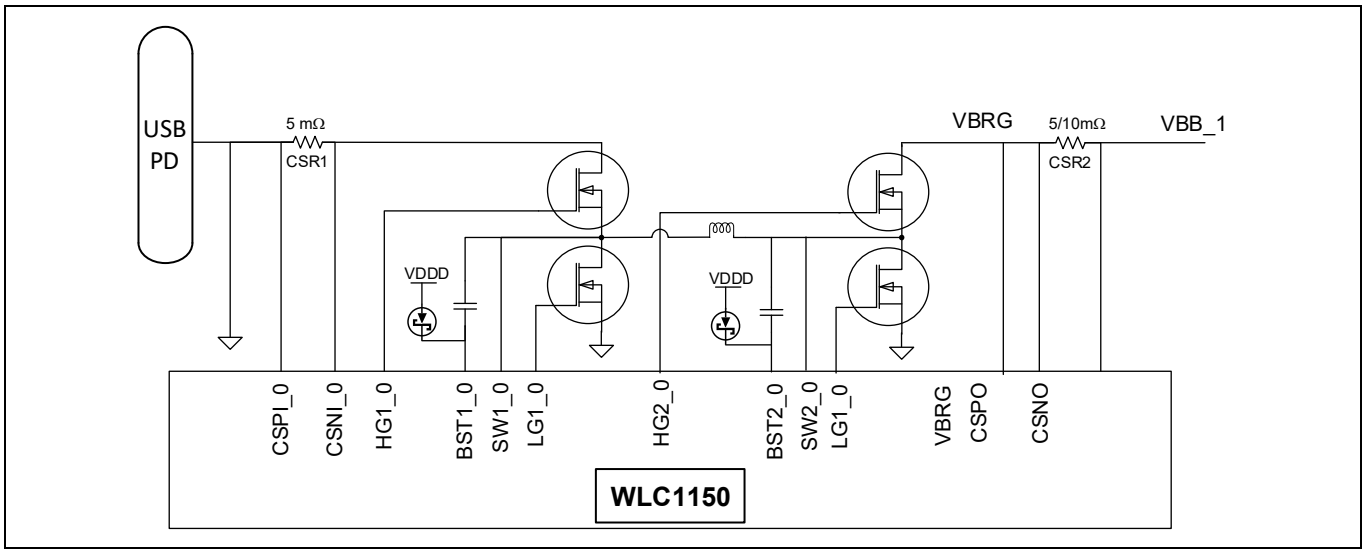


Figure 14 WLC1150 typical buck-boost converter schematic

5.11 Buck/buck-boost operating modes

5.11.1 Pulse-width modulator (PWM)

WLC1150 generates the control signals for the gate drivers driving the external FETs in peak current mode control. WLC1150 has two firmware-selectable operating modes to optimize efficiency and reduce losses under light load conditions: pulse-skipping mode (PSM) and forced-continuous-conduction mode (FCCM).

5.11.2 Pulse-skipping mode (PSM)

In PSM, the controller reduces the total number of switching pulses without reducing the active switching frequency by working in “bursts” of normal nominal-frequency switching interspersed with intervals without switching. The output voltage thus increases during a switching burst and decreases during a quiet interval. This mode results in minimal losses with a tradeoff of having higher output voltage ripple. When in this mode, WLC1150 devices monitor the voltage across the buck/buck-boost sync FET to detect when the inductor current reaches zero; when this occurs, the WLC1150 devices switch off the buck/buck-boost sync FET to prevent reverse current flow from the output capacitors (i.e. diode emulation mode).

5.11.3 Forced-continuous-conduction mode (FCCM)

In forced-continuous-conduction mode (FCCM), the nominal switching frequency is maintained at all times, with the inductor current going below zero (i.e. “backwards” or from the output to the input) for a portion of the switching cycle as necessary to maintain the output voltage and current. This keeps the output voltage ripple to a minimum at the cost of light-load efficiency.

5.11.4 Overvoltage protection (OVP)

The WLC1150 offers two types of overvoltage protections. The device monitors and limits VIN and VBRG. In case of a USB VIN overvoltage event detected, WLC1150 can be configured to shutdown the Type-C port completely. In case of VBRG over voltage events, the buck/buck-boost regulator is immediately shut down. The IC can be re-enabled after a physical disconnect and reconnect. The over-voltage fault thresholds are configurable.

5.11.5 Overcurrent protection (OCP)

The WLC1150 protects the inverter from over-current and short-circuit faults by monitoring the input inverter current and continuously inspecting for over-current events using the internal CSAs that check the voltage on the current sense resistor. Similar to OVP, the OCP and SCP fault thresholds and response times are configurable as well. The IC can be re-enabled after a physical disconnect and reconnect.

5.11.6 USB PD controller

The WLC1150 interfaces directly to Type-C USB power supplies and USB PD/PPS adaptors. The WLC1150 manages the incoming power supply throughout operation using the D+, D-, and CC lines. The WLC1150 manages the USB-PD physical communication layer, the VCONN switches, as well as monitoring to prevent under-voltage events caused by drawing too much power from the supply. The WLC1150 offers all the necessary electrical controls to be fully compliant with revisions 3.1 and 2.0 of the USB-PD specification and includes SCP.

The USB-PD physical layer consists of the power transmitter and power receiver that communicates BMC encoded data over the CC channel per the PD 3.1 standard. All communication is half-duplex. The physical layer or PHY includes collision avoidance to minimize communication errors on the channel. The WLC1150 uses the RP and RD resistors to implement connection detection and plug orientation detection. The RD resistor establishes the role of the transmitter system as a USB sink. The device supports PPS operation at all valid voltages from 3V to 22V when connected to a power adaptor.

Further, the WLC1150 device supports USB-PD extended messages containing data of up to 260 bytes by implementing a chunking mechanism; messages are limited to revision 2.0 sizes unless both source and sink confirm and negotiate compatibility with longer message lengths.

The WLC1150 USB controller also supports battery charger emulation and detection (source and sink) for USB legacy QC 2.0/3.0 and AFC protocols.

5.11.7 MCU

The Cortex®-M0 in WLC1150 device is a 32-bit MCU, which is optimized for low-power operation with extensive clock gating. The device utilizes an interrupt controller (the NVIC block) with 32 interrupt inputs and a wakeup interrupt controller (WIC), which can wake the processor up from Deep Sleep mode. Additionally, the WLC1150 device has 128-KB Flash and 32-KB ROM for nonvolatile storage. ROM stores libraries for device drivers such as I^2C, SPI, and so on. The main wireless power firmware is stored in Flash memory to provide the flexibility to store code for all wireless power features, enable the use of configuration tables, and allow firmware upgrades to meet the latest USBPD specifications and application requirements. The device may be reset anytime by toggling the XRES pin to force a full hardware and software reset.

The TCPWM block of the WLC1150 device has four timers, counters, or PWM (TCPWM) generators. These timers are used by FW to run the wireless power Tx system as required by WPC and USB compliance directives. The WLC1150 device also has a watchdog timer (WDT) that can be used by FW for various timeout events.

5.11.8 ADC

The WLC1150 device has 8-bit SAR ADCs available for general purpose analog-to-digital conversion applications within the chip and system. The ADCs are accessed from the GPIOs or directly on power supply pins through an on-chip analog mux. See the **“Electrical specifications”** on page 13 for detailed specifications of the ADCs.

5.11.9 Serial communications block (SCB)

The WLC1150 devices have four SCB blocks that can be configured for I^2C, SPI, or UART. These blocks implement full multi-master and slave I^2C interfaces capable of multi-master arbitration. I^2C is compatible with the standard Philips I2C specification V3.0. These blocks operate at speeds of up to 1Mbps and have flexible buffering options to reduce interrupt overhead and latency for the CPU. The SCB blocks support 8-byte deep FIFOs for Receive and Transmit to decrease the time needed to interface by the MCU also reducing the need for clock stretching caused by the CPU not having read data on time.

5.11.10 I/O subsystem

The WLC1150 devices have 13 GPIOs but many of them have dedicated functions for 50W applications such as I2C comm, LED and temperature sensing in the wireless power application and cannot be re-purposed. The GPIOs output states have integrated controls modes that can be enabled by FW which include: weak pull-up with strong pull-down, strong pull-up with weak pull-down, open drain with strong pull-down, open drain with strong pull-up, strong pull-up with strong pull-down, disabled, or weak pull-up with weak pull-down and offer selectable slew rates for dV/dt output control. When GPIOs are used as inputs they can be configured to support different input thresholds (CMOS or LVTTL).

During POR, the GPIO blocks are forced to the disable state preventing any excess currents from flowing.

5.11.11 LDOs (VDDD and VCCD)

The WLC1150 has two integrated LDO regulators. The VDDD LDO is powered by VIN and provides 5 V for the GPIOs, gate drivers, and other internal blocks. The total load on VDDD LDO must be less than 150 mA including internal consumption. VDDD LDO will be externally loaded as shown in the reference schematic. For connecting any additional external load on it, contact Infineon technical support. The VDDD 5 V supply is externally routed to various pins and they should all be externally shorted together. The VCCD LDO is a 1.8 V LDO regulator and is powered by VDDD. Do not externally load VCCD. Both LDOs must have ceramic bypass capacitors placed from each pin to ground close to the WLC1150 device.

6 Programming the WLC1150 device

There are two ways to program application firmware into a WLC1150 device:

1. Programming the device flash over SWD Interface
2. Application firmware update over specific interfaces (CC, I^2C)

Generally, the WLC1150 devices are programmed over the SWD interface only during development or during the manufacturing process of the end-product. Once the end-product is manufactured, the WLC1150 device application firmware can be updated via the appropriate bootloader interface. Infineon strongly recommends customers to use the configuration utility to turn off the Application FW Update over CC or I^2C interface in the firmware that is updated into WLC1150's flash before mass production. This prevents unauthorized firmware from being updated over the CC interface in the field. If you desire to retain the application firmware update over CC/I^2C interfaces features post-production for on-field firmware updates, contact your local Infineon sales representative for further guidelines.

6.1 Programming the device Flash over SWD interface

The WLC1150 family of devices can be programmed using the SWD interface. Infineon provides the MiniProg4 programming kit (**CY8CKIT-005 MiniProg4 Kit**) which can be used to program the flash and debug firmware. The Flash is programmed by downloading the information from a *hex* file.

As shown in **Figure 15**, the SWD_DAT and SWD_CLK pins are connected to the host programmer's SWDIO (data) and SWDCLK (clock) pins respectively. During SWD programming, the device can be powered by the host programmer by connecting its VTARG (power supply to the target device) to the VDDD pins of the WLC1150 device. If the WLC1150 device is powered using an onboard power supply, it can be programmed using the "Reset Programming" option.

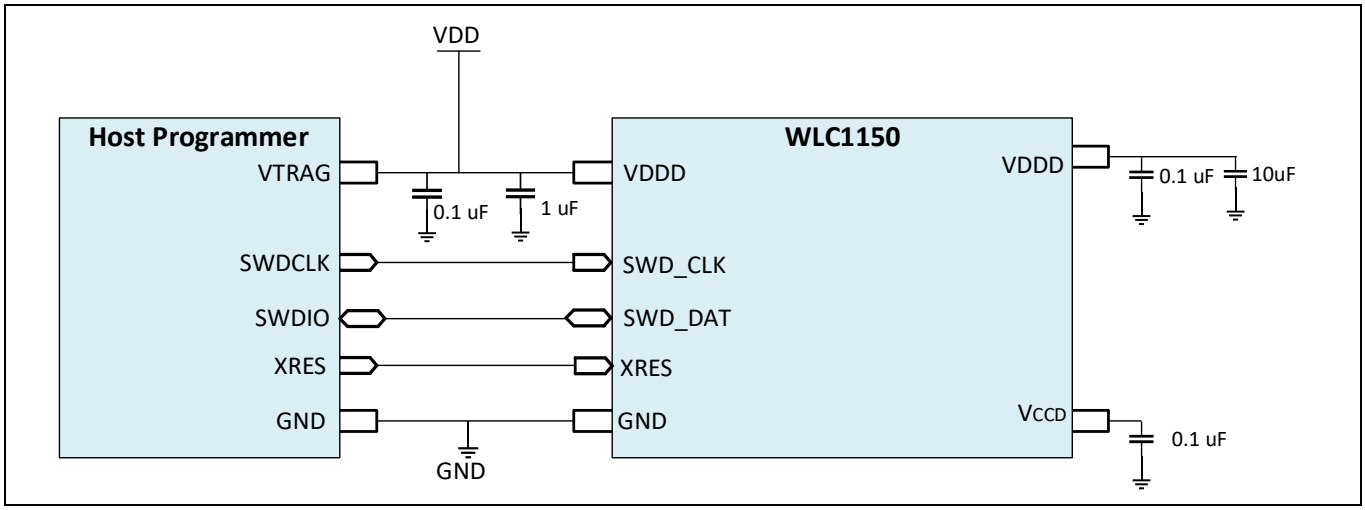


Figure 15 Connecting the programmer to WLC1150

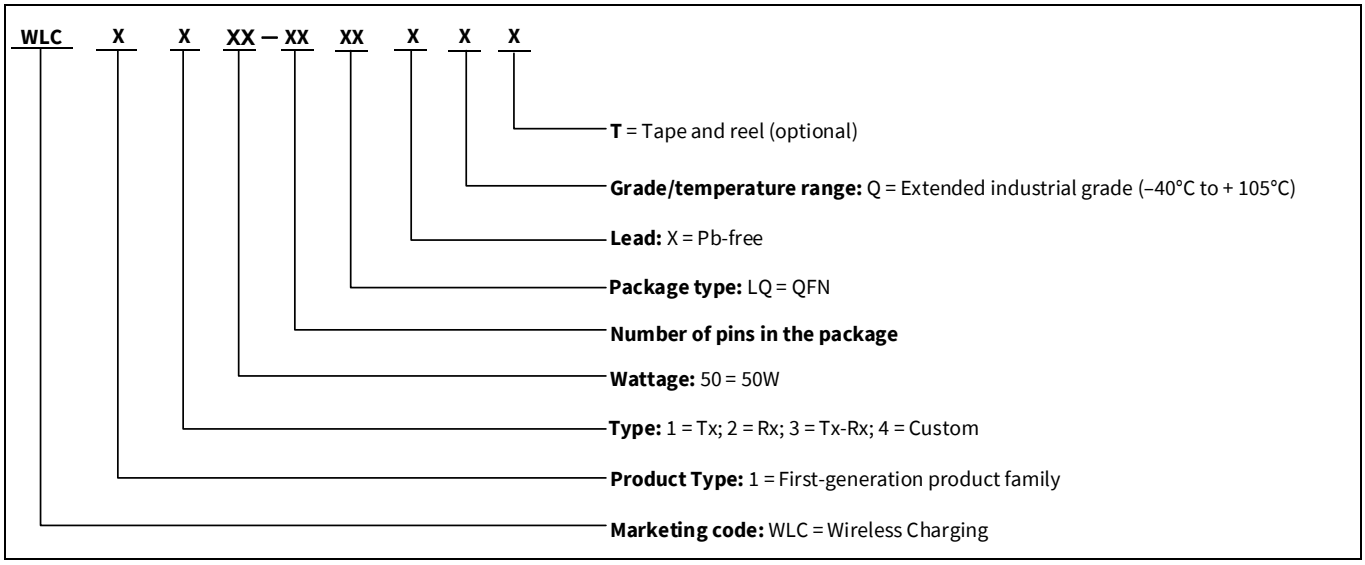
7 Ordering information

Table 21 lists the WLC1150 ordering part numbers and applications.

Table 21 WLC1150 ordering part numbers

MPN	Power	Application
WLC1150-68LQXQ	50W	Infineon high power proprietary protocol and Qi v1.3.x Tx
WLC1150-68LQXQT		Infineon high power proprietary protocol and Qi v1.3.x Tx - Tape and reel option

7.1 Ordering code definitions



8 Packaging

Table 22 Package characteristics

Parameter	Description	Test conditions	Min	Typ	Max	Unit
T_J	Operating junction temperature	–	-40	25	125	°C
T_{JA}	Package θJA		–	–	14.8	°C/W
T_{JB}	Package θJB				4.3	
T_{JC}	Package θJC				12.9	

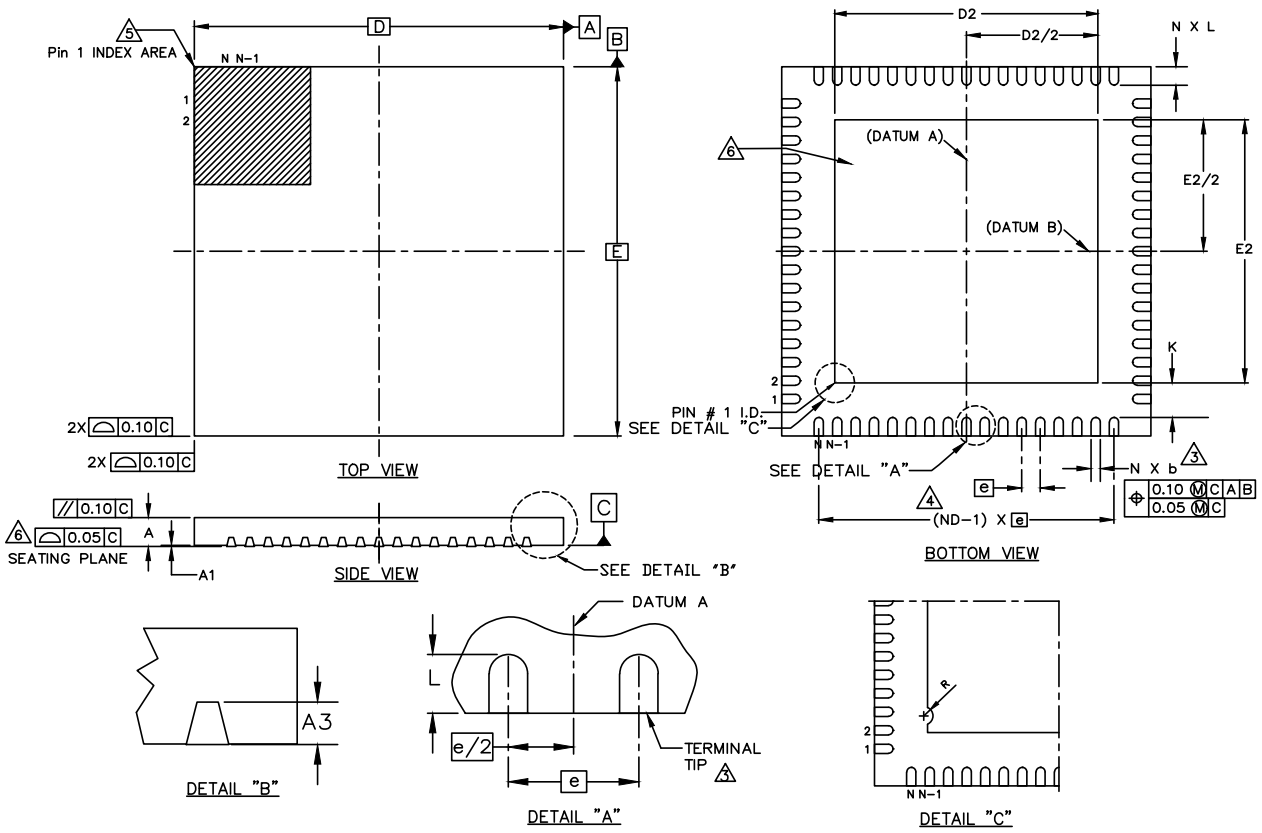
Table 23 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time within 5°C of peak temperature
68-pin QFN	260°C	30 seconds

Table 24 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

Package	MSL
68-pin QFN	MSL 3

9 Package diagram



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		0.40 BSC	
N		68	
ND		17	
L	0.30	0.40	0.50
b	0.15	0.20	0.25
D2	5.60	5.70	5.80
E2	5.60	5.70	5.80
D		8.00 BSC	
E		8.00 BSC	
A	-	-	0.65
A1	0.00	-	0.05
A3		0.203 REF	
R		0.20 TYP	
K		0.75 MIN	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF TERMINALS.
3. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
4. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
5. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
6. COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
7. JEDEC SPECIFICATION NO. REF. : N/A.

002-31802 *D

Figure 16 68LD QFN (8 × 8) device package drawing (PG-VQFN-68)

10 Acronyms

Table 25 Acronyms used in this document

Acronym	Description
ACK	Acknowledge
ADC	Analog-to-digital converter
Arm®	Advanced RISC machine, a CPU architecture
ASK	Amplitude shift key
BPP	Basic power profile
BMC	BiPhase mark code
CEP	Control error packet
CC	Configuration channel
CSA	Current sense amplifier
DCM	Discontinuous-conduction mode
EA	Error amplifier
EPP	Extended power profile
EPT	End power transfer
ESD	Electrostatic discharge
FET	Field effect transistor
FCCM	Forced-continuous-conduction mode
FOD	Foreign object detection
FO	Foreign object
FSK	Frequency shift key
FW	Firmware
GPIO	General-purpose I/O
HBM	Human body model
HS	High speed
I^2C	Inter-integrated circuit
IC	Integrated circuit
IMO	Internal main oscillator
IPT	Inductive power transfer technology
LDO	Linear drop out
MCU	Microcontroller unit
NTC	Negative temperature coefficient
NVIC	Nested vectored interrupt controller
OCP	Overcurrent protection
Opamp	Operational amplifier
OTP	Over temperature protection
OV	Overvoltage
OVP	Overvoltage protection
PCB	Printed circuit board
PD	Power delivery
POR	Power-on reset
PPDE	proprietary power delivery extensions
PPS	Programmable power supply

Table 25 Acronyms used in this document *(continued)*

Acronym	Description
PSM	Pulse-skipping mode
PWM	Pulse-width modulator
QFOD	Q factor FOD
RPP	Received power packet
RCP	Reverse current protection
Rx	Power receiver
SAR	Successive approximation register
SCP	Short circuit protection
SPI	Serial peripheral interface
SSP	Signal strength packet
SWD	Serial wire debug, a test protocol
TCPWM	Timer/counter pulse-width modulation
Tx	Power transmitter
UART	Universal asynchronous receiver transmitter
UFP	Upstream facing port
USB	Universal serial bus
UV	Undervoltage
WDT	Watchdog timer
WIC	Wakeup interrupt controller
WLC	Wireless charging IC
WPC	Wireless power consortium
ZCD	Zero-crossing detector

11 Document conventions

11.1 Units of measure

Table 26 Units of measure

Symbol	Unit of measure
°C	degree Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
LSB	least significant bit
MHz	megahertz
MΩ	mega-ohm
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
%	percent
pF	picofarad
s	second
V	volt
W	watt

Revision history

Document revision	Date	Description of changes
*A	2023-02-01	Release to web.
*B	2023-07-21	Updated Package diagram. Updated Note 1.

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erratum@infineon.com

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