PRELIMINARY

Am29240™EH, Am29245™EH, and Am29243™EH

Enhanced High-Performance RISC Microcontrollers

5/2/97

DISTINCTIVE CHARACTERISTICS

All three microcontrollers in the Am29240™EH microcontroller series have the following characteristics:

- **Completely integrated system for embedded applications**
- **Full 32-bit architecture**
- **4-Kbyte, two-way set-associative instruction cache**
- **4-Gbyte virtual address space, 304-Mbyte physical space implemented**
- **Glueless system interfaces with on-chip wait state control**
- **36 VAX MIPS (million instructions per second) sustained at 25 MHz**
- **Four banks of ROM, each separately programmable for 8-, 16-, or 32-bit interface**
- **Four banks of DRAM**
- **Single-cycle ROM burst-mode and DRAM page-mode access**
- **DRAM timing is software-programmable for 3/1 or 2/1 initial/burst access cycles**
- **6-port peripheral interface adapter**
- **16-line programmable I/O port**
- **Bidirectional parallel port controller**
- **Interrupt controller**
- **Fully pipelined integer unit**
- **Three-address instruction architecture**
- **192 general purpose registers**
- **Traceable Cache™ technology instruction and data cache tracing**
- **IEEE Std 1149.1-1990 (JTAG) compliant Standard Test Access Port and Boundary Scan Architecture**
- **Binary compatibility with all 29K™ family microprocessors and microcontrollers**
- **CMOS technology/TTL compatible**
- **208-pin Plastic Quad Flat Pack (PQFP) package**
- **3.3-V power supply with 5-V-tolerant I/O**

Am29240EH Microcontroller

The Am29240EH microcontroller has the following additional features:

- **2-Kbyte, two-way set-associative data cache**
- **Single-cycle 32-bit multiplier for faster integer math; two-cycle Multiply Accumulate (MAC) function**
- **16-entry on-chip Memory Management Unit (MMU) with one Translation Look-Aside Buffer**
- **4-channel double-buffered DMA controller with queued reload**
- **Two serial ports (UARTs)**
- **Bidirectional bit serializer/deserializer**
- **20- and 25-MHz operating frequencies**

Am29243EH Microcontroller

The Am29243™EH data microcontroller is similar to the Am29240EH microcontroller, without the video interface. It includes the following features:

- **2-Kbyte, two-way set-associative data cache**
- **Single-cycle 32-bit multiplier for faster integer math; two-cycle MAC**
- **32-entry on-chip MMU with dual TLBs**
- **4-channel, double-buffered DMA controller with queued reload**
- **Two serial ports (UARTs)**
- **20- and 25-MHz operating frequencies**
- **DRAM parity**

Am29245EH Microcontroller

The low-cost Am29245™EH microcontroller is similar to the Am29240EH microcontroller, without the data cache and 32-bit multiplier. It includes the following features:

- **16-entry on-chip MMU with one TLB**
- **Two-channel DMA controller**
- **One serial port (UART)**
- **Bidirectional bit serializer/deserializer**
- **16-MHz operating frequency**

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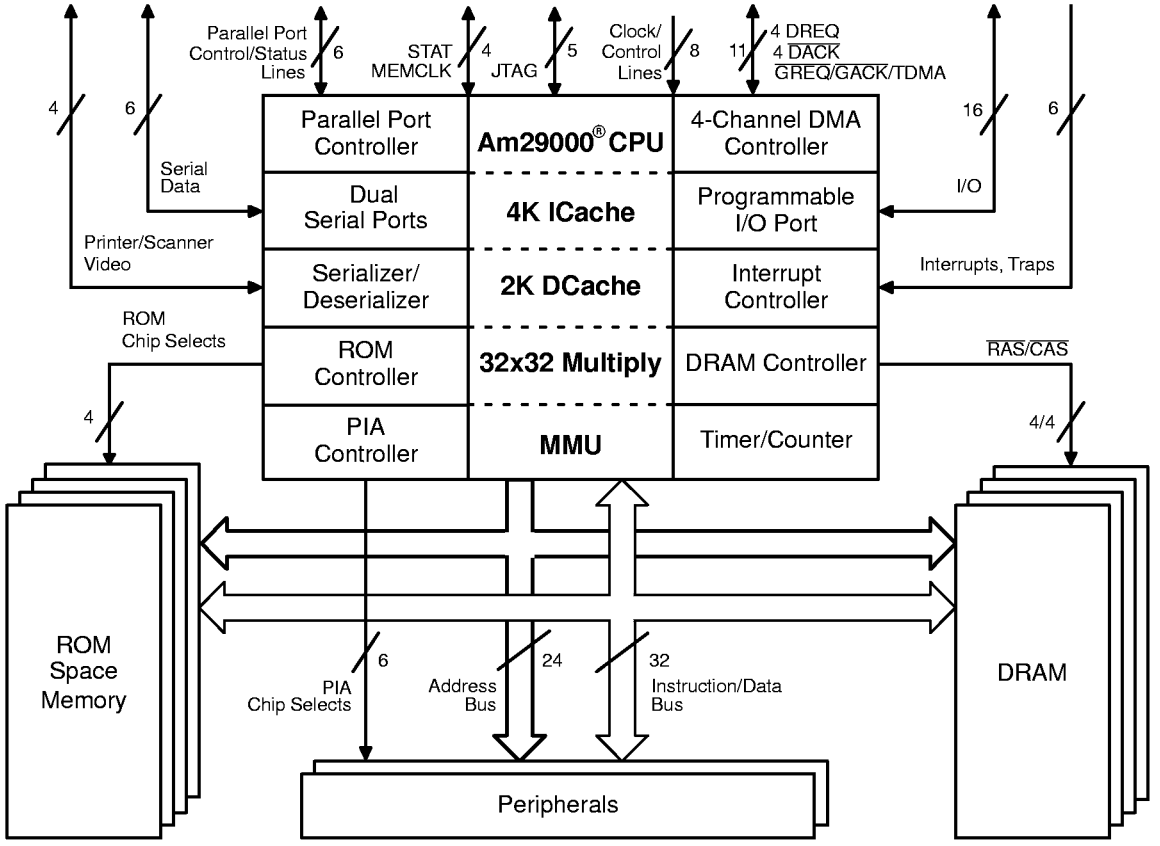
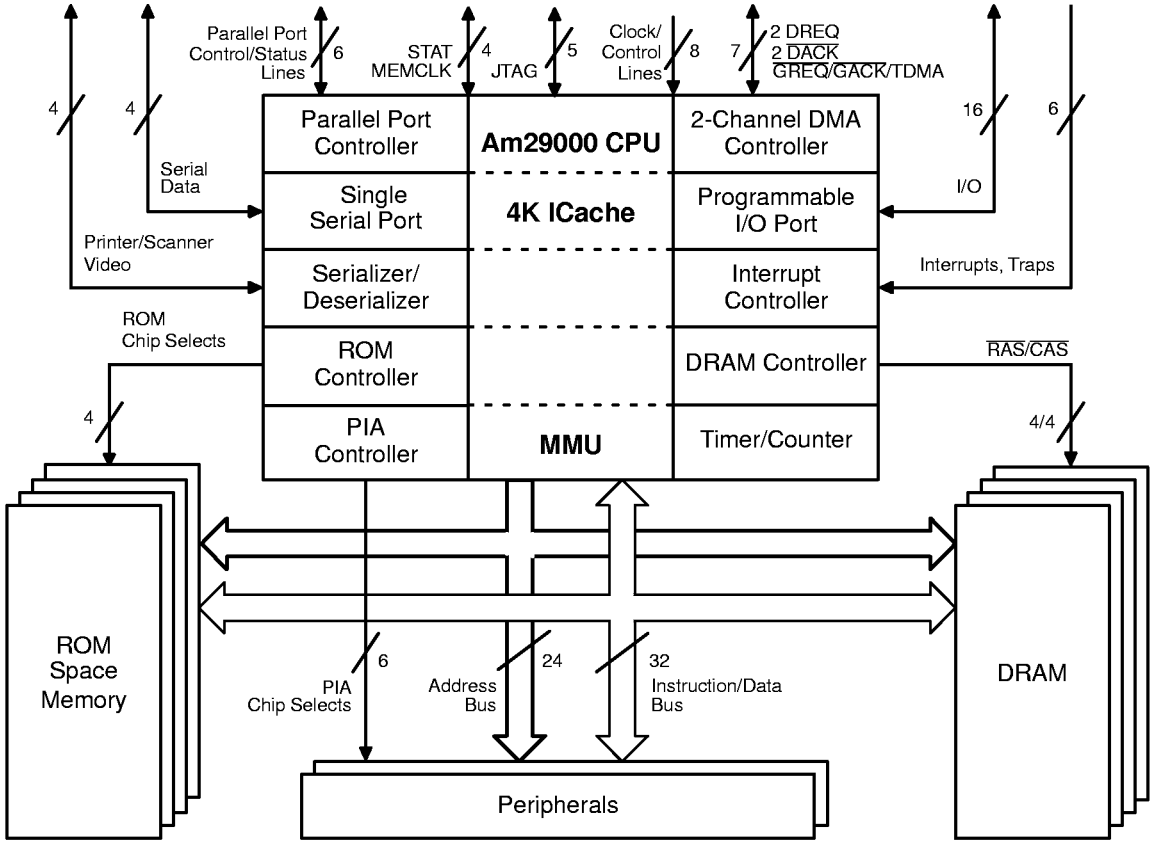
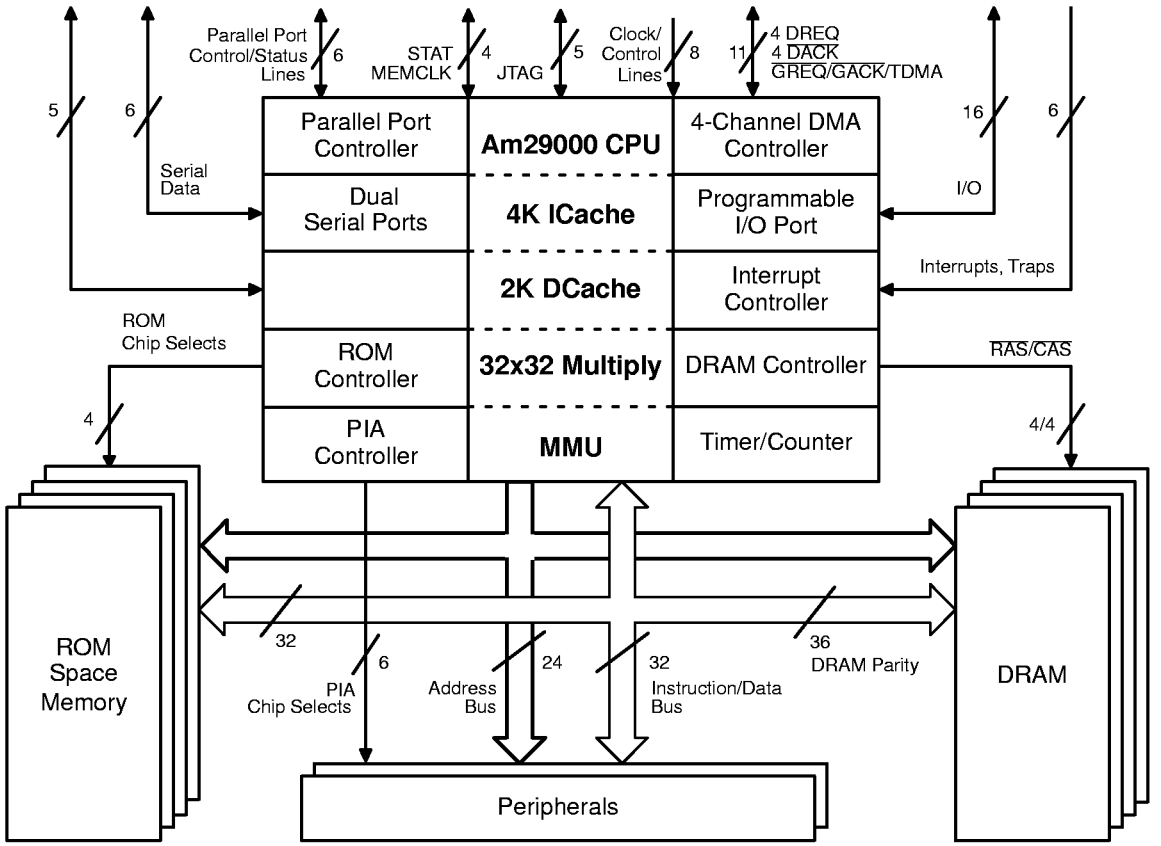
Am29240EH MICROCONTROLLER BLOCK DIAGRAM



Am29245EH MICROCONTROLLER BLOCK DIAGRAM



Am29243EH MICROCONTROLLER BLOCK DIAGRAM



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For answers to technical questions, AMD® provides a toll-free number for direct access to our corporate applications hotline. Also available is the AMD World Wide Web home page and FTP site, which provides the latest 29K family product information.

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Documentation and Literature

A simple phone call gets you free 29K family information such as data sheets, user's manuals, application notes, the Fusion29K Partner Solutions Catalog, and other literature. Internationally, contact your local AMD sales office for complete 29K family literature.

Literature Ordering

(800) 222-9323, option 3	toll-free for U.S.
(512) 602-5651	direct dial worldwide
(800) 222-9323, option 2	AMD Facts-On-Demand™ fax information service toll-free for U.S., Canada

RELATED DOCUMENTS

The *Am29240EH, Am29245EH, and Am29243EH RISC Microcontrollers User's Manual* (order #17741) describes the technical features, programming interface, on-chip peripherals, register set, and instruction set for the Am29240EH microcontroller series.

Programming the 29K RISC Family (order #19243) includes comprehensive information about the 29K family for the software developer.

GENERAL DESCRIPTION

The Am29240EH microcontroller series is an enhanced bus-compatible extension of the Am29200™ RISC microcontroller family, with two to four times the performance. The Am29240EH microcontroller series includes the Am29240EH microcontroller, the low-cost Am29245EH microcontroller, and the Am29243EH data microcontroller. The on-chip caches, MMU, faster integer math, and extended DMA addressing capability of the Am29240EH microcontroller series allow the embedded systems designer to provide increasing levels of performance and software compatibility throughout a range of products (see Table 1 on page 6).

Based on a low-voltage CMOS-technology design, these devices offer a complete set of system peripherals and interfaces commonly used in embedded applications. Compared to CISC processors, the Am29240EH microcontroller series offers better performance, more efficient use of low-cost memories, lower system cost, and complete design flexibility for the designer. Coupled with hardware and software development tools from the AMD Fusion29K® partners, the Am29240EH microcontroller series provides the embedded product designer with the cost and performance edge required by today's marketplace.

For a complete description of the technical features, on-chip peripherals, programming interface, register set, and instruction set, please refer to the *Am29240EH, Am29245EH, and Am29243EH RISC Microcontrollers User's Manual* (order #17741).

Am29240EH Microcontroller

For general-purpose embedded applications, such as mass-storage controllers, communications, digital signal processing, networking, industrial control, pen-based systems, and multimedia, the Am29240EH microcontroller provides a high-performance solution with a low total-system cost. The memory interface of the Am29240EH microcontroller provides even faster direct memory access than the Am29200 microcontroller. This performance improvement minimizes the effect of memory latency, allowing designers to use low-cost memory with simpler memory designs. On-chip instruction and data caches provide even better performance for time-critical code.

Other on-chip functions include: a ROM controller, DRAM controller, peripheral interface adapter controller, DMA controller, programmable I/O port, parallel port controller, serial ports, and an interrupt controller.

Am29245EH Microcontroller

The low-cost Am29245EH microcontroller is designed for embedded applications in which cost and space constraints, along with increased performance requirements, are primary considerations.

The Am29245EH microcontroller also provides an easy upgrade path for Am29200, Am29202™, and Am29205™ microcontroller-based products.

Am29243EH Microcontroller

With DRAM parity support and a full MMU, the Am29243EH data microcontroller is recommended for communications applications that require high-speed data movement and fast protocol processing in a fault-tolerant environment.

Both the Am29243EH and Am29240EH microcontrollers support fly-by DMA at 100 Mbytes/s for LANs and switching applications, and a two-cycle Multiply Accumulate function for DSP applications. The low power requirements make either microcontroller a good choice for field-deployed devices.

Development Support Products

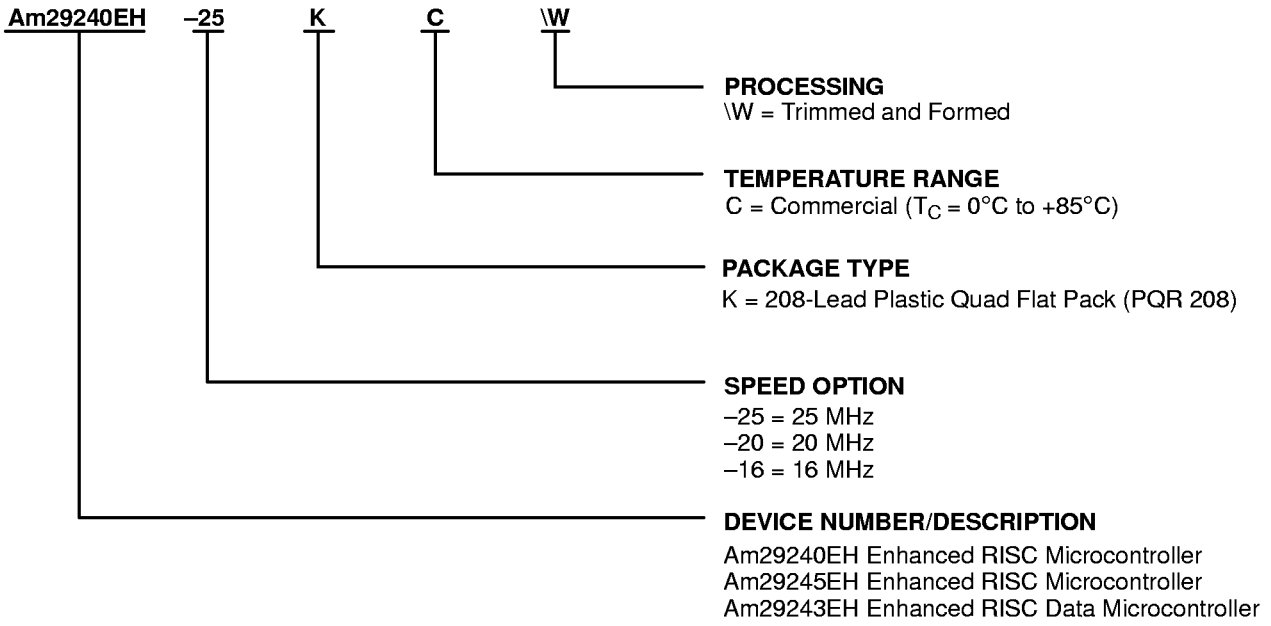
The Fusion29K Program of Partnerships for Application Solutions provides the user with a vast array of products designed to meet critical time-to-market needs. Products/solutions available from the AMD Fusion29K partners include the following:

- Optimizing compilers for common high-level languages
- Assembler and utility packages
- Source- and assembly-level software debuggers
- Target-resident development monitors
- Simulators
- Execution boards
- Hardware development tools
- Silicon products
- Board-level products
- Laser-printer solutions
- Multiuser, kernel, and real-time operating systems
- Graphics solutions
- Networking and communication solutions
- Manufacturing support
- Custom software consulting, support, and training

ORDERING INFORMATION

Standard Products

AMD® standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
Am29240EH–20 Am29240EH–25	KC\W
Am29243EH–20 Am29243EH–25	KC\W
Am29245EH–16	KC\W

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD standard military grade products.

RELATED AMD PRODUCTS

29K Family Devices

Product	Description
Am29000®	32-bit RISC microprocessor
Am29005™	Low-cost 32-bit RISC microprocessor with no MMU and no branch target cache
Am29030™	32-bit RISC microprocessor with 8-Kbyte instruction cache
Am29035™	32-bit RISC microprocessor with 4-Kbyte instruction cache
Am29040™	32-bit RISC microprocessor with 8-Kbyte instruction cache and 4-Kbyte data cache
Am29050™	32-bit RISC microprocessor with on-chip floating point
Am29200™	32-bit RISC microcontroller
Am29202™	Low-cost 32-bit RISC microcontroller with IEEE-1284-compliant parallel interface
Am29205™	Low-cost 32-bit RISC microcontroller

Table 1. Product Comparison—Am29200 Microcontroller Family

FEATURE	Am29205™ Controller	Am29202™ Controller	Am29200™ Controller	Am29245EH Controller	Am29240EH Controller	Am29243EH Controller
Instruction Cache	—	—	—	4 Kbytes	4 Kbytes	4 Kbytes
Data Cache	—	—	—	—	2 Kbytes	2 Kbytes
Cache Associativity	—	—	—	2-way	2-way	2-way
Integer Multiplier	Software	Software	Software	Software	32 x 32-bit	32 x 32-bit
Memory Management Unit (MMU)	—	—	—	1 TLB 16 Entry	1 TLB 16 Entry	2 TLBs 32 Entry
Data Bus Width						
Internal	32 bits	32 bits	32 bits	32 bits	32 bits	32 bits
External	16 bits	32 bits	32 bits	32 bits	32 bits	32 bits
ROM Interface						
Banks	3	4	4	4	4	4
Width	8, 16 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits
ROM Size (Max/Bank)	4 Mbytes	4 Mbytes	16 Mbytes	16 Mbytes	16 Mbytes	16 Mbytes
Boot-Up ROM Width	16 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits
Burst-Mode Access	Not Supported	Not Supported	Supported	Supported	Supported	Supported
DRAM Interface						
Banks	4	4	4	4	4	4
Width	16 bits only	16, 32 bits	16, 32 bits	32 bits	32 bits	32 bits
Size: 32-Bit Mode	—	16 Mbytes/bank	16 Mbytes/bank	16 Mbytes/bank	16 Mbytes/bank	16 Mbytes/bank
Size: 16-Bit Mode	8 Mbytes/bank	8 Mbytes/bank	8 Mbytes/bank	Not supported	Not supported	Not supported
Video DRAM	Not Supported	Not Supported	Supported	Supported	Supported	Not Supported
Access Cycles						
Initial/Burst	3/2	3/2	3/2	2/1 or 3/1	2/1 or 3/1	2/1 or 3/1
DRAM Parity	No	No	No	No	No	Yes
On-Chip DMA						
Width (ext. peripherals)	8, 16 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits
Total Number of Channels	2	2	2	2	4	4
Externally Controlled	1	1	2	2	4	4
External Master Access	No	No	Yes	Yes	Yes	Yes
External Master Burst	No	No	No	Yes	Yes	Yes
External Terminate Signal	No	No	Yes	Yes	Yes	Yes
Low-Voltage Operation	No	No	No	Yes	Yes	Yes
Peripheral Interface Adapter (PIA)						
PIA Ports	2	2	6	6	6	6
Data Width	8, 16 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits
Min. Cycles Access	3	3	3	1	1	1
Programmable I/O Port (PIO)						
Signals	8	12	16	16	16	16
Signals programmable for interrupt generation	8	8	8	8	8	8
Serial Ports						
Ports $\overline{DSR}/\overline{DTR}$	1 Port PIO signals	1 Port PIO signals	1 Port Supported	1 Port Supported	2 Ports 1 Port Supported	2 Ports 1 Port Supported
Interrupt Controller						
External Interrupt Pins	2	2	4	4	4	4
External Trap and Warn Pins	0	0	3	3	3	3
Parallel Port Controller	Yes	Yes	Yes	Yes	Yes	Yes
32-Bit Transfer	No	Yes	Yes	Yes	Yes	Yes
IEEE-1284 Interface	No	Yes	No	No	No	No
JTAG Debug Support	No	Yes	Yes	Yes	Yes	Yes
Serializer/Deserializer	Yes	Yes	Yes	Yes	Yes	No
Pin Count and Package	100 PQFP	132 PQFP	168 PQFP	208 PQFP	208 PQFP	208 PQFP
Operating Voltage						
V_{CC}	5 V	5 V	5 V	3.3 V	3.3 V	3.3 V
I/O Tolerance	5 V	5 V	5 V	5 V	5 V	5 V
Processor Clock Rate	12, 16 MHz	12, 16, 20 MHz	16, 20 MHz	16 MHz	20, 25 MHz	20, 25 MHz

KEY FEATURES AND BENEFITS

The Am29240EH microcontroller series extends the line of RISC microcontrollers based on 29K family architecture, providing performance upgrades to the Am29205 and Am29200 microcontrollers. The RISC microcontroller product line allows users to benefit from the very high performance of the 29K family architecture, while also capitalizing on the very low system cost made possible by integrating processor and peripherals.

The Am29240EH microcontroller series expands the price/performance range of systems that can be built with the 29K family. The Am29240EH microcontroller series is fully software compatible with the Am29000, Am29005, Am29030, Am29035, Am29040, and Am29050 microprocessors, as well as the Am29200 and Am29205 microcontrollers. It can be used in existing 29K family microcontroller applications without software modifications.

On-Chip Caches

The Am29240EH microcontroller series incorporates a 4-Kbyte, two-way instruction cache that supplies most processor instructions without wait states at the processor frequency. For best performance, the instruction cache supports critical-word-first reloading with fetch-through, so that the processor receives the required instruction and the pipeline restarts with minimum delay. The instruction cache has a valid bit per word to minimize the reload overhead. All cache array elements are visible to software for testing and preload.

The Am29240EH and Am29243EH microcontrollers incorporate a 2-Kbyte, two-way set-associative data cache. The data cache appears in the execute stage of the processor pipeline, so that loaded data is available immediately to the next instruction. This provides the maximum performance for loads without requiring load scheduling. This minimizes the time the processor waits on external data as well as minimizing the reload time. The data cache uses a write-through policy with a two-entry write buffer. Byte, half-word, and word reads and writes are supported. All cache array elements are visible to software for testing and preload.

Single-Cycle Multiplier

The Am29240EH and Am29243EH microcontrollers incorporate a full combinatorial multiplier that accepts two 32-bit input operands and produces a 32-bit result in a single cycle. The multiplier can produce a 64-bit result in two cycles. The multiplier permits maximum performance without requiring instruction scheduling, since the latency of the multiply is the same as the latency of other integer operations. High-performance multiplication benefits imaging, signal processing, and state modeling applications.

Complete Set of Common Peripherals

The Am29240EH microcontroller series minimizes system cost by incorporating a complete set of system facilities commonly found in embedded applications, eliminating the cost of additional components. The on-chip functions include: a ROM controller, a DRAM controller, a peripheral interface adapter, a DMA controller, a programmable I/O port, a parallel port, up to two serial ports, and an interrupt controller. A video interface is also included in the Am29240EH and Am29245EH microcontrollers for printer, scanner, and other imaging applications. These facilities allow many simple systems to be built using only the Am29240EH microcontroller series, external ROM, and/or DRAM memory.

ROM Controller

The ROM controller supports four individual banks of ROM or other static memory, each with its own timing characteristics. Each ROM bank may be a different size and may be either 8, 16, or 32 bits wide. The ROM banks can appear as a contiguous memory area of up to 64 Mbytes in size. The ROM controller also supports byte, half-word, and word writes to the ROM memory space for devices such as flash EPROMs and SRAMs.

DRAM Controller

The DRAM controller supports four separate banks of dynamic memory. Each bank may be a different size and must be 32 bits wide. The DRAM banks can appear as a contiguous memory area of up to 64 Mbytes in size. The DRAM controller supports two- or three-cycle accesses (programmable by software), with single-cycle page-mode and burst-mode accesses. Burst accesses are supported at two initial, one burst, or three initial, one burst.

Peripheral Interface Adapter

The Peripheral Interface Adapter (PIA) permits glueless interfacing to as many as six external peripheral chips. The PIA allows for additional system features implemented by external peripheral chips.

DMA Controller

The DMA controller provides up to four channels for transferring data between the DRAM and internal or external peripherals.

Fly-by DMA transfers data directly between an external peripheral and DRAM or ROM, permitting very high data bandwidth. The peripheral must support the timing of the memory (DRAM or ROM). The transfer occurs at the rate of one 32-bit word per cycle, if DRAM page-mode accesses or ROM burst-mode or single-cycle accesses are enabled.

For page-mode DRAM, the TDMA signal is asserted on the rising edge following the last access. For an initial access, TDMA is asserted simultaneously with $\overline{\text{DACK}}$x. DMA wait states and peripheral wait states are ignored

during fly-by transfers. A higher fly-by DMA transfer can interrupt a lower fly-by transfer.

Refresh does not pre-empt a fly-by transfer. A DMA transfer continues until either DREQx is deasserted, the transfer is interrupted by a higher priority DMA, or the Count Terminate Enable (CTE) bit is set. No refreshes will occur until the fly-by transfer is completed, so fly-by transfers must be less than one refresh interval in length. The DREQx signal must be configured as level-sensitive in the DRAM Control Register.

Parity checking and generation cannot be performed during a fly-by transfer. Note also that zero-wait-state ROM cannot be used with fly-by DMA.

I/O Port

The I/O port permits direct access to 16 individually programmable external input/output signals. Eight of these signals can be configured to cause interrupts.

Parallel Port

The parallel port implements a bidirectional IBM PC-compatible parallel interface to a host processor.

Serial Port

The serial port implements up to two full-duplex UARTs.

Serializer/Deserializer

The serializer/deserializer (video interface) on the Am29240EH and Am29245EH microcontrollers permits direct connection to a number of laser-marking engines, video displays, or raster input devices such as scanners.

Interrupt Controller

The interrupt controller generates and reports the status of interrupts caused by on-chip peripherals.

Wide Range of Price/Performance Points

To reduce design costs and time-to-market, the product designer can use the Am29200 microcontroller family and one basic system design as the foundation for an entire product line. From this design, numerous implementations of the product at various levels of price and performance may be derived with minimum time, effort, and cost.

The Am29240EH RISC microcontroller series supports this capability through various combinations of on-chip caches, programmable memory widths, programmable wait states, burst-mode and page-mode access support, bus compatibility, and 29K family software compatibility. A system can be upgraded using various memory architectures without hardware and software redesign.

The ROM controller accommodates memories that are either 8, 16, or 32 bits wide, and the DRAM controller accommodates dynamic memories that are 32 bits wide. This unique feature provides a flexible interface to low-cost memory, as well as a convenient, flexible upgrade path. For example, a system can start with a 16-bit ROM memory design and can subsequently improve performance by migrating to a 32-bit ROM memory design. One particular advantage is the ability to add memory in half-megabyte increments. This provides significant cost savings for applications that do not require larger memory upgrades.

The Am29200, Am29202, Am29205, Am29240, Am29245, and Am29243EH microcontrollers allow users to address an extremely wide range of cost performance points, with higher performance and lower cost than existing designs based on CISC microprocessors.

Glueless System Interfaces

The Am29240EH microcontroller series also minimizes system cost by providing a glueless attachment to external ROMs, DRAMs, and other peripheral components. Processor outputs have edge-rate control that allows them to drive a wide range of load capacitances with low noise and ringing. This eliminates the cost of external logic and buffering.

Bus and Software Compatibility

Compatibility within a processor family is critical for achieving a rational, easy upgrade path. Processors in the Am29240EH microcontroller series are all members of a bus-compatible family of RISC microcontrollers. All members of this family—the Am29205, Am29202, Am29200, Am29240, Am29245, and Am29243EH microcontrollers—allow improvements in price, performance, and system capabilities without requiring that users redesign their system hardware or software. Bus compatibility ensures a convenient upgrade path for future systems.

The Am29240EH microcontroller series is available in a 208-pin plastic quad flat-pack (PQFP) package. The Am29240EH microcontroller series is signal-compatible with the Am29200 and the Am29205 microcontrollers.

Moreover, the Am29240EH microcontroller series is binary compatible with existing RISC microcontrollers and other members of the 29K family (the Am29000, Am29005, Am29030, Am29035, Am29040, and Am29050 microprocessors, as well as the Am29200, Am29202, and Am29205 microcontrollers). The Am29240EH microcontroller series provides a migration path to low-cost, high-performance, highly integrated systems from other 29K family members, without requiring expensive rewrites of application software.

Debugging and Testing

The Am29240EH microcontroller series provides debugging and testing features at both the software and hardware levels.

Software debugging is facilitated by the instruction trace facility and instruction breakpoints. Instruction tracing is accomplished by forcing the processor to trap after each instruction has been executed. Instruction breakpoints are implemented by the HALT instruction or by a software trap.

The processor provides several additional features to assist system debugging and testing:

- The Test/Development Interface is composed of a group of pins that indicate the state of the processor and control the operation of the processor.
- A Traceable Cache feature permits a hardware-development system to track accesses to the on-chip caches, permitting a high level of visibility into processor operation.
- An IEEE Std 1149.1-1990 (JTAG) compliant Standard Test Access Port and Boundary-Scan Architecture. The Test Access Port provides a scan interface for testing processor and system hardware in a production environment, and contains extensions that allow a hardware-development system to control and observe the processor without interposing hardware between the processor and system.

PERFORMANCE OVERVIEW

The Am29240EH microcontroller series offers a significant margin of performance over CISC microprocessors in existing embedded designs, since the majority of processor features were defined for the maximum achievable performance at very low cost. This section describes the features of the Am29240EH microcontroller series from the point of view of system performance.

Instruction Timing

The Am29240EH microcontroller series uses an arithmetic/logic unit, a field shift unit, and a prioritizer to execute most instructions. Each of these is organized to operate on 32-bit operands and provide a 32-bit result. All operations are performed in a single cycle.

The performance degradation of load and store operations is minimized in the Am29240EH microcontroller series by overlapping them with instruction execution, by taking advantage of pipelining, by an on-chip data cache, and by organizing the flow of external data into the processor so that the impact of external accesses is minimized.

Pipelining

Instruction operations are overlapped with instruction fetch, instruction decode and operand fetch, instruction execution, and result write-back to the Register File. Pipeline forwarding logic detects pipeline dependencies and routes data as required, avoiding delays that might arise from these dependencies. Pipeline interlocks are implemented by processor hardware. Except for a few special cases, it is not necessary to rearrange programs to avoid pipeline dependencies, although this is sometimes desirable for performance.

On-Chip Instruction and Data Caches

On-chip instruction and data caches satisfy most processor fetches without wait states. The caches are pipelined for best performance. The reload policies minimize the amount of time spent waiting for reload, while optimizing the benefit of locality of reference.

Burst-Mode and Page-Mode Memories

The Am29240EH microcontroller series directly supports burst-mode memories. The burst-mode memory supplies instructions at the maximum bandwidth, without the complexity of an external cache or the performance degradation due to cache misses.

The processor can also use the page-mode capability of common DRAMs to improve the access time in cases where page-mode accesses can be used.

Instruction Set Overview

All 29K family members employ a three-address instruction set architecture. The compiler or assembly-language programmer is given complete freedom to allocate register usage. There are 192 general-purpose registers, allowing the retention of intermediate calculations and avoiding needless data destruction. Instruction operands may be contained in any of the general-purpose registers, and the results may be stored into any of the general-purpose registers.

The Am29240EH microcontroller series instruction set contains 117 instructions that are divided into nine classes. These classes are integer arithmetic, compare, logical, shift, data movement, constant, floating point, branch, and miscellaneous. The floating-point instructions are not executed directly, but are emulated by trap handlers.

All directly implemented instructions are capable of executing in one processor cycle, with the exception of interrupt returns, loads, and stores.

Data Formats

The Am29240EH microcontroller series defines a word as 32 bits of data, a half-word as 16 bits, and a byte as 8 bits. The hardware provides direct support for word-integer (signed and unsigned), word-logical, word-Boolean, half-word integer (signed and unsigned), and character data (signed and unsigned).

Word-Boolean data is based on the value contained in the most significant bit of the word. The values TRUE and FALSE are represented by the most significant bit values 1 and 0, respectively.

Other data formats, such as character strings, are supported by instruction sequences. Floating-point formats

(single and double precision) are defined for the processor; however, there is no direct hardware support for these formats in the Am29240EH microcontroller series.

Protection

The Am29240EH microcontroller series offers two mutually exclusive modes of execution—the User and Supervisor modes—that restrict or permit accesses to certain processor registers and external storage locations.

The register file may be configured to restrict accesses to Supervisor-mode programs on a bank-by-bank basis.

Memory Management Unit

The Am29240EH microcontroller series provides a memory-management unit (MMU) for translating virtual addresses into physical addresses. The page size for translation ranges from 1 Kbyte to 16 Mbytes in powers of 4. The Am29245EH and Am29240EH microcontrollers each have a single, 16-entry TLB. The Am29243EH microcontroller has dual 16-entry TLBs, each capable of mapping pages of different size.

Interrupts and Traps

When the microcontroller takes an interrupt or trap, it does not automatically save its current state information in memory. This lightweight interrupt and trap facility greatly improves the performance of temporary interruptions such as simple operating-system calls that require no saving of state information.

In cases where the processor state must be saved, the saving and restoring of state information is under the control of software. The methods and data structures used to handle interrupts—and the amount of state saved—may be tailored to the needs of a particular system.

Interrupts and traps are dispatched through a 256-entry vector table that directs the processor to a routine that handles a given interrupt or trap. The vector table may be relocated in memory by the modification of a processor register. There may be multiple vector tables in the system, though only one is active at any given time.

The vector table is a table of pointers to the interrupt and trap handlers, and requires only 1 Kbyte of memory. The processor performs a vector fetch every time an interrupt or trap is taken. The vector fetch requires at least three cycles, in addition to the number of cycles required for the basic memory access.

PIN DESCRIPTIONS

A23–A0

Address Bus (output, synchronous)

The Address Bus supplies the byte address for all accesses, except for DRAM accesses. For DRAM accesses, multiplexed row and column addresses are provided on A14–A1. A2–A0 are also used to provide a clock to an optional burst-mode EPROM.

BOOTW

Boot ROM Width (input, asynchronous)

This input configures the width of ROM Bank 0, so the ROM can be accessed before the ROM configuration has been set by the system initialization software. The BOOTW signal is sampled during and after a processor reset. If BOOTW is High before and after reset (tied High), the boot ROM is 32 bits wide. If BOOTW is Low before and after reset (tied Low), the boot ROM is 16 bits wide. If BOOTW is Low before reset and High after reset (tied to $\overline{\text{RESET}}$), the boot ROM is 8 bits wide. This signal has special hardening against metastable states, allowing it to be driven with a slow-rise-time signal and permitting it to be tied to $\overline{\text{RESET}}$.

$\overline{\text{BURST}}$

Burst-Mode Access (output, synchronous)

This signal is asserted to perform sequential accesses from a burst-mode device.

$\overline{\text{CAS}}$3–$\overline{\text{CAS}}$0

Column Address Strobes, Byte 3–0 (output, synchronous)

A High-to-Low transition on these signals causes the DRAM selected by $\overline{\text{RAS}}$3–$\overline{\text{RAS}}$0 to latch the column address and complete the access. To support byte and half-word writes, column address strobes are provided for individual DRAM bytes. $\overline{\text{CAS}}$3 is the column address strobe for the DRAMs, in all banks, attached to ID31–ID24. $\overline{\text{CAS}}$2 is for the DRAMs attached to ID23–ID16, and so on. These signals are also used in other special DRAM cycles.

CNTL1–CNTL0

CPU Control (input, asynchronous, internal pull-ups)

These inputs specify the processor mode: Load Test Instruction, Step, Halt, or Normal.

$\overline{\text{DACK}}$D–$\overline{\text{DACK}}$A

DMA Acknowledge D through A (output, synchronous)

These signals acknowledge an external transfer on a DMA channel. DMA acknowledgments are not dedicated to a particular DMA channel—each channel specifies which acknowledge line, if any, it is using. Only one

channel at a time can use either $\overline{\text{DACK}}$D, $\overline{\text{DACK}}$C, $\overline{\text{DACK}}$B, or $\overline{\text{DACK}}$A, and the same channel uses the respective DREQD–DREQA signal for transfer requests. DMA transfers can occur to and from internal peripherals independent of these acknowledgments. The $\overline{\text{DACK}}$D and $\overline{\text{DACK}}$C signals are supported on the Am29240EH and Am29243EH microcontrollers only.

DREQD–DREQA

DMA Request D through A
(input, asynchronous, pull-up resistors)

These inputs request an external transfer on a DMA channel. DMA requests are not dedicated to a particular channel—each channel specifies which request line, if any, it is using. Only one channel at a time can use either DREQD, DREQC, DREQB, or DREQA. This channel acknowledges a transfer using the respective $\overline{\text{DACK}}$D–$\overline{\text{DACK}}$A signal. These requests are individually programmable to be either level- or edge-sensitive for either polarity of level or edge. DMA transfers can occur to and from internal peripherals independent of these requests.

The DMA request/acknowledge pairs DREQA/$\overline{\text{DACK}}$A and DREQB/$\overline{\text{DACK}}$B correspond to the Am29200 microcontroller signals DREQ0/$\overline{\text{DACK}}$0 and DREQ1/$\overline{\text{DACK}}$1, respectively. The pin placement reflects this correspondence, and a processor reset dedicates these request/acknowledge pairs to DMA channels 0 and 1, respectively. This permits backward-compatible upgrade to an Am29200 microcontroller. The DREQD and DREQC signals are supported on the Am29240EH and Am29243EH microcontrollers only.

$\overline{\text{DSR}}$A

Data Set Ready, Port A (output, synchronous)

This indicates to the host that the serial port is ready to transmit or receive data on Serial Port A.

$\overline{\text{DTR}}$A

Data Terminal Ready, Port A
(input, asynchronous)

This indicates to the processor that the host is ready to transmit or receive data on Serial Port A.

$\overline{\text{GACK}}$

External Memory Grant Acknowledge
(output, synchronous)

This signal indicates to an external device that it has been granted an access to the processor's ROM or DRAM, and that the device should provide an address.

The processor can be placed into a slave configuration that allows tracing of a master processor. In this configuration, $\overline{\text{GACK}}$ is used to indicate that the processor pipeline was held during the previous processor cycle.

$\overline{\text{GREQ}}$

External Memory Grant Request
(input, synchronous, pull-up resistor)

This signal is used by an external device to request an access to the processor's ROM or DRAM. To perform this access, the external device supplies an address to the ROM controller or DRAM controller.

To support a hardware-development system, $\overline{\text{GREQ}}$ should be either tied High or held at a high-impedance state during a processor reset.

ID31–ID0

Instruction/Data Bus (bidirectional, synchronous)

The Instruction/Data Bus (ID Bus) transfers instructions to, and data to and from the processor.

IDP3–IDP0

Instruction/Data Parity
(bidirectional, synchronous)

If parity checking is enabled by the PCE bit of the DRAM Control Register, IDP3–IDP0 are parity bits for the ID Bus during DRAM accesses. IDP3 is the parity bit for ID31–ID24, IDP2 is the parity bit for ID23–ID16, and so on. If parity is enabled, the processor drives IDP3–IDP0 with valid parity during DRAM writes, and expects IDP3–IDP0 to be driven with valid parity during DRAM reads. These signals are supported on the Am29243EH microcontroller only.

INCLK

Input Clock (input)

This is an oscillator input at twice the system operating frequency.

$\overline{\text{INTR}}$3–$\overline{\text{INTR}}$0

Interrupt Requests 3–0
(input, asynchronous, internal pull-up resistors)

These inputs generate prioritized interrupt requests. The interrupt caused by $\overline{\text{INTR}}$0 has the highest priority, and the interrupt caused by $\overline{\text{INTR}}$3 has the lowest priority. The interrupt requests are masked in prioritized order by the Interrupt Mask field in the Current Processor Status Register and are disabled by the DA and DI bits of the Current Processor Status Register. These signals have special hardening against metastable states, allowing them to be driven with slow-transition-time signals.

LSYNC

Line Synchronization (input, asynchronous)

This signal indicates the start of a raster line. This signal is supported on the Am29240EH and Am29245EH microcontrollers only.

MEMCLK

Memory Clock (output)

MEMCLK is an output clock only. It operates at the system operating frequency, which is half of the INCLK frequency. Most processor inputs and outputs are synchronous to MEMCLK. Note that MEMCLK as an input is not supported on the Am29240EH microcontroller series.

MEMDRV

MEMCLK Drive Enable (input, internal pull-up resistor)

The MEMDRV signal is reserved on the Am29240EH microcontroller series. This pin should be either tied High or left unconnected.

PACK

Parallel Port Acknowledge (output, synchronous)

This signal is used by the processor to acknowledge a transfer from the host or to indicate to the host that data has been placed on the port.

PAUTOFD

Parallel Port Autofeed (input, asynchronous)

This signal is used by the host to indicate how line feeds should be performed or is used to indicate that the host is busy and cannot accept a data transfer.

$\overline{\text{PBUSY}}$

Parallel Port Busy (output, synchronous)

This indicates to the host that the Parallel Port is busy and cannot accept a data transfer.

$\overline{\text{PIACS}}5$–$\overline{\text{PIACS}}0$

Peripheral Chip Selects, Regions 5–0 (output, synchronous)

These signals are used to select individual peripheral devices. DMA channels may be programmed to use dedicated chip selects during an external peripheral access.

$\overline{\text{PIAOE}}$

Peripheral Output Enable (output, synchronous)

This signal enables the selected peripheral device to drive the ID bus.

$\overline{\text{PIAWE}}$

Peripheral Write Enable (output, synchronous)

This signal causes data on the ID bus to be written into the selected peripheral.

PIO15–PIO0

Programmable Input/Output (input/output, asynchronous)

These signals are available for direct software control and inspection. PIO15–PIO8 may be individually programmed to cause processor interrupts. These signals have special hardening against metastable states, allowing them to be driven with slow-transition-time signals.

The PIO signals are sampled during a processor reset. After reset, the sampled value is held in the PIO Input Register. This sampled value is supplied the first time this register is read, unless the read is preceded by write to the PIO Input Register or by a read or write of any other PIO register. This may be used to indicate system configuration information to the processor during a reset.

$\overline{\text{POE}}$

Parallel Port Output Enable (output, synchronous)

This signal enables an external data buffer containing data from the host to drive the ID Bus.

PSTROBE

Parallel Port Strobe (input, asynchronous)

This signal is used by the host to indicate that data is on the Parallel Port or to acknowledge a transfer from the processor.

PSYNC

Page Synchronization (input/output, asynchronous)

This signal indicates the beginning of a raster page. This signal is supported on the Am29240EH and Am29245EH microcontrollers only.

$\overline{\text{PWE}}$

Parallel Port Write Enable (output, synchronous)

This signal writes a buffer with data on the ID Bus. Then, the buffer drives data to the host.

R/$\overline{\text{W}}$

Read/Write (output, synchronous)

During an external ROM, DRAM, DMA, or PIA access, this signal indicates the direction of transfer: High for a read and Low for a write.

$\overline{\text{RAS}}3$–$\overline{\text{RAS}}0$

Row Address Strobe, Banks 3–0 (output, synchronous)

A High-to-Low transition on one of these signals causes a DRAM in the corresponding bank to latch the row address and begin an access. $\overline{\text{RAS}}3$ starts an access in DRAM Bank 3, and so on. These signals also are used in other special DRAM cycles.

$\overline{\text{RESET}}$

Reset (input, asynchronous)

This input places the processor in the Reset mode. This signal has special hardening against metastable states, allowing it to be driven with a slow-rise-time signal.

$\overline{\text{ROMCS3}}$–$\overline{\text{ROMCS0}}$

ROM Chip Selects, Banks 3–0 (output, synchronous)

A Low level on one of these signals selects the memory devices in the corresponding ROM bank. $\overline{\text{ROMCS3}}$ selects devices in ROM Bank 3, etc. The timing and access parameters of each bank are individually programmable.

$\overline{\text{ROMOE}}$

ROM Output Enable (output, synchronous)

This signal enables the selected ROM Bank to drive the ID bus. It is used to prevent bus contention when switching between different ROM banks or switching between a ROM bank and another device or DRAM bank.

$\overline{\text{RSWE}}$

ROM Space Write Enable (output, synchronous)

This signal is used to write an alterable memory in a ROM bank (such as an SRAM or Flash EPROM).

RXDA

Receive Data, Port A (input, asynchronous)

This input is used to receive serial data to Serial Port A.

RXDB

Receive Data, Port B (input, asynchronous)

This input is used to receive data to Serial Port B. This signal is supported on the Am29240EH and Am29243EH microcontrollers only.

STAT2–STAT0

CPU Status (output, synchronous)

These outputs indicate information about the processor or the current access for the purposes of hardware debug.

TCK

Test Clock Input
(input, asynchronous, pull-up resistor)

This input is used to operate the Test Access Port. The state of the Test Access Port must be held if this clock is held either High or Low. This clock is internally synchronized to MEMCLK for certain operations of the Test Access Port controller, so signals internally driven and sampled by the Test Access Port are synchronous to processor internal clocks.

TDI

Test Data Input
(input, synchronous to TCK, pull-up resistor)

This input supplies data to the test logic from an external source. It is sampled on the rising edge of TCK. If it is not driven, it appears High internally.

TDMA

Terminate DMA (input/output, synchronous)

This signal is either an input or an output as controlled by the corresponding DMA Control Register. As an input, this signal can be asserted during an external DMA transfer (non-fly-by) to terminate the transfer after the current access. The TDMA input is ignored during fly-by transfers. As an output, this signal is asserted to indicate the final transfer of a sequence.

TDO

Test Data Output
(three-state output, synchronous to TCK)

This output supplies data from the test logic to an external destination. It changes on the falling edge of TCK. It is in the high-impedance state except when scanning is in progress.

TMS

Test Mode Select
(input, synchronous to TCK, pull-up resistor)

This input is used to control the Test Access Port. If it is not driven, it appears High internally.

$\overline{\text{TR}}$/$\overline{\text{OE}}$

Video DRAM Transfer/Output Enable
(output, synchronous)

This signal is used with video DRAMs to transfer data to the video shift register. It is also used as an output enable in normal video DRAM read cycles. This signal is supported on the Am29240EH and Am29245EH microcontrollers only.

$\overline{\text{TRAP1}}$–$\overline{\text{TRAP0}}$

Trap Requests 1–0
(input, asynchronous, internal pull-ups)

These inputs generate prioritized trap requests. The trap caused by $\overline{\text{TRAP0}}$ has the highest priority. These trap requests are disabled by the DA bit of the Current Processor Status Register. These signals have special hardening against metastable states, allowing them to be driven with slow-transition-time signals.

$\overline{\text{TRIST}}$

Three-State Control
(input, asynchronous, pull-up resistor)

This input is asserted to force all processor outputs into the high-impedance state. This signal is tied High through an internal pull-up resistor.

$\overline{\text{TRST}}$

Test Reset Input
(input, asynchronous, pull-up resistor)

This input asynchronously resets the Test Access Port. If $\overline{\text{TRST}}$ is not driven, it appears High internally. $\overline{\text{TRST}}$ must be tied to $\overline{\text{RESET}}$, even if the Test Access Port is not being used.

TXDA

Transmit Data, Port A (output, asynchronous)

This output is used to transmit serial data from Serial Port A.

TXDB

Transmit Data, Port B (output, asynchronous)

This output is used to transmit data from Serial Port B. This signal is supported on the Am29240EH and Am29243EH microcontrollers only.

UCLK

UART Clock (input)

This is an oscillator input for generating the UART (Serial Port) clock. To generate the UART clock, the oscillator frequency may be divided by any amount up to 65,536. The UART clock operates at 16 times the Serial Port's baud rate. As an option, UCLK may be driven with MEMCLK or INCLK. It can be driven with TTL levels.

VCLK

Video Clock (input, asynchronous)

This clock is used to synchronize the transfer of video data. As an option, VCLK may be driven with MEMCLK or INCLK. It can be driven with TTL levels. This signal is supported on the Am29240EH and Am29245EH microcontrollers only.

VDAT

Video Data (input/output, synchronous to VCLK)

This is serial data to or from the video device. This signal is supported on the Am29240EH and Am29245EH microcontrollers only.

$\overline{\text{WAIT}}$

Add Wait States
(input, synchronous, internal pull-up)

External accesses are normally timed by the processor. However, the $\overline{\text{WAIT}}$ signal may be asserted during a PIA, ROM, or DMA access to extend the access indefinitely. For external DMA accesses, the number of wait states taken by the DRAM controller (this includes peripheral read and write wait states during DMA transfers) is determined by the actual value in the DMAWAIT field of the DMA Control Register or the number of wait states specified by the IOWAIT field in the PIA Control Register, whichever is greater.

$\overline{\text{WARN}}$

Warn (input, asynchronous, edge-sensitive, internal pull-up)

A High-to-Low transition on this input causes a non-maskable $\overline{\text{WARN}}$ trap to occur. This trap bypasses the normal trap vector fetch sequence, and is useful in situations where the vector fetch may not work (e.g., when data memory is faulty). This signal has special hardening against metastable states, allowing it to be driven with a slow-transition-time signal. $\overline{\text{WARN}}$ must be held active for at least four system clocks for the processor to recognize it.

$\overline{\text{WE}}$

Write Enable (output, synchronous)

This signal is used to write the selected DRAM bank. "Early write" cycles are used so the DRAM data inputs and outputs can be tied to the common ID Bus.

PRODUCT ENHANCEMENTS

Programmable DRAM Timing

Through Bit 24 in the DRAM Control Register, the DRAM controller now supports programmable DRAM timing, for either two- or three-cycle simple accesses, with single-cycle page-mode accesses. The new bit defined below.

Bit 24: Programmable DRAM Timing (PDT)—A 1 in this bit sets the DRAM timing to 2/1, for two-cycle simple accesses and single-cycle page-mode accesses. A 0 in this bit sets the DRAM timing to 3/1, for three-cycle simple accesses and single-cycle page-mode accesses.

FEATURES NO LONGER SUPPORTED

The following features are no longer supported on the Am29240EH, Am29245EH, and Am29243EH microcontrollers:

- 33 MHz operating frequency
- Scalable Clocking™ technology (also known as turbo mode or clock doubling)
- 16-bit DRAM memory
- MEMDRV signal
- MEMCLK as an input

CONNECTION DIAGRAM

208-Pin PQFP

Top Side View

Note:

Pin 1 is marked for orientation.

PQFP PIN DESIGNATIONS (Pin Number)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	Reserved	53	Reserved	105	Reserved	157	Reserved
2	MEMCLK	54	V_{CC}	106	V_{CC}	158	V_{CC}
3	MEMDRV	55	GND	107	GND	159	GND
4	INCLK	56	Reserved	108	Reserved	160	PIO12
5	V_{CC}	57	TXDB [3]	109	A23	161	PIO11
6	GND	58	RXDB [3]	110	A22	162	PIO10
7	ID31	59	$\overline{DTR}$A	111	A21	163	PIO9
8	ID30	60	RXDA	112	A20	164	PIO8
9	ID29	61	UCLK	113	A19	165	PIO7
10	ID28	62	$\overline{DSR}$A	114	A18	166	PIO6
11	ID27	63	TXDA	115	A17	167	PIO5
12	ID26	64	$\overline{ROMCS}$3	116	A16	168	PIO4
13	ID25	65	$\overline{ROMCS}$2	117	GND	169	GND
14	ID24	66	$\overline{ROMCS}$1	118	V_{CC}	170	V_{CC}
15	GND	67	$\overline{ROMCS}$0	119	A15	171	PIO3
16	V_{CC}	68	V_{CC}	120	A14	172	PIO2
17	ID23	69	GND	121	A13	173	PIO1
18	ID22	70	$\overline{BURST}$	122	A12	174	PIO0
19	ID21	71	$\overline{RSWE}$	123	A11	175	TDO
20	ID20	72	$\overline{ROMOE}$	124	A10	176	STAT2
21	ID19	73	$\overline{RAS}$3	125	A9	177	STAT1
22	ID18	74	$\overline{RAS}$2	126	A8	178	STAT0
23	ID17	75	$\overline{RAS}$1	127	GND	179	VDAT [2]
24	ID16	76	$\overline{RAS}$0	128	V_{CC}	180	PSYNC [2]
25	GND	77	$\overline{CAS}$3	129	A7	181	GND
26	V_{CC}	78	$\overline{CAS}$2	130	A6	182	V_{CC}
27	ID15	79	V_{CC}	131	A5	183	$\overline{GREQ}$
28	ID14	80	GND	132	A4	184	DREQB
29	ID13	81	$\overline{CAS}$1	133	A3	185	DREQA
30	ID12	82	$\overline{CAS}$0	134	A2	186	TDMA
31	ID11	83	$\overline{TR}$/$\overline{OE}$	135	A1	187	$\overline{TRAP}$0
32	ID10	84	$\overline{WE}$	136	A0	188	$\overline{TRAP}$1
33	ID9	85	$\overline{GACK}$	137	GND	189	$\overline{INTR}$0
34	ID8	86	$\overline{PIACS}$5	138	V_{CC}	190	$\overline{INTR}$1
35	GND	87	$\overline{PIACS}$4	139	BOOTW	191	$\overline{INTR}$2
36	V_{CC}	88	$\overline{PIACS}$3	140	$\overline{WAIT}$	192	$\overline{INTR}$3
37	ID7	89	$\overline{PIACS}$2	141	PAUTOFD	193	GND
38	ID6	90	V_{CC}	142	PSTROBE	194	V_{CC}
39	ID5	91	GND	143	$\overline{PWE}$	195	$\overline{WARN}$
40	ID4	92	$\overline{PIACS}$1	144	$\overline{POE}$	196	VCLK [2]
41	ID3	93	$\overline{PIACS}$0	145	PACK	197	LSYNC [2]
42	ID2	94	$\overline{PIAWE}$	146	$\overline{PBUSY}$	198	TMS
43	ID1	95	$\overline{PIAOE}$	147	GND	199	$\overline{TRST}$
44	ID0	96	R/$\overline{W}$	148	V_{CC}	200	TCK
45	GND	97	$\overline{DACK}$B	149	PIO15	201	TDI
46	V_{CC}	98	$\overline{DACK}$A	150	PIO14	202	$\overline{RESET}$
47	IDP3 [1, 3]	99	$\overline{DACK}$D [3]	151	PIO13	203	CNTL1
48	IDP2 [1, 3]	100	$\overline{DACK}$C [3]	152	DREQD [3]	204	CNTL0
49	IDP1 [1, 3]	101	V_{CC}	153	DREQC [3]	205	$\overline{TRIST}$
50	IDP0 [1, 3]	102	GND	154	GND	206	V_{CC}
51	GND	103	Reserved	155	V_{CC}	207	GND
52	Reserved	104	Reserved	156	Reserved	208	Reserved

Notes:

1. *Defined as no-connect on Am29240EH microcontroller.*
2. *Defined as no-connect on Am29243EH microcontroller.*
3. *Defined as no-connect on Am29245EH microcontroller.*

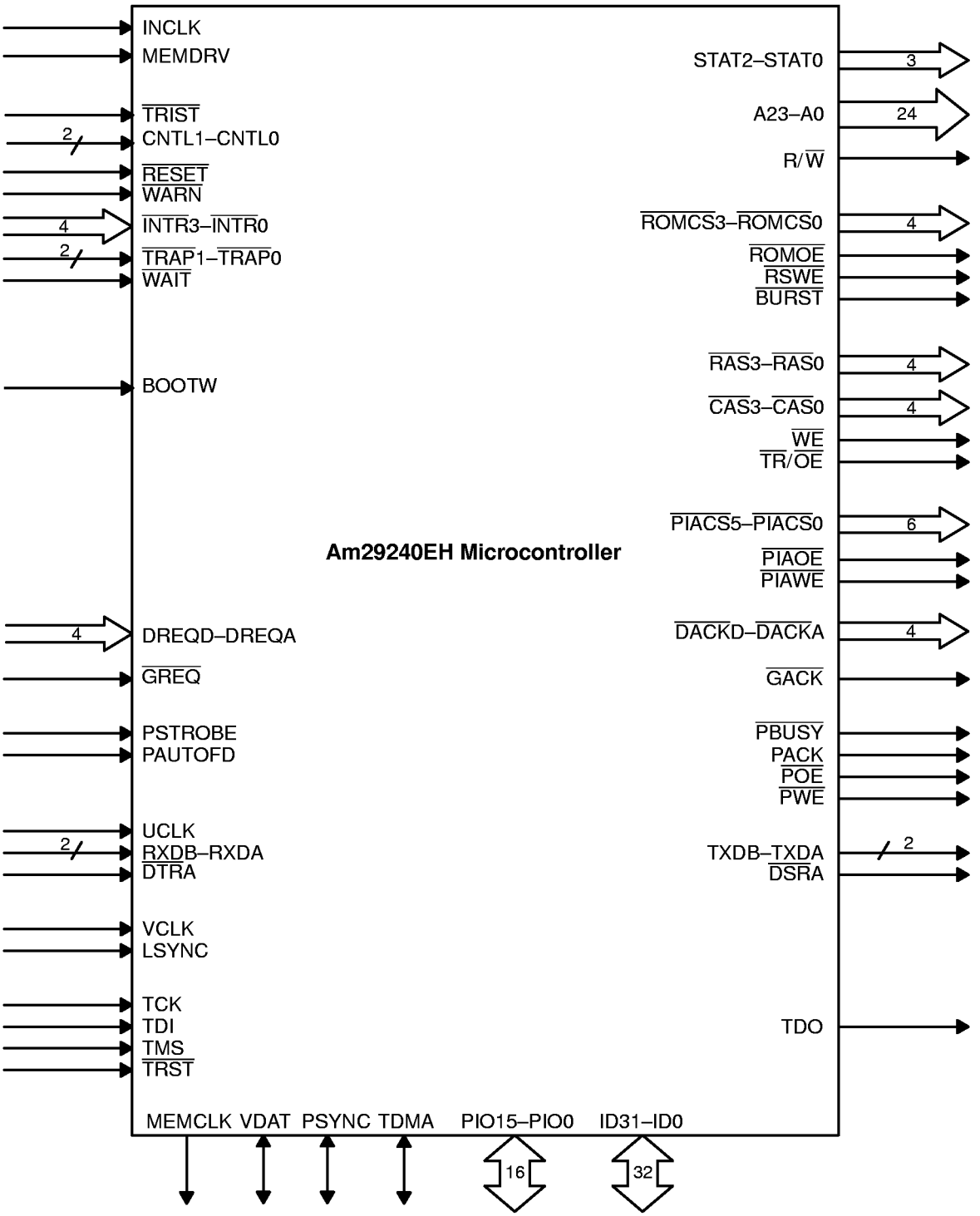
PQFP PIN DESIGNATIONS (Pin Name)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
A0	136	GND	91	$\overline{\text{INTR0}}$	189	$\overline{\text{RESET}}$	202
A1	135	GND	102	$\overline{\text{INTR1}}$	190	$\overline{\text{ROMCS0}}$	67
A2	134	GND	107	$\overline{\text{INTR2}}$	191	$\overline{\text{ROMCS1}}$	66
A3	133	GND	117	$\overline{\text{INTR3}}$	192	$\overline{\text{ROMCS2}}$	65
A4	132	GND	127	LSYNC [2]	197	$\overline{\text{ROMCS3}}$	64
A5	131	GND	137	MEMCLK	2	$\overline{\text{ROMOE}}$	72
A6	130	GND	147	MEMDRV	3	$\overline{\text{RSWE}}$	71
A7	129	GND	154	PACK	145	RXDA	60
A8	126	GND	159	PAUTOFD	141	RXDB [3]	58
A9	125	GND	169	$\overline{\text{PBUSY}}$	146	STAT0	178
A10	124	GND	181	$\overline{\text{PIACS0}}$	93	STAT1	177
A11	123	GND	193	$\overline{\text{PIACS1}}$	92	STAT2	176
A12	122	GND	207	$\overline{\text{PIACS2}}$	89	TCK	200
A13	121	Reserved	208	$\overline{\text{PIACS3}}$	88	TDI	201
A14	120	$\overline{\text{GREQ}}$	183	$\overline{\text{PIACS4}}$	87	TDMA	186
A15	119	ID0	44	$\overline{\text{PIACS5}}$	86	TDO	175
A16	116	ID1	43	$\overline{\text{PIAOE}}$	95	TMS	198
A17	115	ID2	42	$\overline{\text{PIAWE}}$	94	$\overline{\text{TR/OE}}$	83
A18	114	ID3	41	PIO0	174	$\overline{\text{TRAP0}}$	187
A19	113	ID4	40	PIO1	173	$\overline{\text{TRAP1}}$	188
A20	112	ID5	39	PIO2	172	$\overline{\text{TRIST}}$	205
A21	111	ID6	38	PIO3	171	$\overline{\text{TRST}}$	199
A22	110	ID7	37	PIO4	168	TXDA	63
A23	109	ID8	34	PIO5	167	TXDB [3]	57
BOOTW	139	ID9	33	PIO6	166	UCLK	61
$\overline{\text{BURST}}$	70	ID10	32	PIO7	165	Reserved	1
$\overline{\text{CAS0}}$	82	ID11	31	PIO8	164	V_{CC}	5
$\overline{\text{CAS1}}$	81	ID12	30	PIO9	163	V_{CC}	16
$\overline{\text{CAS2}}$	78	ID13	29	PIO10	162	V_{CC}	26
$\overline{\text{CAS3}}$	77	ID14	28	PIO11	161	V_{CC}	36
CNTL0	204	ID15	27	PIO12	160	V_{CC}	46
CNTL1	203	ID16	24	PIO13	151	V_{CC}	54
$\overline{\text{DACKA}}$	98	ID17	23	PIO14	150	V_{CC}	68
$\overline{\text{DACKB}}$	97	ID18	22	PIO15	149	V_{CC}	79
$\overline{\text{DACKC}}$ [3]	100	ID19	21	$\overline{\text{POE}}$	144	V_{CC}	90
$\overline{\text{DACKD}}$ [3]	99	ID20	20	PSTROBE	142	V_{CC}	101
DREQA	185	ID21	19	PSYNC [2]	180	V_{CC}	106
DREQB	184	ID22	18	$\overline{\text{PWE}}$	143	V_{CC}	118
DREQC [3]	153	ID23	17	R/$\overline{\text{W}}$	96	V_{CC}	128
DREQD [3]	152	ID24	14	$\overline{\text{RAS0}}$	76	V_{CC}	138
$\overline{\text{DSRA}}$	62	ID25	13	$\overline{\text{RAS1}}$	75	V_{CC}	148
$\overline{\text{DTRA}}$	59	ID26	12	$\overline{\text{RAS2}}$	74	V_{CC}	155
$\overline{\text{GACK}}$	85	ID27	11	$\overline{\text{RAS3}}$	73	V_{CC}	158
GND	6	ID28	10	Reserved	52	V_{CC}	170
GND	15	ID29	9	Reserved	53	V_{CC}	182
GND	25	ID30	8	Reserved	56	V_{CC}	194
GND	35	ID31	7	Reserved	103	V_{CC}	206
GND	45	IDP0 [1,3]	50	Reserved	104	VCLK [2]	196
GND	51	IDP1 [1,3]	49	Reserved	105	VDAT [2]	179
GND	55	IDP2 [1,3]	48	Reserved	108	$\overline{\text{WAIT}}$	140
GND	69	IDP3 [1,3]	47	Reserved	156	$\overline{\text{WARN}}$	195
GND	80	INCLK	4	Reserved	157	$\overline{\text{WE}}$	84

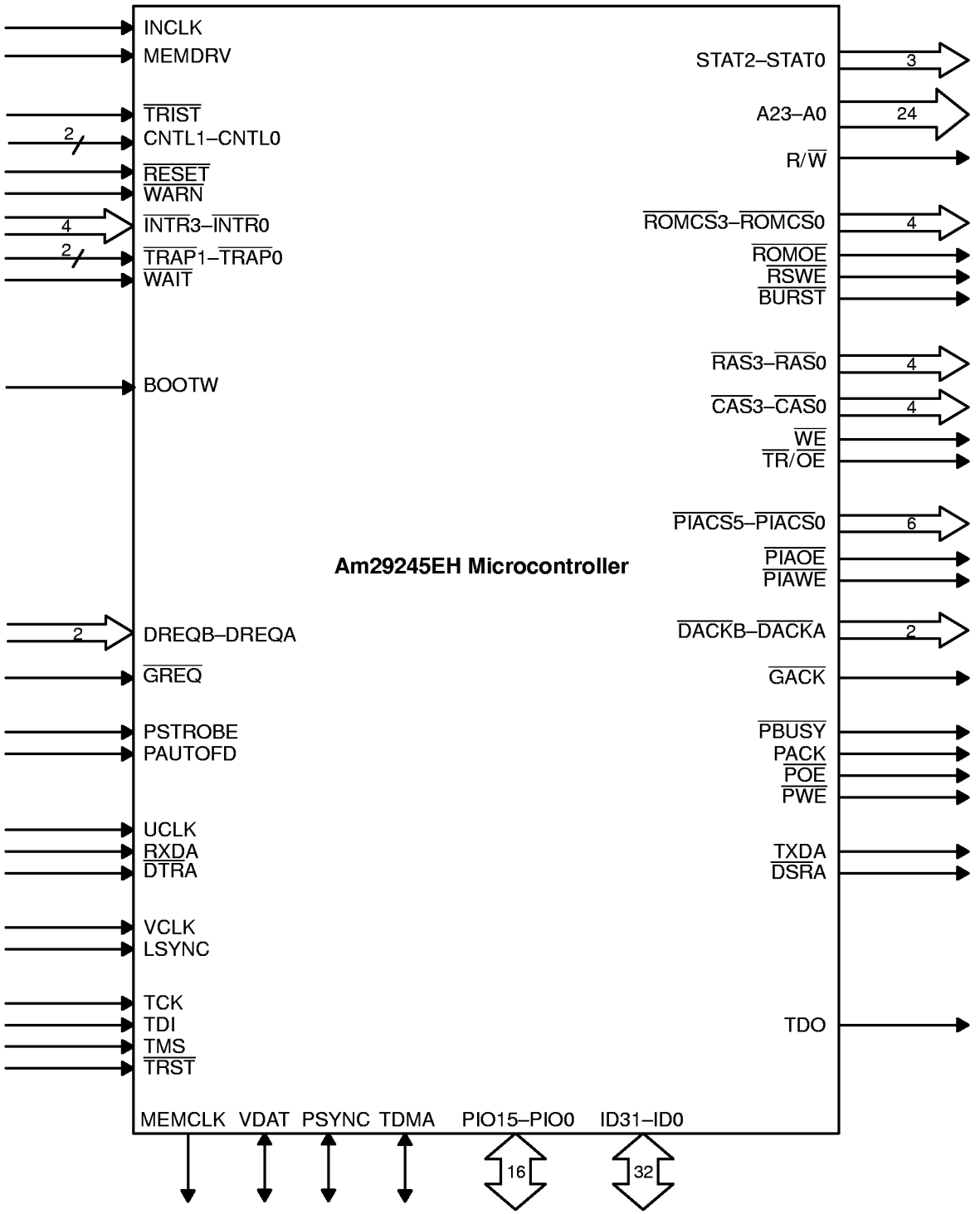
Notes:

1. *Defined as no-connect on Am29240EH microcontroller.*
2. *Defined as no-connect on Am29243EH microcontroller.*
3. *Defined as no-connect on Am29245EH microcontroller.*

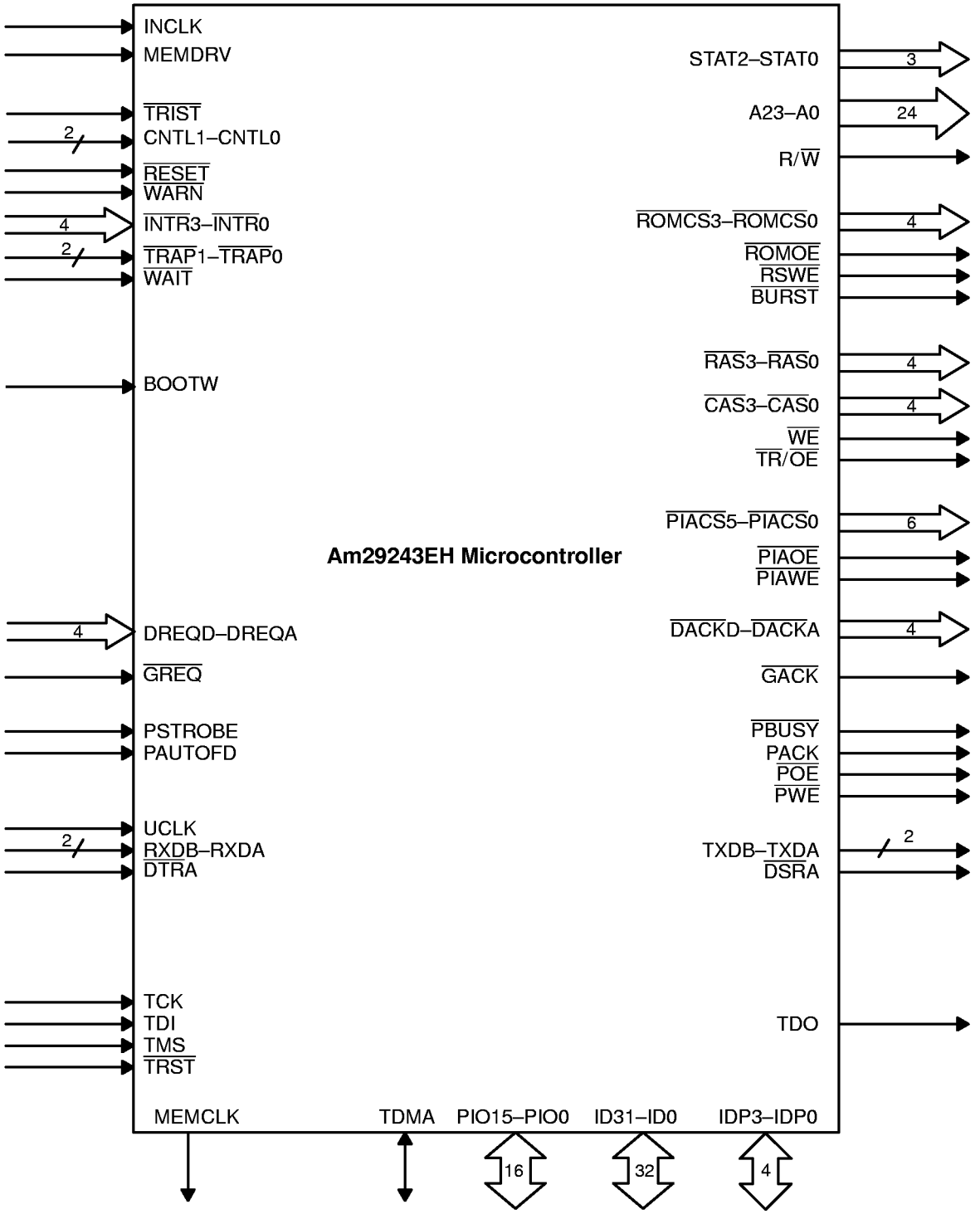
Am29240EH MICROCONTROLLER LOGIC SYMBOL



Am29245EH MICROCONTROLLER LOGIC SYMBOL



Am29243EH MICROCONTROLLER LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +125°C
Voltage on any Pin
with Respect to GND . . . . . –0.5 V to V_{CC} +2.4

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C) . . . . . 0°C to +85°C
Supply Voltage (V_{CC}) . . . . . +3 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL Operating Ranges

Symbol	Parameter Description	Test Conditions	Preliminary		Unit
			Min	Max	
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} +2.4	V
$V_{ILINCLK}$	INCLK Input Low Voltage		–0.5	0.8	V
$V_{IHINCLK}$	INCLK Input High Voltage		2.4	5.5	V
V_{OL}	Output Low Voltage for All Outputs except MEMCLK	I_{OL} = 3.2 mA		0.5	V
V_{OH}	Output High Voltage for All Outputs except MEMCLK	I_{OH} = –400 µA	2.4		V
I_{LI}	Input Leakage Current	0.45 V ≤ V_{IN} ≤ V_{CC} –0.45 V Note 1		±10 or +10/–200	µA
I_{LO}	Output Leakage Current	0.45 V ≤ V_{OUT} ≤ V_{CC} –0.45 V		±10	µA
I_{CCOP}	Operating Power-Supply Current with respect to MEMCLK	V_{CC} = 3.6 V, Outputs Floating; Holding $\overline{\text{RESET}}$ active at 25 MHz		8	mA/MHz
V_{OLC}	MEMCLK Output Low Voltage	I_{OLC} = 20 mA		0.6	V
V_{OHC}	MEMCLK Output High Voltage	I_{OHC} = –20 mA	2.4		V
I_{OSGND}	MEMCLK GND Short Circuit Current	V_{CC} = 3.3 V	100		mA
I_{OSVCC}	MEMCLK V_{CC} Short Circuit Current	V_{CC} = 3.3 V	100		mA

Notes:

1. *The Low input leakage current for the inputs* CNTL1–CNTL0, $\overline{\text{INTR}}$3–$\overline{\text{INTR}}$0, $\overline{\text{TRAP}}$1–$\overline{\text{TRAP}}$0, DREQD–DREQA, TCK, TDI, $\overline{\text{RESET}}$, $\overline{\text{TRST}}$, TMS, $\overline{\text{GREQ}}$, $\overline{\text{WARN}}$, MEMDRV, $\overline{\text{WAIT}}$, *and* $\overline{\text{TRIST}}$ *is –200 µA. These pins have internal pull-up resistors.*

CAPACITANCE

Symbol	Parameter Description	Test Conditions	Preliminary		Unit
			Min	Max	
C_{IN}	Input Capacitance	fC = 10 MHz		15	pF
C_{INCLK}	INCLK Input Capacitance			15	pF
C_{MEMCLK}	MEMCLK Capacitance			20	pF
C_{OUT}	Output Capacitance			20	pF
$C_{I/O}$	I/O Pin Capacitance			20	pF

Note: *Limits guaranteed by characterization.*

SWITCHING CHARACTERISTICS over COMMERCIAL Operating Ranges

No.	Parameter Description	Test Conditions [1]	Preliminary						Unit
			16 MHz		20 MHz		25 MHz		
			Min	Max	Min	Max	Min	Max	
1	INCLK Period (=0.5T)		30	50	25	50	20	50	ns
2	INCLK High Time		10		8		6		ns
3	INCLK Low Time		10		8		6		ns
4	INCLK Rise Time		0	5	0	5	0	5	ns
5	INCLK Fall Time		0	5	0	5	0	5	ns
6	MEMCLK Delay from INCLK	Note 1C, 3	1	7	1	7	1	7	ns
8	MEMCLK High Time	Note 1C	0.5T–3		0.5T–3		0.5T–3		ns
9	MEMCLK Low Time	Note 1C	0.5T–3		0.5T–3		0.5T–3		ns
10	MEMCLK Rise Time	Note 1C	1	4	1	4	1	4	ns
11	MEMCLK Fall Time	Note 1C	1	4	1	4	1	4	ns
12a	Synchronous Output Valid Delay from MEMCLK Rising Edge								
	PIO15–PIO0, STAT2–STAT0, $\overline{\text{PIACS}}$5–$\overline{\text{PIACS}}$0, and $\overline{\text{RAS}}$3–$\overline{\text{RAS}}$0	Note 1A	1	13	1	12	1	11	ns
	$\overline{\text{CAS}}$3–$\overline{\text{CAS}}$0 Rising Edge/ $\overline{\text{CAS}}$3–$\overline{\text{CAS}}$0 Falling Edge	Notes 1B, 4B	1	17/11	1	15/9	1	13/7	ns
	All others	Note 1B	1	12	1	11	1	10	ns
12b	Synchronous Output Valid Delay from MEMCLK Falling Edge								
	PIO15–PIO0, STAT2–STAT0, $\overline{\text{PIACS}}$5–$\overline{\text{PIACS}}$0	Note 1A	1	12	1	11	1	10	ns
	$\overline{\text{RAS}}$3–$\overline{\text{RAS}}$0	Note 1B	1	15	1	14	1	13	ns
	$\overline{\text{CAS}}$3–$\overline{\text{CAS}}$0 Falling Edge	Notes 1B, 4B	1	11	1	9	1	7	ns
	All others	Note 1B	1	11	1	10	1	9	ns
13	Synchronous Output Disable Delay from MEMCLK Rising Edge		1	12	1	11	1	10	ns
14	Synchronous Input Setup Time to MEMCLK Rising Edge								
	ID31–ID0 and IDP3–IDP0 for DRAM access	Parity Enabled Note 4A	18		16		15		ns
	ID31–ID0 for DRAM access	Parity Disabled Note 4A	10		8		7		ns
	All others		10		8		7		ns
15	Available CAS Access Time ($\overline{\text{TCAS}}$–T_{Setup})	Note 4B		25		24		19	ns
16a	Synchronous Input Hold Time to MEMCLK Rising Edge	Note 4A	0		0		0		ns
16b	Synchronous Input Hold Time to $\overline{\text{CAS}}$ Rising Edge	Note 4B	3		3		3		ns

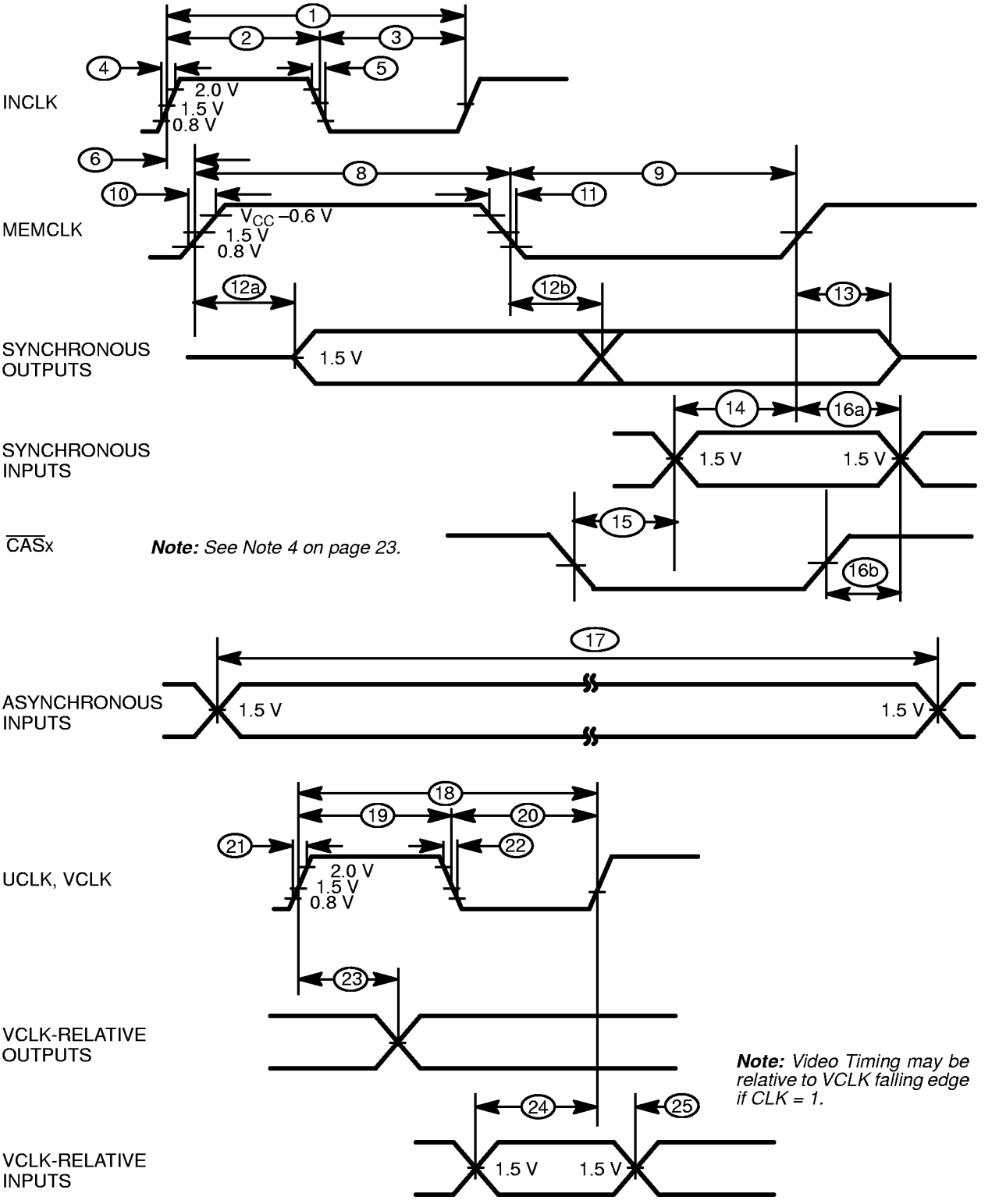
SWITCHING CHARACTERISTICS over COMMERCIAL Operating Ranges (continued)

No.	Parameter Description	Test Conditions [1]	Preliminary						Unit
			16 MHz		20 MHz		25 MHz		
			Min	Max	Min	Max	Min	Max	
17	Asynchronous Input Pulse Width								
	LSYNC and PSYNC		Note 5		Note 5		Note 5		
	All others		4T		4T		4T		ns
18	UCLK Period	Note 2	30		25		20		ns
	VCLK Period	Note 2	25		20		15		ns
19	UCLK High Time	Note 2	10		8		6		ns
	VCLK High Time	Note 2	8		6		4		ns
20	UCLK Low Time	Note 2	10		8		6		ns
	VCLK Low Time	Note 2	8		6		4		ns
21	UCLK Rise time	Note 2	0	5	0	5	0	5	ns
	VCLK Rise time	Note 2	0	3	0	3	0	3	ns
22	UCLK Fall Time	Note 2	0	5	0	5	0	5	ns
	VCLK Fall Time	Note 2	0	3	0	3	0	3	ns
23	Synchronous Output Valid Delay from VCLK Rise and Fall	Note 6	1	16	1	14	1	14	ns
24	Input Setup Time to VCLK Rise and Fall	Notes 6, 7	10		9		9		ns
25	Input Hold Time to VCLK Rise and Fall	Notes 6, 7	0		0		0		ns
26	$\overline{\text{RAS}}$ Low Time		50		50		50		ns
27	$\overline{\text{CAS}}$ Low Time		13		13		13		ns

Notes:

1. *All outputs driving 80 pF, measured at V_{OL} = 1.5 V and V_{OH} = 1.5 V using the switching test circuit shown on page 33. For higher capacitance loads:*
   A. Add 1 ns output delay per 15 pF loading above 80 pF, up to 150 pF total. The minimum delay from $\overline{\text{PIAOE}}$ to $\overline{\text{PIACS}}$x is 0 ns if the capacitance loading on $\overline{\text{PIACS}}$x is equal to or higher than the capacitance loading on $\overline{\text{PIAOE}}$.
   B. Add 1 ns output delay per 25 pF loading above 80 pF, up to 300 pF total. For 2/1 DRAM timing, in order to meet the setup time (t_{ASR}) from A23–A0 to $\overline{\text{RAS}}$3–$\overline{\text{RAS}}$0 for DRAM, the capacitive loading of A23–A0 must not exceed the capacitance loading of $\overline{\text{RAS}}$3–$\overline{\text{RAS}}$0 by more than 150 pF.
   C. Add 1 ns of output delay for MEMCLK to drive an external load of 100 pF.
2. *VCLK and UCLK can be driven with TTL inputs. UCLK must be tied High if it is unused.*
3. *Maximum INCLK-to-MEMCLK delay can be decreased by 0.5 ns for each 10 mA increase in I_{OL} up to the maximum of 20 mA, i.e., 6 ns maximum delay at I_{OL} = 20 mA.*
4. *ID31–ID0 and IDP3–IDP0 are sampled on the rising edge of MEMCLK for all non-DRAM accesses, simple DRAM accesses, and the first access of a DRAM page-mode access. ID31–ID0 and IDP3–IDP0 are sampled on the rising edge of $\overline{\text{CAS}}$x for all DRAM page-mode accesses, except the first access of a DRAM page-mode access. (See Figures 1–12 on pages 25–32.)*
   A. Applies to ID31–ID0 and IDP3–IDP0 for simple DRAM accesses and the first access of a DRAM page-mode access.
   B. Applies to ID31–ID0 and IDP3–IDP0 for DRAM page-mode accesses, except the first access of a DRAM page-mode access. When ID31–ID0 and IDP3–IDP0 are sampled on $\overline{\text{CAS}}$x, there is no additional setup time required for ID31–ID0 and IDP3–IDP0 when the parity is enabled.
5. *LSYNC and PSYNC minimum width is two bit-times. A bit-time is one period of the internal video clock, which is determined by the CLKDIV field in the Video Control Register and VCLK.*
6. *Active VCLK edge depends on the CLKI bit in the Video Control Register.*
7. *LSYNC and PSYNC can be treated as synchronous signals by meeting the setup and hold times, though the synchronization delay still applies.*

SWITCHING WAVEFORMS



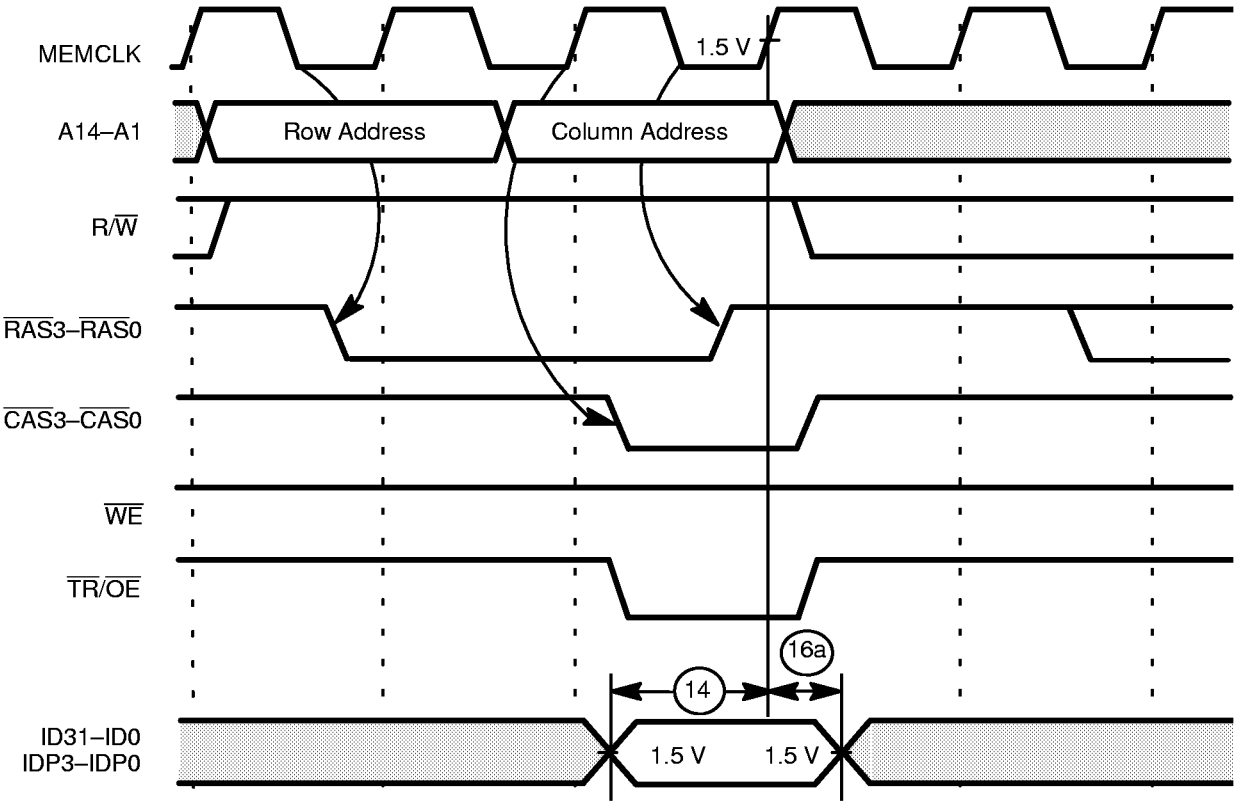
Note: *See Note 4 on page 23.*

Note: *Video Timing may be relative to VCLK falling edge if CLK = 1.*

Note:

During AC testing, all inputs are driven at V_{IL} = 0.4 V, V_{IH} = 2.4 V.

SWITCHING WAVEFORMS (continued)



Note: The RAS3–RAS0 *signals are asserted and deasserted on the falling edge of* MEMCLK.

Figure 1. Simple 3/1 DRAM Read Cycle

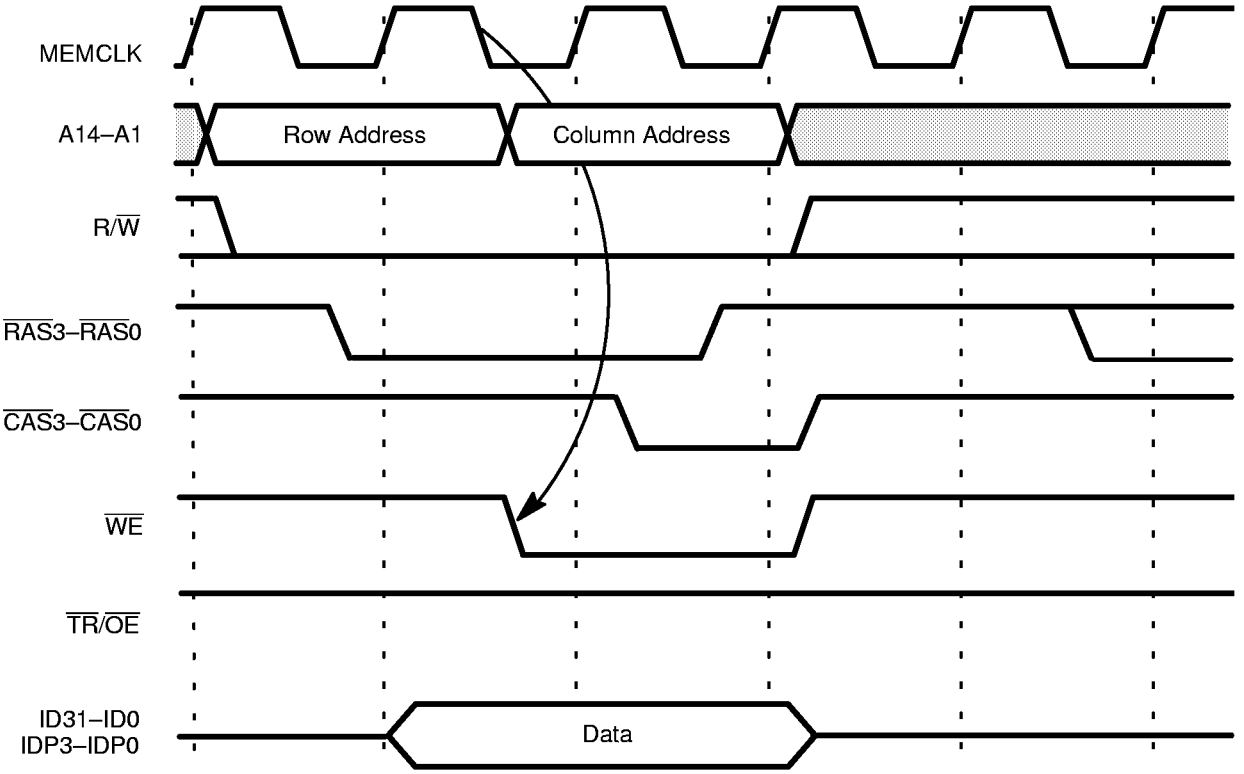
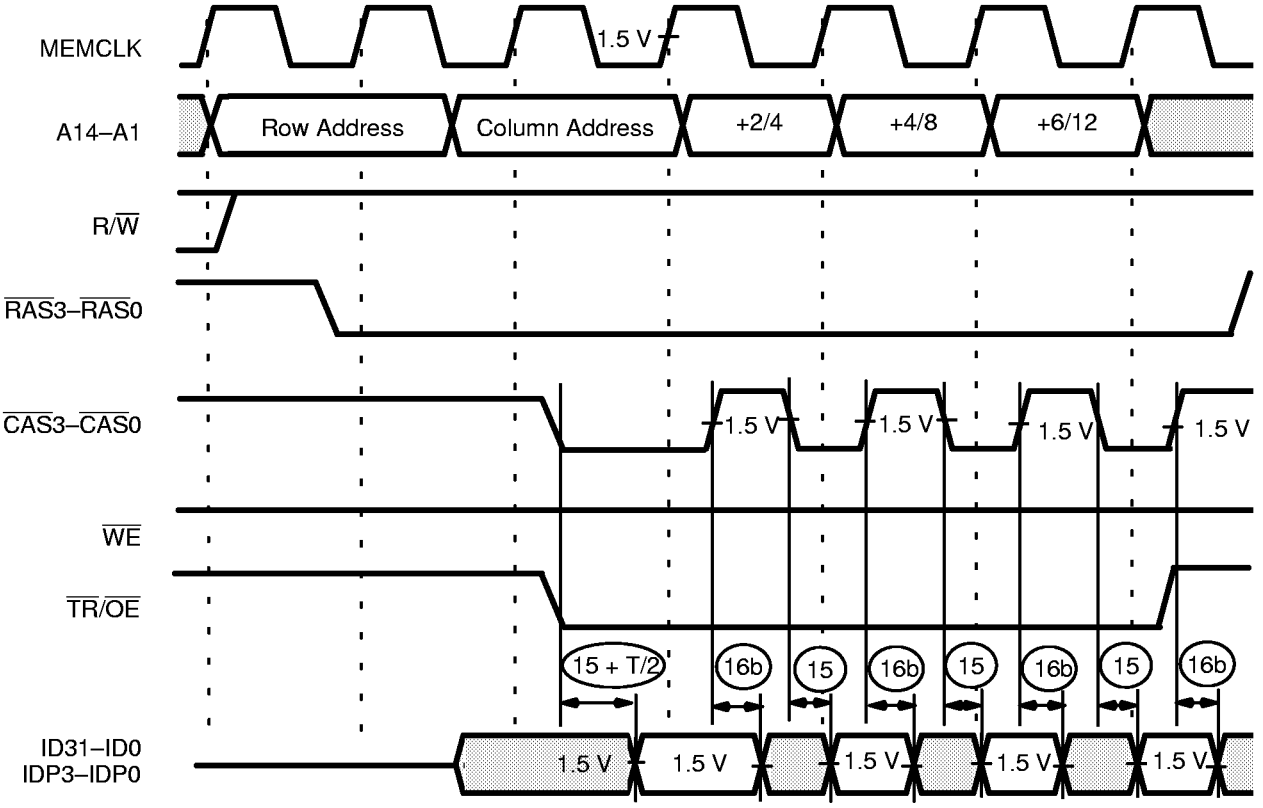


Figure 2. Simple 3/1 DRAM Write Cycle

SWITCHING WAVEFORMS (continued)



Note: The RAS3–RAS0 signals are *asserted and deasserted on the falling edge of* MEMCLK.

Figure 3. 3/1 DRAM Page-Mode Read

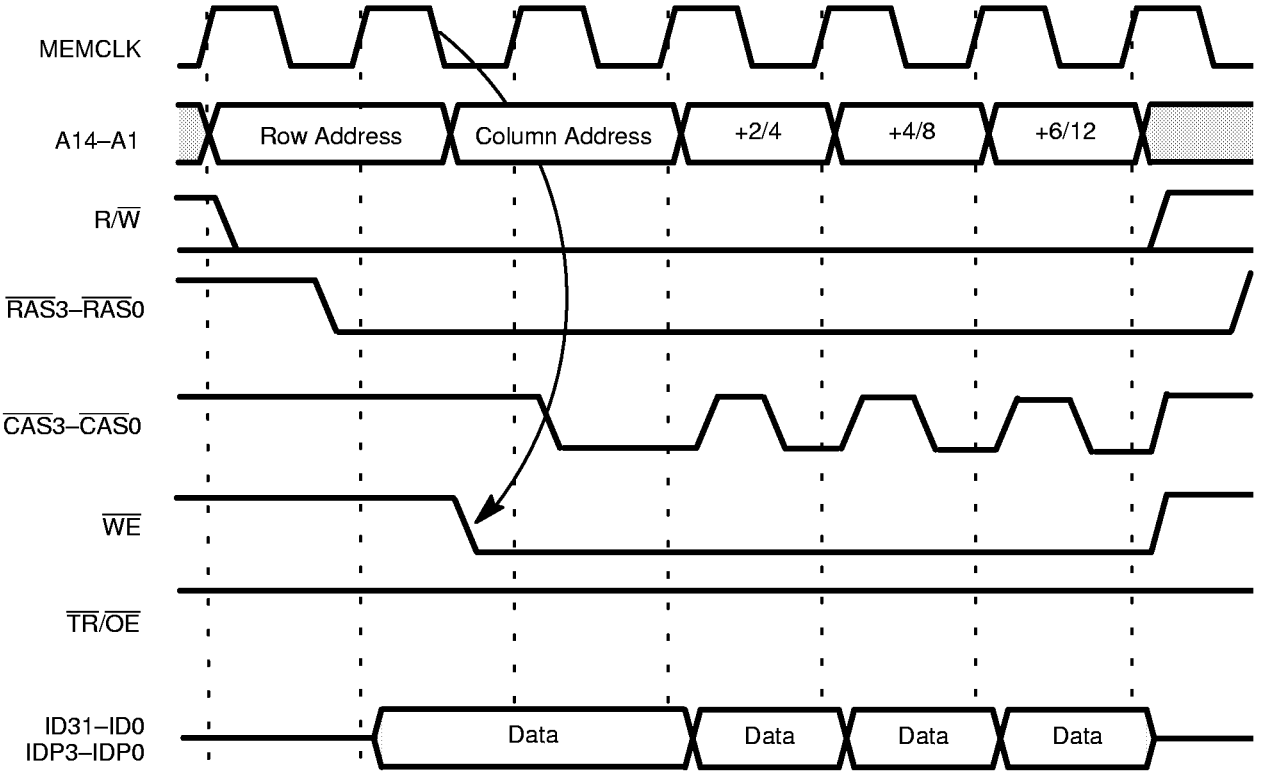


Figure 4. 3/1 DRAM Page-Mode Write

SWITCHING WAVEFORMS (continued)

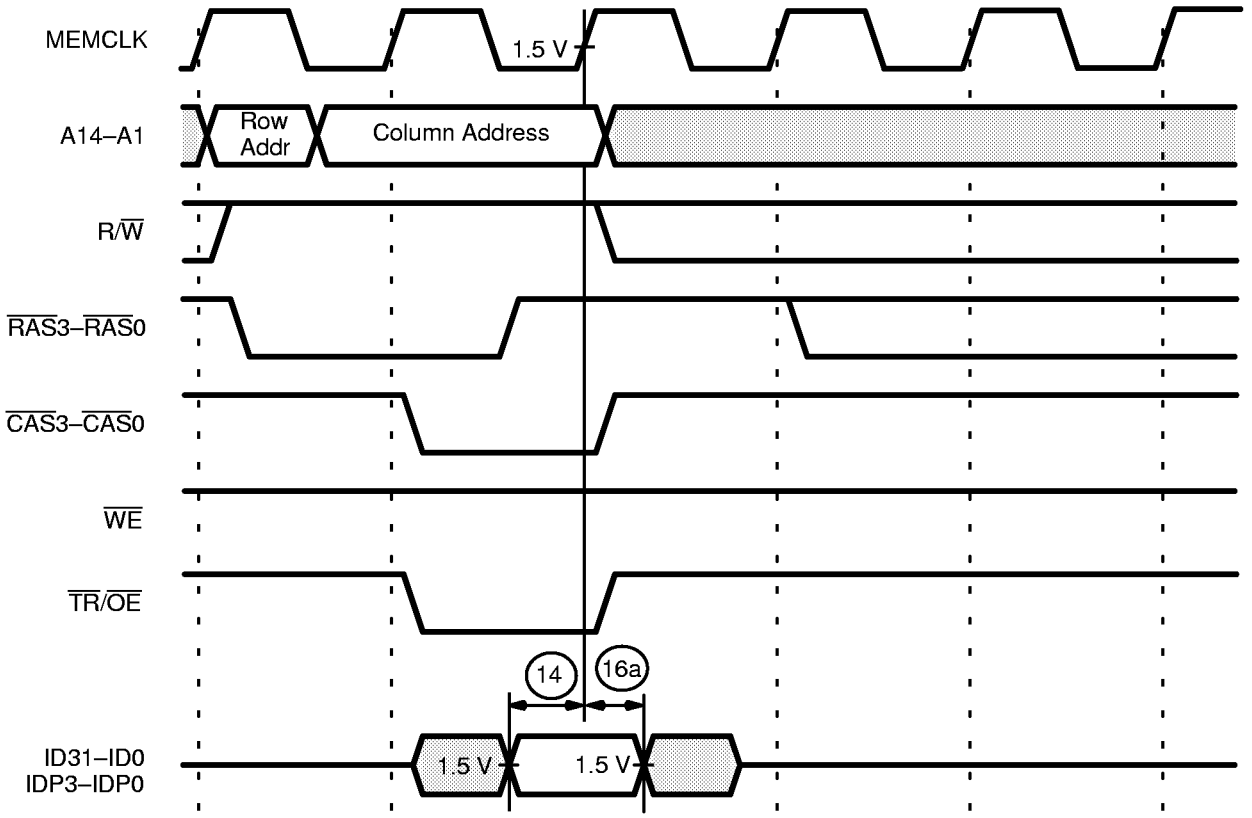


Figure 5. Simple 2/1 DRAM Read Cycle

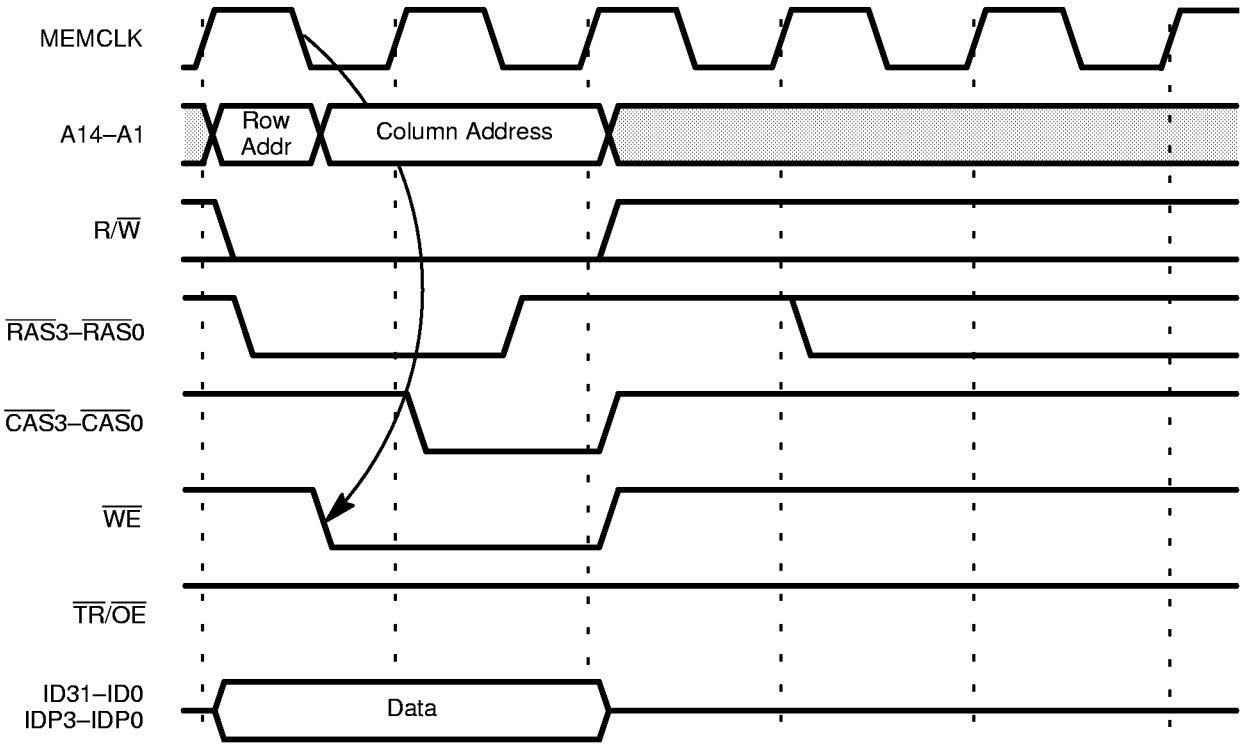
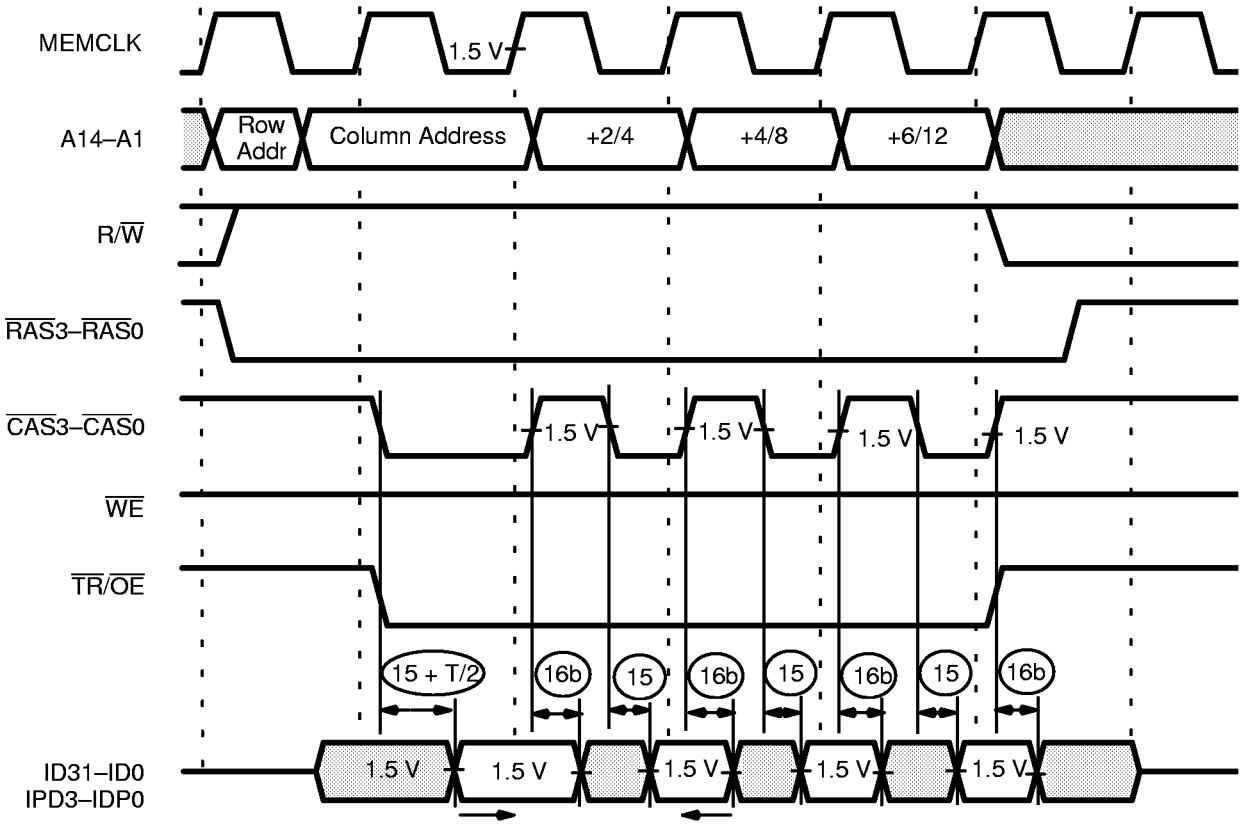


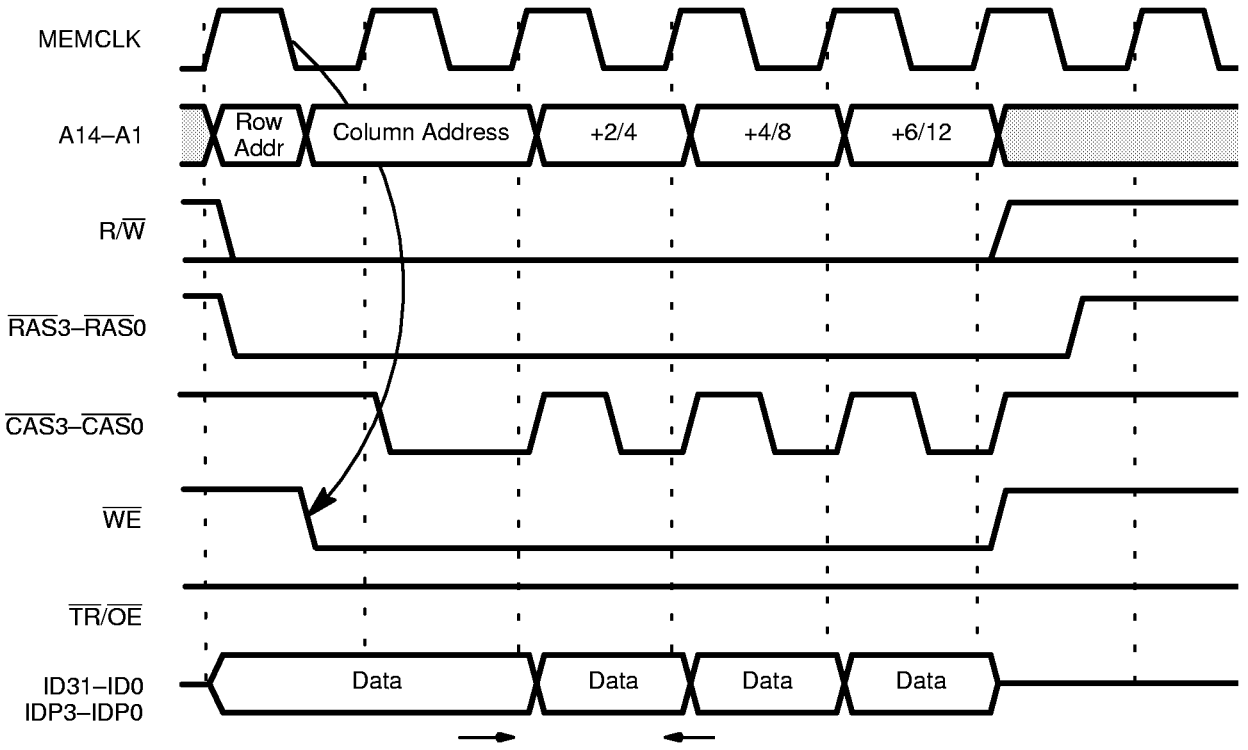
Figure 6. Simple 2/1 DRAM Write Cycle

SWITCHING WAVEFORMS (continued)



***Note**: May be repeated up to 1-Kbyte address boundary.*

Figure 7. 2/1 DRAM Page-Mode Read Cycle



***Note**: May be repeated up to 1-Kbyte address boundary.*

Figure 8. 2/1 DRAM Page-Mode Write Cycle

SWITCHING WAVEFORMS (continued)

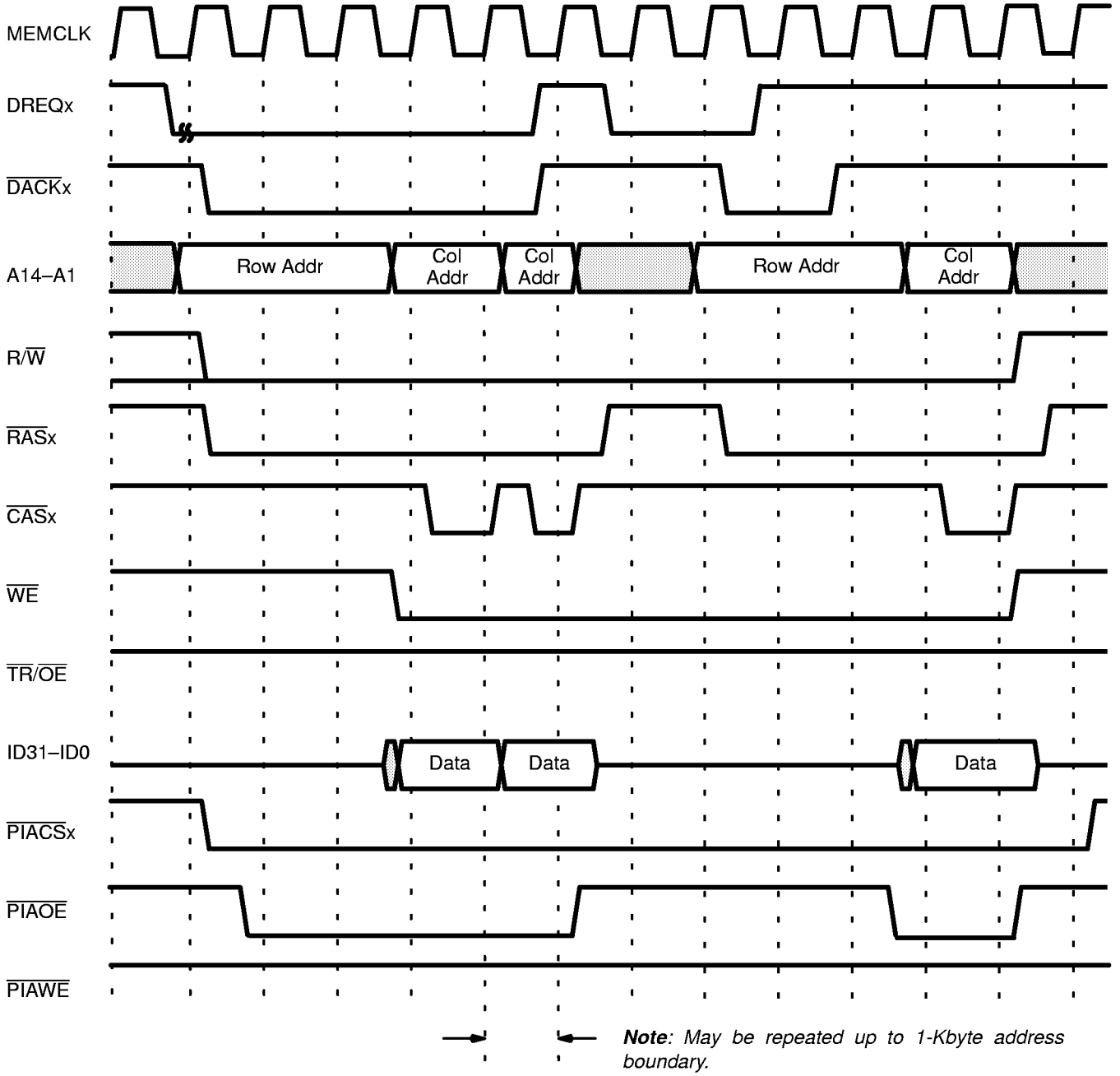


Figure 9. Fly-By DMA Reads (Read Peripheral, Write DRAM)—3/1 DRAM Accesses

SWITCHING WAVEFORMS (continued)

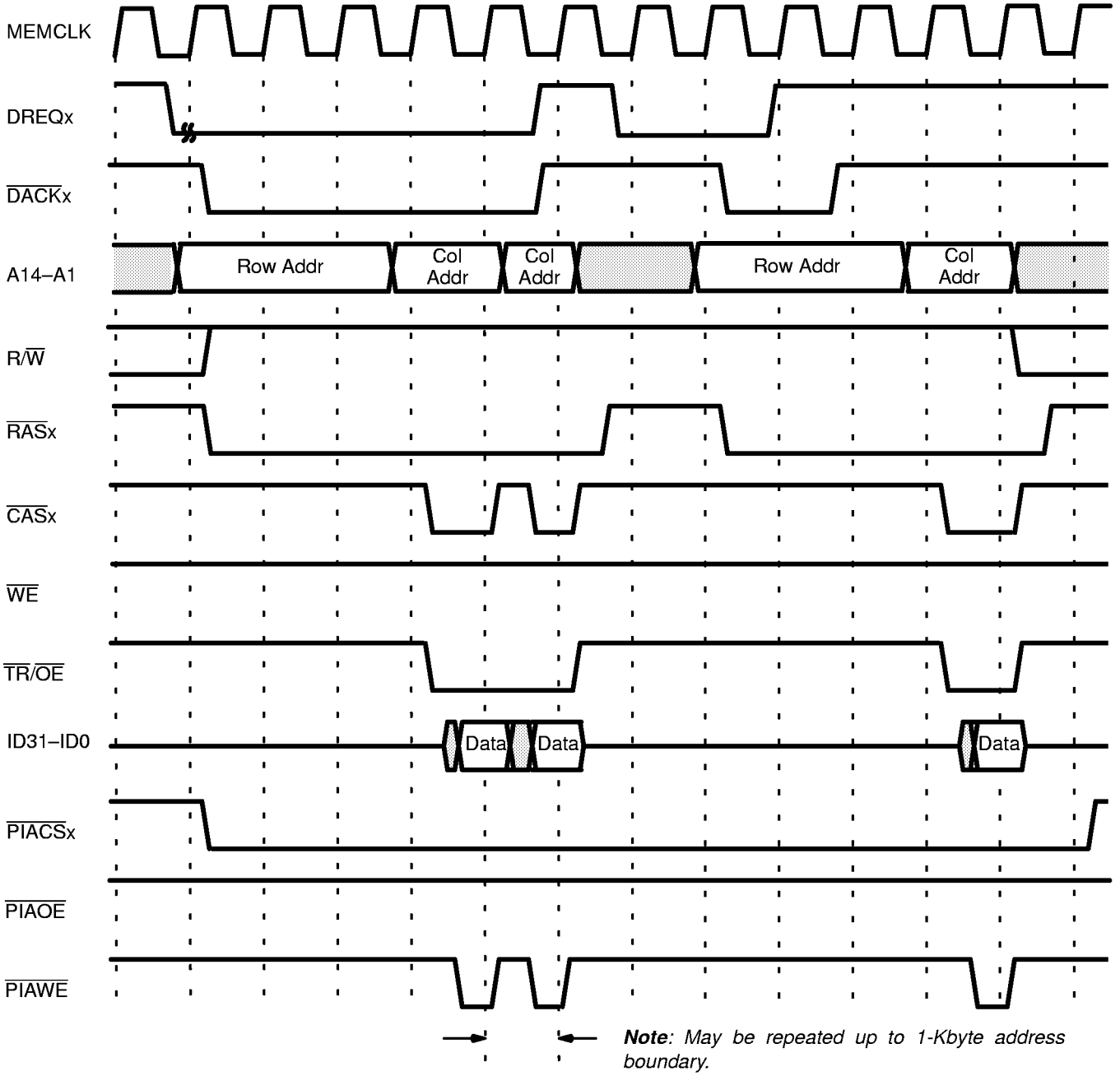


Figure 10. Fly-By DMA Writes (Read DRAM, Write Peripheral)—3/1 DRAM Accesses

SWITCHING WAVEFORMS (continued)

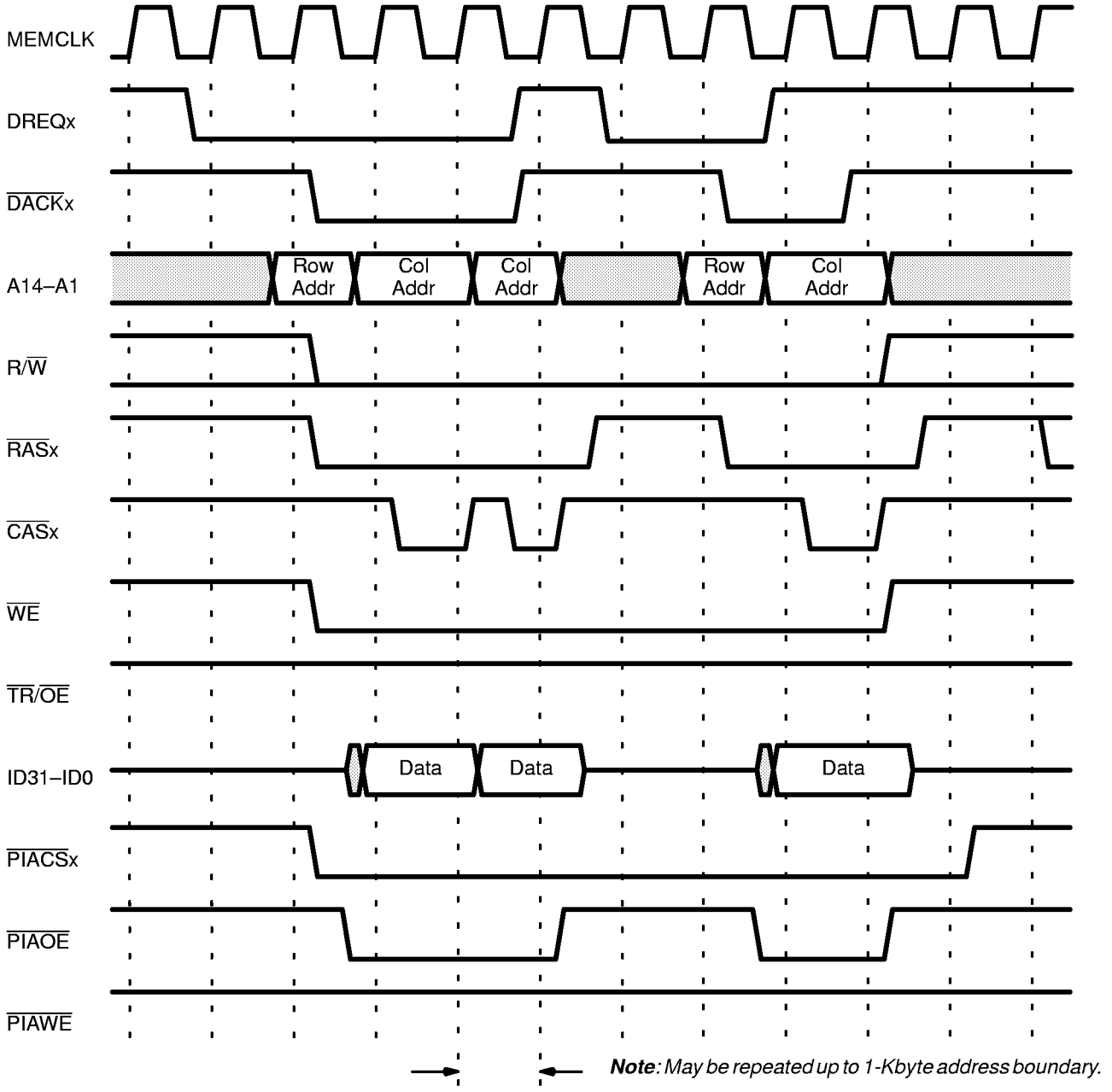


Figure 11. Fly-By DMA Reads (Read Peripheral, Write DRAM)—2/1 DRAM Accesses

SWITCHING WAVEFORMS (continued)

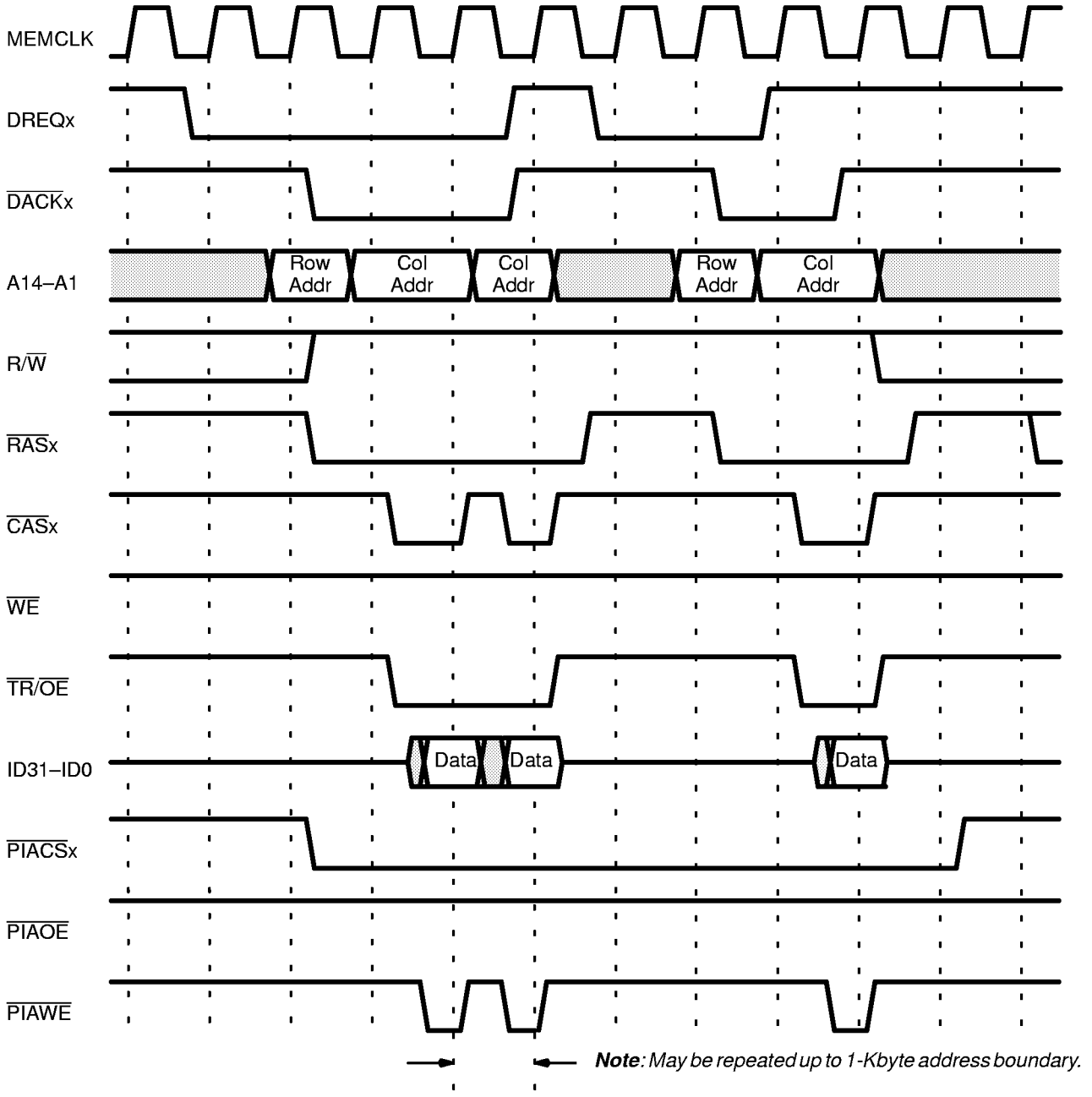
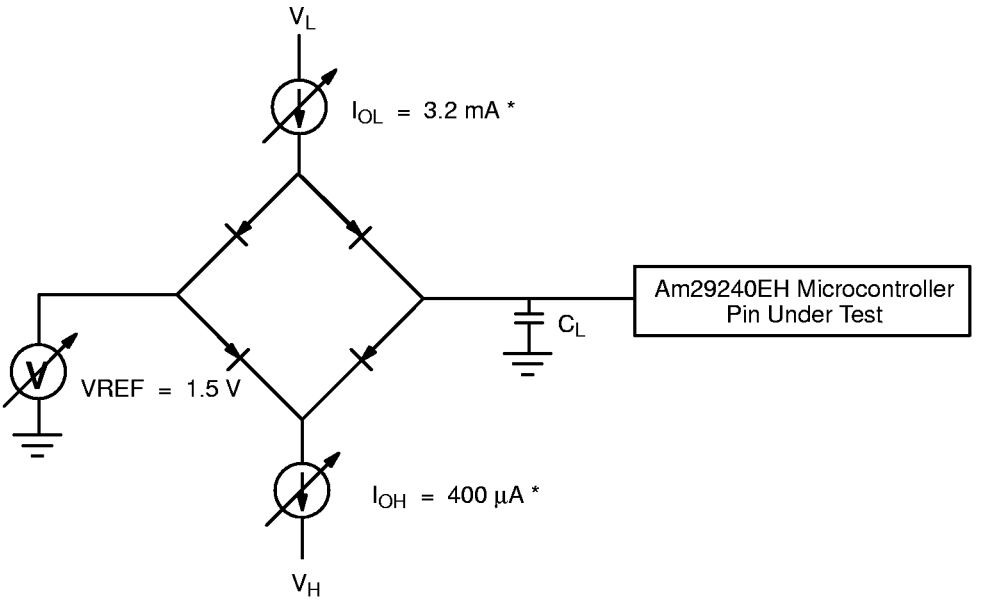


Figure 12. Fly-By DMA Writes (Read DRAM, Write Peripheral)—2/1 DRAM Accesses

SWITCHING TEST CIRCUIT

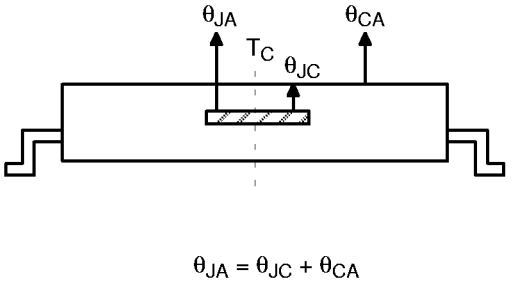


Note:

**All outputs except MEMCLK. MEMCLK is tested with I_{OL} = 20 mA and I_{OH} = –20mA.*

THERMAL CHARACTERISTICS

The Am29240EH microcontroller series is specified for operation with case temperature ranges for a commercial temperature device. Case temperature is measured at the top center of the PQFP package as shown in Figure 13.



$\theta_{JA} = \theta_{JC} + \theta_{CA}$

Figure 13. Thermal Resistance — °C/Watt

The various temperatures and thermal resistances can be determined using the equations shown in Figure 14 along with information given in Table 2. (The variable *P* is power in watts.)

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$
$$P = I_{CCOP} \cdot freq \cdot V_{CC}$$
$$T_J = T_C + P \cdot \theta_{JC}$$
$$T_J = T_A + P \cdot \theta_{JA}$$
$$T_C = T_J - P \cdot \theta_{JC}$$
$$T_C = T_A + P \cdot \theta_{CA}$$
$$T_A = T_J - P \cdot \theta_{JA}$$
$$T_A = T_C - P \cdot \theta_{CA}$$

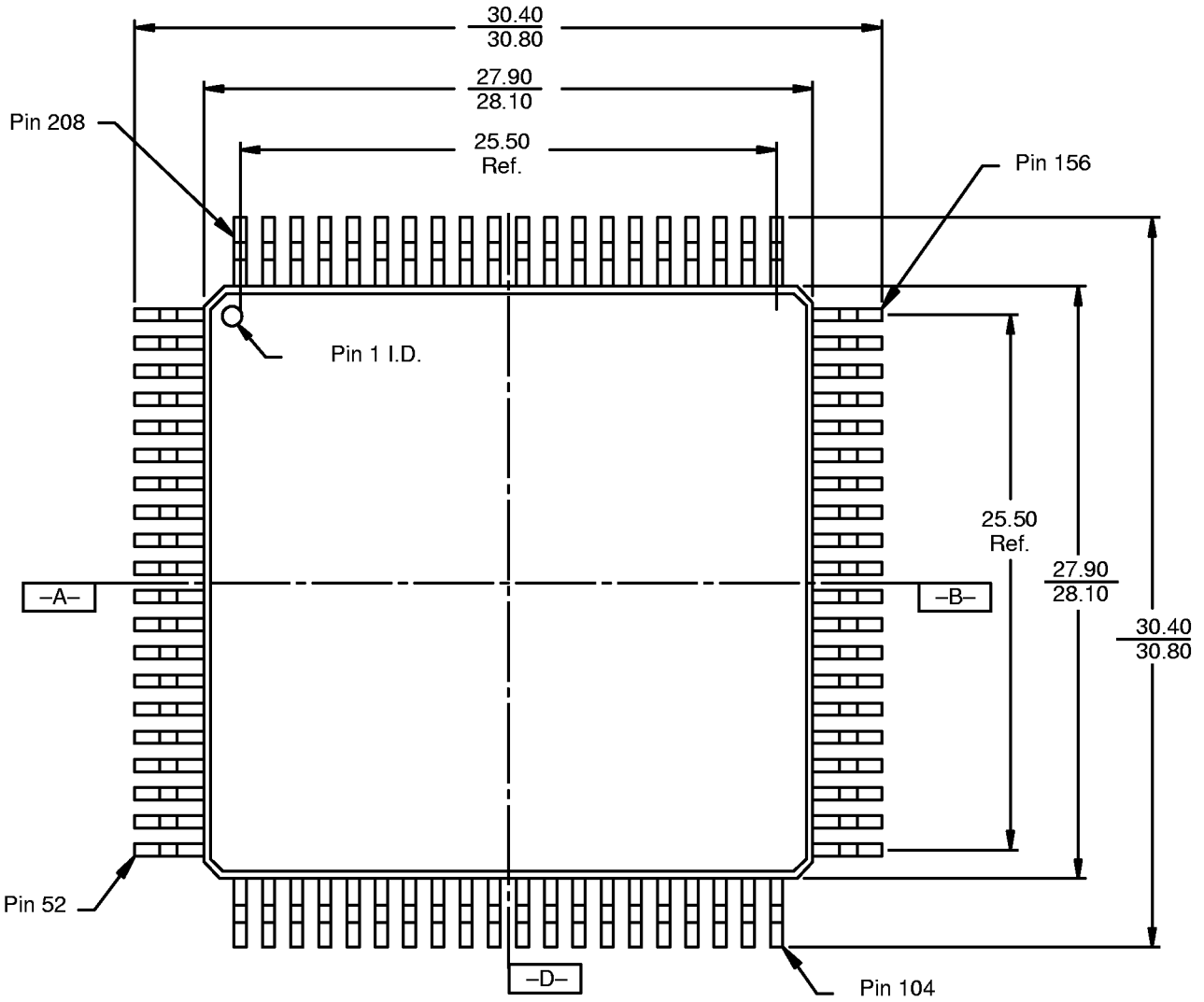
Figure 14. Thermal Characteristics Equations

Table 2. Thermal Characteristics (°C/Watt) Surface Mounted

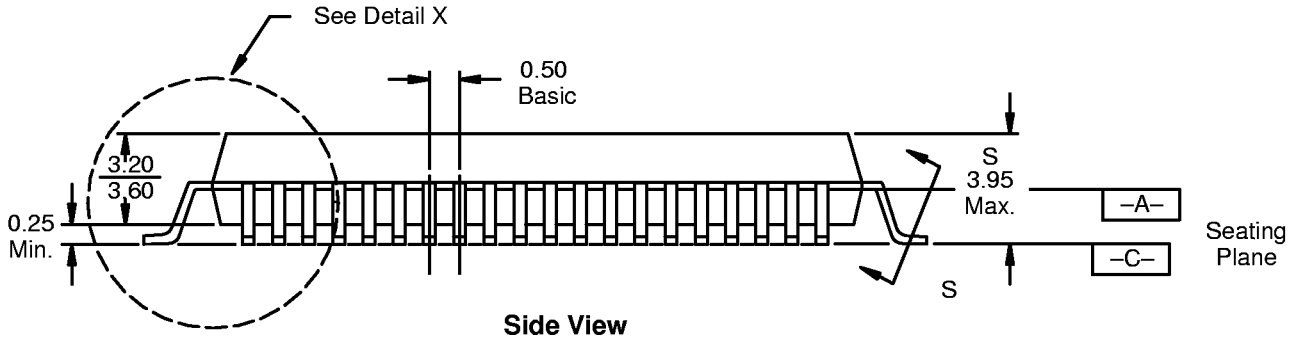
Parameter		°C/Watt
θ_{JA}	Junction-to-Ambient	38
θ_{JC}	Junction-to-Case	8
θ_{CA}	Case-to-Ambient	30

PHYSICAL DIMENSIONS

PQR 208, Trimmed and Formed Plastic Quad Flat Pack



Top View



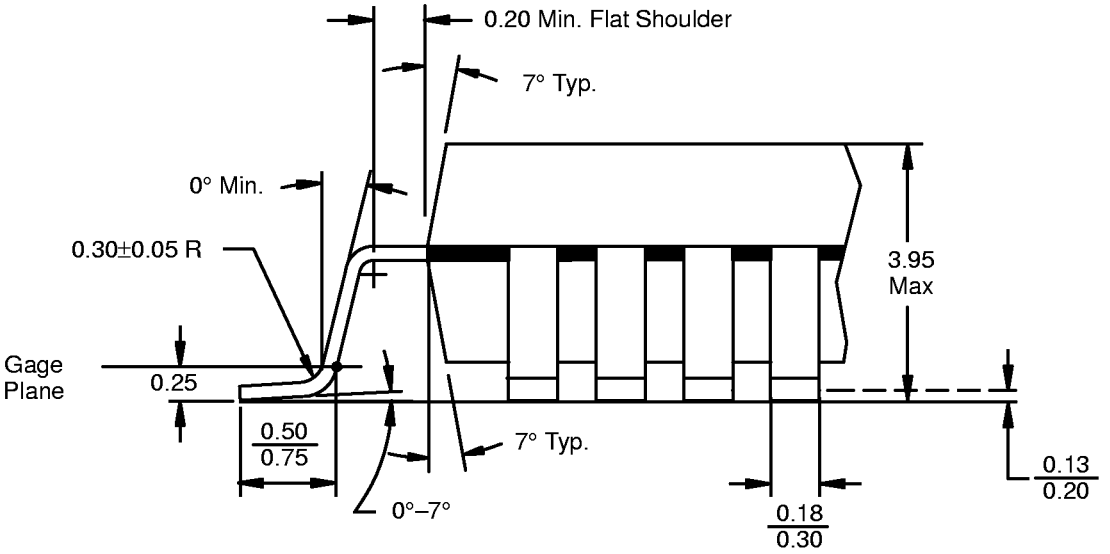
Side View

Notes:

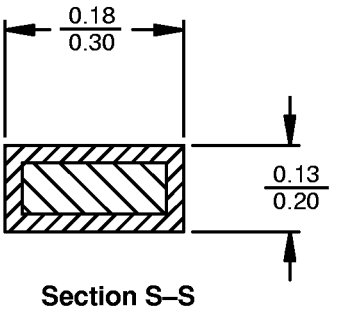
All measurements are in millimeters unless otherwise noted.

Not to scale. For reference only.

PQR 208 (continued)



Detail X



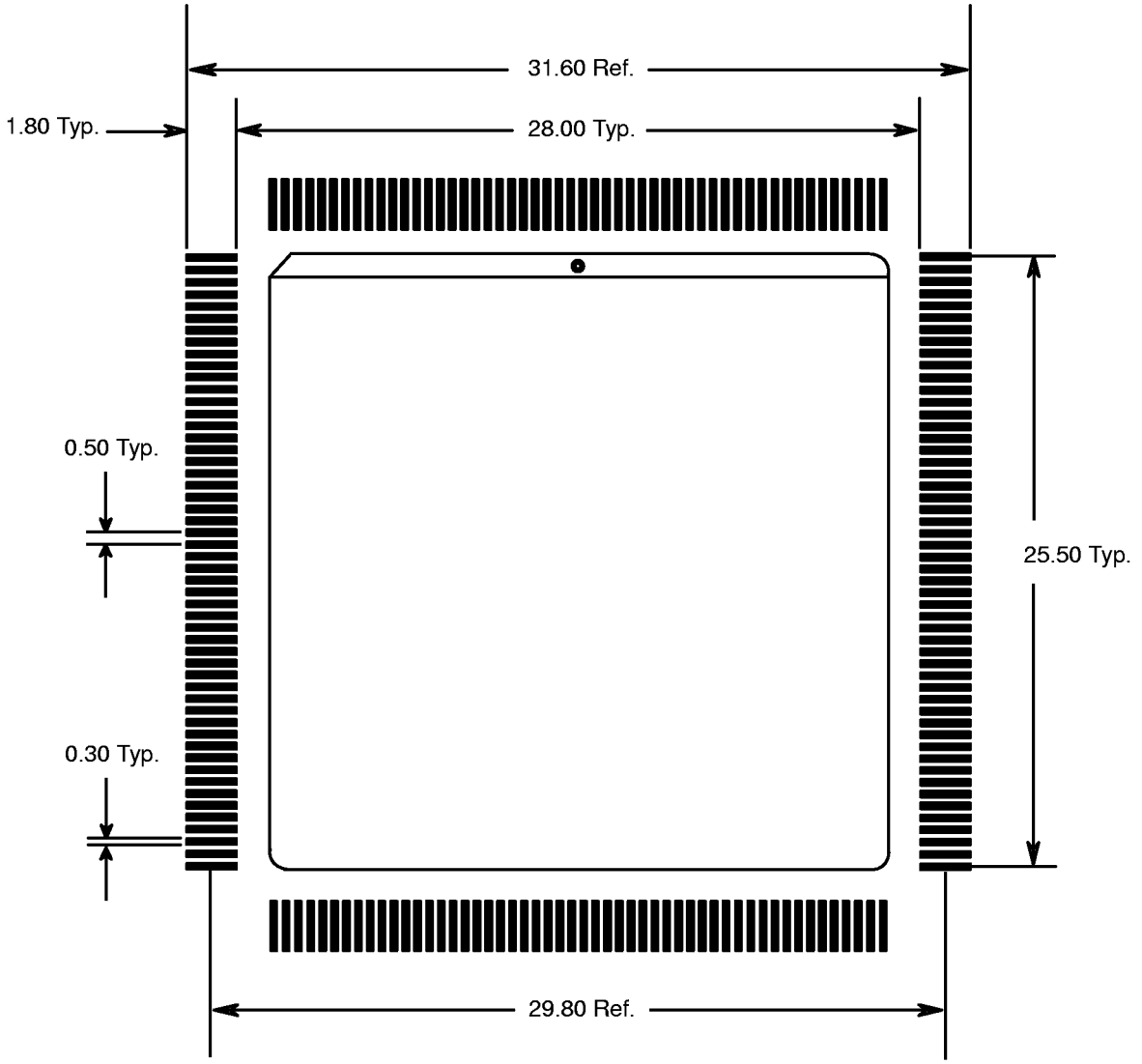
Section S–S

Notes:

All measurements are in millimeters unless otherwise noted.

Not to scale. For reference only.

PHYSICAL DIMENSIONS (continued)
Solder Land Recommendations—208-Lead PQFP



Notes:

All measurements are in millimeters unless otherwise noted.

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