10.3Gbps Thunderbolt™ and DisplayPort™ Switch

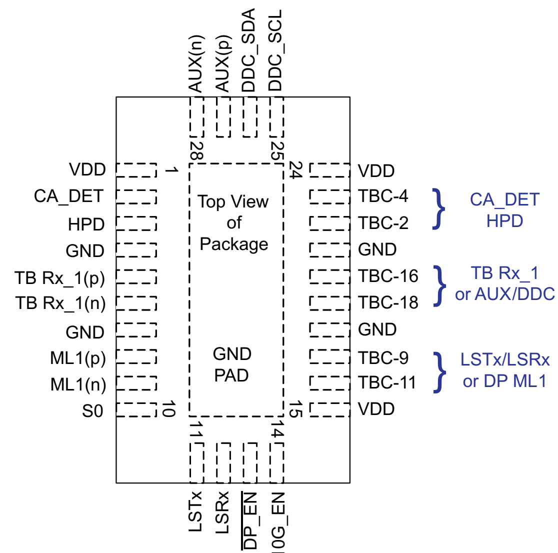
Check for Samples: HD3SS0001

FEATURES

- **Compatible with DisplayPort™ 1.2 and Thunderbolt™**
  - **Supports DP and DP++ Configurations**
  - **Handles HPD (5V tolerant) and CA_DET**
  - **Supports AUX and DDC MUX**
- **Wide –3dB Differential BW of over 10GHz for 10G Link**
- **Excellent Dynamic Characteristics (at 5GHz)**
  - **Crosstalk = –30dB**
  - **Isolation = –20dB**
  - **Insertion Loss = –1.5dB**
  - **Return Loss = –16dB**
  - **Max Bit-Bit Skew = 4 ps**
- **VDD Operating Range 3.3 V ±10%**
- **Small 3.5 mm x 5.5 mm, 28-Pin TQFN Package**
- **Reduced Power Consumption in Detect and Sleep Power Modes**

HOST APPLICATIONS

- **Thunderbolt™ Applications**



DESCRIPTION

HD3SS0001 is a high-speed passive switch designed to support low speed and high speed signals required for Thunderbolt™(TBT) applications using the mDP connector. The HD3SS0001 switches between DDC, AUX, and the 10Gbps TBT signal in order to support DisplayPort, Dual Mode DisplayPort, and Thunderbolt™. The HD3SS0001 also switches between the Thunderbolt™ Low Speed UART transmit/receive pair and DisplayPort Main Link 1 (ML1) pair. The device supports 5.4Gbps for DisplayPort and 10.3Gbps for Thunderbolt. Switch control is determined by three control pins and the mDP connector pin used for cable detect.

The HD3SS0001 is offered in a 28-pin QFN package and specified to operate from a single supply voltage of 3.3V over the full industrial temperature range of –40°C to 85°C.

PRODUCT PREVIEW

ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE
HD3SS0001RLFR	HD3SS0001	28-pin RLF Reel (Large)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

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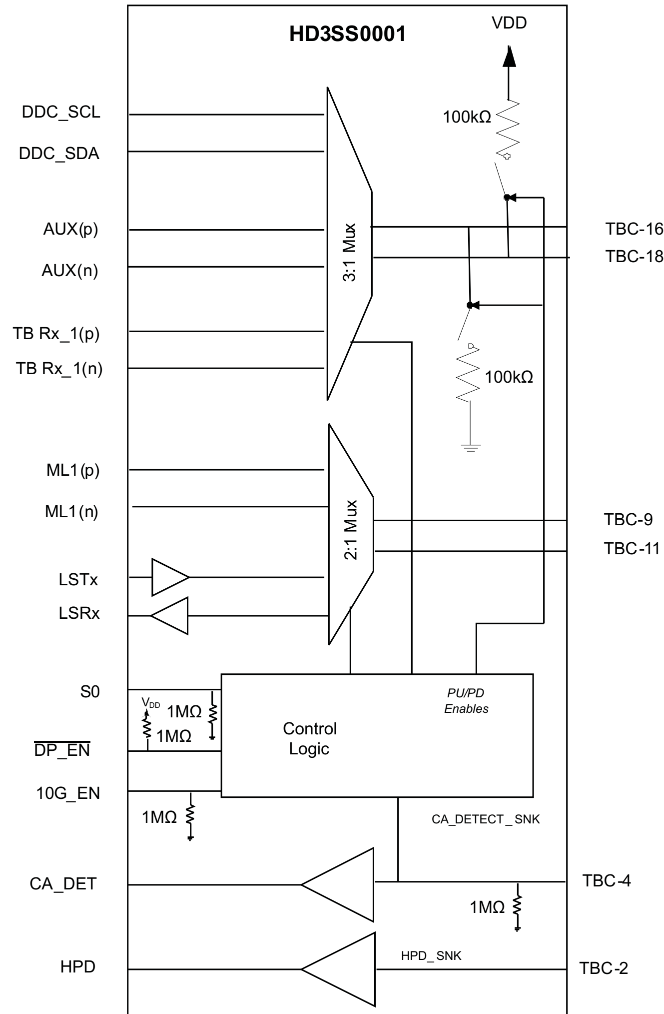
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL DIAGRAM



PRODUCT PREVIEW

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TRUTH TABLE

Device Mode States	Control Lines				Device & PU/PD Configurations		
	S0 (System Power State)	DP_EN	10G_EN	TBC-4 (CA_Detect)	MUX Outputs 2:1 Mux (DP ML)	MUX Outputs 3:1 Mux (TB 10Gbps)	TBC-16/TBC-18 (AUX) Integrated PU/PD State
Thunderbolt 10G Mode	1 (System Active) 0 (System Sleep)	1 1	1 1	X - Don't Care X - Don't Care	LSTx & LSRx LSTx & LSRx	TB Rx_1 3-stated	Off Off
DisplayPort Mode	1 (System Active) 0 (System Sleep)	0 0	0 0	0 0	DP ML1 3-stated	AUX 3-stated	On On
TMDS Mode	1 (System Active) 0 (System Sleep)	0 0	0 0	1 1	DP ML1 3-stated	DDC 3-stated	Off Off
Detect Mode	1 (System Active) 0 (System Sleep)	1 1	0 0	X - Don't Care X - Don't Care	LSTx & LSRx LSTx & LSRx	3-stated 3-stated	On On
Sleep Power Mode/ Invalid State Modes	X - Don't Care	0	1	X - Don't Care	3-stated	3-stated	Off

MUX PIN CONNECTION TABLE(1)

CONNECTOR SIDE PIN	CONTROLLER SIDE PIN
TBC-16	DDC_SCL or AUX(p) or TB Rx_1(p)
TBC-18	DDC_SDA or AUX(n) or TB Rx_1(n)
TBC-9	ML1(p) or LSTx
TBC-11	ML1(n) or LSRx
TBC-4	CA_DET
TBC-2	HPD

(1) The HD3SS0001 can tolerate polarity inversions for the differential signals denoted by the (p) and (n) terminology to ease potential board routing issues.The LSTx/LSRx cannot be swapped since they are buffered and therefore uni-directional. Also, note the integrated pullup on TBC-18 and the integrated pulldown on TBC-16 cannot be swapped.

PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NUMBER	NAME		
27 28	AUX(p) AUX(n)	I/O	Controller Side AUX Positive Signal Controller Side AUX Negative Signal
5 6	TB Rx_1(p) TB Rx_1(n)	O	Controller Side 10Gbps Positive Signal Controller Side 10Gbps Negative Signal
8 9	ML1(p) ML1(n)	I	Controller Side Channel 1, DisplayPort Main Link 1 Positive Signal Controller Side Channel 1, DisplayPort Main Link 1 Negative Signal
20 19	TBC-16 TBC-18	I/O	Connector Side 10G or AUX Positive Signal or DDC CLK with integrated pulldown Connector Side 10G or AUX Negative Signal or DDC Data with integrated pullup
17 16	TBC-9 TBC-11	I/O	Connector Side DP Main Link 1 Positive Signal or UART TX Connector Side DP Main Link 1 Negative Signal or UART RX
25 26	DDC_SCL DDC_SDA	I/O	Controller Side DDC ClockController Side DDC Data
2	CA_DET	O	Controller Side Cable Detect
23	TBC-4	I	Connector Side Cable Detect with integrated pulldown
3	HPD	O	Controller Side Hot Plug Detect
22	TBC-2	I	Connector Side Hot Plug Detect

PRODUCT PREVIEW

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PRODUCT PREVIEW

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NUMBER	NAME		
11 12	LSTx LSRx	I/O	Controller Side UART TX SignalController Side UART RX Signal
10 13 14	S0 $\overline{DP_EN}$ 10G_EN	I	Control Lines for configuring device. S0 and 10G_EN incorporate integrated pulldowns and $\overline{DP_EN}$ incorporates a pullup. Therefore, the default device state will be “Detect Mode” per the Truth Table provided these lines are not driven.
1, 15, 24	VDD	Supply	Positive power supply voltage
4, 7, 18, 21, Center Pad	GND	Supply	Negative power supply voltage

ABSOLUTE MAXIMUM RATINGS[1][2]

Over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Supply voltage range[2]	V_{DD}	–0.5	4	V
Voltage range	Differential I/O	–0.5	4	V
	Control pin/buffers	–0.5	VDD+0.5	
Electrostatic discharge	Human body model[3]		±1,500	V
	Charged-device model[4]		±500	
Continuous power dissipation			See Thermal Table	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC/ESDA JS-001-2011
(4) Tested in accordance with JEDEC JESD22 C101-E

THERMAL INFORMATION

THERMAL METRIC[1]		HD3SS0001	UNITS
		28-PIN TQFN (RLF)	
θ_{JA}	Junction-to-ambient thermal resistance	37.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	34.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.4	
θ_{JB}	Junction-to-board thermal resistance	8.7	
ψ_{JT}	Junction-to-top characterization parameter	0.6	
ψ_{JB}	Junction-to-board characterization parameter	8.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX[1]	UNIT
P_D	Device power dissipation			4.6	7.6	mW
$P_{(Detect)}$	Device power dissipation in detect mode				5	mW
P_{Sleep}	Device power dissipation in sleep mode				15	µW

(1) The maximum rating is simulated under 3.6V VDD.

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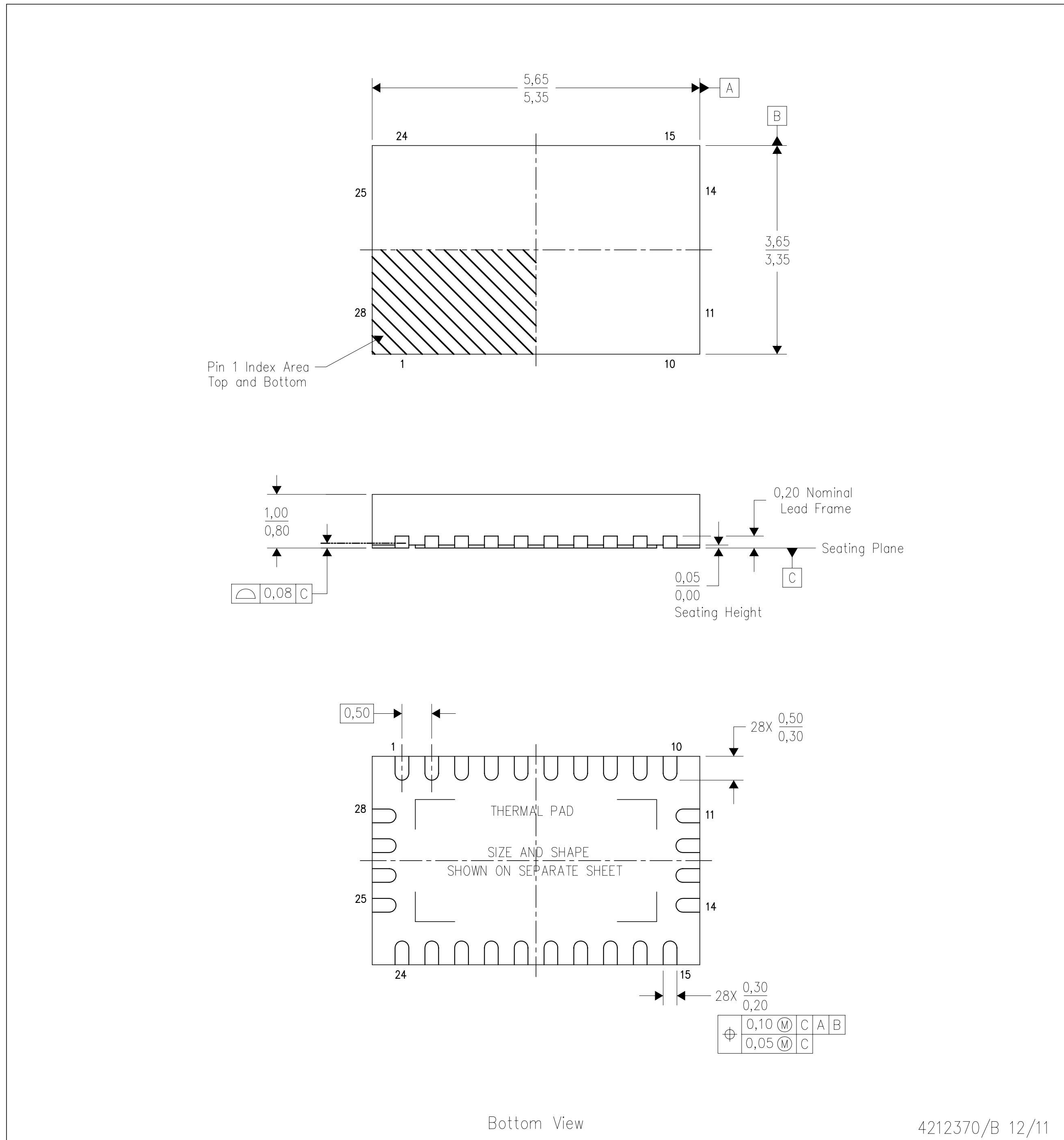
RLF (R-PVQFN-N28) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. JEDEC MO-241 package registration pending.

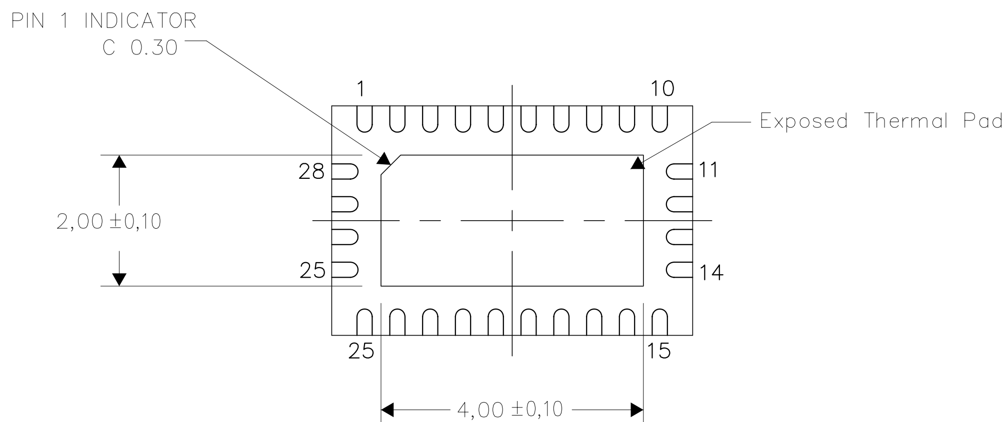
RLF (R–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4212399/A 12/11

NOTE: All linear dimensions are in millimeters

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
HD3SS0001RLFR	PREVIEW	VQFN	RLF	28	3000	TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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