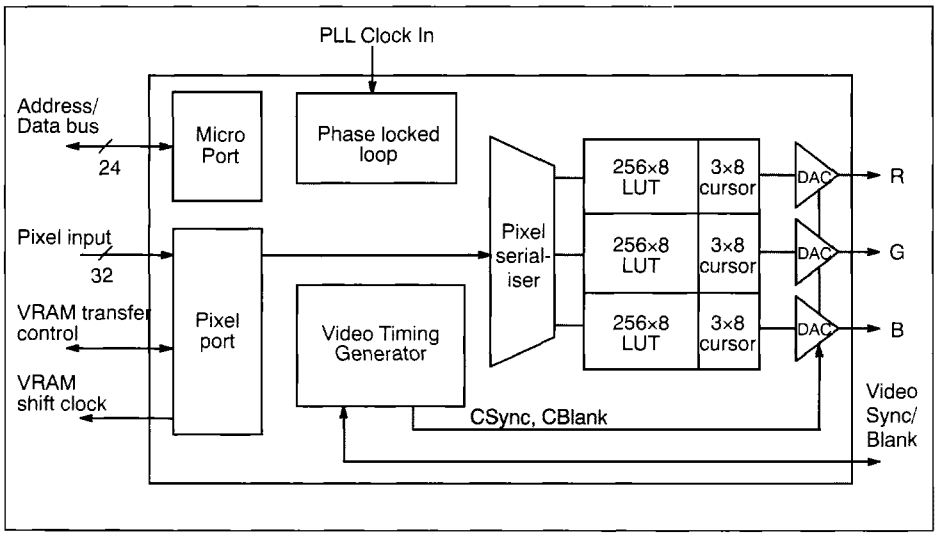
COLOR VIDEO CONTROLLER

PRODUCT OVERVIEW



FEATURES

Software configurable video timing generator
Interlaced or non-interlaced video
Generates Studio broadcast standard Sync signals
Supplies blanked analogue video outputs
Internal or external Sync options
Single or synchronous multiple operation

Variable multiplexed Pixel input
1, 2, 4, 8 and 24 bit pixels
On chip triple lookup table
Triple high speed 8 bit video DACs
CCIR and EIA 343-A compatible
Full color mode with hardware gamma translation

General purpose Video RAM support
Synchronous VRAM Data Transfer strobing
Video RAM Row address auto-increment
Screen width independent of VRAM architecture
On-chip phase-locked loop (PLL)
All external signals and clocks at 1/4 video rate

APPLICATIONS

High resolution graphics and imaging
Broadcast/CC television systems
Color X-terminals
Low-cost workstations
High-resolution color PC add-in boards
Multimedia display systems

DESCRIPTION

The IMS G300 is a high performance CMOS device which provides high integration and flexibility for the control of a color graphics display subsystem.

The IMS G300 has now been superseded by the IMS G335, which boasts a number of new features as well as a higher maximum pixel rate (up to 135MHz). The IMS G300 is not recommended for new designs, and will be obsoleted early in 1993. An Application Note is available describing the conversion of IMS G300 designs to IMS G335, providing a more cost-effective solution. Please contact your local sales office for a copy.

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16.1 Introduction

The IMS G300C is a dedicated support chip which provides all necessary functions for controlling real time operation of a raster scan video system, using dual ported video DRAMs. The facilities provided are designed to isolate the host processor from the constraints of the real time system without in any way interfering with the ability of the processor to specify and manipulate screen data.

The device consists of a programmable video timing generator with screen refresh and auto line increment capability, a triple 256 location by 8 bit lookup table (LUT), a triple 8 bit video DAC and an on chip phase-locked loop (PLL); see Figure 16.1.

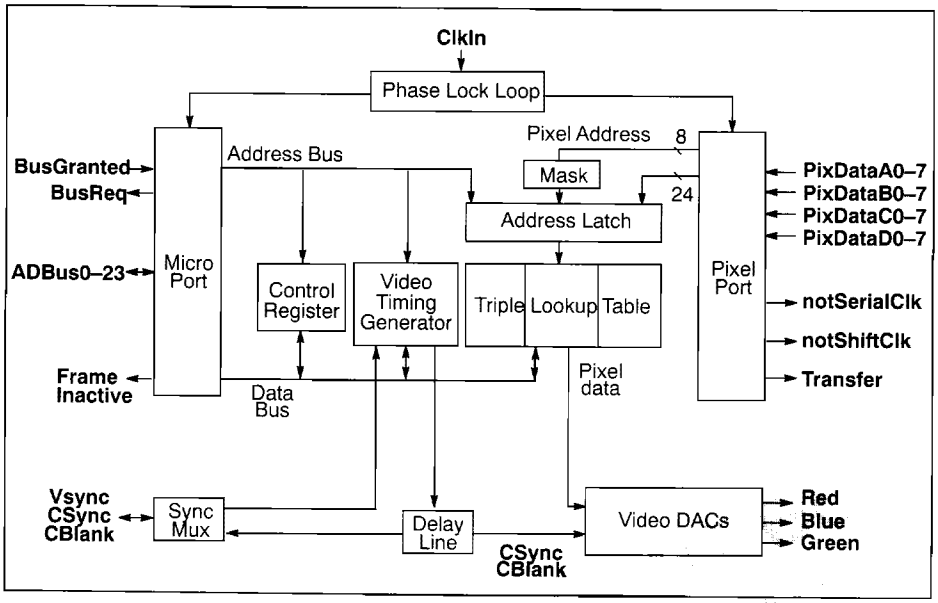


Figure 16.1 IMS G300C Block Diagram

16.1.1 Clocks

Use of the phase-locked loop allows the part to be driven from a low speed clock in the 5MHz to 10MHz range, which is internally multiplied by a user-specified factor to achieve video data rates. The controller can be clocked by a full rate system clock if desired, although at a reduced frequency compared to that achievable with the PLL.

16.1.2 Micro port

The IMS G300C has a memory mapped architecture which enables fast configuration and color cycling through the use of block move or some other simple memory write cycle. Its micro-port appears as a block of memory (occupying 1/2Kword of address space) with the additional capability of operating in byte-wide or word-wide (24-bit) modes.

16.1.3 Video timing

The video timing generator is a programmable finite state machine which is programmed by loading a number of screen description parameters. It can be configured to free run, providing composite or separate sync, or to lock onto an external synchronizing source which may be another IMS G300C, giving the potential for multiple, synchronous video systems. In either mode, it supplies composite blank and can

supply tesselated or plain composite sync to the video DACs. The timing generator runs at one quarter of the video dot rate and the screen parameters are defined in terms of its resolution. Thus the screen is defined in multiples of four pixels.

16.1.4 Framestore management

Video RAM support is provided by a screen refresh mechanism which performs a DMA to the video RAM and which allows seamless mid-line update of the screen. The video RAM shift register can be made to behave as though it is infinitely long and the flow of pixels onto the screen is controlled by starting and stopping the pixel shift clock at the appropriate times (a true serial clock output is also provided for system synchronization). This method of control divorces the screen line length from dependence on the video RAM shift register length, allowing for very long display lines without extra multiplexing and for efficient use of memory irrespective of screen dimensions.

16.1.5 Pixel port

The pixel port is 32 bits wide and has a number of operating modes, which are selectable in software.

In pseudo color mode (mode 1), the 32 bit word can be interpreted as consisting of one, two, four or eight bit pixels. These are loaded at the relevant multiplex ratio and accelerated to the full dot rate before addressing the LUT. The 24 bits of pixel data thus accessed are then sent to the video DACs for display.

In full color mode (mode 2), the top byte of the input word is ignored and the remaining three bytes are used as separate addresses into the triple LUT. No acceleration takes place before the data is sent to the LUT.

Mode 2 is usable only when an external dot-rate clock is supplied, mode 1 can also be used with the phase-locked loop.

16.1.6 Video DACs

The triple video DAC has 8 bit resolution at the full video rate and produces blanked video signals. It is possible to select various styles of analogue output to conform with generally approved monitor and broadcast television output levels and timings, including EIA-343 and CCIR.

16.1.7 System Operation

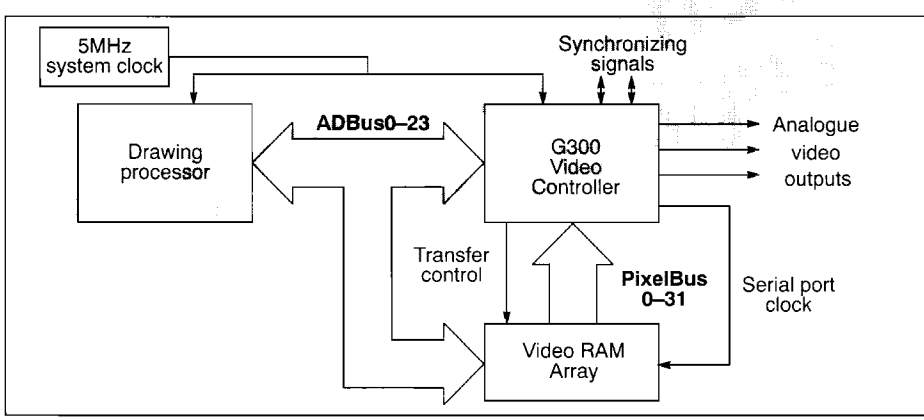


Figure 16.2 IMS G300C operating in a simple graphics system

Figure 16.2 shows how the IMS G300C would fit into a typical single-bitmap display system. The clock is sourced from a 5MHz crystal and the video data is being streamed to the screen at the full video rate of 110MHz. The video RAM array is directly accessed by the drawing processor and screen management is performed by the G300C on a DMA basis. All external digital signals and clocks are running at one quarter of the video rate.

16.2 Package specifications

16.2.1 84 pin grid array package

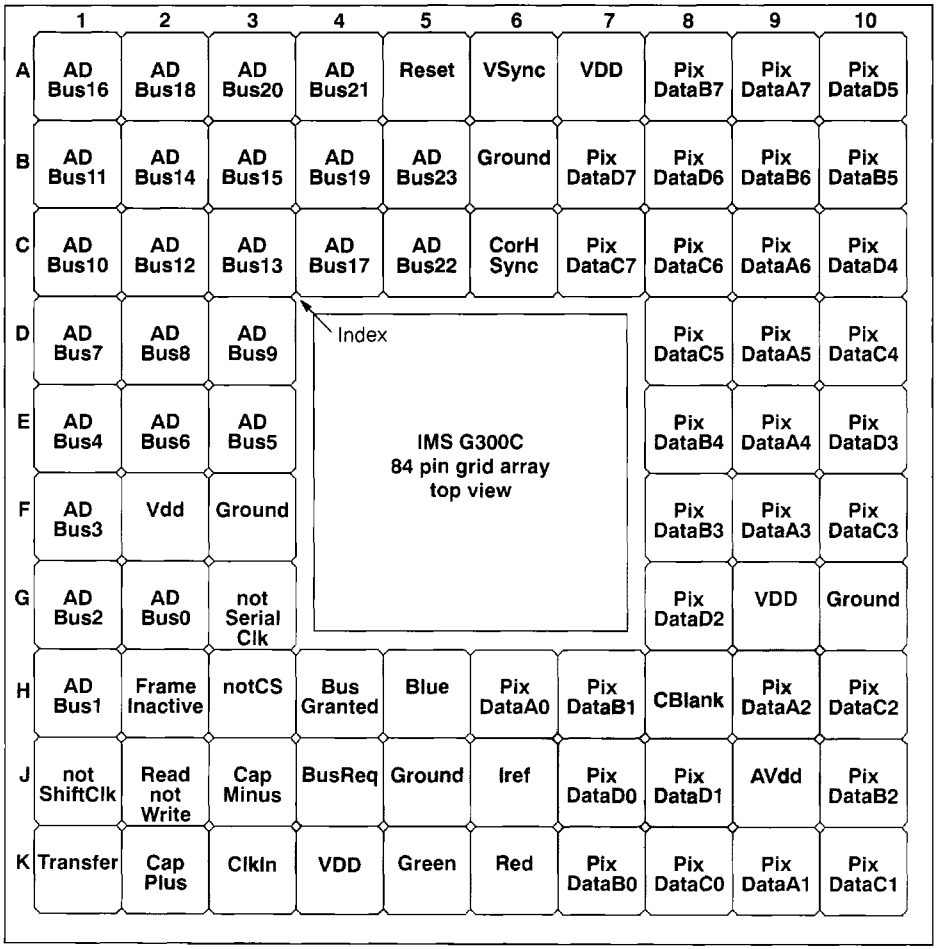


Figure 16.3 IMS G300C 84 pin grid array package pinout

DIM	CONTROL DIMENSIONS INCH			ALTERNATIVE DIMENSIONS mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.135	0.147	0.160	3.429	3.734	4.064
A1	–	0.050REF	–	–	1.270REF	–
A2	0.085	0.097	0.110	2.159	2.464	2.794
B	–	0.018	–	–	0.457	–
B1	–	0.050REF	–	–	1.270REF	–
D	1.050	1.060	1.070	35.179	35.560	36.068
D1	–	0.900REF	–	–	22.86REF	–
e	–	0.100BSC	–	–	2.540BSC	–
E	1.050	1.060	1.070	35.179	35.560	36.068
E1	–	0.900REF	–	–	22.86REF	–
L	–	0.130	–	–	3.302	–

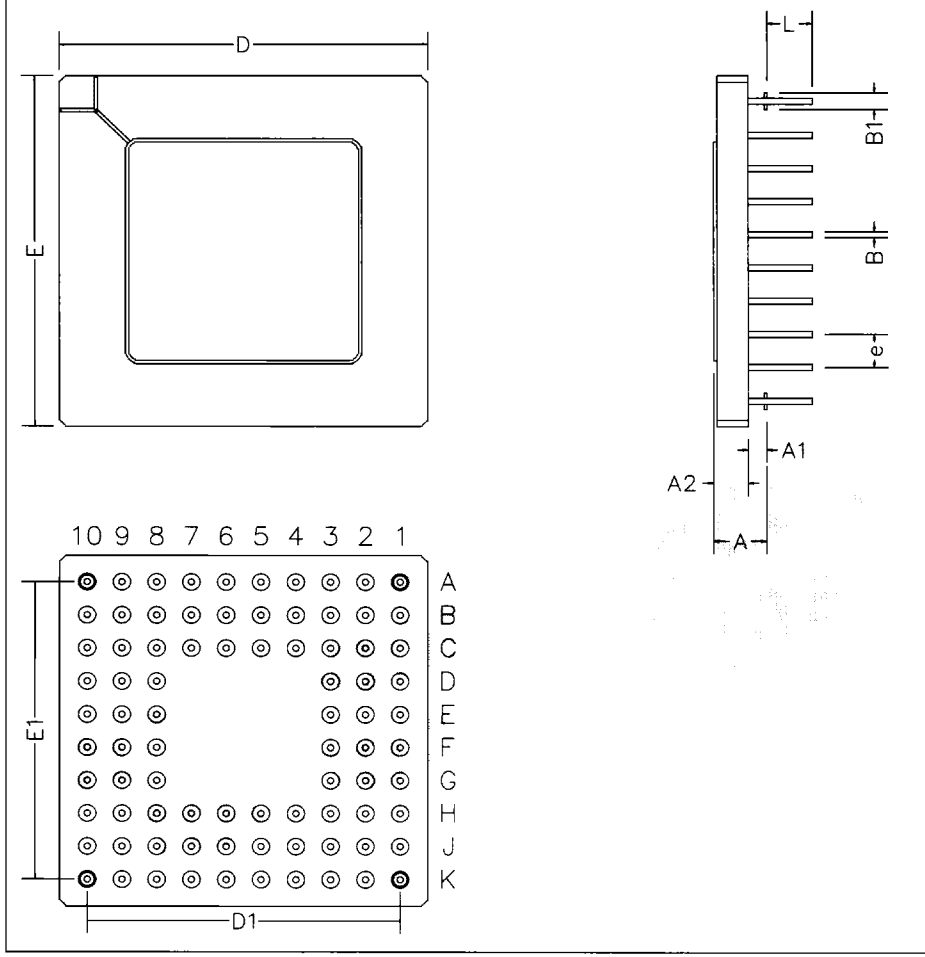


Figure 16.4 84 pin grid array package dimensions

16.2.2 100 pin ceramic quad flatpack package

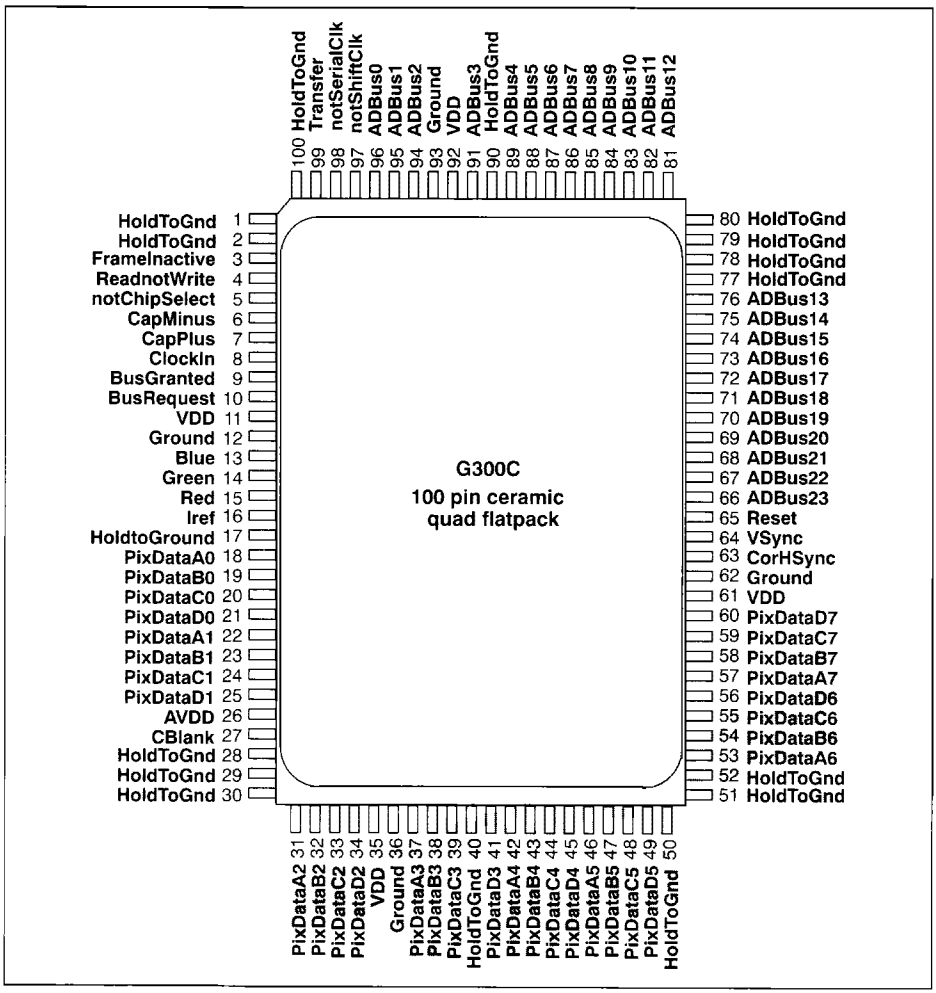


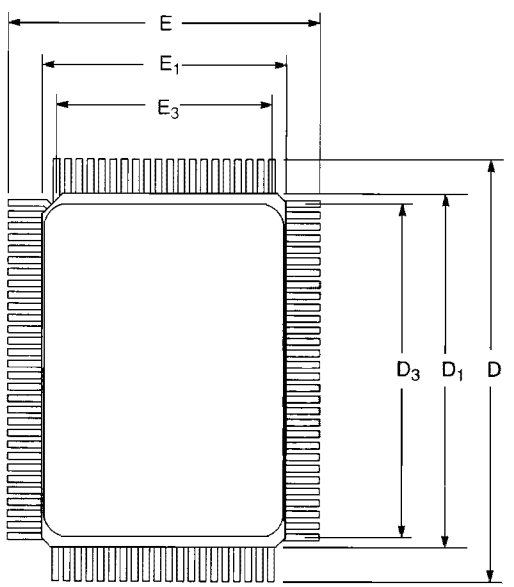
Figure 16.5 IMS G300C ceramic quad flatpack package pinout

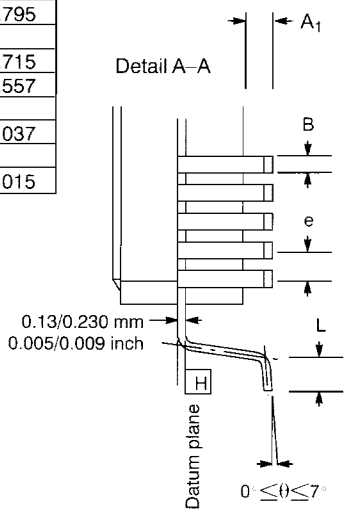
	CONTROL DIMENSIONS mm			ALTERNATIVE DIMENSIONS INCH		
DIM	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
A			3.400			0.134
A_1	0.250			0.010		
A_2			3.073			0.121
D	23.65	23.90	24.15	0.931	0.941	0.951
D_1	19.80	20.00	20.20	0.780	0.787	0.795
D_3		18.85 REF			0.742 REF	
E	17.65	17.90	18.15	0.695	0.705	0.715
E_1	13.84	14.00	14.15	0.545	0.551	0.557
E_3		12.35 REF			0.486 REF	
L	0.650	0.800	0.950	0.026	0.031	0.037
e		0.650 BSC			0.026 BSC	
B	0.22		0.38	0.009		0.015

Notes

1 Dimension D1 and E1 measured at the ceramic side. Base to window frame misalignment is 0.40mm max. An additional glass meniscus of 0.2mm max is allowed at the leadframe interface.

2 Coplanarity 0.1 mm Max





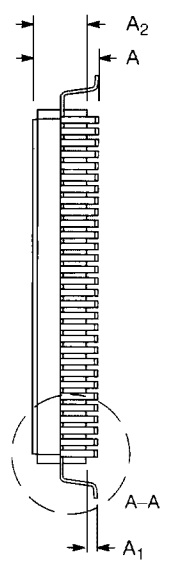


Figure 16.6 100 pin cavity-up ceramic quad flat pack dimensions

16.3 Ordering information

Device	Clock rate	Package	Part number
IMS G300C	85MHz	84 pin PGA	IMS G300G–85C
IMS G300C	100MHz	84 pin PGA	IMS G300G–10C
IMS G300C	110MHz	84 pin PGA	IMS G300G–11C
IMS G300C	85MHz	100 pin ceramic quad flatpack	IMS G300F–85C
IMS G300C	100MHz	100 pin ceramic quad flatpack	IMS G300F–10C
IMS G300C	110MHz	100 pin ceramic quad flatpack	IMS G300F–11C