

Preliminary Information  
Standard Product  
April, 1991

# LXT325

## T1/E1 Integrated Quad Receiver with LOS

T-75-11-37

### General Description

The LXT325 is a fully integrated quad PCM receiver for both North American 1.544 MHz (T1), and European 2.048 MHz (E1) applications. It incorporates four independent receivers in a single 28-pin DIP or PLCC. Each receiver incorporates a Loss Of Signal (LOS) detection circuit and output driver. The operating frequency is pin selectable.

The LXT325 receiver performs data and timing recovery, and uses peak detection and a variable threshold to reduce impulsive noise. LXT325 receiver sensitivity down to 500 mV allows for up to 13.6 dB of cable attenuation.

The LXT325 is an advanced double-poly, double-metal CMOS device and requires only a single 5-volt power supply.

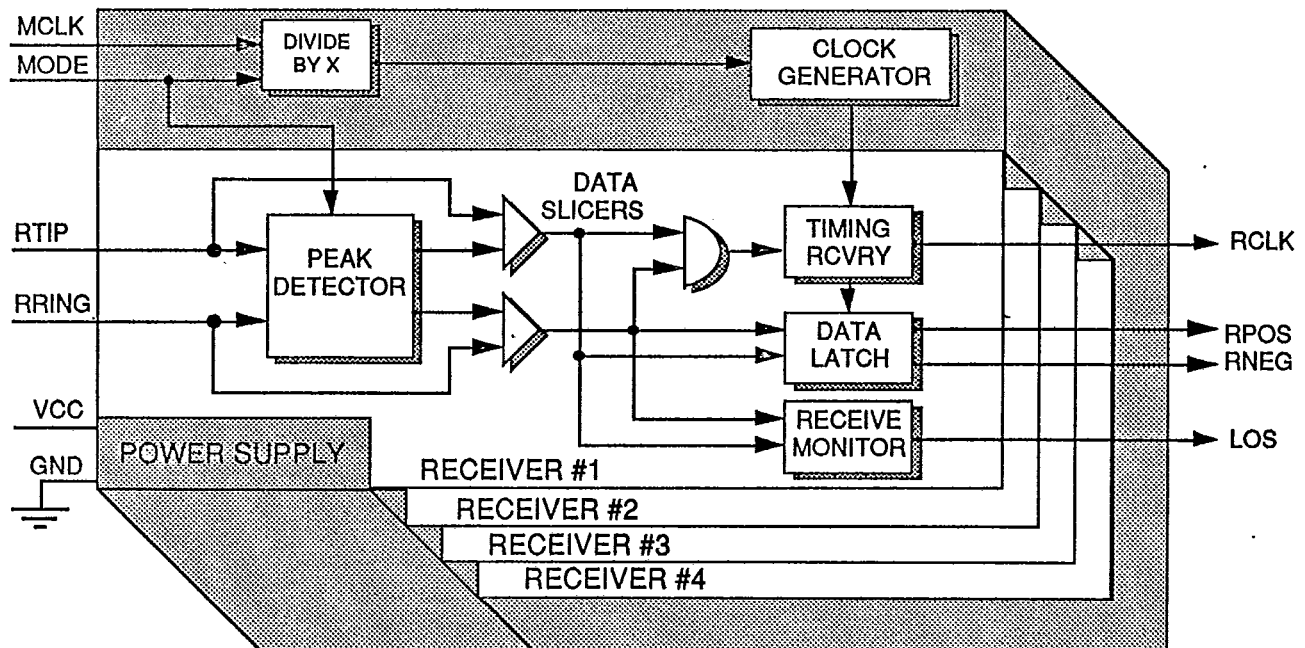
### Applications

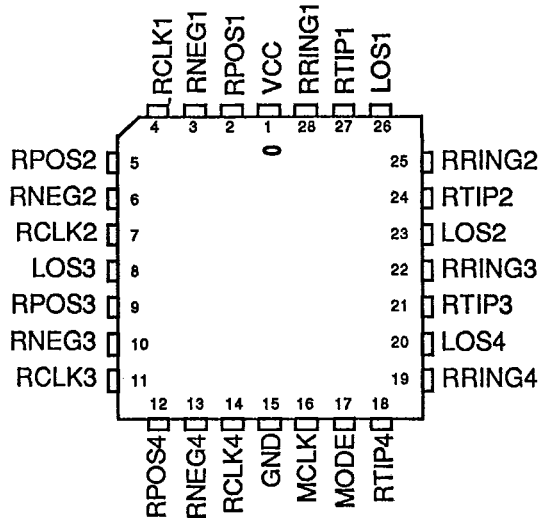
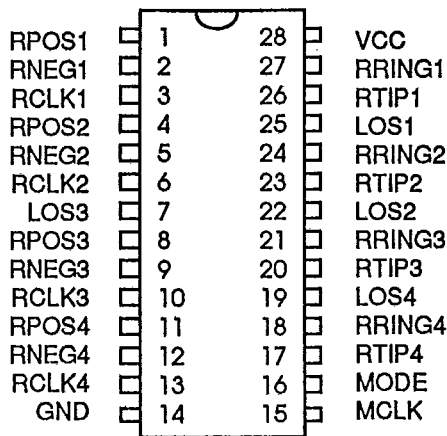
- DSX-1/CEPT test equipment
- DSX-1/CEPT line monitoring
- DSX-1/CEPT receive line interface

### Features

- 4 independent DSX-1/CEPT receivers
- Loss Of Signal (LOS) output for each receiver
- Circuit functions include data and clock recovery
- Single Master Clock input
- Meets or exceeds AT&T PUB 62411 requirements
- Unipolar RPOS and RNEG outputs
- Minimum receive signal of 500 mV
- Selectable slicer levels (DSX-1/CEPT) to provide improved SNR
- Single 5 V only CMOS technology
- Available in 28-pin DIP and PLCC

Figure 1: Block Diagram





**Pin Descriptions**

Pin #		Sym	I/O	Name	Description
DIP	PLCC				
1	2	RPOS1	O	Receiver 1 Positive Data	Receiver 1 data outputs. A signal on RNEG1 corresponds to receipt of a negative pulse on RTIP1 and RRING1. A signal on RPOS1 corresponds to receipt of a positive pulse on RTIP1 and RRING1. RNEG1 and RPOS1 outputs are Non-Return-to-Zero (NRZ). Both outputs are stable and valid on the rising edge of RCLK1.
2	3	RNEG1	O	Receiver 1 Negative Data	
3	4	RCLK1	O	Recovered Clock 1	This is the clock recovered from the signal received at RTIP1 and RRING1.
4	5	RPOS2	O	Receiver 2 Positive and Negative Data and Recovered Clock	These are the data and clock outputs recovered from the signal received at RTIP2 and RRING2.
5	6	RNEG2	O		
6	7	RCLK2	O		
7	8	LOS3	O	Loss of Signal 3	LOS pins go high when the associated receiver detects 175 consecutive spaces. The LOS output returns low when a mark is received.
8	9	RPOS3	O	Receiver 3 Positive and Negative Data and Recovered Clock	These are the data and clock outputs recovered from the signal received at RTIP3 and RRING3.
9	10	RNEG3	O		
10	11	RCLK3	O		
11	12	RPOS4	O	Receiver 4 Positive and Negative Data and Recovered Clock	These are the data and clock outputs recovered from the signal received at RTIP4 and RRING4.
12	13	RNEG4	O		
13	14	RCLK4	O		
14	15	GND	--	Ground	Ground.
15	16	MCLK	I	Master Clock	A 1.544 MHz or 2.048 MHz clock input used to generate internal clocks. Upon loss of signal, the RCLKs are derived from MCLK.

T-75-11-37

**Pin Descriptions continued**

Pin #		Sym	I/O	Name	Description
DIP	PLCC				
16	17	MODE	I	Mode Select	Setting MODE to logic 1 sets the data slicer thresholds to 50% of the incoming signal (CEPT mode). Setting MODE to logic 0 sets the data slicer thresholds to 70% of the incoming signal (DSX-1 mode). The Mode Select operates independently from the MCLK rate. This allows the 50% slicer ratio to be used with a 1.544 MHz MCLK, for improved sensitivity.
17	18	RTIP4	I	Receiver 4 Tip	The AMI signal received from the fourth twisted-pair line is applied at these pins. A center-tapped, center-grounded transformer is required on these pins. Data and clock from the signal applied at these pins are recovered and output on the RPOS4/RNEG4, and RCLK4 pins.
18	19	RRING4	I	Receiver 4 Ring	
19	20	LOS4	O	Loss of Signal	LOS output for receiver 4.
20	21	RTIP3	I	Receiver 3 Tip and Ring	The AMI signal received from the third twisted-pair line is applied to the LXT325 at these pins.
21	22	RRING3	I		
22	23	LOS2	-	Loss of Signal	LOS output for receiver 2.
23	24	RTIP2	I	Receiver 2 Tip and Ring	The AMI signal received from the second twisted-pair line is applied to the LXT325 at these pins.
24	25	RRING2	I		
25	26	LOS1	O	Loss of Signal	LOS output for receiver 1.
26	27	RTIP1	I	Receiver 1 Tip and Ring	The AMI signal received from the first twisted-pair line is applied to the LXT325 at these pins.
27	28	RRING1	I		
28	1	VCC	I	Power Supply	+5 VDC power supply.

**Absolute Maximum Ratings\***

\* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

- Supply voltage  $V_{CC}$  -0.3V to 6V
- Voltage on any I/O pin<sup>1</sup>  $V_{I/O}$  GND -0.3V to  $V_{CC} + 0.3V$
- Current on any I/O pin<sup>2</sup>  $I_{I/O}$  ±10 mA
- Package power dissipation  $P_D$  1 W
- Storage temperature  $T_{ST}$  -65 °C (min) to 150 °C (max)

<sup>1</sup> Excluding RTIP and RRING which must stay within -6V to RV + 0.3V.

<sup>2</sup> Transient currents of up to 100 mA will not cause SCR latch-up.

**Recommended Operating Conditions** (Voltages are with respect to ground unless otherwise stated)

Parameter	Sym	Min	Typ	Max	Units
Supply voltage	$V_{CC}$	4.75	5	5.25	V
Operating Temperature	$T_{OP}$	-40	-	85	°C

**DC Electrical Characteristics** (Clocked operation over recommended temperature and power supply ranges.)

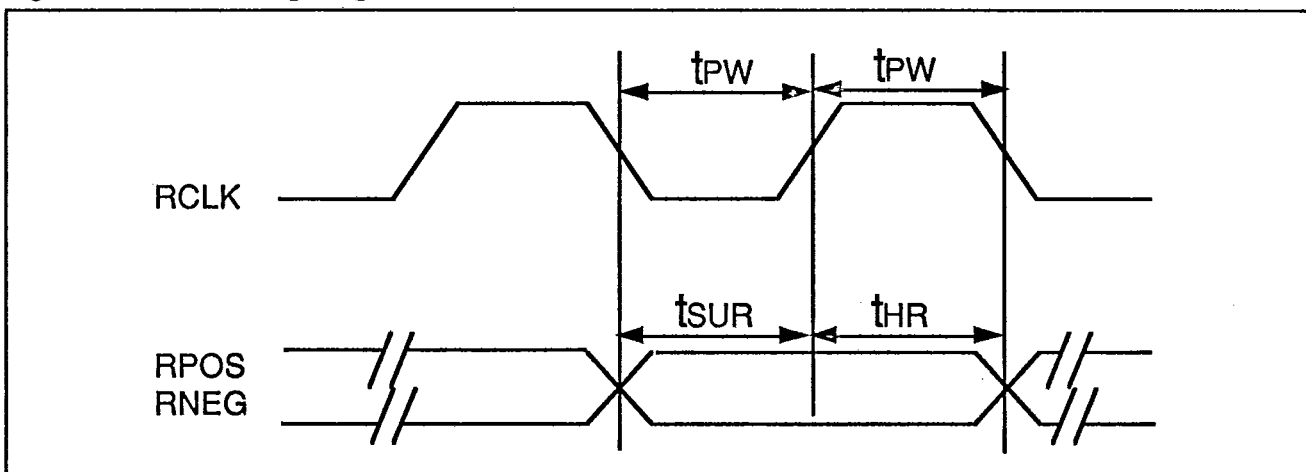
Parameter	Sym	Min	Typ <sup>1</sup>	Max	Units	Test Conditions
Supply current	$I_{CC}$	-	-	40	mA	
Input high voltage	$V_{IH}$	2.0	-	-	V	Digital inputs
Input low voltage	$V_{IL}$	-	-	0.8	V	Digital inputs
Output high voltage	$V_{OH}$	2.4	-	-	V	$I_o = 4mA$
Output low voltage	$V_{OL}$	-	-	0.4	V	$I_o = 1.6mA$
Input leakage current	$I_{LL}$	-	-	$\pm 10$	$\mu A$	Digital inputs
Output current	$I_o$	-	-	1.6	mA	$V_o = 0.4 V$
Output Rise/Fall time	$T_{RF}$	-	-	25	ns	15 pF load

**Master and Receive Clock Timing Characteristics** (See Figure 2)

Parameter	Sym	Min	Typ <sup>1</sup>	Max	Units	Test Conditions
Master clock frequency	DSX-1 MCLK	-	1.544	-	MHz	
	CEPT MCLK	-	2.048	-	MHz	
Master clock tolerance	MCLKt	-	$\pm 100$	-	ppm	
Master clock duty cycle	MCLKd	40	50	60	%	
Receive clock duty cycle	RCLKd	40	50	60	%	
Receive clock pulse width	DSX-1 $t_{PW}$	270	325	378	ns	
	CEPT $t_{PW}$	203	244	285	ns	
RPOS / RNEG to RCLK rising setup time	DSX-1 $t_{SUR}$	50	270	-	ns	
	CEPT $t_{SUR}$	50	203	-	ns	
RCLK rising to RPOS / RNEG hold time	DSX-1 $t_{HR}$	50	270	-	ns	
	CEPT $t_{HR}$	50	203	-	ns	
Rise/fall time - any digital output	$t_{RF}$	-	-	25	ns	15 pF load

<sup>1</sup>Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

**Figure 2: Clock Timing Diagram**



LXT325 T1/E1 Integrated Quad Receiver with LOS

T-75-11-37

Functional Description

The LXT325 is a fully integrated PCM receiver for both 1.544 MHz (DSX-1) and 2.048 MHz (CEPT) applications. The mode of operation is set by the MCLK frequency and the MODE pin logic level. The LXT325 is a low-power CMOS device which operates from a single +5 V power supply.

Figure 1 is a simplified block diagram of the LXT325. Receiver characteristics are listed in Table 1. The signal is received from the twisted-pair line on each side of a center-grounded transformer. (Positive pulses are received at RTIP and negative pulses are received at RRING.) This differential signal is processed through the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. For DSX-1 applications (MODE Select = 0) the threshold is set to 70% of the peak value. This threshold is maintained above 65% for up to 15 successive zeros over the range of specified operating conditions. For CEPT applications (MODE Select = 1) the threshold is set to 50%. The slicer threshold is maintained through a capacitive storage arrangement and a combination of Refresh and Bleed-off circuitry. This design balance prevents the refresh circuitry from driving the threshold too high, while ensuring that it is maintained over long strings of successive zeros.

The LXT325 is capable of accurately recovering signals with up to 13.6 dB of cable attenuation (from 2.4 V), corresponding to a received signal level of 500 mV (1500 feet of ABAM cable). Regardless of received signal level, the peak detectors are held above a minimum level of 0.15 V to provide immunity from impulsive noise.

After processing through the data slicers, the received signal is routed to the data and clock recovery sections, and to the receive monitor. Recovered clock signals are supplied to the data latch. The recovered data is synchronized with the recovered clock (RCLK), then output at RNEG and RPOS. RPOS and RNEG outputs are valid on the rising edge of RCLK. The receive monitor loads a digital counter at the RCLK frequency. The count is incremented each time a zero (space) is received, and reset to zero each time a one (mark) is received. When the counter reaches 175 the LOS pin goes high and a smooth transition replaces the RCLK output with the MCLK. The LOS condition is reset when a mark is received.

Line Interface

The LXT325 interfaces with four twisted-pair lines (one twisted-pair for each receiver) through standard pulse transformers and appropriate resistors. Recommended transformer characteristics are listed in Table 2.

Table 1: Receiver Characteristics

Parameter		Sym	Min	Typ <sup>1</sup>	Max	Units
Slicer ratio	DSX-1	SRd	65	70	75	%
	CEPT	SRc	45	50	55	%
Dynamic range		DR	0.50	-	3.6	V <sub>peak</sub>
Undershoot		US	-	-	62	%
Sensitivity below DSX (0dB = 2.4V)		-	13.6	-	-	dB
		-	500	-	-	mV

Table 2: Recommended Transformer Characteristics

Parameter		1 : 1 : 1	1 : 2 : 2	Units
DC resistance	Primary	1.0 maximum	1.0 maximum	Ω
	Secondary	1.0 maximum	2.0 maximum	Ω
Primary inductance		1.2 typical	0.5 minimum	mH
Leakage inductance		0.5 maximum	1.0 maximum	μH
Interwinding capacitance		25 maximum	40 maximum	pF

<sup>1</sup>Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

LXT325 T1/E1 Integrated Quad Receiver with LOS

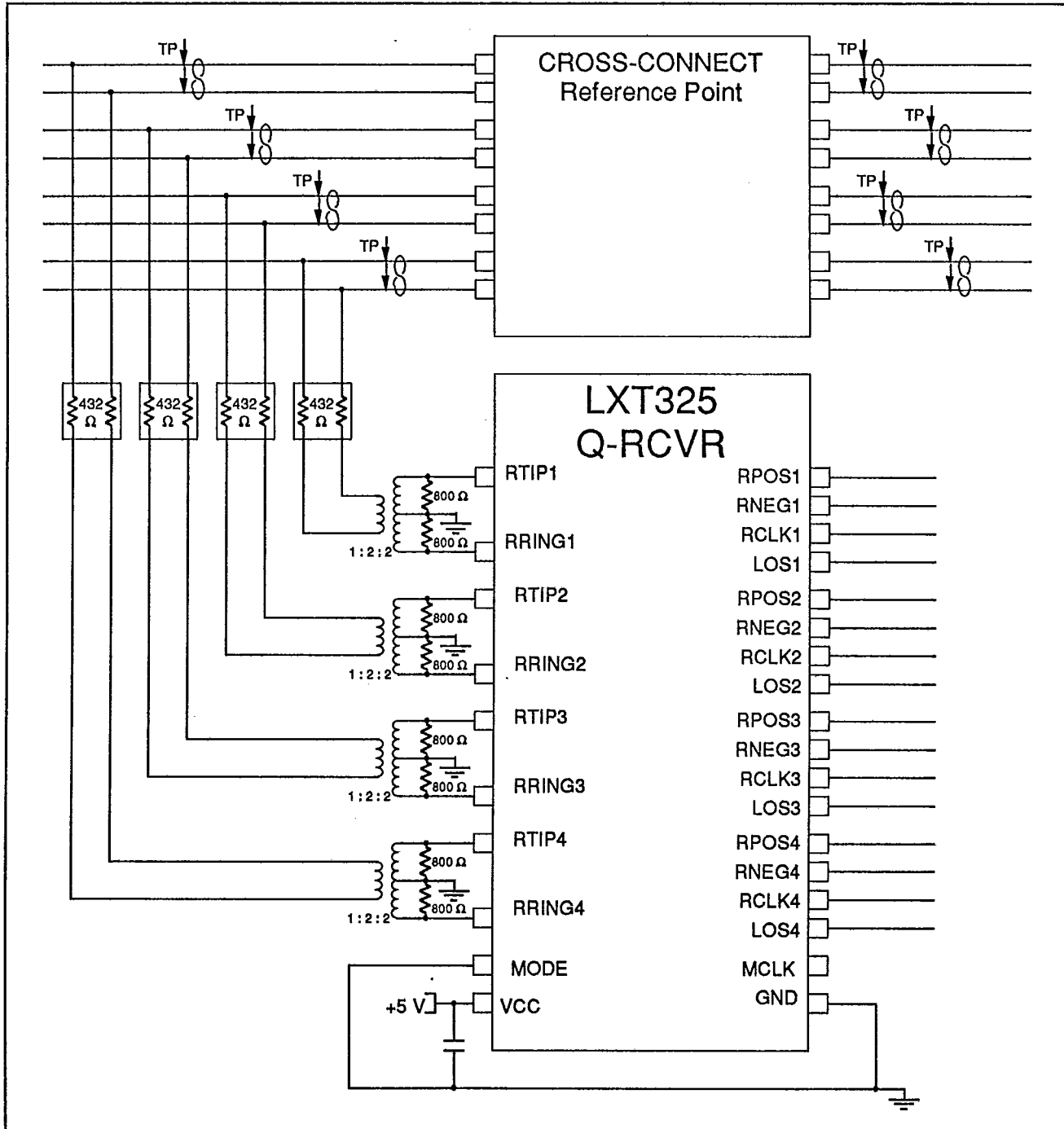
T-75-11-37

Applications

The LXT325 is compatible with both DSX-1 and CEPT systems. Low +5 V only power consumption simplifies design considerations where multiple receivers are required. The LXT325 is well suited for use in both test equipment and monitor applications. The primary difference in circuit design for these two applications is the input transformer. The typical DSX-1 pulse seen in test equipment applications

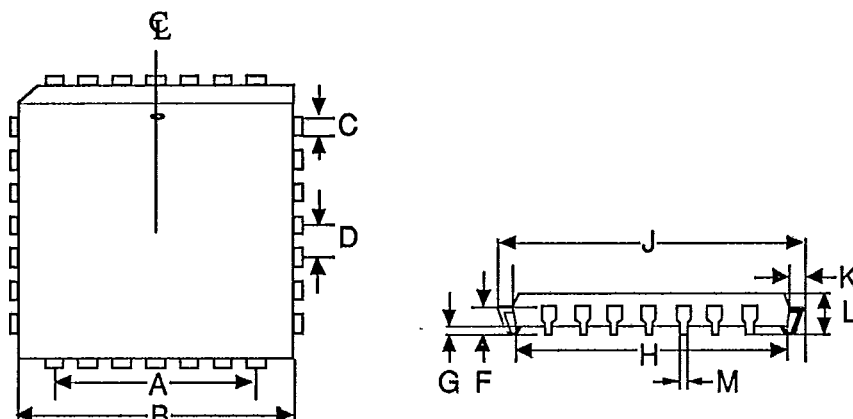
requires a 1:1:1 transformer at the receiver input. The attenuated pulse seen in monitor applications may require a 1:2:2 transformer to boost the input signal. Figure 3 is a typical 1.544 MHz DSX-1 application. The LXT325 is shown tapped into the Cross Connect frame with 800 Ω resistors across each leg of the center tapped, center grounded 1:2:2 step-up transformer.

Figure 3: Test / Monitor Equipment Application Diagram



T-75-11-37

**Packaging Information**  
**28-pin PLCC**

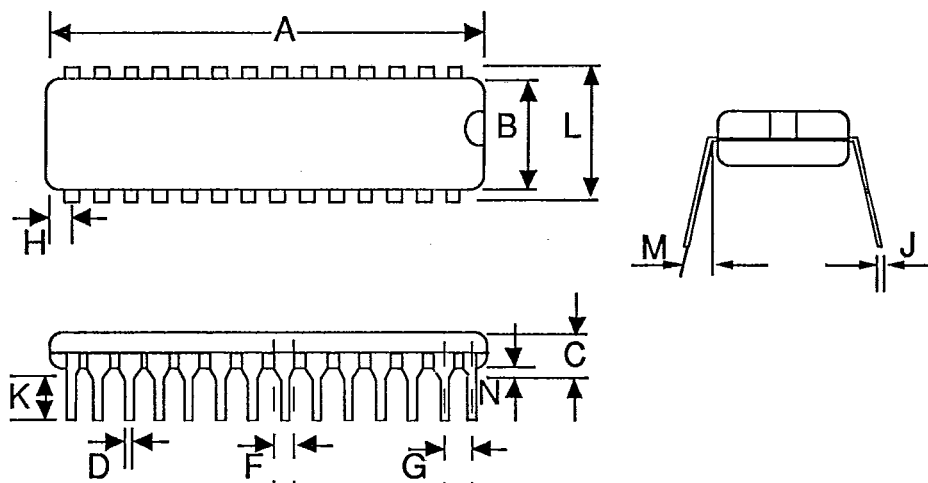


**Plastic Leaded Chip Carrier**

- Part Number LXT325PE
- Extended Temperature Range
- 28-pin PLCC

Dim.	Inches		Millimeters	
	Min	Max	Min	Max
A	.290	.310	7.37	7.87
B	.450	.456	11.43	11.58
C	.026	.032	0.66	0.81
D	.050 BSC		1.27 BSC	
F	.090	.120	2.27	3.05
G	.020	—	0.51	—
H	.390	.430	9.91	10.92
J	.485	.495	12.32	12.57
K	.018	.022	0.46	0.56
L	.165	.180	4.20	4.57
M	.013	.021	0.33	0.53

**28-pin DIP**



**Dual In-Line Ceramic Case**

- Part Number LXT325JE
- Extended Temperature Range
- 28-pin DIP

Dim.	Inches		Millimeters	
	Min	Max	Min	Max
A	—	1.490	—	37.85
B	.500	.600	12.70	15.20
C	—	.230	—	5.84
D	.014	.023	0.36	0.58
F	.035	.070	0.76	1.78
G	.100 BSC		2.54 BSC	
H	—	.095	—	2.41
J	.008	.015	0.20	0.38
K	.125	.200	3.18	5.08
L	.590	.625	14.99	15.90
M	0°	15°	0°	15°
N	.015	.060	0.38	1.52

**Dual In-Line Plastic Case**

- Part Number LXT325NE
- Extended Temperature Range
- 28-pin DIP

Dim.	Inches		Millimeters	
	Min	Max	Min	Max
A	—	1.490	—	37.85
B	.500	.600	12.70	15.20
C	—	.230	—	5.84
D	.014	.023	0.36	0.58
F	.035	.070	0.76	1.78
G	.100 BSC		2.54 BSC	
H	—	.095	—	2.41
J	.008	.015	0.20	0.38
K	.125	.150	3.18	3.81
L	.590	.625	14.99	15.90
M	0°	15°	0°	15°
N	.015	.060	0.38	1.52