MV1449

PCM HDB3 ENCODER/DECODER

The MV1449, along with other devices in the GPS 2Mbit PCM signalling series comprise a group of circuits which will perform the common channel signalling and error detection functions for a 2.048Mbit PCM transmission link operating in accordance with the appropriate CCITT Recommendations. The MV1449 is also capable of operation at the next CCITT hierarchical bit rate of 8.448Mbit. The MV1449 circuit is fabricated in CMOS and operates from a single +5V supply with all inputs and outputs being TTL compatible.

The MV1449 is an encoder/decoder for the HDB3 pseudo-ternary transmission code, described in Annex A of CCITT Recommendation G.703. The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of the HDB3 coding, all ones detection and loss of input (all zero's detection). In addition a loop back function is provided for terminal testing.

FEATURES

- Single +5V supply.
- All Inputs and Outputs TTL compatible.
- HDB3 Encoding and Decoding to CCITT Recommendation G.703.
- Simultaneous Encoding and Decoding.
- Clock Recovery Signal allows Clock Regeneration from Incoming HDB3 Data.
- Loop Back Control.
- HDB3 Error Monitor.
- Alarm Indication Signal Monitor.
- Loss of Input Alarm.
- Low Power Operation.
- 2.048MHz or 8.448MHz Operation.

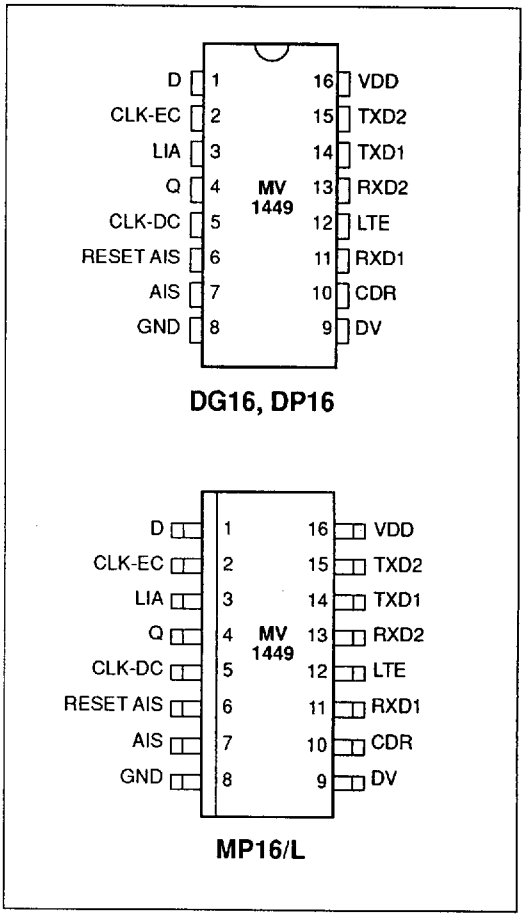


Fig. 1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

ELECTRICAL RATINGS

Supply Voltage	-0.5V to +7V
Input Voltage	-0.5V to VDD +0.5V
Output Voltage	-0.5V to VDD +0.5V

ORDERING INFORMATION

MV1449/IG/DGAS
MV1449/IG/DPAS
MV1449/IG/MPES

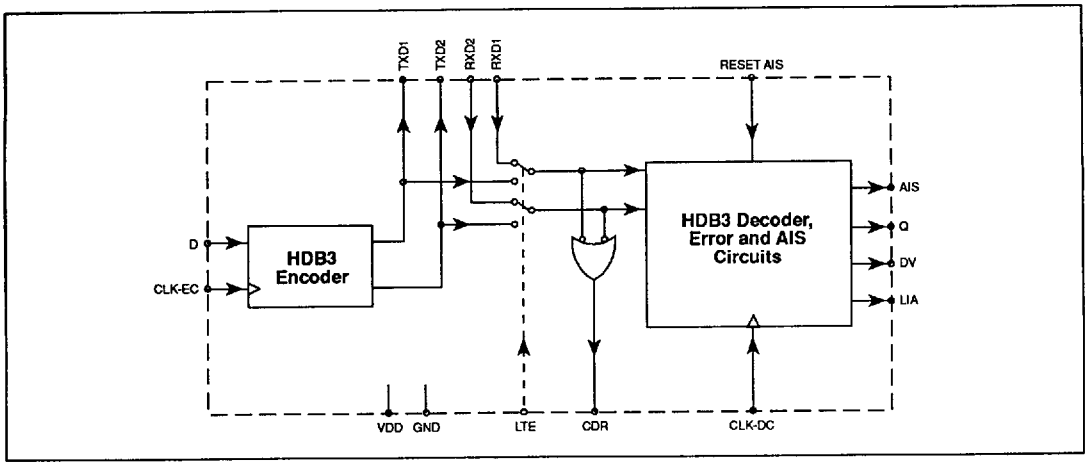


Fig. 2 Block diagram

FUNCTIONAL DESCRIPTION

High Density Bipolar 3 (HDB3) is a ternary transmission code in which the number of consecutive zeros which may occur is restricted to three, to ensure adequate clock recovery at the receiver. In any sequence of four consecutive binary zero's, the last zero is substituted by a mark of the same polarity of the previous mark, thus breaking the Alternate Mark Inversion (AMI) code. This mark is termed a violation. In addition, the first zero may also be substituted by a mark if the last mark and last violation are of the same polarity. This mark does not violate the AMI code and ensures that successive violations alternate in polarity and as such introduce no DC component to the HDB3 signal.

The MV1449 consists of two main blocks, the HDB3 Encoder and the HDB3 Decoder, with the Block Diagram being shown in Fig. 2. The function of each block is now described separately.

HDB3 Encoder

The HDB3 Encoder is responsible for converting the incoming NRZ data into HDB3 Encoded pseudo-ternary form for transmission over a 2.048Mbit/8.448Mbit PCM link. This conversion is carried out in accordance with the HDB3 coding laws specified in CCITT Recommendation G.703, Annex A.

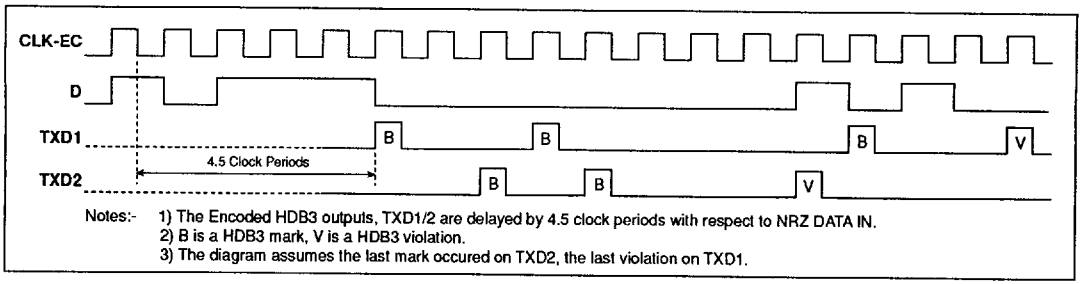
The data to be encoded is input on the D input pin and the encoding process is synchronised to the 2.048MHz/8.448MHz clock signal being input on the CLK-EC pin. The HDB3 Encoder has two outputs, TXD1 and TXD2, which represent the HDB3 encoded PCM data stream in pseudo-ternary form. If a mark or violation is to be transmitted the output pulses high after the rising edge of clock, with the length of the pulse set by the clock high pulse width. The timing diagram of the HDB3 Encoder is shown in Fig. 3.

HDB3 Decoder

The HDB3 Decoder circuit is responsible for converting the 2.048Mbit/8.448Mbit HDB3 encoded pseudo-ternary PCM data stream on its inputs, RXD1 and RXD2, into NRZ binary form to be output on the Q output pin. This conversion is carried out in accordance with the HDB3 coding laws specified in CCITT Recommendation G.703, Annex A. The HDB3 Decoder synchronously decodes the data on its RXD input pins into NRZ form under control of the 2.048MHz/8.448MHz clock being input on its CLK-DC pin. There is a 5 clock period delay between the HDB3 data being clocked in from the RXD inputs and the NRZ data appearing on the Q output. The Decoder clock must be externally regenerated from the incoming HDB3 data stream and in order to aid this clock recovery a logical 'OR' function of the inverted HDB3 inputs is output on the CDR pin.

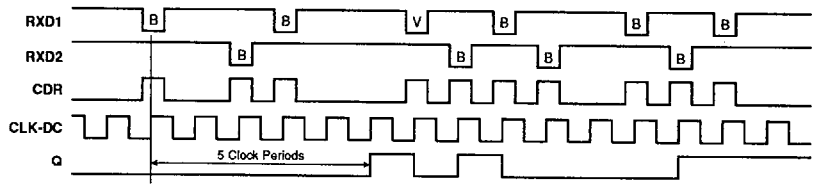
In addition to the basic HDB3 decoding the circuit also provides three alarm outputs. The first of these alarms is DV (Double Violation) and a logic high on this output denotes that two successive violations have been received with the same polarity, thus violating the HDB3 decoding laws. The second alarm, LIA (Loss of Input Alarm), is used to denote that 11 consecutive zero's have been received on the RXD inputs. The third alarm output is AIS (Alarm Indication Signal). This output will go high if less than 3 decoded zero's have been detected in the preceding RESET AIS=1 period (i.e. between RESET AIS=0 pulses) and as such this alarm can be used to detect the CCITT Alarm Indication Signal. All the alarm circuitry as well as the decoding process is synchronised to the clock signal being input on the CLK-DC pin. The clock signal may be asynchronous with the CLK-EC signal. The timing diagrams of the HDB3 Decoder circuit are shown in Fig. 4.

In addition to the normal mode of operation, a loop test mode is available for terminal testing. This mode is selected by taking the LTE (Loop Test Enable) input high. In this mode, the HDB3 encoded pseudo-ternary data outputs of the encoder block are inverted and fed back as the inputs to the decoder block, which in turn decodes this data and outputs it in NRZ form.



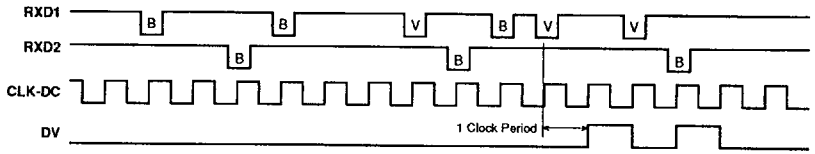
Notes:- 1) The Encoded HDB3 outputs, TXD1/2 are delayed by 4.5 clock periods with respect to NRZ DATA IN.
2) B is a HDB3 mark, V is a HDB3 violation.
3) The diagram assumes the last mark occured on TXD2, the last violation on TXD1.

Fig. 3 HDB3 Encoder waveforms



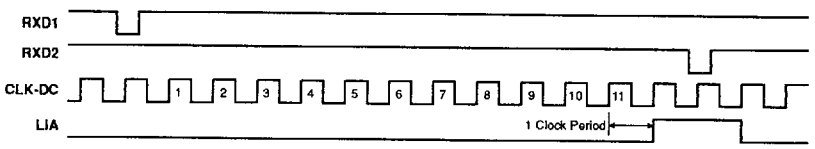
Notes:- 1) The Decoded NRZ output is delayed by 5 clock periods with respect to the HDB3 inputs.
2) The diagram assumes the last violation occured on RXD2.
3) B is HDB3 mark, V is a HDB3 violation.

Decoder waveforms



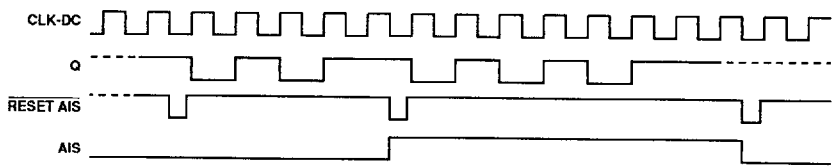
Notes:- 1)There is a single period delay between detection of an error and the rising edge of DOUBLE VIOLATION
2) The diagram assumes the last violation occured on RXD2.
3) B is HDB3 mark, V is a HDB3 violation.

HDB3 Double violation waveforms



Note:- 1)The 'LOSS OF INPUT' is delayed by a single clock period with respect to the incoming HDB3 waveforms.

Loss of input violations



AIS and $\overline{\text{RESET AIS}}$ waveforms

Fig. 4 HDB3 Decoder waveforms

PIN DESCRIPTIONS

Pin Name	Pin no.	Pin description
D	1	NRZ Data Input pin to HDB3 Encoder. The NRZ binary data on this pin is input to the HDB3 Encoder for conversion to HDB3 pseudo-ternary form under control of the CLK-EC signal. The D input is latched into the Encoder block by the falling edge of CLK-EC.
CLK-EC	2	2.048MHz/8.448MHz Clock Input to HDB3 Encoder. The clock signal on this input pin is used for the encoding of data on pin 1.
LIA	3	Loss of Input Alarm Output from HDB3 Decoder. This output goes high one period after the detection of 11 consecutive zeroes on the RXD inputs. Any HDB3 mark on the inputs (RXD1 or RXD2=0) resets this output low after a single clock period delay.
Q	4	NRZ Data Output from HDB3 Decoder. This output represents the HDB3 input data decoded back into NRZ binary form, with a 5 clock period delay from the HDB3 inputs to the NRZ output. This decoding process is carried out under control of the CLK-DC signal.
CLK-DC	5	2.048MHz/8.448MHz clock Input to HDB3 Decoder. The clock signal on this pin is used for the decoding of data on the RXD input pins, or the TXD pins in Loop Test Mode. This pin is used to input the externally regenerated clock signal recovered from the incoming HDB3 waveforms back to the Decoder block.
RESET AIS	6	Reset AIS Input to HDB3 Decoder. A logic '0' on this input resets a decoded zeros counter in the HDB3 Decoder. It will also reset the AIS output to '0' provided 3 or more zeros have been decoded in the preceding RESET AIS=1 period, or set AIS to '1' if less than 3 zeros have been decoded in the preceding RESET AIS=1 period. This may be used to detect the CCITT Alarm Indication Signal. A logic '1' on this pin enables the decoded zeros counter.
AIS	7	Alarm Indication Signal Output from HDB3 Decoder. See description for RESET AIS pin.
GND	8	Digital Ground. 0V
DV	9	Double Violation Alarm Output from HDB3 Decoder. This output goes high for one period of CLK-DC, one period after the detection of a HDB3 violation of the same polarity as the previous HDB3 violation.
CDR	10	Clock Recovery Output from HDB3 Decoder. This pin is used to output the logical 'OR' function of the inverted HDB3 inputs for the use of the external clock recovery circuit.

PIN DESCRIPTIONS (continued)

Pin Name	Pin no.	Pin description
RXD1	11	HDB3 Encoded Input 1 to HDB3 Decoder. This is one of the pair of 2.048Mbit pseudo-ternary HDB3 encoded PCM data stream inputs to the HDB3 Decoder. This input asynchronously latches the incoming HDB3 data and is falling edge sensitive. Since the input is asynchronously latched it is not necessary for the RXD pulse to straddle a rising clock edge.
LTE	12	Loop Test Enable Control Input. A logic low on this pin selects normal operation, with encoding and decoding being independent and asynchronous. A logic high on this pin internally connects TXD1 to RXD1 and TXD2 to RXD2. Note that in loop back mode, a decoder clock must be supplied (or regenerated from CDR) along with the encoder clock.
RXD2	13	HDB3 Encoded Input 2 to HDB3 Decoder. See description for pin RXD1.
TXD1	14	HDB3 Encoded Pseudo-Ternary Output 1 from HDB3 Encoder. The NRZ PCM data stream being input on the D pin is HDB3 encoded and output on this pin and pin TXD2. This output is always low during the low half cycle of clock and is only high during the high half cycle of clock if a mark is to be output. There is a 4.5 clock period delay from the falling edge of CLK-EC to TXD1.
TXD2	15	HDB3 Encoded Pseudo-Ternary Output 2 from HDB3 Encoder. See Pin TXD1 description.
VDD	16	Digital Supply Voltage. 5V

NOTES

1. All inputs have 100K on-chip pull down resistors.

ELECTRICAL CHARACTERISTICS

Test Conditions:
Supply Voltage VDD = 5V ± 0.5V Ambient Temperature T_{amb} = -40°C to +85°C

STATIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Low Level Input Voltage	V_{IL}	0.0		0.8	V	
High Level Input Voltage	V_{IH}	2.0		V_{DD}	V	
Low Level Output Voltage	V_{OL}			0.4	V	Isink=2mA
High Level Output Voltage	V_{OHT}	2.4			V	Isource=2mA
	V_{OHC}	V_{DD}-1.0			V	Isource=lmA
Input Leakage Current	I_{IL}	-10		200	uA	$V_{IN}=V_{DD}$ or V_{SS}
Supply Current	I_S			5	mA	2.048MHz Operation, Note 1.
				15	mA	8.448MHz Operation, Note 1.
Input Capacitance	C_{IN}		5		pF	All Inputs
Output Capacitance	C_{OUT}		5		pF	All Outputs

NOTES

1. All supply currents measured with outputs unloaded.

DYNAMIC CHARACTERISTICS

Note: Two sets of dynamic characterisitics are supplied, for use over the Commercial and Industrial Temperature ranges. The parameter set for the Commercial temperature range is aimed at customers wishing to switch from either the MJ1440 or MV1448 devices to the MV1449 since both the older devices were specified over the Commercial temperature range.

Test Conditions:
Supply Voltage VDD = 5V ± 0.5V Ambient Temperature T_{amb} = 0°C to +70°C

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
CLOCK						
Clock Period	t_{CP}	100			ns	See Fig. 5
Clock Rise/Fall Time	t_{CR}/t_{CF}			20	ns	See Fig. 5
Clock High/Low Time	t_{CH}/t_{CL}	30			ns	See Fig. 5
ENCODER						
Encoder Data Setup Time	t_{EDS}	15			ns	See Fig. 6
Encoder Data Hold Time	t_{EDH}	15			ns	See Fig. 6
TXD1/TXD2 Output Propagation Delay	t_{EPDR}/ t_{EPDF}			45	ns	See Fig. 6, Note 1.
DECODER						
RXD1/2 Data Setup Time	t_{RS}	15			ns	See Fig. 7
RXD1/2 Pulse Width	t_{RW}	20			ns	See Fig. 7
CDR Propagation Delay	t_{CPDR}/ t_{CPDF}			40	ns	See Fig. 7, Note 1.
Decoder Output Propagation Delay.	t_{OPD}			45	ns	See Fig. 7, Notes 1 and 2.
RESET AIS Hold-Off Time	t_{RAHO}	15			ns	See Fig. 7
RESET AIS Pulse Width	t_{RAW}	15			ns	See Fig. 7
Reset AIS Setup Time	t_{RAS}	10			ns	See Fig. 7
AIS Propagation Delay	t_{APD}			45	ns	See Fig. 7, Note 1.

Test Conditions:
Supply Voltage VDD = 5V ± 0.5V Ambient Temperature T_{amb} = -40°C to +85°C

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
CLOCK						
Clock Period	t_{CP}	100			ns	See Fig. 5
Clock Rise/Fall Time	t_{CR}/t_{CF}			20	ns	See Fig. 5
Clock High/Low Time	t_{CH}/t_{CL}	35			ns	See Fig. 5
ENCODER						
Encoder Data Setup Time	t_{EDS}	20			ns	See Fig. 6
Encoder Data Hold Time	t_{EDH}	20			ns	See Fig. 6
TXDI/TXD2 Output Propagation Delay	t_{EPDR}/ t_{EPDF}			50	ns	See Fig. 6, Note 1.
DECODER						
RXD1/2 Data Setup Time	t_{RS}	20			ns	See Fig. 7
RXD1/2 Pulse Width	t_{RW}	25			ns	See Fig. 7
CDR Propagation Delay	t_{CPDR}/ t_{CPDF}			45	ns	See Fig. 7, Note 1.
Decoder Output Propagation Delay.	t_{OPD}			50	ns	See Fig. 7, Notes 1 and 2.
RESET AIS Hold-Off Time	t_{RAHO}	15			ns	See Fig. 7
RESET AIS Pulse Width	t_{RAW}	20			ns	See Fig. 7
Reset AIS Setup Time	t_{RAS}	15			ns	See Fig. 7
AIS Propagation Delay	t_{APD}			55	ns	See Fig. 7, Note 1.

NOTES

1. All output propagation delays are measured with a 50pF load.
2. The t_{OPD} parameter applies to outputs Q, LIA and DV, but does not apply to AIS.

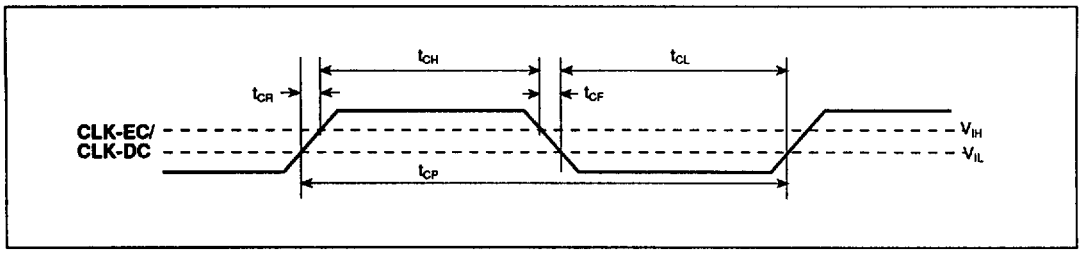


Fig. 5 Clock timing parameters

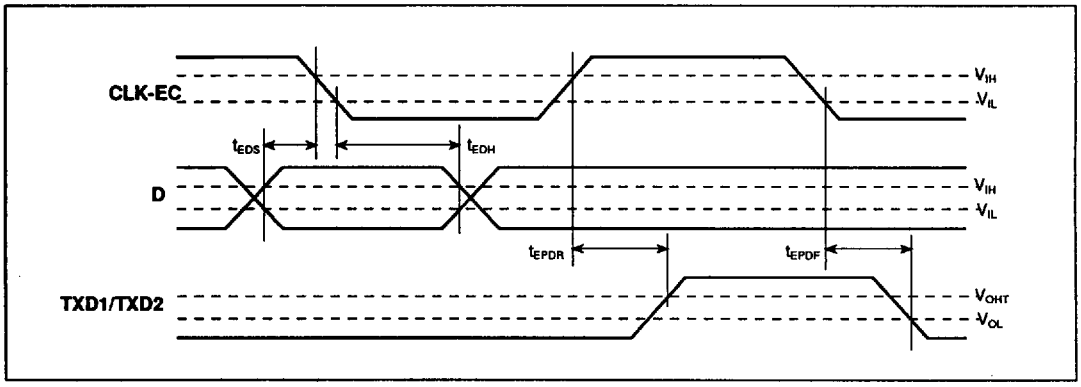


Fig. 6 Encoder timing parameters

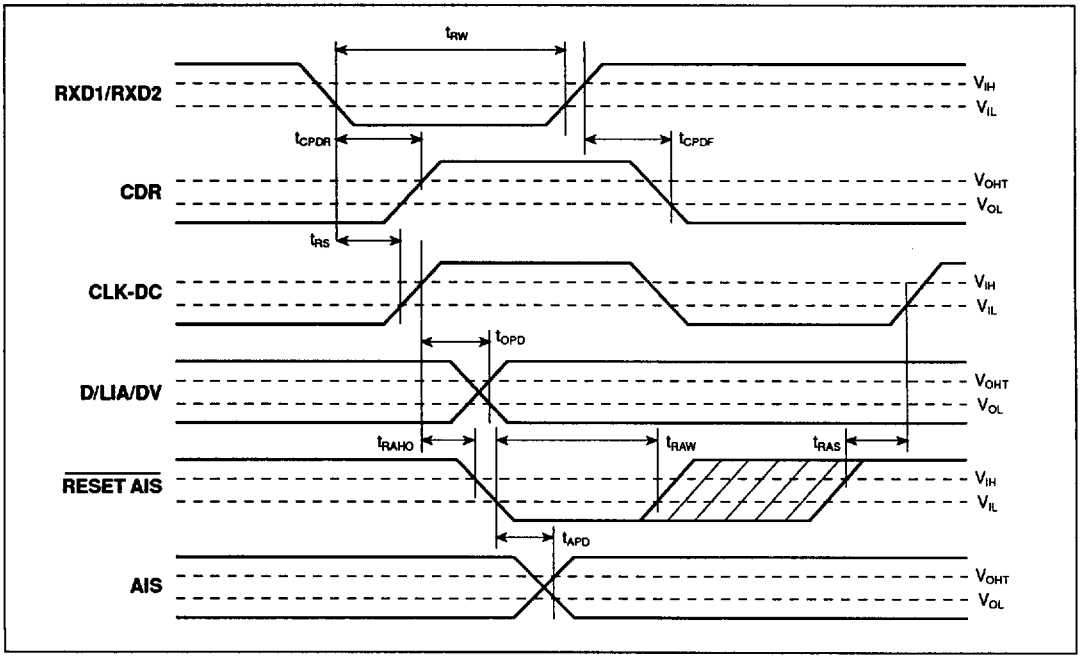


Fig. 7 Decoder timing parameters