National Semiconductor

ADVANCED INFORMATION

54F/74F598
Shift Register

General Description

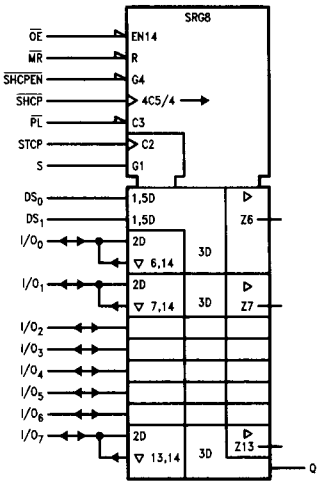
The 'F598 comes in a 20-pin package and consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and reset inputs. The 'F598 has TRI-STATE® I/O ports that provide parallel shift register outputs and also has multiplexed serial data inputs.

Features

- 8-bit parallel storage register inputs
- Shift register has direct overriding load and reset
- Guaranteed shift frequency DC to 120 MHz
- Separate clocks for storage and shift registers

Logic Symbols

IEEE/IEC



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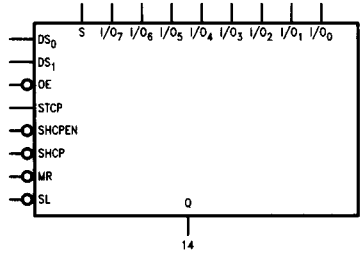

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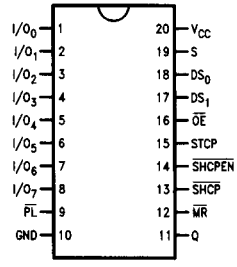
Connection Diagram

Pin Assignment for DIP, SOIC and Flatpak



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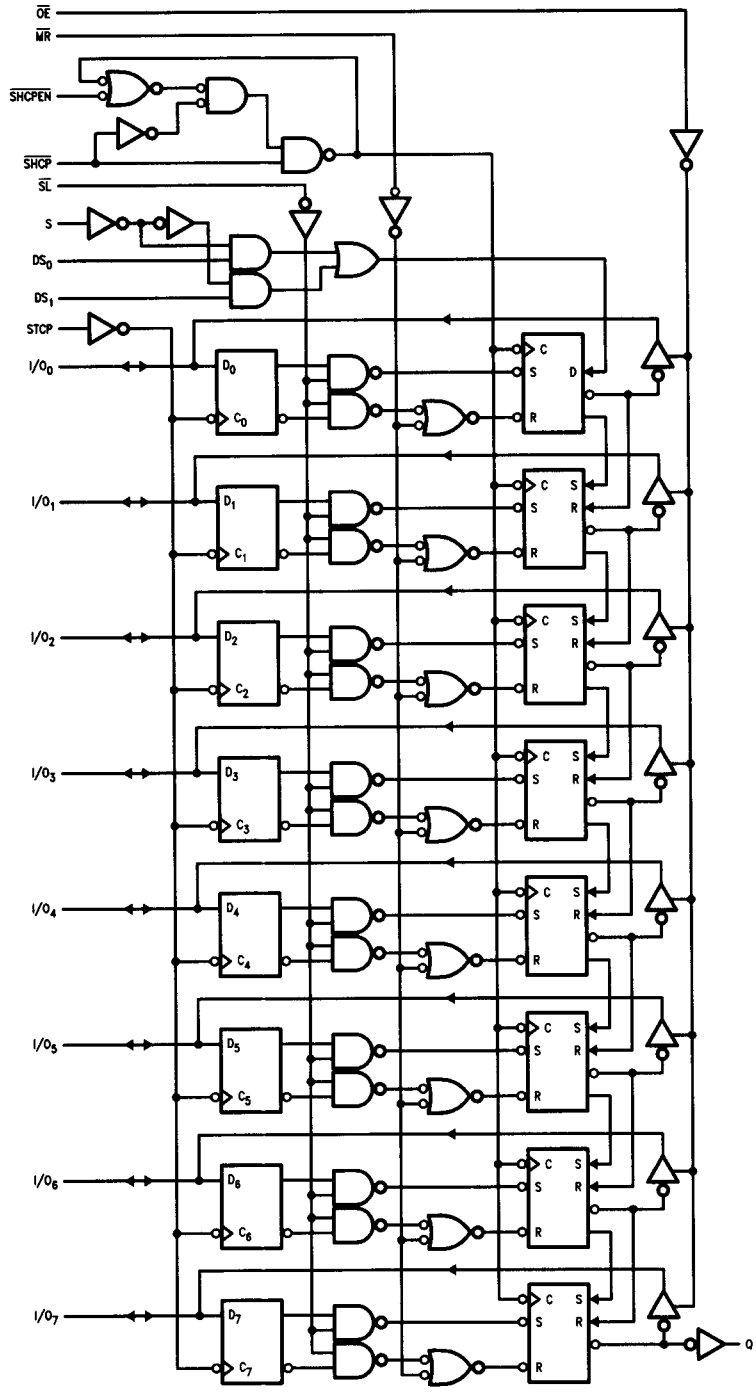
Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.