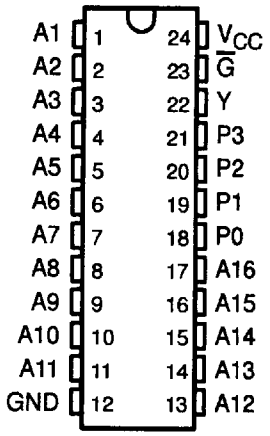
SDAS012C – JUNE 1982 – REVISED JANUARY 1995

- **16-Bit Address Comparator With Enable**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs**

**DW OR NT PACKAGE**
**(TOP VIEW)**




## description

This 16-bit address comparator simplifies addressing of memory boards and/or other peripheral devices. The four P inputs are normally hardwired with a preprogrammed address. An internal decoder determines what input information applied to the A inputs must be low or high to cause a low state at the Y output. For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A16 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

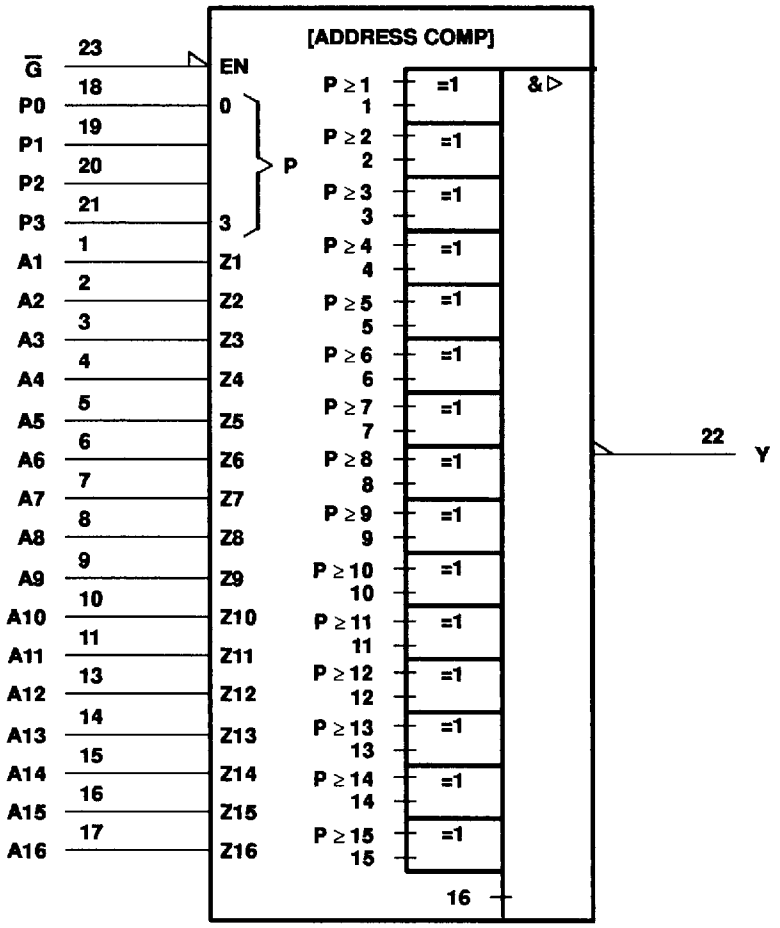
This device features an enable ($\overline{G}$) input. When $\overline{G}$ is low, the device is enabled. When $\overline{G}$ is high, the device is disabled and the output is high, regardless of the A and P inputs.

The SN74ALS677A is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

| INPUTS | | | | | | | | | | | | | | | | | | | | OUTPUT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{G}$ | P3 | P2 | P1 | P0 | A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | A9 | A10 | A11 | A12 | A13 | A14 | A15 | A16 | |
| L | L | L | L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L |
| L | L | L | L | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L |
| L | L | L | H | L | L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L |
| L | L | L | H | H | L | L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | L |
| L | L | H | L | L | L | L | L | L | H | H | H | H | H | H | H | H | H | H | H | H | L |
| L | L | H | L | H | L | L | L | L | L | H | H | H | H | H | H | H | H | H | H | H | L |
| L | L | H | H | L | L | L | L | L | L | L | H | H | H | H | H | H | H | H | H | H | L |
| L | L | H | H | H | L | L | L | L | L | L | L | H | H | H | H | H | H | H | H | H | L |
| L | H | L | L | L | L | L | L | L | L | L | L | L | H | H | H | H | H | H | H | H | L |
| L | H | L | L | H | L | L | L | L | L | L | L | L | L | H | H | H | H | H | H | H | L |
| L | H | L | H | L | L | L | L | L | L | L | L | L | L | L | H | H | H | H | H | H | L |
| L | H | L | H | H | L | L | L | L | L | L | L | L | L | L | L | H | H | H | H | H | L |
| L | H | H | L | L | L | L | L | L | L | L | L | L | L | L | L | L | H | H | H | H | L |
| L | H | H | L | H | L | L | L | L | L | L | L | L | L | L | L | L | L | H | H | H | L |
| L | H | H | H | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | H | H | L |
| L | H | H | H | H | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | H | L |
| L | All other combinations | | | | | | | | | | | | | | | | | | | | H |
| H | Any combination | | | | | | | | | | | | | | | | | | | | H |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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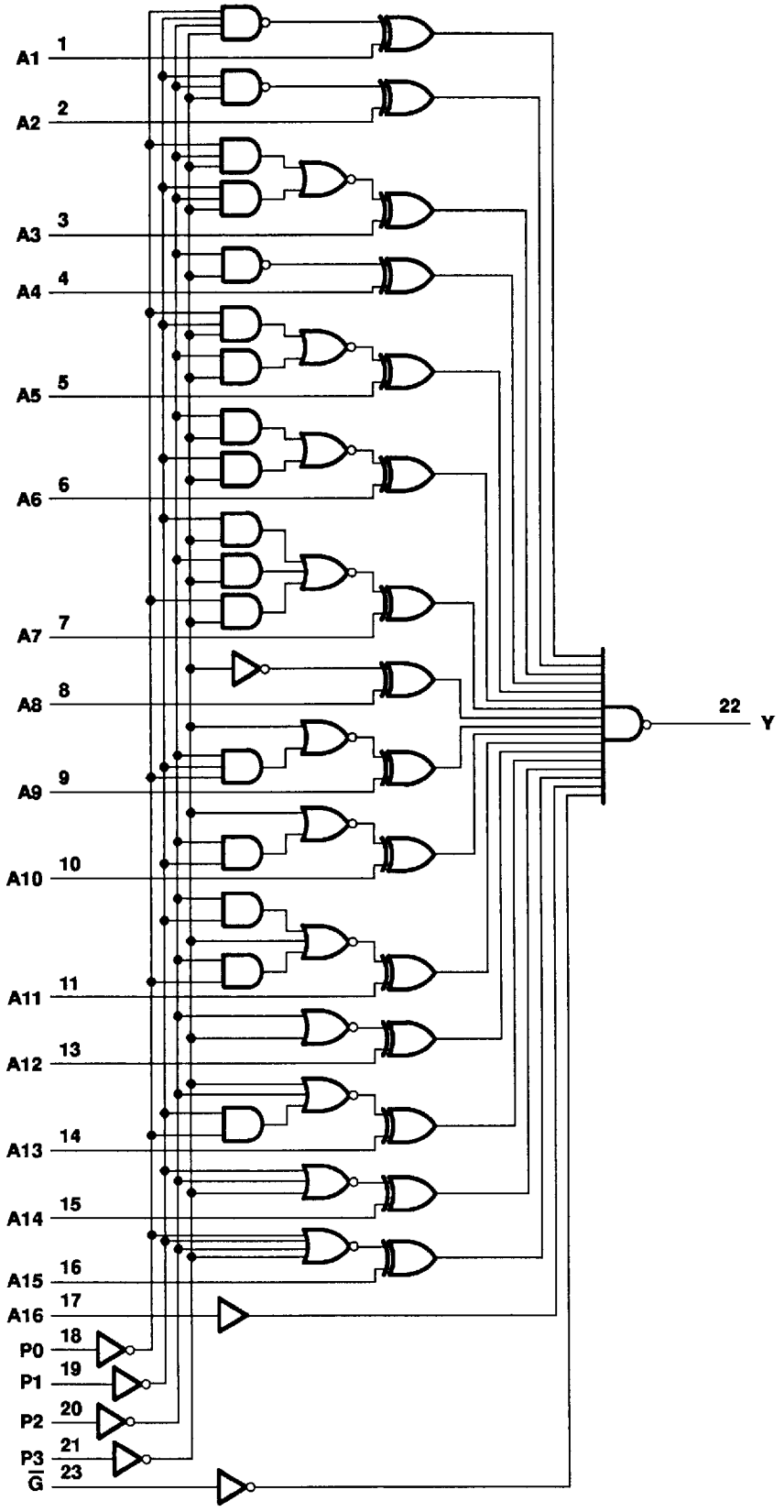
## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ ..... 7 V
Input voltage, $V_I$ ..... 7 V
Operating free-air temperature range, $T_A$ ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | | | 24 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = −0.4 mA | $V_{CC}$ −2 | | | V |
| | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −2.6 mA | 2.4 | 3.2 | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | V |
| | | $I_{OL}$ = 24 mA | | 0.35 | 0.5 | |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | −0.1 | mA |
| $I_O$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | −30 | | −112 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V | | | 21 | 33 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

## switching characteristics (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX¶ | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $t_{PLH}$ | Any P | Y | 4 | 25 | ns |
| $t_{PHL}$ | | | 8 | 38 | |
| $t_{PLH}$ | Any A | Y | 5 | 22 | ns |
| $t_{PHL}$ | | | 5 | 30 | |
| $t_{PLH}$ | $\overline{G}$ | Y | 3 | 13 | ns |
| $t_{PHL}$ | | | 5 | 35 | |

¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



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## APPLICATION INFORMATION

The SN74ALS677A can be wired to recognize any one of $2^{16}$ addresses. The number of lows in the address determines the input pattern for the P inputs. Those system address lines that are low in the address to be recognized are connected to the lowest-numbered A inputs of the address comparator. The system address lines that are high are connected to the highest-numbered A inputs.

For example, assume the comparator is to enable a device when the 16-bit system address is:

| A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| H | H | L | L | H | H | L | L | H | H | L | L | H | H | H | H |

Because the address contains six lows and ten highs, the following connections are made:

- P3 to 0 V, P2 to $V_{CC}$, P1 to $V_{CC}$, and P0 to 0 V
- System address lines A13, A12, A9, A8, A5, and A4 to comparator inputs A1 through A6 in any convenient order
- The remaining ten system address lines to comparator inputs A7 through A16 in any convenient order

The output provides an active-low enabling signal.

Figure 1 shows a modulo-N synchronous counter. The 'ALS163B provides a low-level clear signal when N = $FEFF_{16}$.

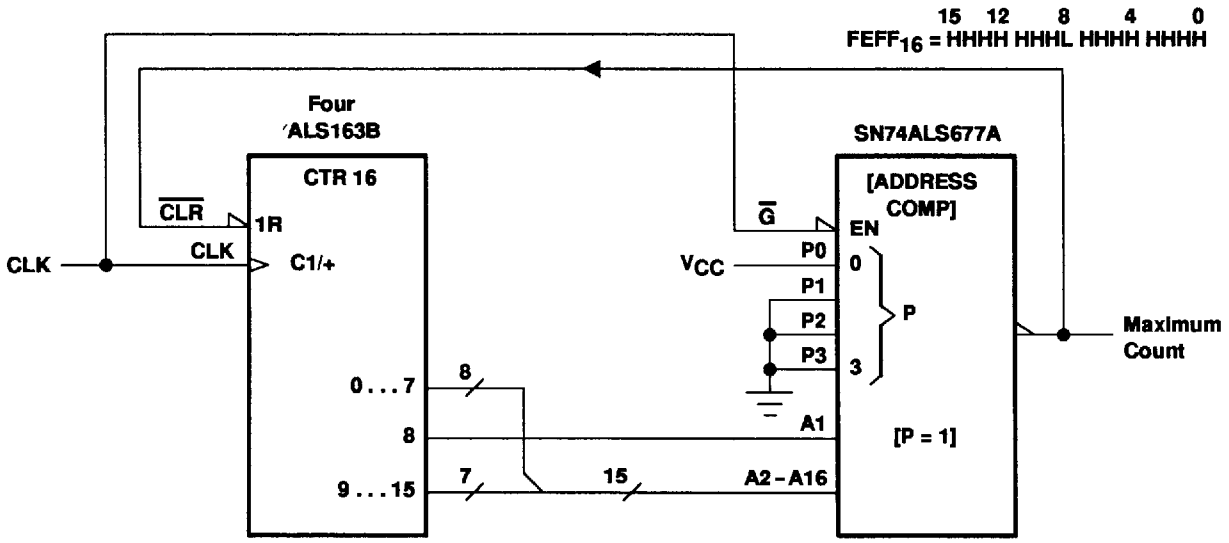
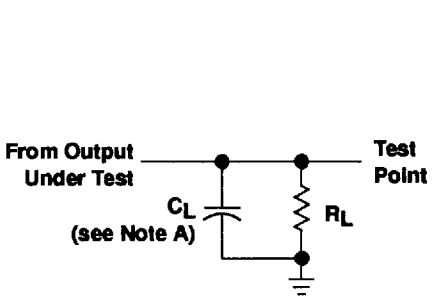
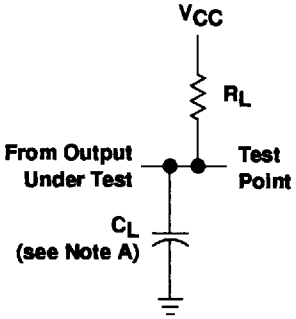



**Figure 1. Modulo-N Synchronous Counter**

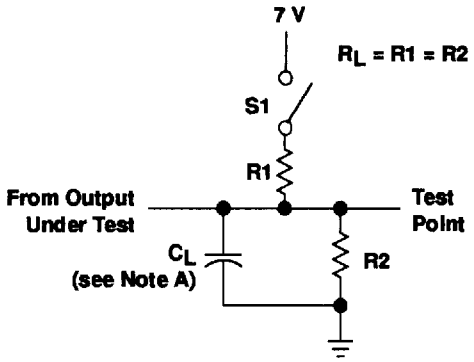
## PARAMETER MEASUREMENT INFORMATION
## SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



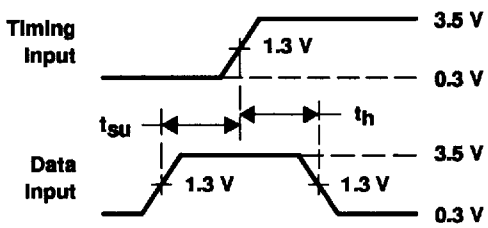

LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS



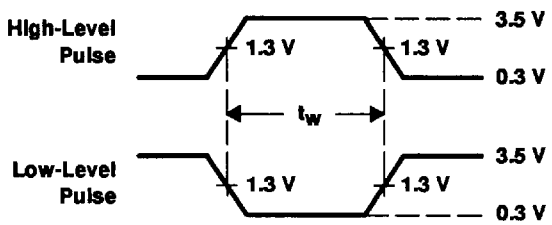

LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



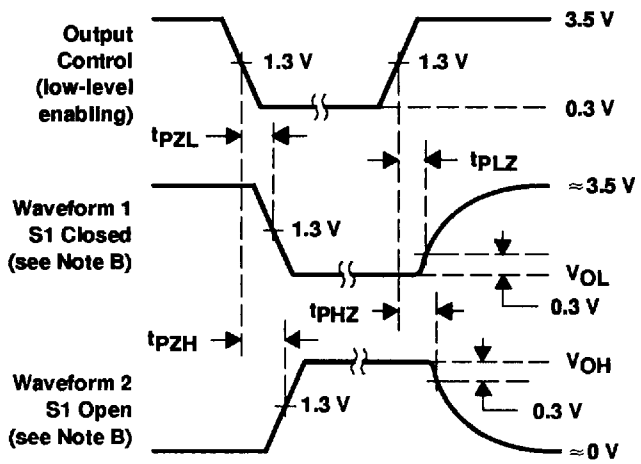

LOAD CIRCUIT
FOR 3-STATE OUTPUTS



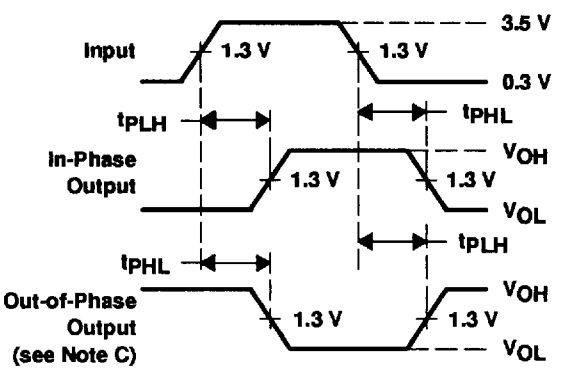

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PULSE DURATIONS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

**Figure 2. Load Circuits and Voltage Waveforms**