SSI 32C260
PC AT/XT Combo Controller

Advance Information

July, 1990

FEATURES

- PC AT/XT Bus Interface
  - Single Chip PC AT/XT Controller
  - Supports ST506/412, ST412HP, ESDI, and SMD disk interfaces
  - Direct bus interface logic with on-chip 24 mA drivers
  - Logic for daisy chaining 2 embedded controller drives on a PC AT
  - Supports 15 Mbit/s concurrent disk transfer on a 12 MHz PC AT without wait states
- Buffer Manager
  - Supports Buffer Memory throughput to 6 MB/s
  - Direct Buffer Memory addressing up to 64 kB static RAM
  - Dual port circular buffer control
- Storage Controller
  - NRZ Data rate up to 15 Mbit/s
  - Selectable 16-bit CRC or 56-bit ECC polynomial with fast hardware correction circuitry
  - Support sector level defect management
  - Support 1:1 interleaved operation
- Microprocessor Interface
  - Supports both Intel 8051, and Motorola 68HC11 family of microprocessors
  - Interrupt or polled microprocessor interface
- Others
  - Low power CMOS technology
  - Plug and Play compatible with Cirrus CL-SH 260 chip
  - Available in 84-pin PLCC or 100-pin QFP

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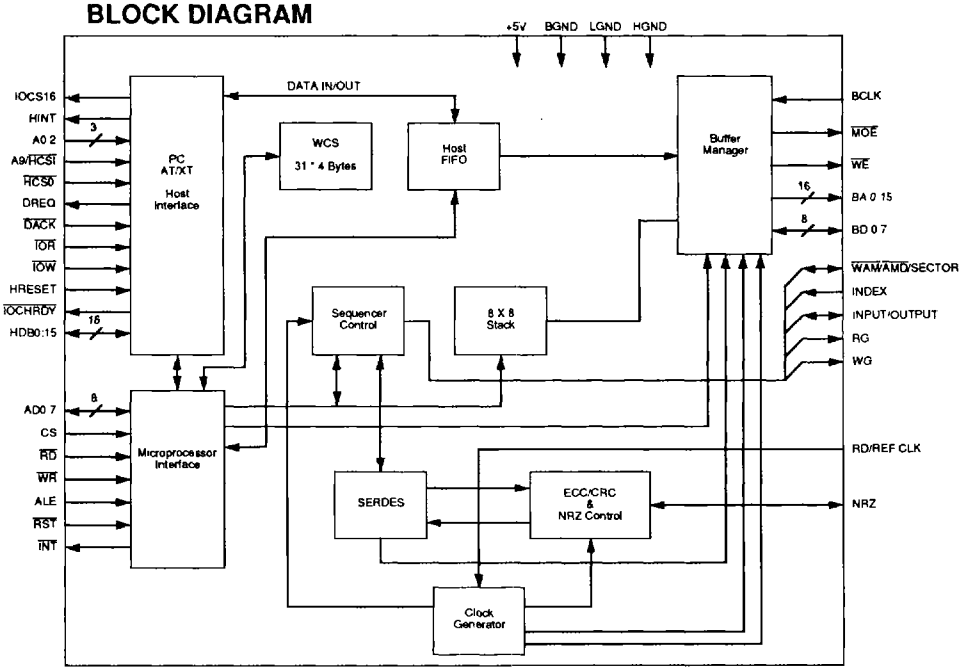
BLOCK DIAGRAM



SSI 32C260
PC AT/XT Combo Controller

DESCRIPTION

The SSI 32C260 is a CMOS VLSI device which integrates the major portion of the hardware needed to build a PC AT/XT driven hard disk controller. The 32C260 is capable of supporting interleaved data transfer rate up to 15 Mbit/s. This chip represents a major reduction in part count when used with the SSI 32D5322 Data Separator, 32P541 Pulse Detector, the SSI 32R4610 Read/Write device, and the SSI 32H4631 Servo and Motor Speed Controller device, implementing a powerful and cost efficient 5-chip set intelligent drive solution. It also has the flexibility to be used as a stand-alone combo controller.

The SSI 32C260 includes a dual port Buffer Manager, a storage controller and a extensive hardware support, including 24 mA drivers, for the PC AT/XT and other compatible interfaces.

The SSI 32C260 performs all the controller functions for the peripheral device, such as serialization/ deserialization, ECC generation and checking on the data stream, and CRC generation and checking on the header of the data stream.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
GENERAL		
+5V		POWER SUPPLY pin, VCC
BGND		BUFFER BUS GROUND
LGND		LOGIC GROUND
HGND		HOST GROUND
HOST INTERFACE		
A0:2	I	HOST ADDRESS LINES. These pins are used to address the internal registers by the AT bus.
A9/$\overline{HCS1}$	I	HOST ADDRESS LINE 9/ HOST CHIP SELECT 1. A9, this pin is used in conjunction with the A0:2 address lines to address the internal task file registers. HCS1 is an active low pin, used to qualify Host access.
$\overline{HCS0}$	I	HOST CHIP SELECT 0. Active low, this pin selects access to the control, status and data registers.
$\overline{IOCS16}$	O	I/O SELECT 16. An open drain output that indicates that a 16-bit sector buffer transfer is active.
HINT	O	HOST INTERRUPT. Asserted to indicate to the Host that the controller needs attention.
$\overline{IOCHRDY}$	O	I/O CHANNEL READY. Active low, this signal is asserted whenever that internal host FIFO is not ready to transfer data.
DREQ	O	DMA REQUEST. This pin is programmed to function as the PC/AT bus signal in the PC/ AT DMA mode.
$\overline{DACK}$	I	DMA ACKNOWLEDGE. Active low, in the PC/AT DMA mode this pin is programmed to be the PC/AT channel signal - DACK.
$\overline{IOR}$	I	INPUT READ SELECT. Active low, this pin is asserted by the Host during a Host read operation.
$\overline{IOW}$	I	INPUT WRITE SELECT. Active low, asserted by the HOST during a HOST write operation.

NAME	TYPE	DESCRIPTION
HOST INTERFACE (Continued)		
HRESET	I	HOST RESET. This signal resets all commands in progress when active, and initializes the control/status registers.
HDB 15:0	I/O	HOST DATA BUS. Active high bi-directional pins. These bits are used for data transfers between the Host and the Buffer Manager.
DISK INTERFACE		
INDEX	I	INDEX. Input for index pulse received from the drive
INPUT/ OUTPUT	I/O	INPUT/OUTPUT. A general purpose control and status pin. It can be either an input or an output. At power-on, this pin is an input.
$\overline{WAM}$/ $\overline{AMD}$/ SECTOR	I/O	WRITE ADDRESS MARK/ADDRESS MARK DETECT/SECTOR. This pin becomes an active low address mark detect if the read gate is on, or write address mark if write gate in on. It operates in hard or soft sector modes. The default is soft sector. In hard sector mode this is the input for the sector pulse.
RG	O	READ GATE. During NRZ data read, this pin is asserted. Active high.
WG	O	WRITE GATE. During NRZ data write, this pin is asserted. Active high.
RD/REF/ CLK	I	READ/REFERENCE CLOCK. This pin is used in conjunction with the NRZ pin to clock data in and out of the SSI 32C260 device.
NRZ	I/O	NRZ. This pin is used in conjunction with the RG and WG when reading and writing from and to the disk.
MICROPROCESSOR INTERFACE		
$\overline{RST}$	I	RESET. Active low input, when pulled low, the internal registers of the SSI 32C260 are held at reset.
ALE	I	ADDRESS LATCH ENABLE. This control signal latches the address on the address/data lines.
CS	I	CHIP SELECT. Active high signal, when asserted, the internal registers of the SSI 32C260 can be accessed.
$\overline{WR}$	I	WRITE. Active low input, when active the data is written to the internal registers.
$\overline{RD}$	I	READ. Active low input, when active the data is read from the internal registers.
$\overline{INT}$	O	INTERRUPT. An open drain output, when active, the microprocessor is requesting controller service.
AD7:0	I/O	ADDRESS/DATA BUS. 8-bit bus for both microprocessor register address and data.
BUFFER MANAGER INTERFACE		
BA0:15	O	BUFFER MANAGER ADDRESS LINES. Active high, for direct connection to a static RAM.
BD0:7	I/O	BUFFER MANAGER DATA BUS. 7 through 0. Active high, buffer data bus that connects directly to the buffer RAM.
$\overline{MOE}$	O	MEMORY OUTPUT ENABLE. Active low select for the buffer RAM.
$\overline{WE}$	O	WRITE ENABLE. Active low, write enable for the buffer RAM.
BCLK	I	SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address bits, write enable $\overline{WE}$, and memory output enable $\overline{MOE}$.

ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where a permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics

PARAMETER	RATING	UNITS
Power Supply Voltage, VCC	7	V
Ambient Temperature	0 to 70	°C
Storage Temperature	-65 to 150	°C
Power Dissipation	750	mW
Input, Output pins	-0.5 to VCC+0.5	V

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
VCC Power Supply Voltage		4.75		5.25	V
VIL Input Low Voltage		-0.5		0.8	V
VIH Input High Voltage		2.0		VCC+0.5	V
VOL Output Low Voltage	All pins except PC interface, IOL = 2 mA			0.4	
VOL Output Low Voltage	PC interface pins, IOL = 24 mA			0.5	V
VOH Output High Voltage	IOH = -400 µA			2.4	V
ICC Supply Current				50	mA
ICCS Supply Current Standby	All Inputs at GND or VCC	250			µA
IL Input Leakage Current	0 < VIN < VCC	-10		10	µA
CIN Input Capacitance				10	pF
COUT Output Capacitance				10	pF

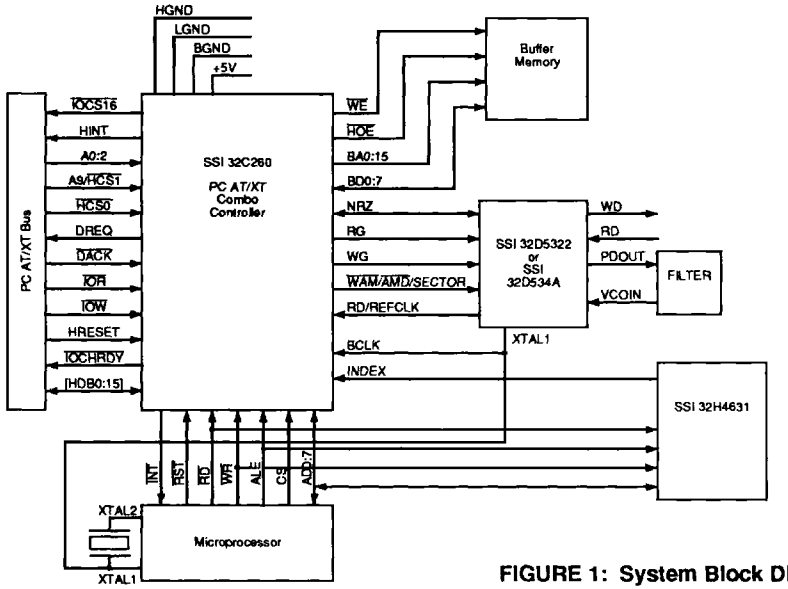


FIGURE 1: System Block Diagram using the SSI 32C260 PC AT/XT Combo Controller

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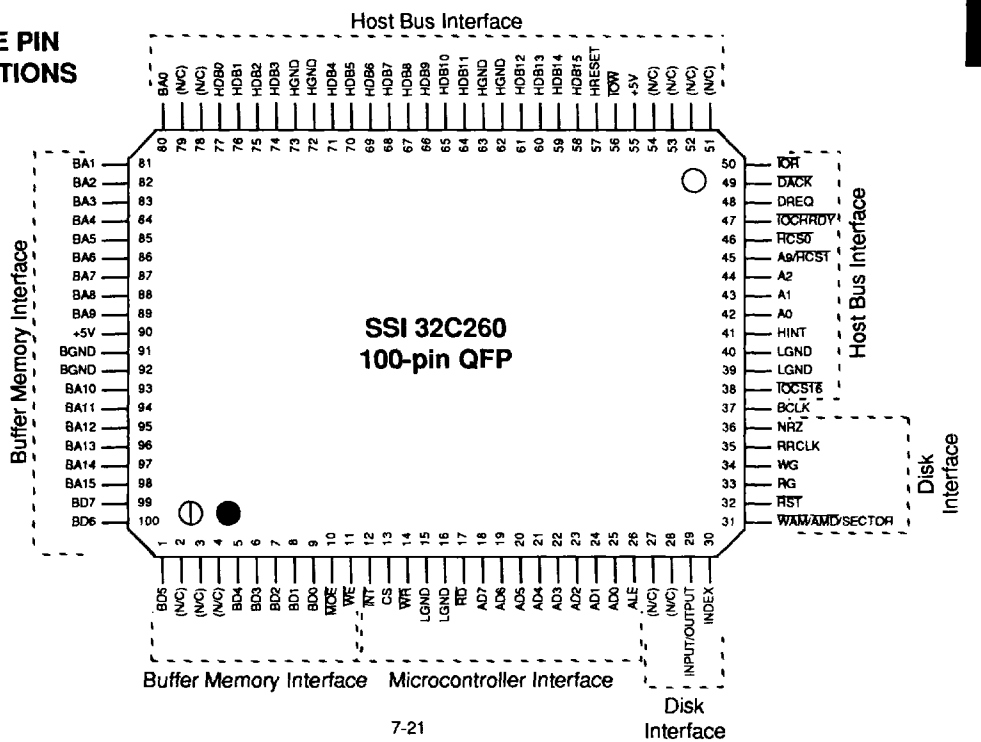
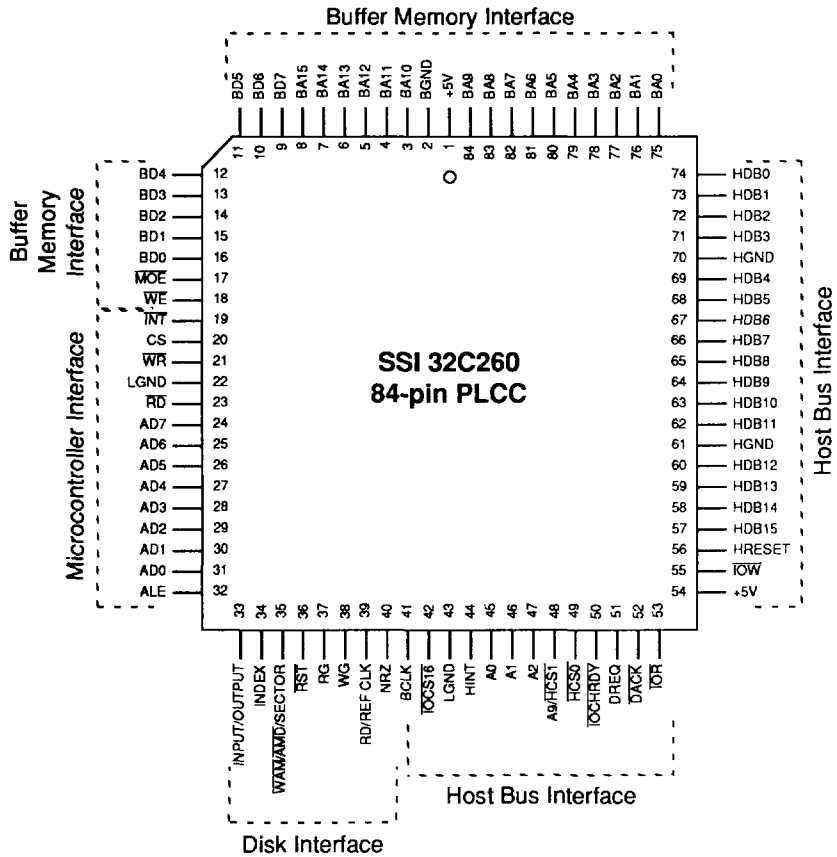
PACKAGE PIN DESIGNATIONS
(TOP VIEW)



PACKAGE PIN DESIGNATIONS (Continued)

(TOP VIEW)

CAUTION: Use handling procedures necessary for a static sensitive component.



Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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